entity FFSR\_tb is

end FFSR\_tb;

architecture Behavioral of FFSR\_tb is

component FFSR

Port (

S : in STD\_LOGIC;

R : in STD\_LOGIC;

CLK : in STD\_LOGIC;

Q : out STD\_LOGIC;

Q\_N : out STD\_LOGIC

);

End component;

signal S : STD\_LOGIC :=’0’;

signal R : STD\_LOGIC :=’0’;

signal CLK : STD\_LOGIC;

signal Q : STD\_LOGIC;

signal Q\_N : STD\_LOGIC;

begin

uut: FFSR

port map(

S => S,

R => R,

CLK => CLK,

Q => Q,

Q\_N => Q\_N

);

Tb: process

Begin

Wait for 100ns;

S <=’1’;

R <=’0’;

Wait for 100ns;

S <=’0’;

R <=’1’;

Wait for 100ns;

S <=’1’;

R <=’1’;

Wait for 100ns;

S <=’0’;

R <=’0’;

assert false

report "Fin de la simulación..."

severity failure;

end process;

end Behavioral;