entity INV\_tb is

end INV\_tb;

architecture Behavioral of INV\_tb is

component INV

Port (

I : in STD\_LOGIC;

O : out STD\_LOGIC

);

End component;

Signal I : std\_logic :=’0’;

Signal O : std\_logic;

begin

uut:INV

port map(

I => I0,

O => O

);

Tb: process

Begin

I0 <= ‘0’;

Wait for 50ns;

I0 <= ‘1’;

assert false

report "Fin de la simulación..."

severity failure;

end process;

end Behavioral;