

IN3170 V24 - Lab 3

Andreas Engøy, Simen Norrud, Erik Røset & Daniel Tran

May 2024

1 Task 1

1.1 Equipment

Component	Model	Quantity
Resistor	100k Ω	1

Table 1: List of components used in task 1.

2 Task 2

In an ideal current source, the output current is independent of the voltage across the terminals. I.e. the current source maintains the same current throughout the circuit, despite changes to V_{DS} .

A Field-Effect Transistor (FET) operating in the saturation region exhibits the same characteristics as an ideal current source. This can be seen from the I_D vs V_{DS} curve in the saturation region, where the current is almost constant. This is because V_{DS} approaching the saturation region is high enough that it has maxed out the number of charge carriers that can contribute to current flow, making the gate voltage the primary factor to the current flow.

In the plot, the curve will flatten out in this region. In a practical FET, the curve will not be completely flat (indicating that the current is not completely constant), but it will give a good approximation of an ideal current source.

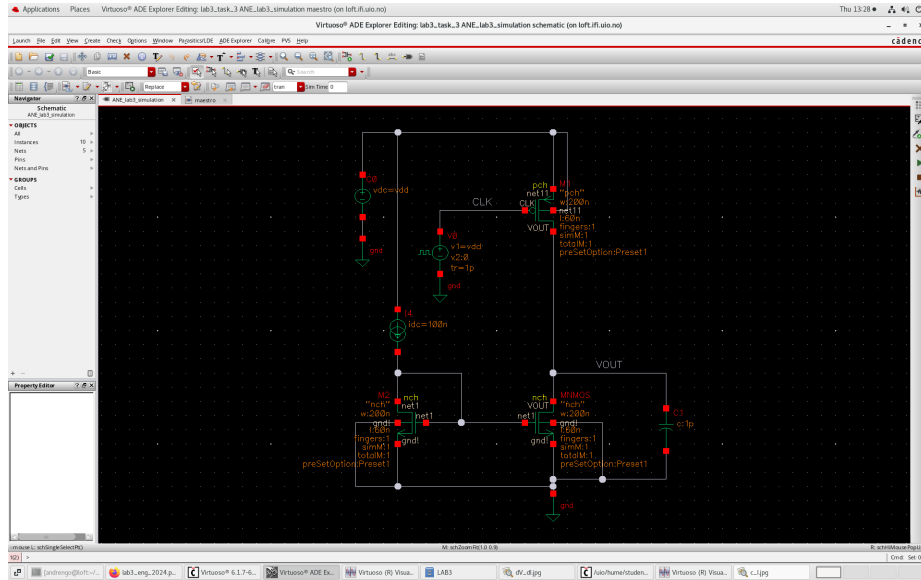


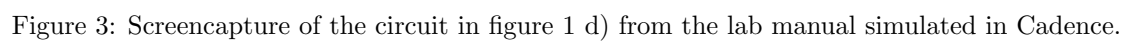
Figure 1: Screenshot of the circuit in figure 1 c) from the lab manual simulated in Cadence.

The bias current is implemented as a current mirror, consisting of $M2$ and $I4$, which sets the current that flows through $MNMOS$.

As suggested in the lab manual, a DC analysis is performed with V_C as a sweep parameter. This results in the following plot:

I_D is calculated as the difference between two points on the *most linear* part of the curve. In figure 2, this is chosen to be a segment at the end of the curve.

$$\begin{aligned}
 I_D &= 362.855 \text{ nA} - 283.135 \text{ nA} \\
 &= 79.72 \text{ nA}
 \end{aligned}$$


$$V_{DS} = 199.07 \text{ mV}$$
$$R_{on} = \frac{V_{DS}}{I_D} = \frac{V_{DS} = 199.07 \text{ mV}}{79.72 \text{ nA}} = 2.497 \text{ M}\Omega \quad (1)$$


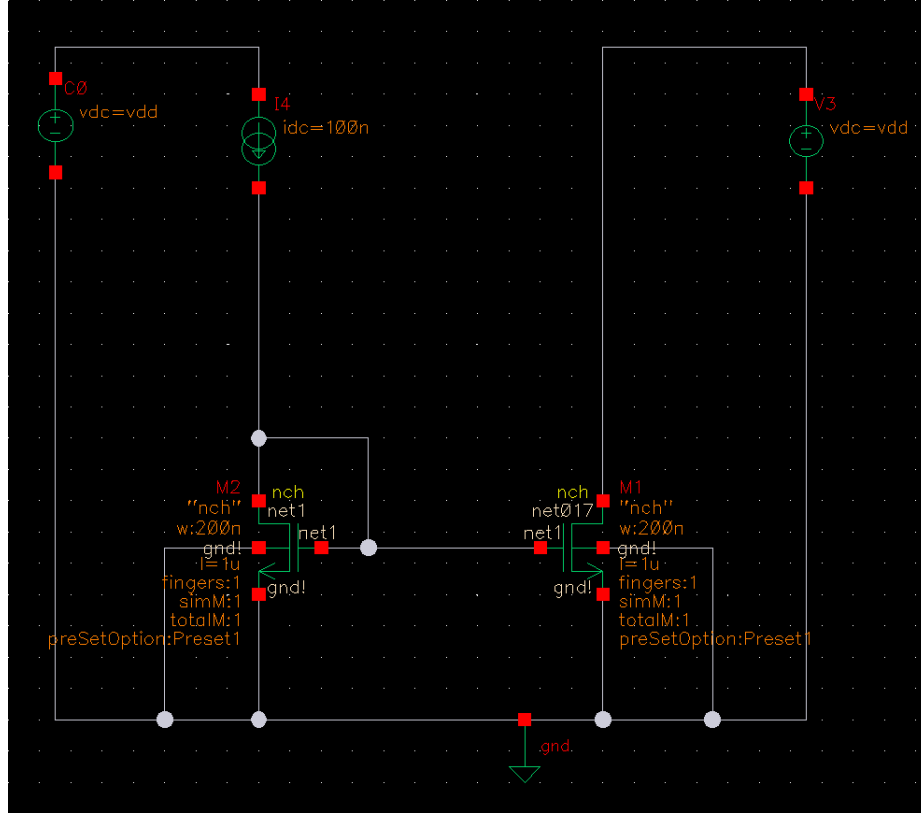


Figure 4: Screenshot of the circuit in figure 1 d) from the lab manual simulated in Cadence.

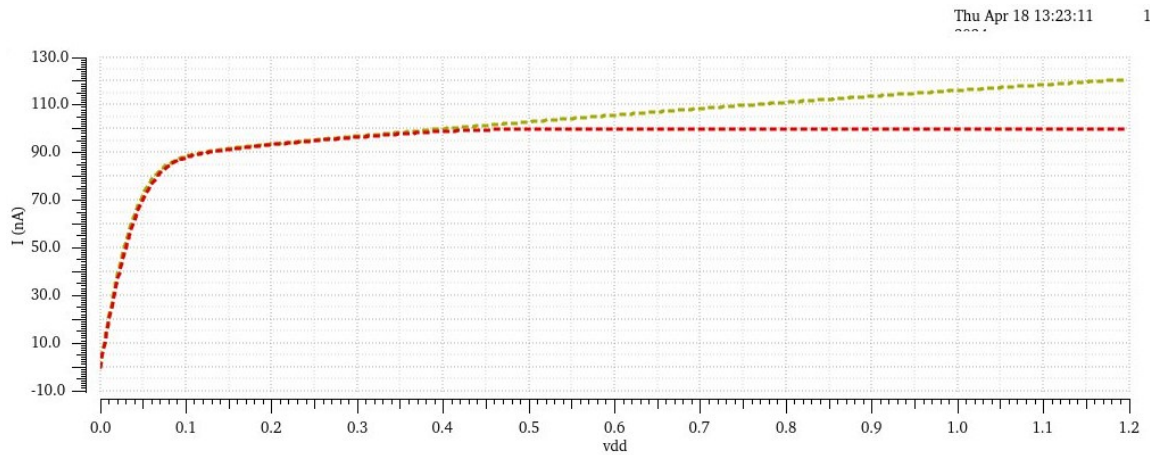


Figure 5: Screenshot of the DC sweep of both circuits in figure 1 d).