IN3170, spring 2024, mandatory laboratory exercise 2: Input capacitance and gate delay (deadline 2-Apr-2024, 14:15!)

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change log	
13-Mar-2024	Supplemented instructions: where to find 'initial condition', and use 'vpulse' as signal source.

Abstract

In this lab we shall measure the input capacitance of an inverter and estimate it's output resistance experimentally. Then, in simulation, we will investigate how the resistive switch model holds up when placing two PD transistors in series.

This is the second in a series of three lab tasks that will be graded and will count 40% towards the final grade. The first lab is only be 'pass' or 'fail'and the students are required to pass this lab assignment to be admitted to the exam. The second and third labs will get a score of between 0% and 100% and will each count 20% towards the course score. The deadline in the title is a hard deadline! Do not miss it! Plan to submit well ahead of the deadline! We will use devilry.ifi.uio.no for submission of you lab report.

1 Report and Group Assignments

1.1 Requirements for the Lab Report (read carefully!)

You are required to execute the tasks and answer all the questions posed below and to submit a report on your work. The report needs to be explaining clearly what you have done, how you have done it, what the results were and what you conclude from them. A good basic rule for any scientific writing is that a document should provide sufficient detail for someone reading it to be able to replicate the results that are presented. Make sure to answer all

questions! Supply the report with drawings of the circuits (including the values of the components and parameters you used where appropriate, e.g. bias voltages/currents, component sizes etc.) and measurement setups! Show your measurements in graphs! Use labels in the schematics that you draw, such as M_1, M_2 (M is often used fro labelling CMOS transistors), $opamp_1$, I_1, V_1 etc. You should then use those labels in your text, since it is much easier to write: 'transistor M_1 in figure 1' than 'the transistor third from the top and second from the left in the righthand side circuit in figure 1'. **MANDATORY when assembling a circuit in the lab**: Include a photograph of your circuit into the report!

1.2 Graded Mandatory Group Assignments

Note that this is part of the course's exam and strict rules apply as described in the document https://www.uio.no/english/studies/examinations/compulsory-activities/mn-ifi-mandatory.html . The page explains the significance of mandatory assignments in a course and in particular group assignments. It also specifies your responsibility to not plagiarize anybody else's work and that you are required to conduct and understand your own experiments and obtain your own results, while you are still allowed and encouraged to exchange advice and experiences also between groups.

Each group must deliver a written lab report using the Devilry online submission system **before** the **hard** deadline indicated in the title. Note that you can submit multiple times and the last submission before the deadline will be graded, so it might be a good idea to plan to submit preliminary versions well before the deadline. The points given for this lab assignment will determine if the lab assignment is accepted or rejected. You will need to pass this lab assignment in order to be admitted to the exam. The next two lab assignments will be weighted as 20% of the total score of the course, i.e. your final grade.

Each task is labelled with how many points it will contribute towards the score.

2 Lab Rules

2.1 Safety

Voltages over 40 Volt can in some cases be harmful, even though it usually requires more than that. The lab equipment is thus not able to provide voltages higher than 36V. Do not use equipment other than that provided in the lab! If a part of the skin is covered with a conductive fluid or is pierced and exposed to such voltages, a current could bypass the "insulator" of the skin and run through the body. If this current passes through the heart it can cause fibrillations or even cardiac arrest. Even higher more extreme currents could also give rise to internal burns. If this happens to anybody or something else happens in the lab, seek medical help immediately: heart fibrillations can last and cause trouble

long after the incident. Also notify the person in charge of the lab.

Some electronic components can explode if they are exposed to high currents. This is important to remember when working with electrolytic capacitors. However, none of the capacitors provided in the lab are electrolytic capacitors. Never bring your own electronic components into the lab!

2.2 Conduct

Good routines are necessary to make the work in the lab effective and safe:

- Food and drinks are prohibited from every lab.
- In general everybody is responsible for keeping the lab tidy.
- Always turn off the power supply before you start adding and/or removing components.
- Use an ESD protection wrist strap when handling ICs and other sensitive components.(ESD: electrostatic discharge)
- Always clean up after using equipment and tools:
  - Turn off all equipment, except for lab computer.
  - Throw away cutoffs and vacuum clean the desk, chair, and floor if necessary.
  - Place all components you have used back to their respective places. (Do this while you work, if you have a component you don't use anymore, put it back.)
- When you leave; the desk should be clean and ready for the next group.
- Read the information posters in the lab describing what to do in case of fire or medical emergency.

3 Task

3.1 Tools

See lab 1 for a description of the tools, both software and equipment in the lab!

For the GPIB instruments there is a short guide to get started, including a *constantly updated list of known issues* here: https://www.uio.no/studier/emner/matnat/ifi/IN3170/v24/materiale/lab-gpib-instrument-guide.html

Additional items to be used in lab 2:

- Hex-inverter IC, 74HCT14, find a datasheet here: https://www.uio.no/studier/emner/matnat/ifi/IN3170/v24/materiale/cd74hc14.pdf

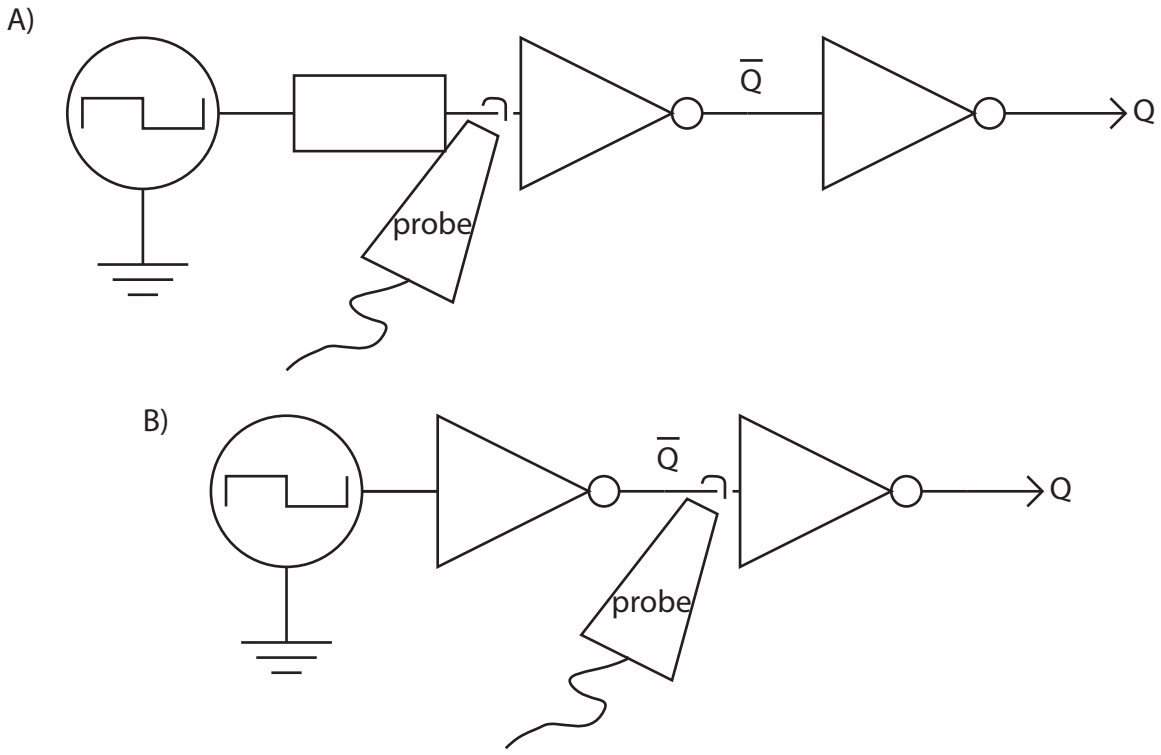

Figure 1: Schematics of a double inverter and setup to measure input capacitance C_I and transition time/propagation delay.

3.2 Tasks

Task 1 (8p): Using the IC in the lab labelled 74HCT14 containing 6 Schmitt trigger inverters (data sheet on the course web-page under 'resources': cd74hc14.pdf), build a double inverter (see figure 1), i.e. two inverters in series. Use 5V Vdd. You shall measure its input capacitance (Fig. 1 A)) and the gate delay of the first inverter (Fig. 1 B)) where the second inverter's input serves as output load. Note that the scope probe also has an input capacitance of 15pF! So you will need to subtract that from your result for the input capacitance! Use an appropriate resistor to get a signal transition curve that allows to estimate C_I with good accuracy and confidence. Maybe you can even observe some Miller effect that momentarily increases the perceived capacitance when the output switches?

From the transition of the output of the first inverter with a step at the input and assuming the capacitance being dominated by the scope probe and input capacitance of the second inverter you can then deduct an equivalent R_{ON} of the inverter for both the pull-up and pull-down. Be aware that also the output capacitance of the first inverter will contribute and possibly your cabling: you may neglect those two contributions though, unless they you see clear signs that they influence your result significantly. It may be the case that the scope's temporal resolution is not quite sufficient to see the transition time clearly. In that case you may employ an additional capacitor at node $\overline{\mathrm{Q}}$ to get a more reliable estimate of R_{ON}

Please report your findings (i.e. at least C_I, t_{pHL} and t_{pLH} or alternatively $\tau_{LH} = R_{ONp}C_{tot}$ and $\tau_{HL} = R_{ONn}C_{tot}$, and R_{ONp} and R_{ONn}) and illustrate well how you computed them from the data!

Task 2 (8p): Using Cadence (!) you shall assess the quality of the switched resistor model for a digital transistor when two transistors in series are used to pull down the voltage on a capacitor from Vdd to Gnd. The switched resistor model is popular particularly because it's easy to predict what happens when you put multiple transistors in series. However, this prediction is actually not 100% accurate.

Use 'initial condition' in the simulation set up (top menu: simulation→convergence aids→initial condition) to set the drain to Vdd at the start of the simulation. Use a capacitance (cell 'cap' from library 'analogLib') of about 1nF at the output that allows you to clearly determine a time constant for the pull down. 'Parasitic' capacitances at FET terminals are in the order of 10fF, so the 1nF should be significantly bigger than that, thus rending the influence of parasitic capacitances negligible. (Note that the 'probes' are merely symbolic here, indicating where you might want to measure. Simply measuring a node voltage in simulation will not add additional capacitance, such as a scope probe does in real life.)

Set up two simulations like depicted in figure 2 A). Use the cell 'vpulse' to

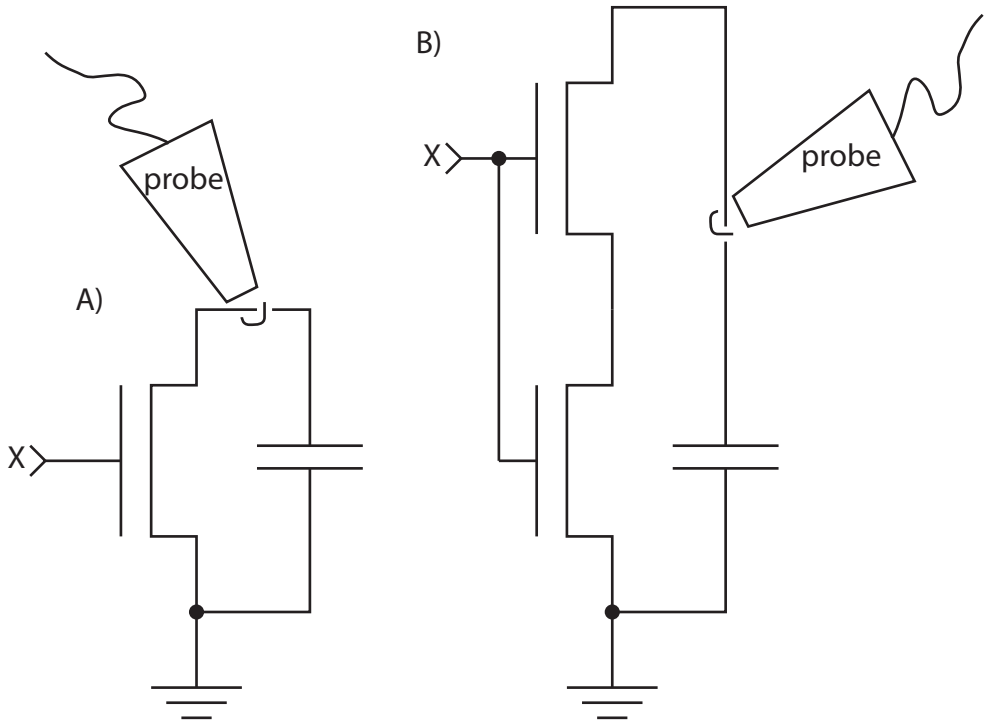

Figure 2: Circuit to assess the switched resistor model of a transistor used in a digital gate, when two transistors are used in series. Since this is in simulation, the 'probes' are just symbolic for where you likely should measure the voltage for your analysis.

initiate a step on terminal X. Make sure to set a 'rise time' (choose the cell and hit 'Q' to get to the parameters of the cell) to a short enough time, such that it is virtually an instantaneous step compared to the propagation delay. Determine R_{ON} in the single pull-down transistor case. Then simulate the pull down in figure 2 B) with two transistors in series the time constant or propagation delay should be double, if it were simply two R_{ON} in series. How does the real number deviate. Does the transition curve more or less resemble a RC decay or are there obvious differences? Can you speculate a bit about the deviation, if any, and if considering a large signal EKV model could one have predicted your result (just qualitatively, i.e. just if you would have predicted a longer or shorter transition time, not computing any numbers. Keep it simple!).

Clearly document how you arrived at your numbers, hypotheses, and conclusions! Good figures and markers in the figures might replace a lot of text.