

IN3170 - Lab 2

Andreas Engøy, Erik Røset & Daniel Tran

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1 Introduction

The purpose of this lab is to investigate the switching behavior of digital circuits, specifically Complementary Metal-Oxide-Semiconductor (CMOS) inverters, and to analyze the effects of parasitic capacitance on the propagation delay of these circuits. The lab is divided into two main tasks: the first task involves measuring the input capacitance of a CMOS inverter, while the second task focuses on the resistive switch model of nMOSFETs in series. The lab is conducted using both physical circuits and simulations in Cadence Virtuoso, with the aim of comparing the results from the two methods. The lab is conducted in the context of digital electronics and is relevant for understanding the behavior of digital circuits in modern electronics.

2 Theory

2.1 FET switch models

Binary variables in digital electronics are represented by high ('H') or low ('L') voltage levels, ideally switching between the power supply voltage (V_{dd}) and ground (Gnd). However, in reality, the switch between these two states is not instantaneous and is modeled using the switching threshold voltage (V_{sw}), leaving a range where signals are undefined. The switching threshold is defined as the voltage at which the output voltage is equal to the input voltage, and is typically set to $V_{dd}/2$ for CMOS inverters.

The switching behavior of field-effect Transistors (FETs) depends on the gate voltage (V_{GS}) relative to the switching threshold, with nFETs conducting for $V_{GS} > V_{sw}$ and pFETs for $V_{GS} < V_{sw}$. R_{ON} , and I_{ON} are parameters used to model propagation delays and are derived from complex transistor models or approximated for relative delay predictions.

2.2 Capacitance at transistor level

In a CMOS circuit, each metal-oxide-semiconductor field-effect transistor (MOSFET) structure exhibits several parasitic capacitance which must be accounted for in the design. By examining the MOSFET structure, one can identify several cases where conductive regions are separated by a dielectric material or a depletion region. These cases are the source of capacitance in a MOSFET, and can be divided into three main components: the gate-to-source capacitance C_{GS} , the gate-to-drain capacitance C_{GD} and the gate-to-bulk capacitance C_{GB} . The total input capacitance of the structure is the sum of these capacitances. The formulas for these capacitances are derived in the compendium for IN3170 course [1].

2.3 Propagation delay

As each gate operation in a CMOS structure requires charging and discharging of these capacitances, the system has a dynamic power consumption. I.e. when the input voltage changes, the circuit will experience a time delay as the output voltage reacts to the change. This propagation delay of a logic gate e.g. CMOS inverter is the time difference for the output signal as the input signal changes. It is usually measured at 50% at the transition from input to output. The propagation delay is a measure of how fast the logic gate can respond to a change in the input signal.

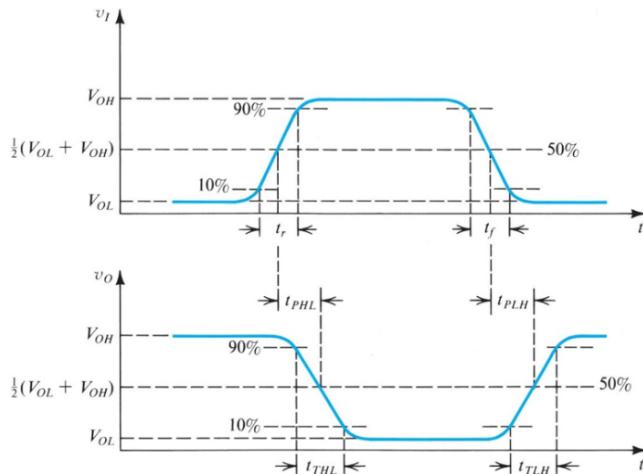


Figure 1: Illustration of propagation delay and transition time of a logic gate. [2]

Figure 1 shows the different timing parameters for a logic gate. The propagation delay high-to-low t_{pHL} and propagation delay low-to-high t_{PLH} are the time it takes for the output to switch as input switches, measured from 50% of the input signal to 50% of the output signal. The rise time t_r is the time it takes during transition for the output to switch from 10% to 90% of maximum output voltage. The fall time t_f is the time it takes for the output to switch from 90% to 10% of maximum output voltage.

2.4 RC circuit model

The switching behavior of a CMOS inverter could be modeled as a first order RC network where the input capacitance of the inverter C_I is charged or discharged through the resistive elements. The system can then be described by the time constant τ of the model circuit, given by the product of the resistance and the capacitance as given in the lab manual:

$$\tau = R_{on} C_{tot} \quad (1)$$

where R_{on} is resistive model for a transistor and C_{tot} is the load capacitance.

2.5 The resistive switch model

The resistive switch model is a method used to analyze dynamic electronic circuits that alternate between distinct resistive states through switches. This model simplifies complex, time-varying systems by treating them as a set of static configurations, making it easier to study their transient and steady-state responses. To get an even more accurate approximation of the system's behavior However, the resistive switch model can be used in conjunction with the circuit's transient response in the form of I_{ON} or t_p . This dynamic resistive switch model is represented by the equation:

$$R_{ON} = \frac{t_p}{0.69 \cdot C_L} \quad (2)$$

2.6 Miller effect

The Miller effect refers to the phenomenon which describes the increase in effective capacitance between the input and output terminals of an active device due to feedback at the point of amplification. In essence, it refers to the phenomenon where a input capacitance is magnified as a result of the voltage gain of the circuit, leading to an apparent increase in input capacitance during signal transitions. This effect has implications for the design and performance analysis of amplifiers, as well as digital circuits such as CMOS inverters.

In the context of the latter, the Miller effect is especially pronounced during the transition of signal levels, specifically at the switching point. During the critical switching point, the output capacitance effectively gets coupled back to the input through the inverter's feedback mechanism. As a result, a momentary surge in effective capacitance is experienced, the Miller capacitance, coinciding with the maximum voltage gain of the inverter.

3 Materials and Methods

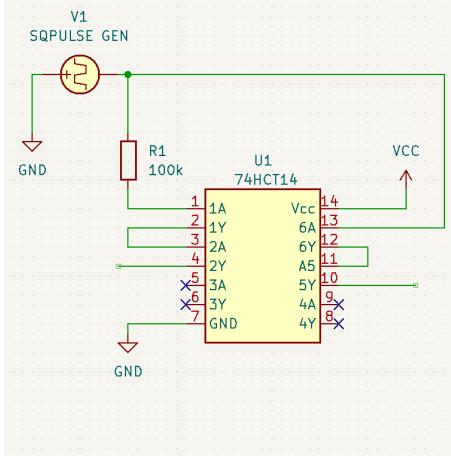
3.1 Equipment

Component	Model	Quantity
Resistor	100kΩ	1
Hex Inverter IC	74HCT14	1
Copper wires	-	12
Printed Circuit Board	-	1
Soldering iron	-	1
Soldering wire	-	1
Oscilloscope	HP54622	1
Waveform generator	HP33120	1
Voltage source	HPE3631	1
Computer w/ "Cadence Virtuoso"	6.1.7	1
NMOSFET*	TSMC 65nm	3
Waveform generator*	-	2
Capacitor*	-	2

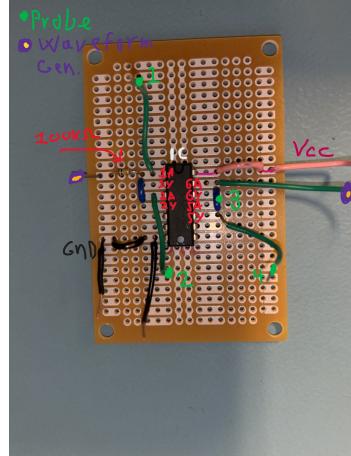
Table 1: List of components used in the experiment. Components marked with * are simulated in Cadence Virtuoso.

3.2 Task 1a

The GPIB instruments are set up according to the lab manual. The circuit is built according to the schematic in Figure 2a. The circuit has two separate serial double inverters, one with a 100kΩ resistor before the first inverter, and one without a resistor. The circuit is powered by a voltage source with a voltage of 5V. The probes of the circuit is connected to an oscilloscope in order to measure the voltage. The input marked 1A of the IC is connected to a waveform generator which



(a) Circuit diagram



(b) Photo of the circuit

Figure 2: Schematic and photo of two double inverters connected in series

generates a square wave with a frequency of 400 Hz. The circuit is then probed according to Figure 1 in the lab manual (point 1 in figure 2b).

Together with the lab manual there is supplied a Matlab script that controls the settings of the waveform generator and the voltage source. It also reads the data from the oscilloscope and plots the data. From the given Matlab script the following modification were made:

- The waveform generator was set to generate a square wave with a frequency of 400 Hz and peak voltage of 5 V on line 35 and 36.
- Autoscale for the oscilloscope was disabled on line 40.
- A system-specific dc offset was added to the oscilloscope to keep the signal within the 0 - 5 V range.
- The for-loop between lines 64 - 69 was swapped for a single line that set the voltage source to a constant 5V.
- All plotting were modified to be labeled with correct axes and title.

In order to capture a single low-to-high transition, the oscilloscope display were manually adjusted as needed.

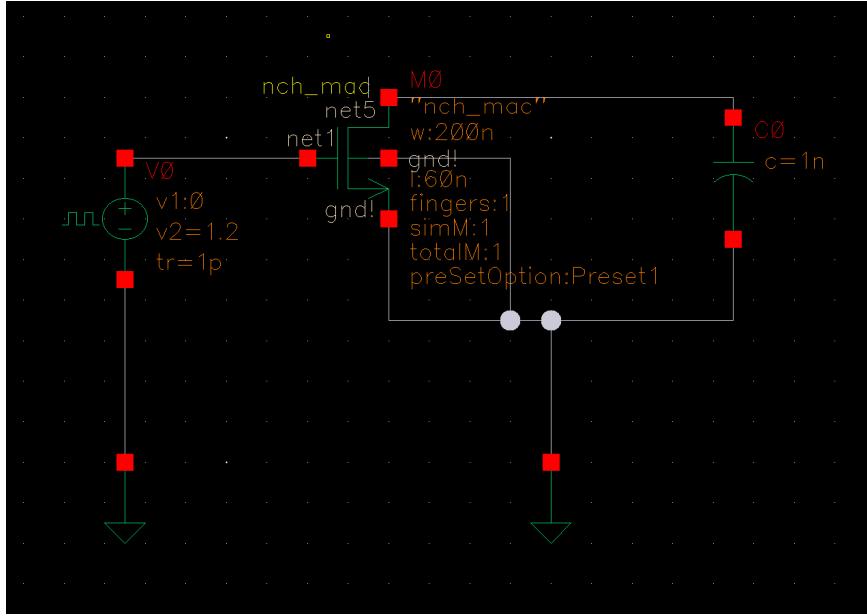
From the plotted data, the start point, end point of the rising edge and the switching point at $V_{dd}/2$ were marked. These were then used to find the input capacitance of the inverter using equation 1.

3.3 Task 1b

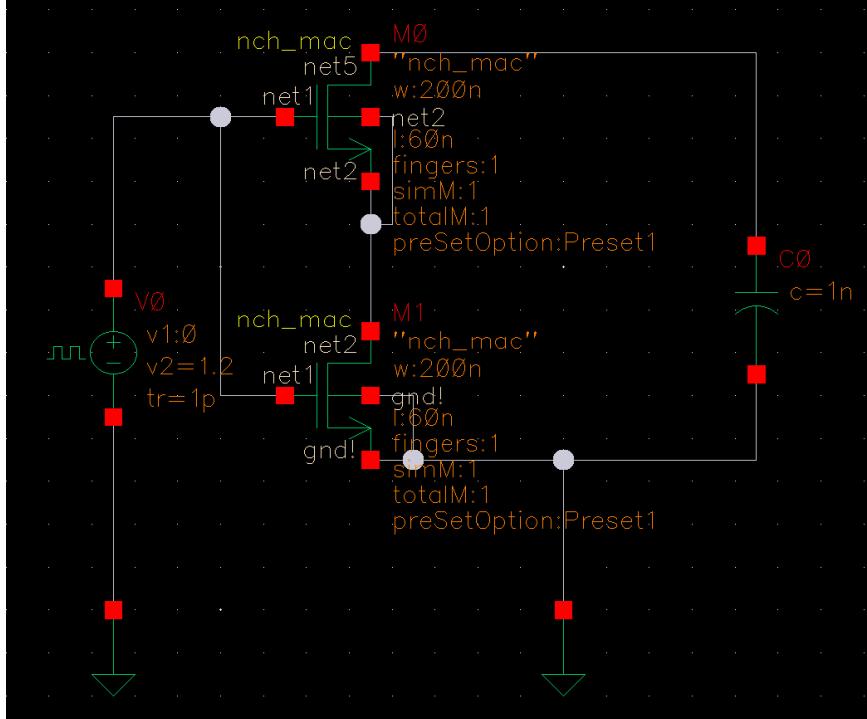
The wavegenerator is connected to input 6A of the IC. The probe measures the signal at point 3 from figure 2b. Another probe measures the output of the second inverter at point 4 from figure 2b. The settings on the instruments are kept the same as in task 1a. The Matlab script is modified to plot the data from both channels from the oscilloscope. The script is then run to capture the high-to-low and low-to-high transitions of the circuit, which were found by manually adjusting the oscilloscope display.

3.4 Task 2

The digital transistor circuits are built and simulated in Cadence Virtuoso as shown in figure 3. Using the 'initial condition' in the simulator set up the drain to source voltage V_{DS} is set to 1.2 V. The circuits consists of waveform generators 'vpuls' that generate a square wave with a frequency of 1 kHz, a 'rise time' of 1ps and a peak voltage of 1.2 V. The capacitors 'cap' are picked from the 'analogLib' and set to 1nF. To simulate the circuits the internal simulation tool Maestro is used and



(a) Circuit A



(b) Circuit B

Figure 3: Schematics of the two digital transistor circuits.

probed at the gate and drain. We then use the t_p from the simulation to calculate the R_{on} of circuit A in the resistive switch model using equation 2. We then compare the calculated t_p of a resistive switch model in series with the observed.

4 Results

4.1 Task 1

Plot of the rising edge of a double inverter circuit with a $100\text{k}\Omega$ resistor before the first inverter:

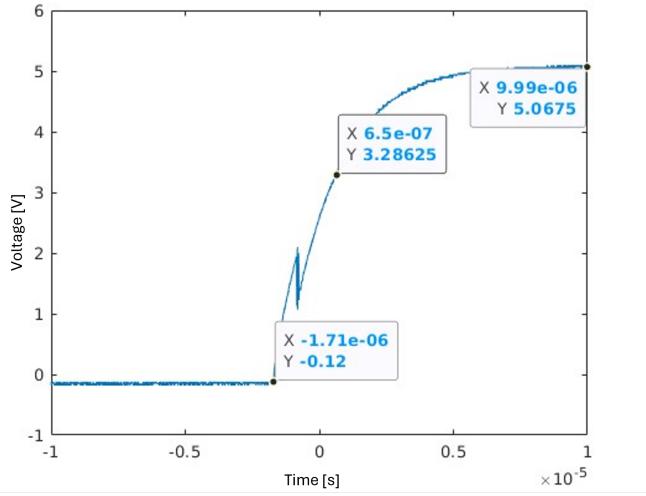


Figure 4: Plot of the rising edge of a double inverter circuit with a $100\text{k}\Omega$ resistor before the first inverter with added points of interest. From left to right the points are: start of rising edge, switching point and stop of rising edge.

Input capacitance of the inverter:

$$C_I = 8.6 \text{ pF} \quad (3)$$

Plot of the edges of a double inverter circuit without a resistor before the first inverter:

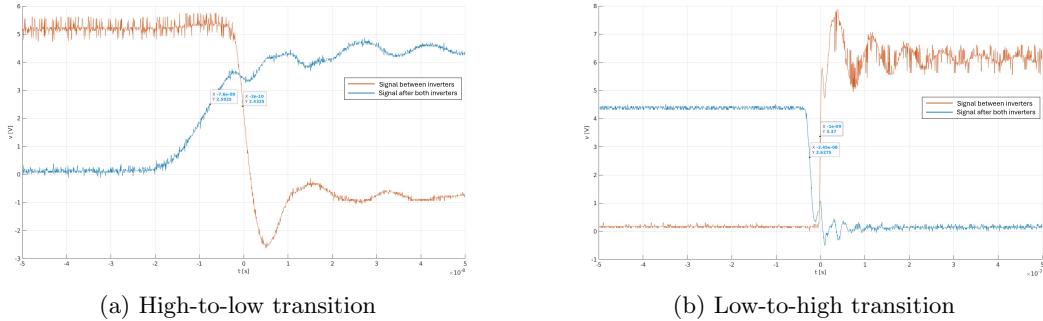


Figure 5: Plots of the edges of a double inverter circuit without a resistor before the first inverter.

4.2 Task 2

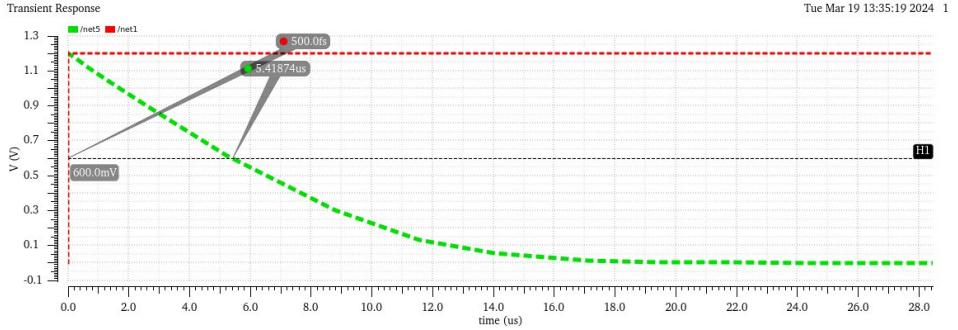
Maestro simulated plots of the gate and drain voltages of circuit A and B:

R_{on} calculated from the resistive switch model:

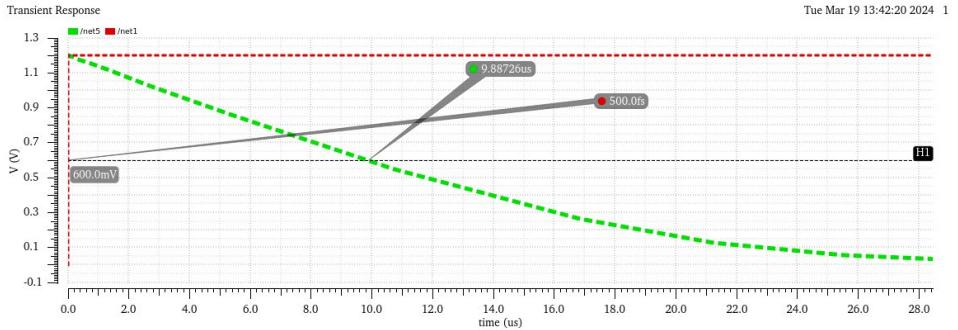
$$R_{on} = 7.854\text{k}\Omega \quad (4)$$

Expected propagation time t_p for two resistive switch model nMOSFETs in series:

$$t_p = 10.84\mu\text{s} \quad (5)$$



(a) Output of circuit A



(b) Output of circuit B

Figure 6: Pulldown transition of circuit A and B. V_{GS} in red and V_{DS} in blue, $V_{sw} = \frac{V_{dd}}{2}$

5 Discussion

5.1 Inaccuracy in measurements

Task 1a: When measuring capacitances in a circuit, it is important to remain aware of several factors that could introduce errors in the measurements. The length of the copper wires, the quality of the soldering, components, and instruments may introduce noise or other parasitic capacitance that alter the measurements. In this experiment, all potential factors have been neglected, with the exception of the oscilloscope probe capacitance which was subtracted from the total capacitance as in accordance with the lab manual.

Task 1b: In figure 5 there are considerable amount of noise distorting the signal. This is especially noticeable in the high-regions of the signal between inverters. Investigation into the cause of this noise considered the oscilloscope probe, the oscilloscope itself and the grounding of the circuit as potential sources of error. The circuit was also replicated once on a new PCB, and also once on a breadboard, but the noise persisted. Changing instruments and cables had little to no effect either. After several attempts to fix the problem and extensive time spent troubleshooting, it was decided, together with the lab supervisor, the noise made it not possible to accurately calculate τ_{LH} , τ_{HL} , R_{ONp} , and R_{ONn} .

As V_{dd} is set to 5 V the expected range of voltages for the input and output signals are 0 - 5 V. In figures 4 and 5 the signals can go both over and under the range. Sources of error discussed in the two above paragraphs could be the cause of this. For task 1A, the points of interest are marked on the graph by method of 'eyeballing', which can cause some inaccuracies in the measurements. The sample rate used to generate the plot is also limiting in how close the points can be marked. All these factors can contribute to the inaccuracy of the measurements and further calculations.

5.2 Repercussions of the Miller effect

In figure 4 there is a noticeable notch in the transition from low-to-high. This kickback on the input happens at the switching point $V_{dd}/2$ in transition and is due to the Miller effect feedback. As

propagation delay is defined to be the time difference between the input and output signal at 50% of the transition, and the miller effect does not eject charge back before the voltage exactly reaches the switching point, the effect is not relevant for the calculations.

5.3 Assement of values

Task 1a: The input capacitance of 8.6 nF is within the expected range as the lab assignment specified that the inherent probe capacitance was too large to not account for.

Task 2: The predicted t_p of the resistive switch model 10.84 μ s, is different from the observed t_p of 9.89 μ s as the lab assignment hinted at. That is a noticeable speedup of 8.764 %. The speedup could be attributed to an increase in the charge mobility, specifically how the geometry of MOSFETs in series may lead to a stronger electric field and by extension drain current. With a higher current the capacitor is discharging faster than accounted for resulting in a switch time faster than a resistive proportionality.

The transition curve from the circuits in task 2 have signs of RC decay at its rising and falling edge, but is pretty linear in between. This aligns with how we modeled the transition period in the resistive switch model. Using a large signal EKV model, we could anticipate that a shorter transition time would potentially be observed in the case of two MOSFETs in series. This prediction comes from the fact that the EKV model takes into account the velocity saturation and channel length modulation of the devices - a phenomena not always accurately represented in simpler MOSFET models. When devices are in series, these effects can lead to faster signal transitions compared to individual devices, especially for larger signals where these effects become more pronounced. Therefore, while it is a somewhat simplified explanation, it is plausible that the EKV model would indeed predict a shorter transition time for two series-connected MOSFETs.

5.4 Comparing task 1 and task 2

By constructing the exercises as has been done in this lab assignment, we can learn different aspects of digital circuits. Task 1 focuses on the input capacitance of a CMOS inverter, while task 2 focuses on the resistive switch model of nMOSFETs in series. The two tasks are related in that they both investigate the switching behavior of digital circuits, but they do so from different perspectives. Task 1 is more focused on the physical properties of the CMOS inverter, while task 2 is more focused on the theoretical properties of the resistive switch model. By comparing the results from the two tasks, we can gain a more comprehensive understanding of the behavior of digital circuits and how they can be analyzed and optimized.

6 Appendix

6.1 Calculations

τ for the input capacitance of the inverter: We find the real voltage span of the inverter by subtracting the maximum and minimum voltage from the plot in figure 4:

$$\begin{aligned}\Delta V &= 5.0675V - (-0.12)V \\ &= 5.1875V\end{aligned}$$

Then we read the time from the x-axis when the voltage reaches 63.2% of the final value.

Input capacitance of the inverter: From equation 1 we solve for C_I with values from figure 4 and adjust the time in accordance with the noted voltage value:

$$\begin{aligned}
\tau &= R_{on} C_{tot} \\
\Rightarrow C_{tot} &= \frac{\tau}{R_{on}} \\
C_I + 15 \text{ pF} &= \frac{\tau}{R_{on}} \\
C_I &= \frac{(6.5 \cdot 10^{-7} \text{ s}) - (-1.71 \cdot 10^{-6} \text{ s})}{100 \text{ k}\Omega} - 15 \text{ pF} \\
C_I &= 8.6 \text{ pF}
\end{aligned}$$

Note: The lab manual states that 15 pF is to be subtracted from the total capacitance to get the input capacitance of the inverter. This is done to account for the capacitance of the oscilloscope probe.

R_{on} from the resistive switch model of nFETs:

$$\begin{aligned}
R_{ON} &= \frac{t_p}{0.69 \cdot C_L} \\
&= \frac{5.419 \mu s}{0.69 \cdot 1nF} \\
&= 7.854k\Omega
\end{aligned}$$

Expected time for two resistive switch model nFETs in series:

$$\begin{aligned}
t_p &= 0.69 \cdot 2R_{on}C_L \\
&= 10.84 \mu s
\end{aligned}$$

References

- [1] Philipp Häfliger. (2024). *Microelectronics Essentials* (beta 0.10). Department of Informatics, University of Oslo.
- [2] Philipp Häfliger (2018). *Excerpt of Sedra/Smith Chapter 15: Inverter Delay* [PDF]. Department of Informatics, University of Oslo. <https://www.uio.no/studier/emner/matnat/ifi/INF3410/h18/forelesningsfoiler/chapter15.pdf>
- [3] Neureuther, A.R. (2001). Lecture 24: CMOS Capacitance and Circuit Delay [PDF]. University of California, Berkeley. https://inst.eecs.berkeley.edu/~ee42/fa01/LectNotes/42_24.pdf