

# IN3170 V24 - Lab 3

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## 1 Task 1

### 1.1 Equipment

Component	Model	Quantity
Resistor	120kΩ	1
Capacitor	390pF	6
Hex inverter	IC CD4007UBE	2
Oscilloscope	HP54622	1
Waveform generator	HP33120	1
Voltage source	HPE3631	1

Table 1: List of components used in task 1.

### 1.2 Objective

The objective of this task is to build two similar current source circuits, one with a CG current conveyor and one without, and observe the voltage discharge of the capacitor when the clock signal of the pFET transistors M2 goes low.

### 1.3 Constructing the circuits

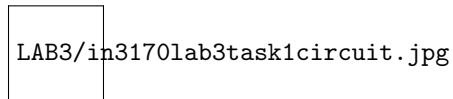


Figure 1: The two current source circuits used

First, we will recreate the circuit from Figure 1 a) in the lab manual. Using the IC CD4007UBE we connected pin 14 to our  $V_{DD}$  of 5V so as to give voltage to the Q1 pFET and the bulk of the pFETs. We connect pin 13, the source for pFETs, to the resistor and capacitors in parallel, and then to GND. Here we have replaced the  $100k\Omega$  resistor with a  $120k\Omega$ . And the  $1\mu F$  capacitor with three  $390pF$  capacitors in parallel, totaling to  $1.17nF$ . This difference is significant as it is approximately three orders of magnitude less than the initial design value. Then, through the gate at pin 6, we connect a  $5V_{pp}$  CLK signal.

To make the circuit from Figure 1 b) in the lab manual, connect the  $V_{DD}$  to pin 14. Pin 13 is connected to the Q2 nFET through the drain at pin 5, the source at pin 4 is connected to the  $120K\Omega$  resistor and further to GND. We apply a voltage ( $V_{bias\_cascode}$ ) to the nFET at the pin 3 gate. Pin 13 is also connected to the capacitors, forming a parallel with the resistor and nFET, and then connected to GND. Then, connect the Q1 gate at pin 6 to the CLK signal and pin 7, the bulk of the nFETs, to GND.

The voltage on C would be a constant voltage, as the current source would be able to supply a constant current to the capacitor. The voltage on the capacitor would then be given by the formula  $V = \frac{Q}{C}$ , where  $Q$  is the charge on the capacitor and  $C$  is the capacitance of the capacitor. The charge on the capacitor is given by  $Q = I \cdot t$ , where  $I$  is the current and  $t$  is the time. As the current is constant, the charge on the capacitor will be linear with time, and the voltage on the capacitor will be linear with time.

As the  $100k\Omega$  resistor was not available at the lab we used a  $120k\Omega$  instead. As per lab instructions we calculated the current through the resistor at 1V to be

$$I = \frac{V}{R} = \frac{1V}{120k\Omega} = 8.33\mu A \quad (1)$$

To get the discharge curve we used the  $I = \frac{V}{dt}C$  relation to get the time it would take for the voltage to drop to 0V, which would be the time it takes for the capacitor to discharge through the resistor.

$$I = \frac{V}{dt}C \Rightarrow dt = \frac{V}{I}C = \frac{5V}{8.33\mu A} \cdot 3 * 0.39nF = 0.702ms \quad (2)$$

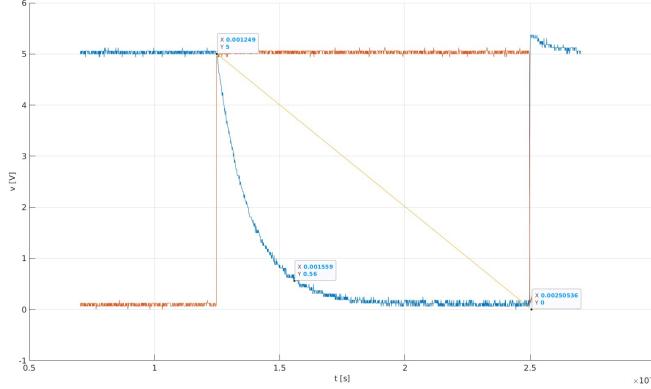


Figure 2: Plot of the circuit in figure 1 a) in the lab manual with the ideal discharge curve in yellow.

As seen in 3 the actual discharge curve is not linear, but rather exponential as per a capacitors normal discharge characteristics. This is due to the fact that M2s gate voltage is 0V when the clocked signal is low which gives a  $|V_{GS}||V_{TH}|$ , moving the pFET from saturation to cutoff. With no voltage at the gate, the pFET will not conduct any current, and the capacitor will discharge through the resistor. The voltage on the capacitor will then be given by  $V = V_{DD} \cdot e^{-\frac{t}{RC}}$ , where  $R$  is the resistance and  $C$  is the capacitance of the capacitor.

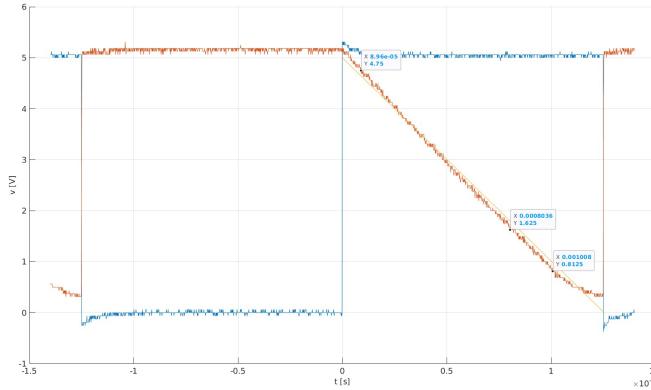


Figure 3: Plot of the circuit in figure 1 b) in the lab manual with the ideal discharge curve in yellow.

In stark contrast to the previous circuit, the circuit in 4 follows the theoretical curve down to what we observe to be around 1.2V when we apply 3V on the gate of M1. This is because of the relations  $I_D$  and  $V_{DS}$  in saturation and triode region. We have that:

$$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 (1 - \lambda \cdot V_{DS}) \quad (3)$$

for the saturation region, aka when  $V_{DS} \geq V_{GS} - V_{TH}$ , and  $V_{GS} \geq V_{TH}$ . For the triode region, aka when  $V_{DS} < V_{GS} - V_{TH}$ , and  $V_{GS} \geq V_{TH}$ , we have that:

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) \cdot V_{DS} \quad (4)$$

From the equations above we can observe

## 2 Task 2

### Objective

The objective of this task is to improve a current source using a FET in saturation. By simulating the circuit in Cadence one can plot the  $I_D$  vs  $V_{DS}$  curve and calculate the output resistance  $r_{ds}$  of the current source. Further, changing the design parameter  $\frac{W}{L}$  of the FET, or adding a voltage cascode to the circuit is carried out to improve the current source capability.

### Theory

In an ideal current source, the output current is independent of the voltage across the terminals. I.e. the current source maintains the same current throughout the circuit, despite changes to  $V_{DS}$ .

A Field-Effect Transistor (FET) operating in the saturation region exhibits the same characteristics as an ideal current source. This can be seen from the  $I_D$  vs  $V_{DS}$  curve in the saturation region, where the current is almost constant. This is because when  $V_{DS}$  approaches the saturation region it becomes high enough that it maxes out the number of charge carriers that can contribute to current flow, making the gate voltage the primary factor to the current flow.

In the plot, the curve will flatten out in this region. In a practical FET, the curve will not be completely flat (indicating that the current is not completely constant), but it will give a good approximation of an ideal current source.

## Designing a current source

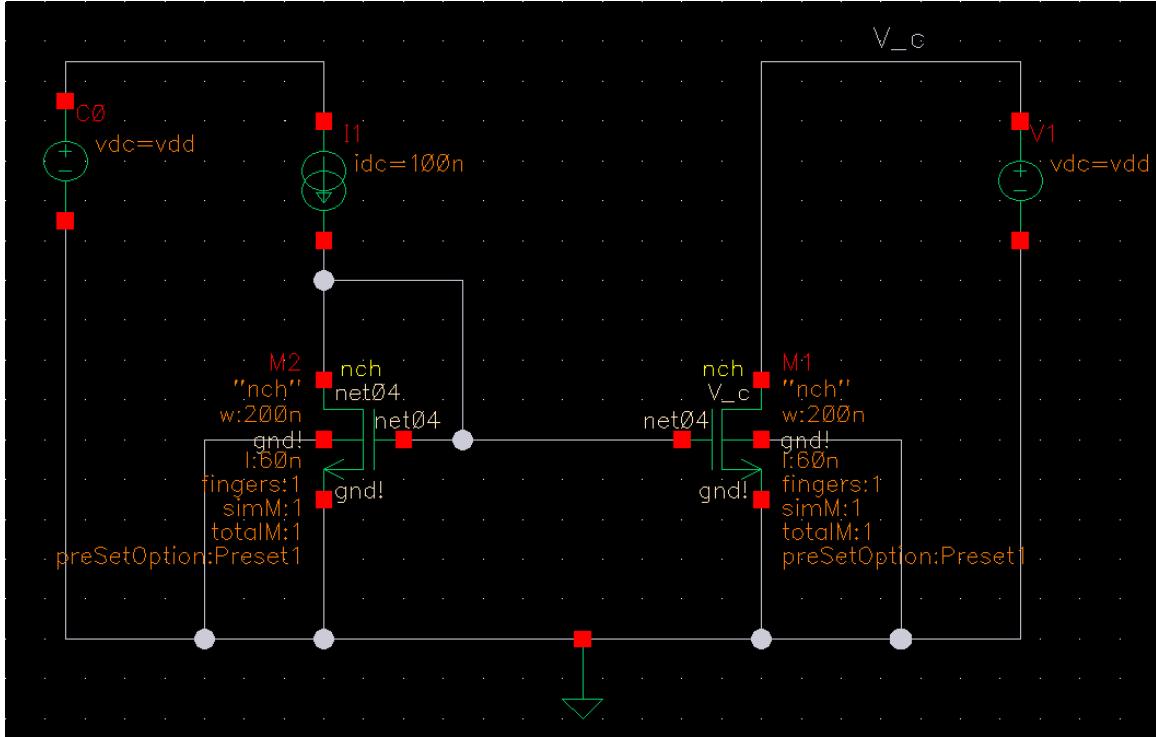


Figure 4: Screencapture of the circuit in figure 1 c) from the lab manual simulated in Cadence.

This design differs a bit from figure 1 d) in the lab manual, following the suggested method of the manual. The bias current is implemented as a current mirror, consisting of  $M_2$  and  $I_1$ , which sets the current that flows through  $M_1$ . Instead of a capacitor in parallel to  $M_1$ , and a clock signal to  $M_2$ , a DC voltage source is used to sweep the voltage  $V_C$  in a range simulating the  $V_{DS}$  of  $M_1$ .

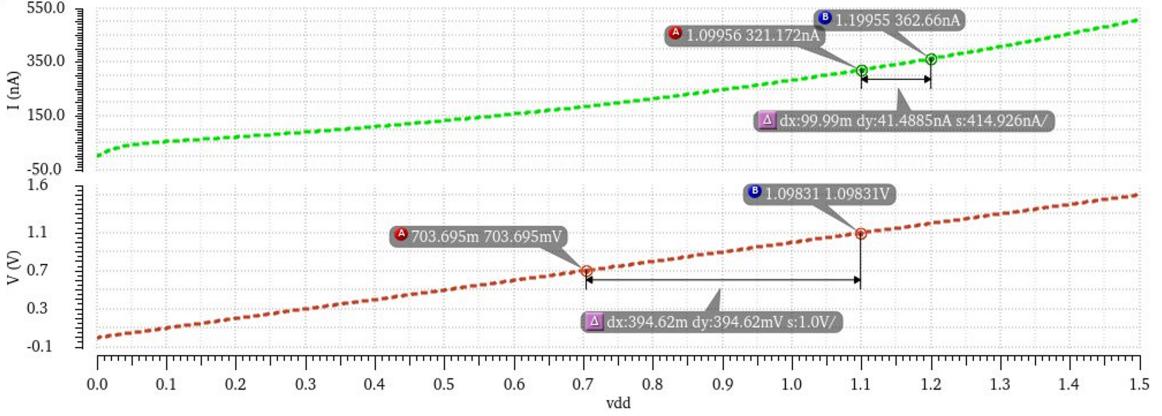


Figure 5: Screencapture of the DC sweep of the circuit in figure 1.

$\Delta I_D$  is calculated as the difference between two points on the *most linear* part of the curve. In figure 6, this is chosen to be a segment at the end of the curve. The DC sweep simulation is set to sweep from 0 V to 1.5 V. The lab manual specifies to use only up to 1.2 V, hence the last point is chosen to be close up to 1.2 V.

$$\Delta I_D = 414.926 \text{ nA} \quad (5)$$

The same method is used to calculate  $\Delta V_{DS}$ , however as  $V_C$  is the sweep parameter, the voltage rises linearly. The difference between two points on this line will be the same wherever. In figure 6, the points are chosen arbitrarily.

$$\Delta V_{DS} = 1 \text{ V} \quad (6)$$

$r_{ds}$  can then simply be calculated using Ohm's Law:

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1 \text{ V}}{414.926 \text{ nA}} = 2.4007 \text{ M}\Omega \quad (7)$$

The next task is to tinker with the design parameter  $\frac{W}{L}$  of  $M1$  in order to improve the current source capability. Even in saturation, real FETs exhibit channel-length modulation, which is a phenomenon where the effective channel length shortens as  $V_{DS}$  increases, leading to a non-ideal increase in current. By increasing the channel length  $L$  of the transistor, the channel-length modulation is reduced, and the current source capability is improved. In this report the channel length was increased to  $L = 1 \mu\text{m}$ . This is an exaggeration of what a normal channel length would be, but will highlight the difference more. A DC sweep is then performed again, resulting in the following plot:

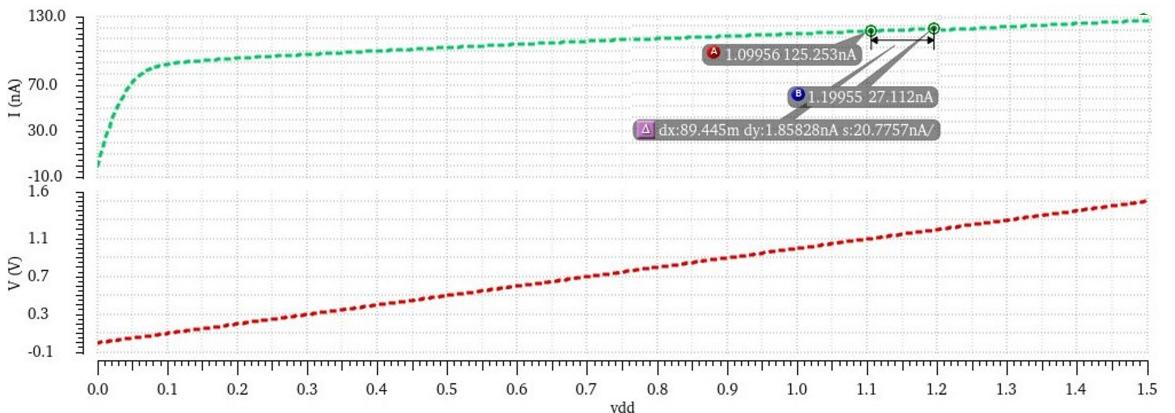


Figure 6: Screencapture of the DC sweep of the circuit in figure 1 with  $L = 1 \mu\text{m}$  for  $M1$  and  $M2$ .

For the circuit in figure 7, the same method is used to calculate  $\Delta I_D$  and  $\Delta V_{DS}$  as for the previous circuit.  $r_{ds}$  is then:

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1 \text{ V}}{20.7757 \text{ nA}} = 4.8133 \text{ M}\Omega \quad (8)$$

In a ideal current source, the output resistance (or  $V_{ds}$ ) is infinite. The new  $r_{ds}$  is higher than the previous, which indicates a better approximation of an ideal current source.

## Implementing a voltage cascode

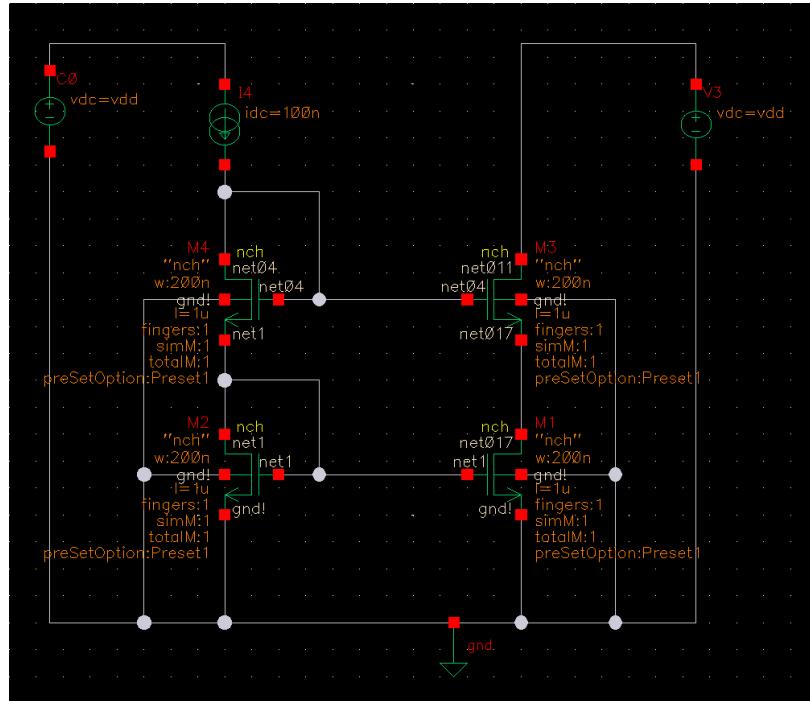


Figure 7: Screencapture of the circuit in figure 1 d) from the lab manual simulated in Cadence.

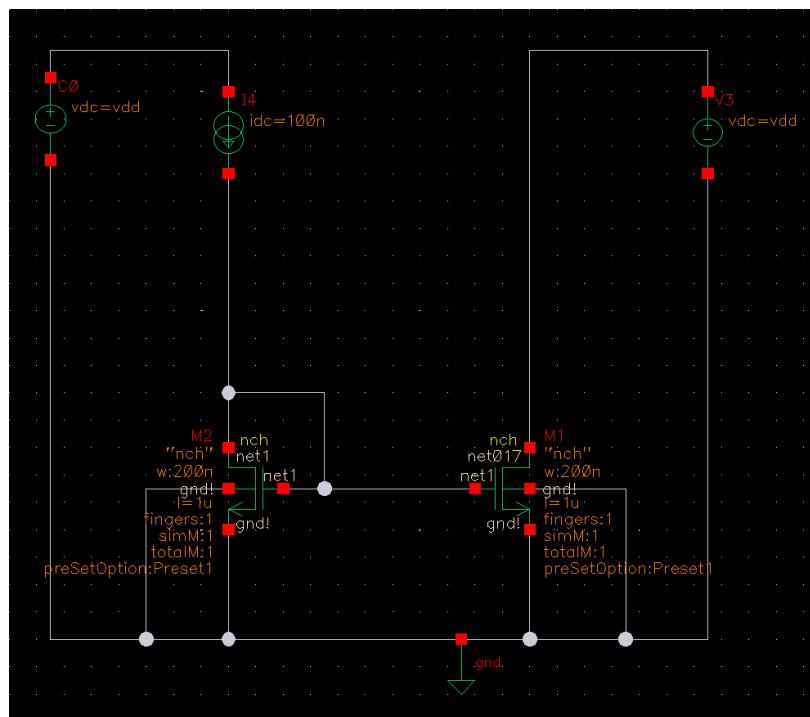


Figure 8: Screencapture of the circuit in figure 1 d) from the lab manual without the voltage cascode.

In similar fashion as the previous circuits, a DC sweep is performed for the circuit in figure 8 and 9:

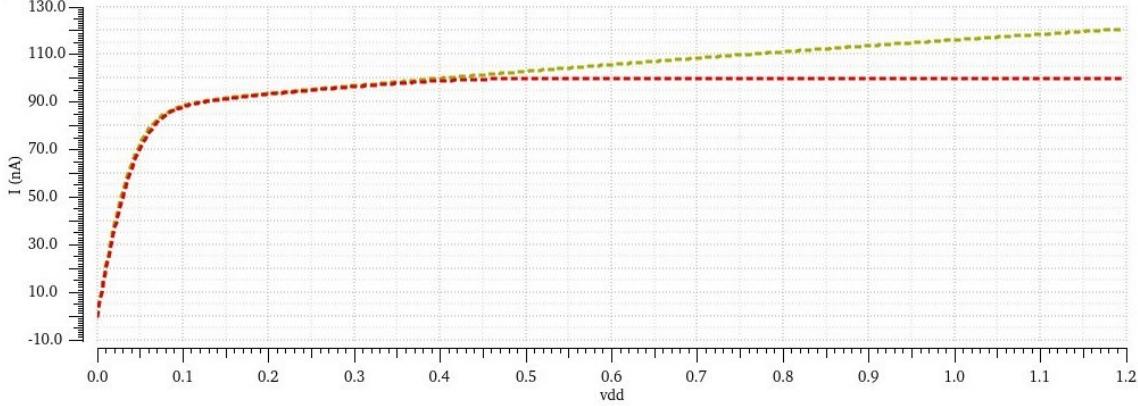


Figure 9: Screencapture of the DC sweep of both circuits in figure 1 d).

In figure 10, the red curve is the simulated  $I_D$  vs  $V_C$  for the circuit in figure 8. The yellow curve is equivalent curve for the circuit in figure 9 plotted alongside for comparison.

Initially one can observe the two curves start off nearly identical. As  $V_C$  increases, the current in both circuits begins with a sharp rise but starts to flatten as the transistors approach the saturation region. The cascode configuration, however, shows a distinct change in behavior around 0.4 V where the current flattens out even more. This enhanced flattening is due to the cascode transistor  $M_3$ , which further restricts the increase in current by also entering saturation and increasing the circuit's output impedance.

Some trade-offs associated with using a cascode configuration include a reduced voltage headroom. That is, the circuit requires a minimum voltage drop across each transistor to ensure that both are operating in saturation. Essentially, the drain-source voltage  $V_{DS}$  of the cascode transistor  $M_3$  must be sufficiently high for it to remain in saturation. A cascode circuit also adds complexity to the system that might be unnecessary. If the applied voltage range is small, there will be no benefit to using a cascode configuration, as the cascode transistor will not enter saturation.