

IN3170 V24 - Lab 3

Andreas Engøy, Simen Norrud, Erik Røset & Daniel Tran

May 2024

1 Task 1

1.1 Equipment

Component	Model	Quantity
Resistor	120kΩ	1
Capacitor	390pF	3

Table 1: List of components used in task 1.

2 Task 2

In an ideal current source, the output current is independent of the voltage across the terminals. I.e. the current source maintains the same current throughout the circuit, despite changes to V_{DS} .

A Field-Effect Transistor (FET) operating in the saturation region exhibits the same characteristics as an ideal current source. This can be seen from the I_D vs V_{DS} curve in the saturation region, where the current is almost constant. This is because when V_{DS} approaches the saturation region it becomes high enough that it maxes out the number of charge carriers that can contribute to current flow, making the gate voltage the primary factor to the current flow.

In the plot, the curve will flatten out in this region. In a practical FET, the curve will not be completely flat (indicating that the current is not completely constant), but it will give a good approximation of an ideal current source.

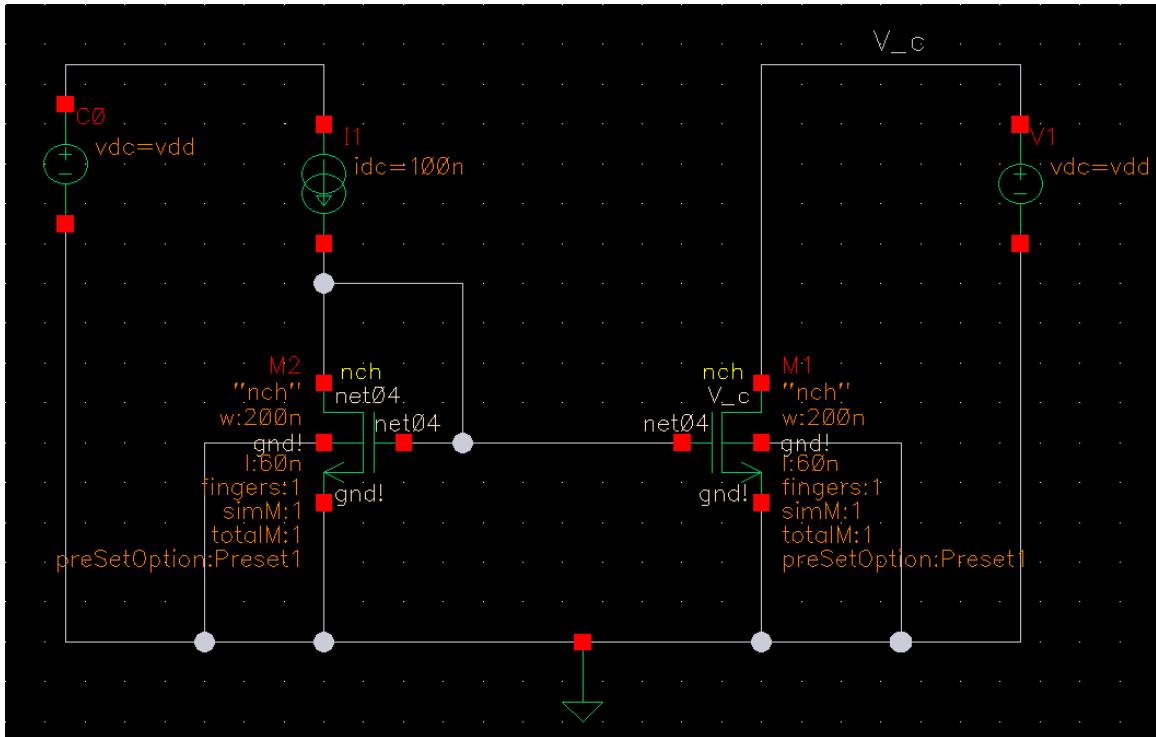


Figure 1: Screencapture of the circuit in figure 1 c) from the lab manual simulated in Cadence.

The bias current is implemented as a current mirror, consisting of M_2 and I_1 , which sets the current that flows through M_1 .

As suggested in the lab manual, a DC analysis is performed with V_C as a sweep parameter. This results in the following plot:

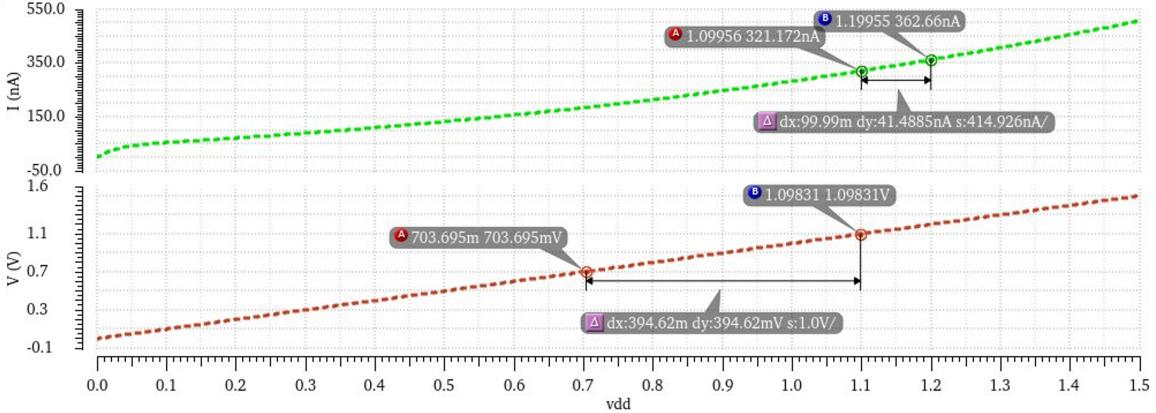


Figure 2: Screenshot of the DC sweep of the circuit in figure 1.

ΔI_D is calculated as the difference between two points on the *most linear* part of the curve. In figure 2, this is chosen to be a segment at the end of the curve. The DC sweep simulation is set to sweep from 0 V to 1.5 V. The lab manual specifies to use only up to 1.2 V, hence the last point is chosen to be close up to 1.2 V.

$$\Delta I_D = 414.926 \text{ nA} \quad (1)$$

The same method is used to calculate ΔV_{DS} , however as V_C is the sweep parameter, the voltage rises linearly. The difference between two points on this line will be the same wherever. In figure 2, the points are chosen arbitrarily.

$$\Delta V_{DS} = 1 \text{ V} \quad (2)$$

r_{ds} can then simply be calculated using Ohm's Law:

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1 \text{ V}}{414.926 \text{ nA}} = 2.4007 \text{ M}\Omega \quad (3)$$

The next task is to tinker with the design parameter $\frac{W}{L}$ of $M1$ in order to improve the current source capability. Even in saturation, real FETs exhibit channel-length modulation, which is a phenomenon where the effective channel length shortens as V_{DS} increases, leading to a non-ideal increase in current. By increasing the channel length L of the transistor, the channel-length modulation is reduced, and the current source capability is improved. In this report the channel length was increased to $L = 1 \mu\text{m}$. This is an exaggeration of what a normal channel length would be, but will highlight the difference more. A DC sweep is then performed again, resulting in the following plot:

For the circuit in figure 3, the same method is used to calculate ΔI_D and ΔV_{DS} as for the previous circuit. r_{ds} is then:

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1 \text{ V}}{20.7757 \text{ nA}} = 4.8133 \text{ M}\Omega \quad (4)$$

In an ideal current source, the output resistance (or V_{ds}) is infinite. The new r_{ds} is higher than the previous, which indicates a better approximation of an ideal current source.

Implementing a voltage cascode

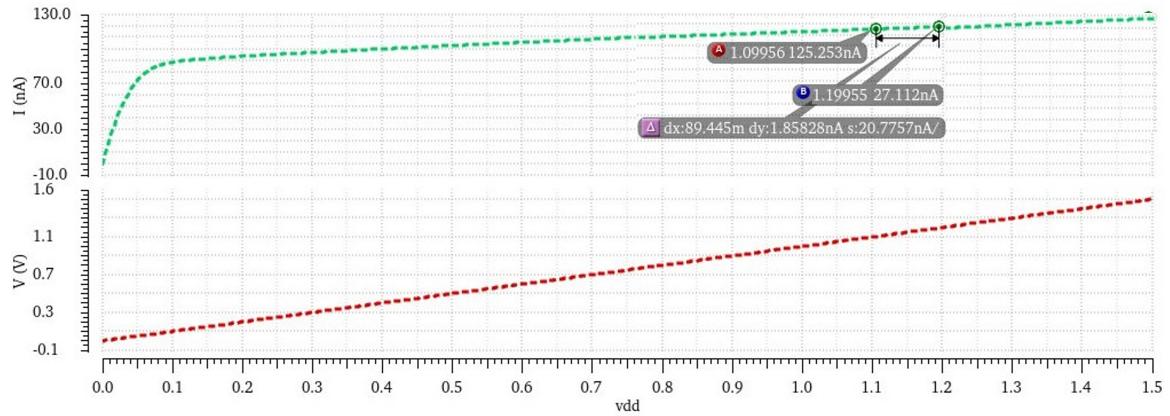


Figure 3: Screencapture of the DC sweep of the circuit in figure 1 with $L = 1 \mu\text{m}$ for $M1$ and $M2$.

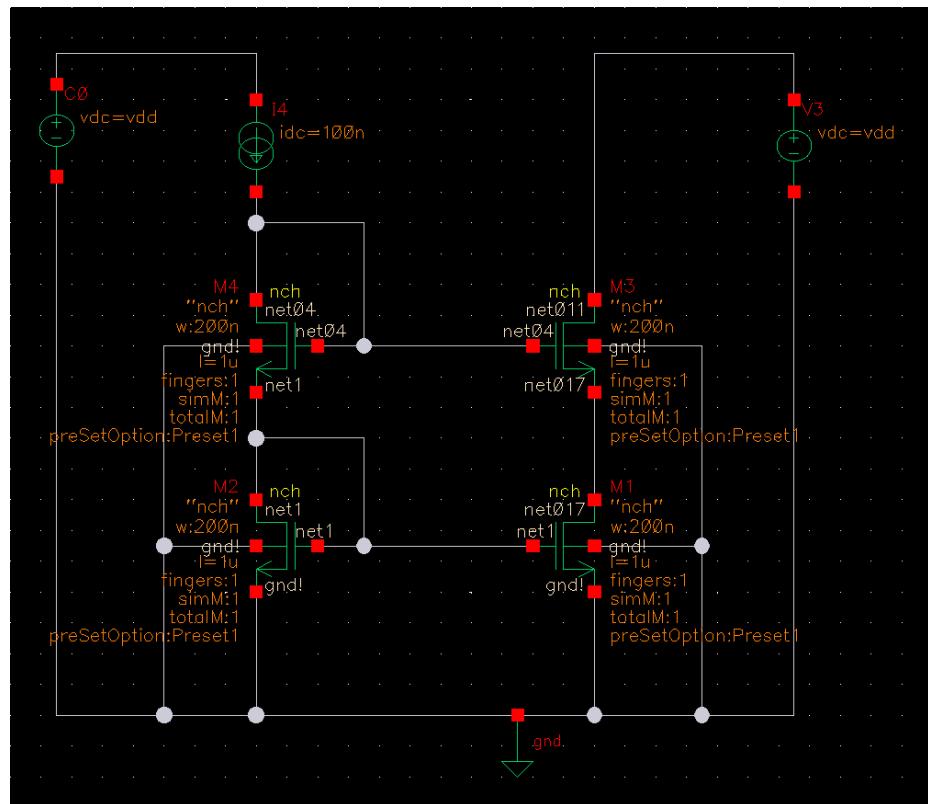


Figure 4: Screencapture of the circuit in figure 1 d) from the lab manual simulated in Cadence.

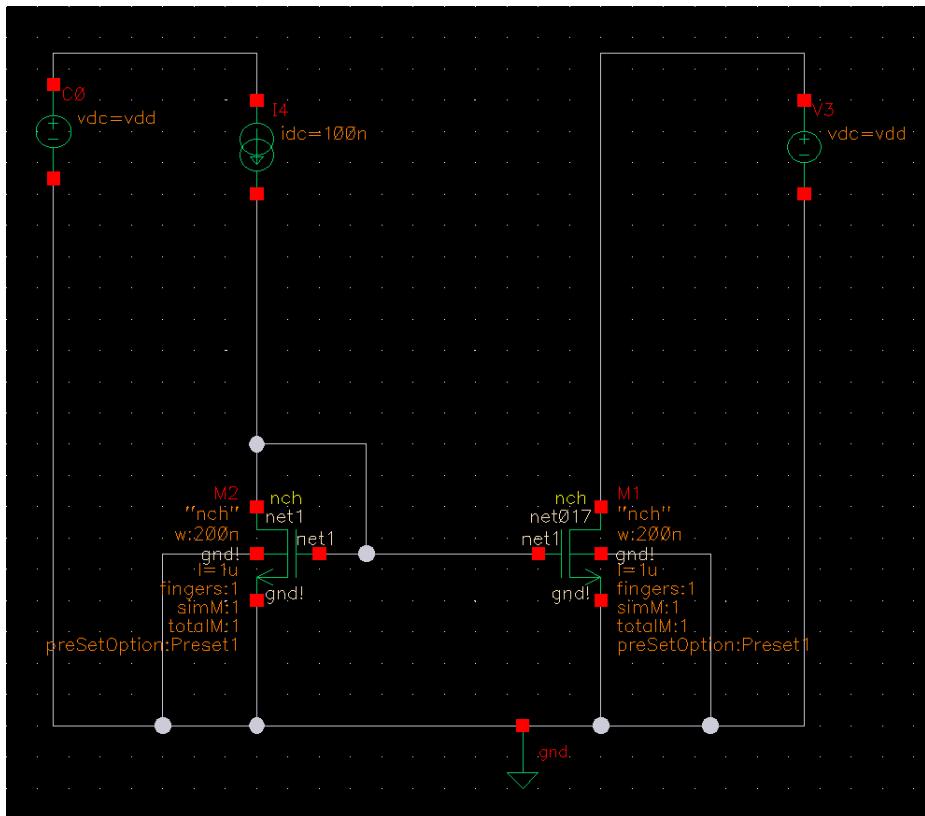


Figure 5: Screencapture of the circuit in figure 1 d) from the lab manual without the voltage cascode simulated in Cadence.

In similar fashion as the previous circuits, a DC sweep is performed for the circuit in figure 4 and 5:

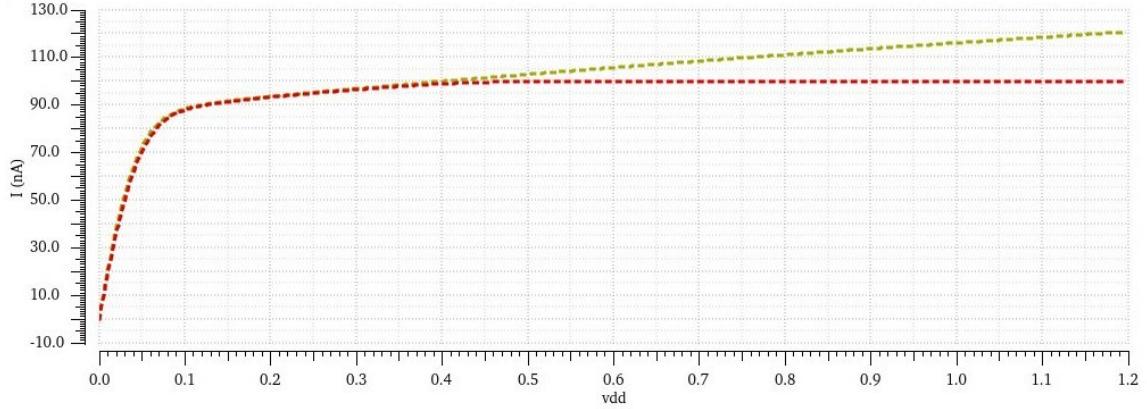


Figure 6: Screencapture of the DC sweep of both circuits in figure 1 d).

In figure 6, the red curve is the simulated I_D vs V_C for the circuit in figure 4. The yellow curve is equivalent curve for the circuit in figure 5 plotted alongside for comparison.

One can see that the two curves start off close to identical. As V_C increases, the current in the circuit starts with a sharp rise, that flattens out as the transistor reaches the saturation region. The cascode kicks in around 0.4 V, and the current flattens out more for that circuit. This is because the cascode transistor $M3$ also reaches saturation.

Some trade-offs of using a cascode is that the circuit will have a reduced voltage headroom. Meaning there is a minimum voltage required for the circuit to operate properly. This is because the cascode transistor $M3$ will not be in saturation if the voltage is too low. The cascode also increases the complexity of the circuit, and will require more power to operate.