IN3170 V24 - Lab 3

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1 Task 1

1.1 Equipment

Component	Model	Quantity
Resistor	120kΩ	1
Capacitor	390pF	3

Table 1: List of components used in task 1.

2 Task 2

In an ideal current source, the output current is independent of the voltage across the terminals. I.e. the current source maintains the same current throughout the circuit, despite changes to V_{DS}.

A Field-Effect Transistor (FET) operating in the saturation region exhibits the same characteristics as an ideal current source. This can be seen from the I_D vs V_{DS} curve in the saturation region, where the current is almost constant. This is because V_{DS} approching the saturation region is high enough that it has maxed out the number of charge carriers that can contribute to current flow, making the gate voltage the primarily factor to the current flow.

In the plot, the curve will flatten out in this region. In a practical FET, the curve will not be completely flat (indicating that the current is not completely constant), but it will give a good approximation of an ideal current source.

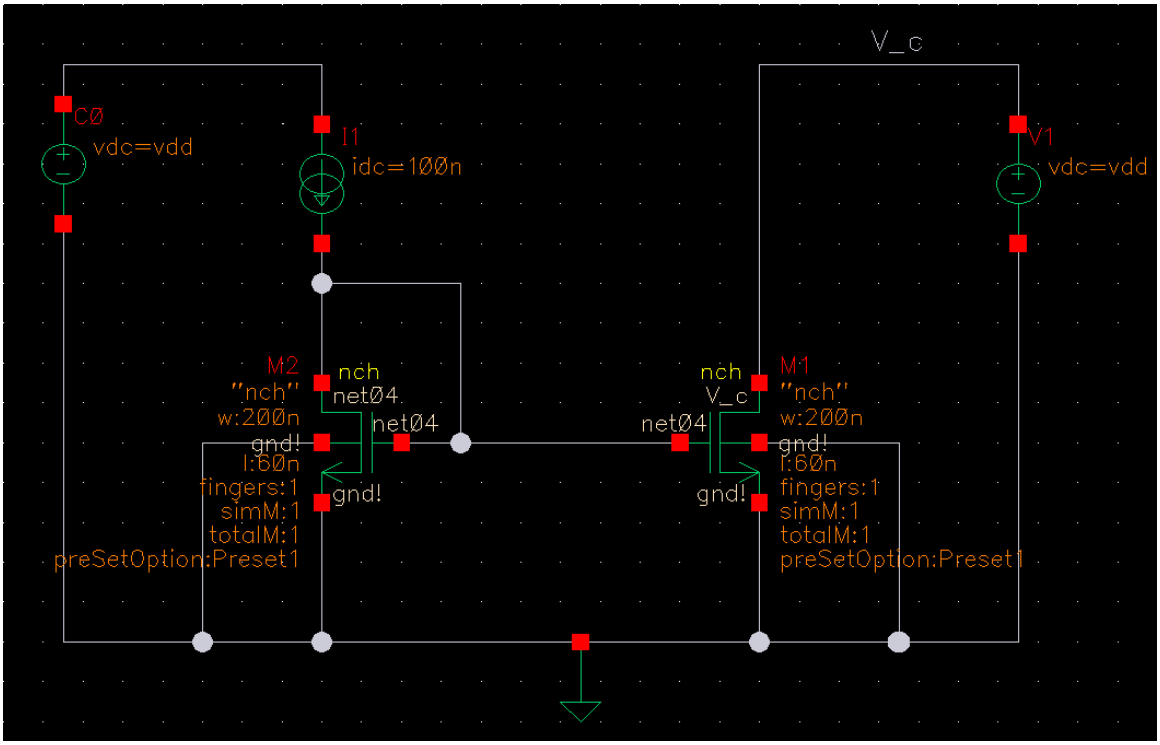

Figure 1: Screencapture of the circuit in figure 1 c) from the lab manual simulated in Cadence.

The bias current is implementet as a current mirror, consisting of $M2$ and $I4$, which sets the current that flows through $M1$.

As suggested in the lab manual, a DC analysis is performed with V_C as a sweep parameter. This results in the following plot:

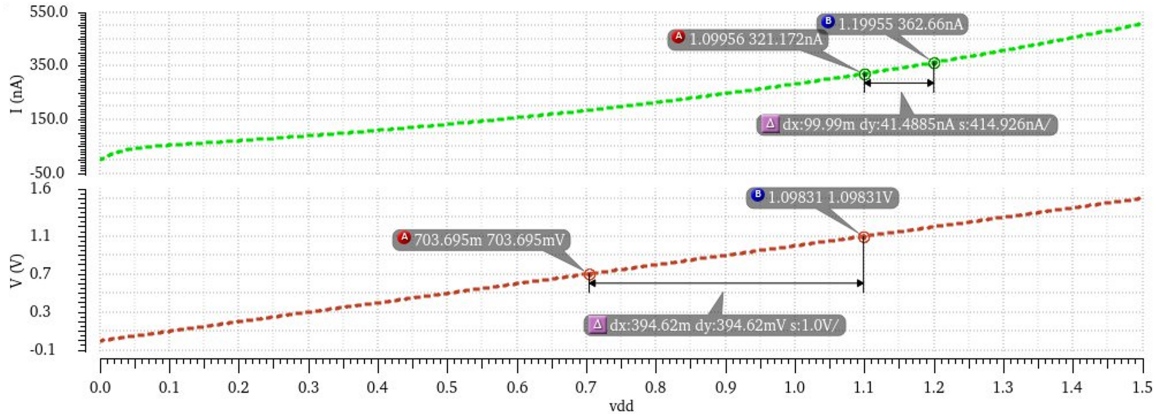

Figure 2: Screencapture of the DC sweep of the circuit in figure 1.

ΔI_D is calculated as the difference between two points on the *most linear* part of the curve. In figure 2, this is chosen to be a segment at the end of the curve. The DC sweep simulation is set to sweep from 0 V to 1.5 V.The lab manual specifies to use only up to 1.2 V, hence the last point is chosen to be close up to 1.2 V.

$$\Delta I_D = 414.926 \text{ nA} \tag{1}$$

The same method is used to calculate ΔV_{DS}, however as V_C is the sweep parameter, the voltage rises lineary. The difference between two points on this line will be the same wherever. In figure 2, the points are chosen arbitrarily.

$$\Delta V_{DS} = 1 \text{ V} \tag{2}$$

R_{ds} can then simply be calculated using Ohms Law:

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1 \text{ V}}{414.926 \text{ nA}} = 2.4007 \text{ M}\Omega \tag{3}$$

The next step is to tinker with the designparameter $\frac{W}{L}$ of $(M1)$ in order to better it as a current source. For this rapport, the length L was increased to 1 μm from the default 60 nm. The DC sweep is then performed again, resulting in the following plot:

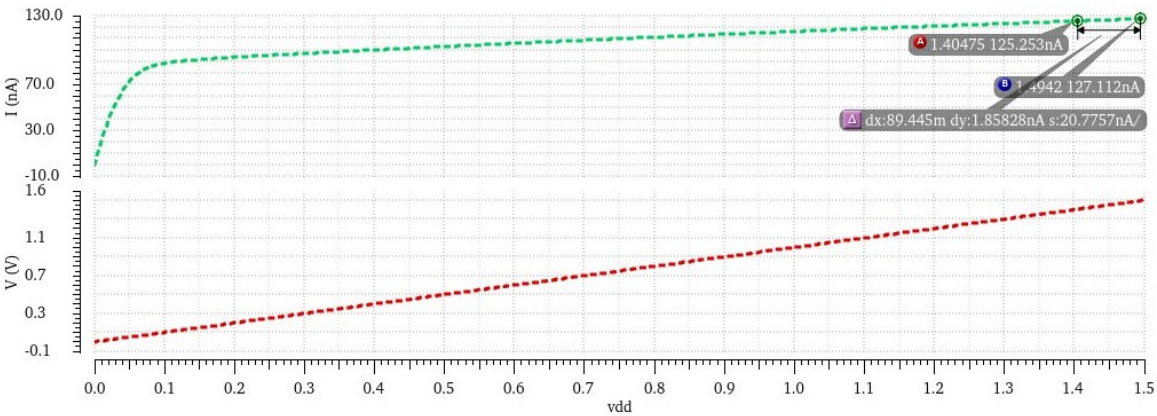

Figure 3: Screencapture of the DC sweep of the circuit in figure 1 with $L = 1$ μm for $M1$ and $M2$.

For the circuit in figure 3, the same method is used to calculate ΔI_D and ΔV_{DS} as for the previous circuit. r_{ds} is then calculated as:

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1\text{ V}}{20.7757\text{ nA}} = 4.8133\text{ M}\Omega \tag{4}$$

Implementing a voltage cascode

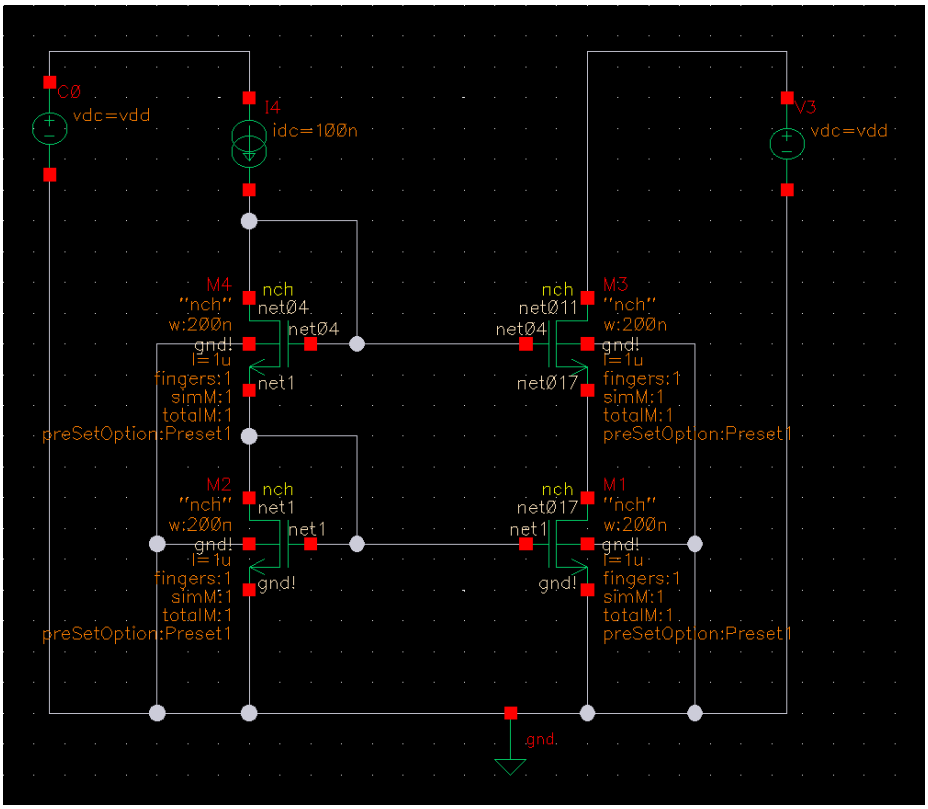

Figure 4: Screencapture of the circuit in figure 1 d) from the lab manual simulated in Cadence.

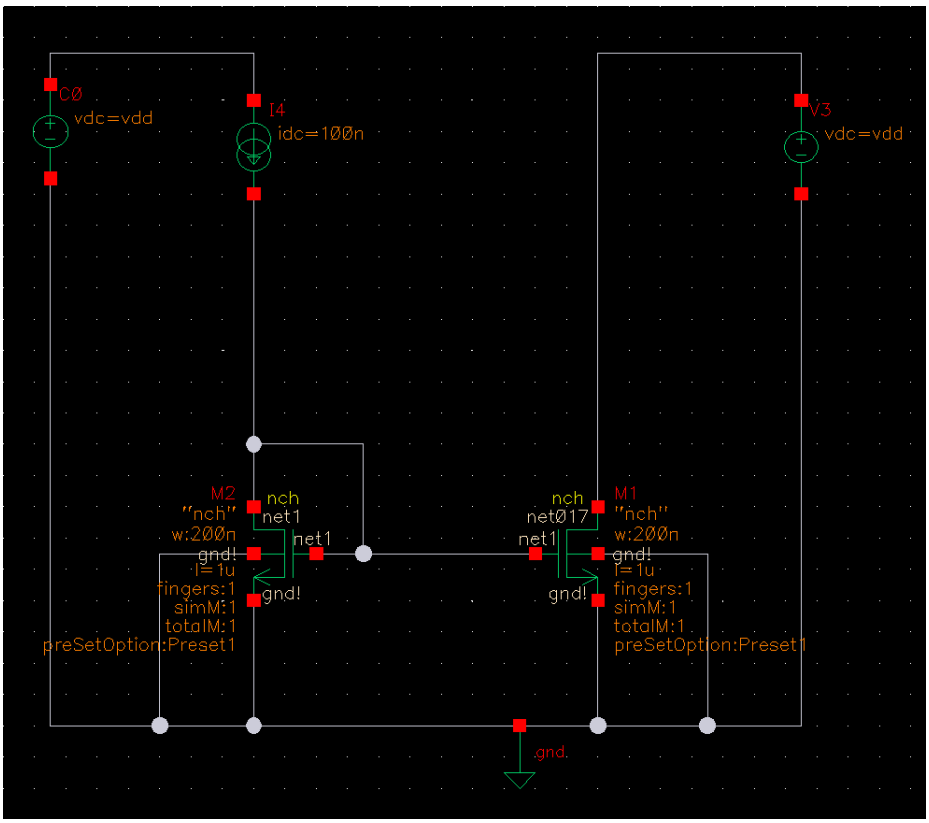

Figure 5: Screencapture of the circuit in figure 1 d) from the lab manual without the voltage cascode simulated in Cadence.

In similar fashion as the previous circuits, a DC sweep is performed for the circuit in figure 4 and 5. The result is shown in figure 6.

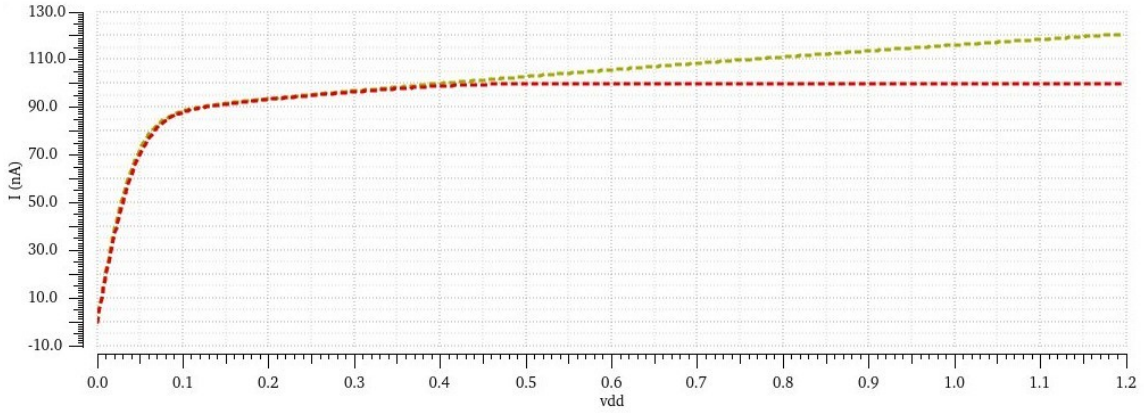

Figure 6: Screencapture of the DC sweep of both circuits in figure 1 d).

In figure 6, the red curve is the simulated I_D vs V_C for the circuit in figure 4. The yellow curve is equivalent curve for the circuit in figure 5 plotted alongside for comparison.