IN5180 - Lab 1

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Part 1: Square law model vs simulation

Task 1

In this task we have been given these specifications:

$$A_v = 5.0V/V \tag{1}$$

$$L_{min} = 90nm \tag{2}$$

$$C_L = 80fF \tag{3}$$

$$\text{Unity gain frequency } (UGF) > 6GHz \tag{4}$$

$$V_{eff} \sim 250mV \tag{5}$$

By using these specifications and the MOSFET parameters for a $45nm$ NMOS transistor, we will be able to find the transistor width W in a single stage amplifier by using the square law model.
First thing is to find the transconductance g_m. By using this formula for UGF:

$$UGF = \frac{g_m}{2\pi C_L} \tag{6}$$

We can find the transconductance g_m by

$$\begin{aligned} g_m &= UGF \cdot 2\pi C_L \\ => g_m &= 6GHz \cdot 2\pi \cdot 80fF = 3.016mS \end{aligned} \tag{7}$$

By using the transconductance g_m that was calculated, we can find the drain current I_D with this formula for V_{eff}:

$$V_eff = \frac{2I_D}{g_m} \tag{8}$$

$$\begin{aligned} I_D &= \frac{V_{eff} \cdot g_m}{2} \\ => I_D &= \frac{250mV \cdot 3.016mS}{2} = 377\mu A \end{aligned} \tag{9}$$

By using the same formula (8), it will now be possible to find the width of the transistor.

$$\begin{aligned} V_eff &= \frac{2I_D}{g_m} \\ => V_eff &= \frac{2I_D}{\mu C_{ox}\frac{W}{L}V_{eff}} \\ => W &= \frac{2I_D L}{\mu C_{ox} V_{eff}^2} \\ => W &= \frac{2 \cdot 377\mu A \cdot 1.5 \cdot 90nm}{280\frac{\mu A}{V^2} \cdot 250mV^2} = 5.8\mu m \end{aligned} \tag{10}$$

Notice that the length used was $L = 1.5 \cdot L_{min}$ and that the μC_{ox} was given by the MOSFET parameters, as mentioned earlier. We also need to find R_L to give the correct DC voltage gain A_v. Voltage gain is given by:

$$A_v = g_m R_L \tag{11}$$

By using formula 11, we find that R_L:

$$\begin{aligned} R_L &= \frac{A_v}{g_m} \\ => R_L &= \frac{5V/V}{3.016mS} = 1658\Omega \end{aligned} \tag{12}$$

Task 2

By using the given specifications and calculated values from task 1, we get this schematic of a common source (CS) amplifier.

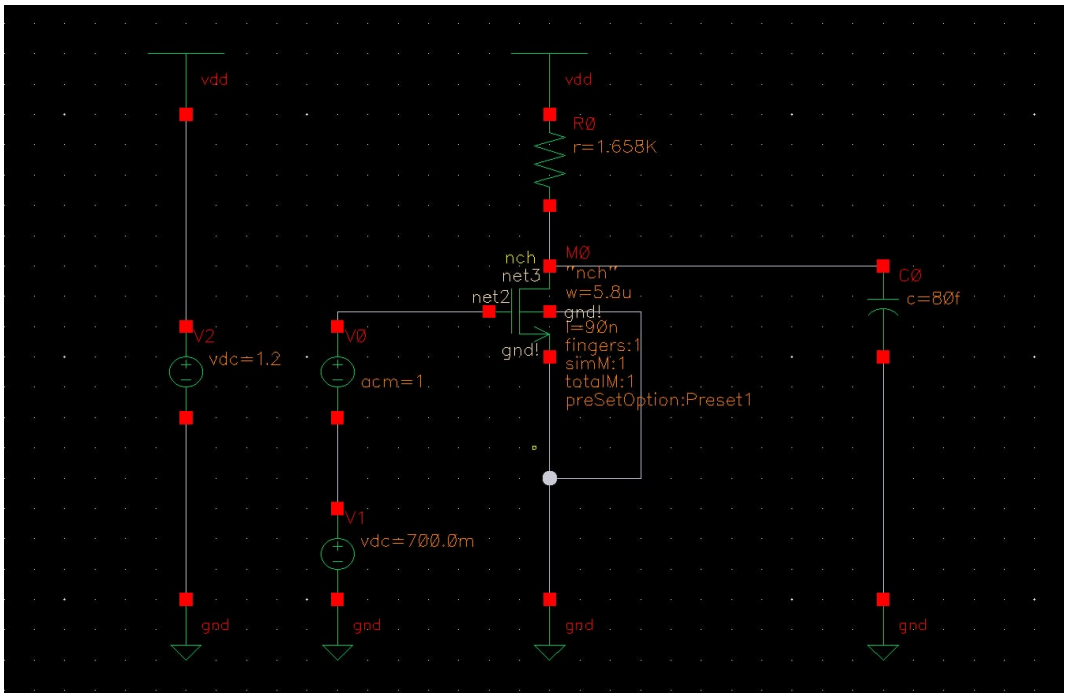

Figure 1: Common source amplifier

Simulating the common source amplifier from Figure 1, gives us this plot of the DC gain over the bandwidth. Where the x-axis is the DC gain and the y-axis is the unity gain frequency.

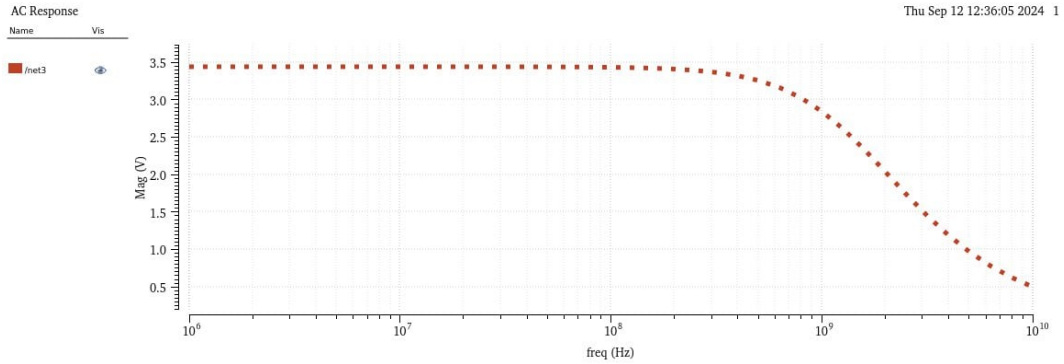

Figure 2: DC gain over bandwidth

From the plot we sees that the DC gain is $A_v = 3.5V/V$ and that the bandwidth is $UGF = 1GHz$. Far below the initial calculated specifications where DC gain $A_v = 5/5$ and $UGF > 6GHz$. The reason for why the values from the simulation is so off compared to the calculated specifications is because of the use of the square law model. The square law model is a simplified representation of MOSFET behaviour, and does not take into factor for example channel-length modulation or threshold voltage modulation. Square law equations are sufficiently accurate for predicting drain current.

Part 2: $\frac{g_m}{I_D}$ - Lookup table generation

Task 3

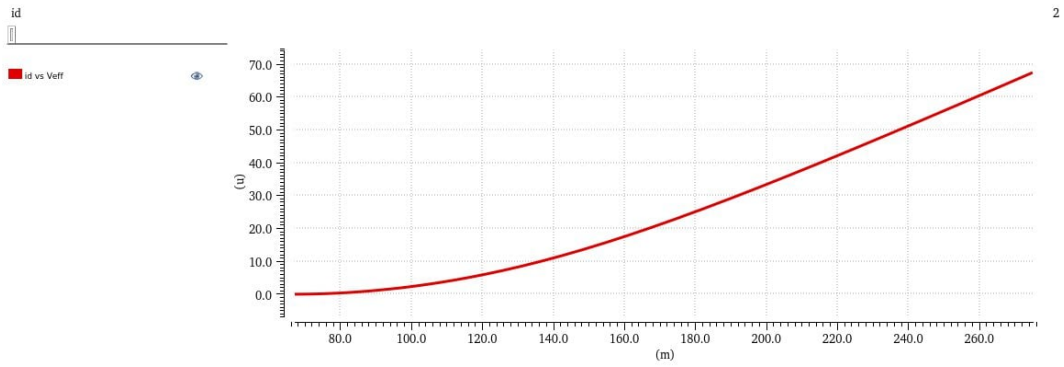

Figure 3: I_D vs V_{eff}

The plot from Figure 3 shows us the relation between I_D and V_{eff}. From the plot we sees that when V_{eff} increases, the drain current I_D also increases, almost linear to V_{eff}. This means that if you apply a higher voltage to the gate, the I_D increases. In other words, V_{GS} controls the conductivity of the MOSFET channel.

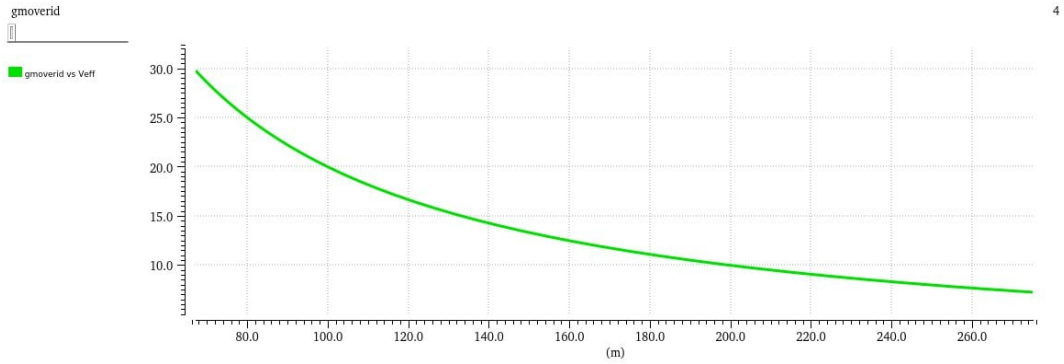

Figure 4: $\frac{g_m}{I_D}$ vs V_{eff}

The plot from Figure 4 shows us the relation between $\frac{g_m}{I_D}$ and V_{eff}. Before we talk about the relation between $\frac{g_m}{I_D}$ and V_{eff}, lets talk about transconductance over drain current, $\frac{g_m}{I_D}$ first. It is possible to say that the relation between g_m and I_D is how efficient the transistor is. This means that you would want a transistor with a high $\frac{g_m}{I_D}$ ratio. If we now look at the relation between $\frac{g_m}{I_D}$ and V_{eff} from the plot shown in Figure 4. We sees that the transistor efficiency decreases when V_{GS} increases. This means that you generally prefer to operate at a lower V_{GS} for a more efficient transistor.

Task 4

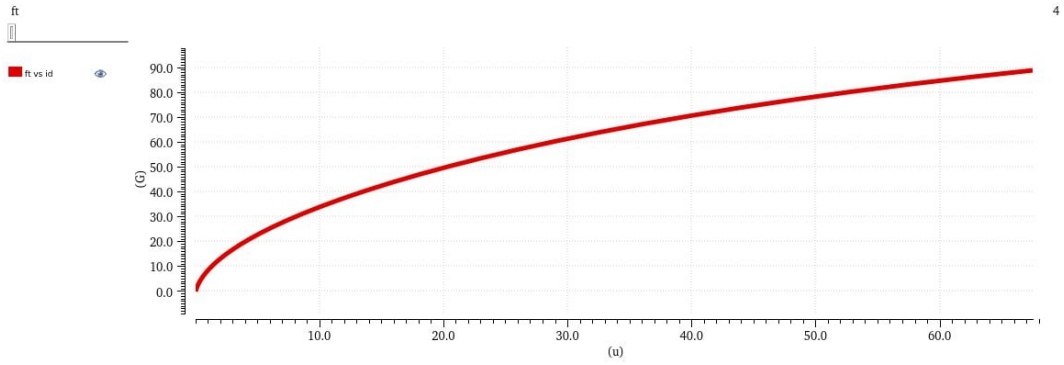

Figure 5: f_t vs I_D

The plot from Figure 5 shows us the relation between f_t and I_D. From the plot we can see that the f_t gradually decreases when we increase I_D. f_t sets and upper limit on the frequency range over which the MOSFET can function effectively as an amplifier. This is relevant for when designing a amplifier, because we aim to strike a balance between power consumption and high-frequency performance.

Part 3: $\frac{g_m}{I_D}$ - Amplifier design

To choose an appropriate value for gm/Id in an amplifier design you firstly have to consider the Transition Frequency (or Cutoff Frequency), ft. It is by definition the frequency at which the current gain of the transistor (β or hfe) falls to unity (1) when the transistor is operated in common-emitter or common-source. ft is indicative of the intrinsic speed of the transistor. It is primarily determined by the internal capacitances and the transconductance (gm) of the device.

As we know the UGF is the frequency at which the gain of the amplifer falls to unity (1). This is also often referred to as the gain-bandwidth product(GBW). UGF characterizes the frequency at which the amplifier can no longer provide sufficient gain, essentially defining the useful bandwidth of the amplifier.

The reasons, then, for choosing ft » UGF, is important. If ft is much greater than UGF, the transistor's intrinsic limitations (due to internal capacitances and gm) are far removed from the operating frequencies of the amplifier. This ensures that the transistor's own frequency response does not add significant phase shift or gain roll-off within the operating range of the amplifier. As a result, the overall bandwidth of the amplifier is dominated by external elements (e.g., load capacitances, resistances), which can be more easily controlled or compensated

When ft is significantly higher than UGF, the phase shift introduced by the transistor itself (which evolves gradually as the frequency approaches ft) remains minimal at frequencies around UGF. This is crucial for maintaining stability in feedback amplifiers. Excess phase shift approaching -180 degrees around the UGF can lead to instability (oscillations). By ensuring ft is much higher, you minimize the risk of insufficient phase margin and potential oscillations.

Amplifiers are often designed with specific gain-bandwidth products in mind. Ensuring ft » UGF means the transistor's gain does not fall off significantly before the desired UGF, preserving the intended amplifier performance. This allows for higher gain stages without compromising on bandwidth.

Selecting transistors with ft » UGF gives the designer more headroom to accommodate unforeseen variations in the process, temperature, and other parasitic elements that might inadvertently affect the amplifier's characteristics. It also provides robustness against manufacturing variations and ensures consistent performance across different operating conditions.

Therefore we only parsed the values with a ft greater than 5-10 the UGF.

Task 5

When we are discussing the trade-offs for choosing a higher or lower ratio of gm/Id on MOSFETs a high gm/Id ratio generally implies high transconductance efficiency. Since voltage gain (Av) is proportional to gm, a higher gm/Id leads to a higher intrinsic gain, desirable for amplification stages. High gm/Id suggests that for a given gm, less current (Id) is required, leading to lower power consumption. This is crucial for battery-powered

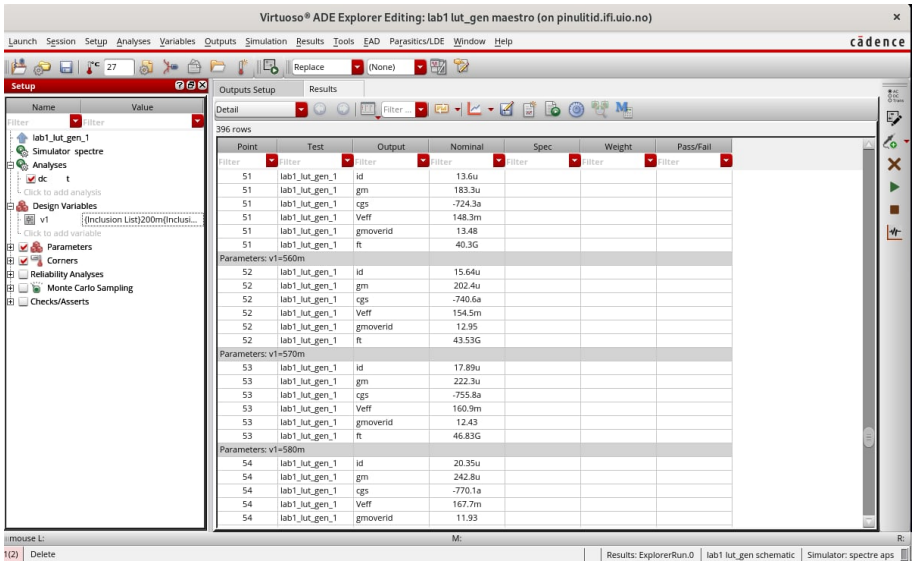

Figure 6: Look-up table extracted from Task 3.

applications. High gm/Id typically reduces the noise figure, as noise is often inversely proportional to gm.

But there are also drawbacks to a high gm/Id. High gm/Id implies a longer channel length and often higher capacitance (both gate and parasitic), which can degrade the frequency response (lower bandwidth). Operating in the sub-threshold or near-threshold regions typically associated with high gm/Id reduces the available voltage swing, which may limit headroom in analog circuits. While high gm/Id can improve gain, it often comes at the cost of linearity, making the circuit more susceptible to distortion.

On the other hand a lower ratio of gm/Id implies less transconductance efficiency, but can be beneficial in other aspects. Lower gm/Id usually corresponds to shorter channel lengths and reduced parasitic capacitances, thus enhancing the frequency response. Operating in regions such as strong inversion (lower gm/Id) often provides better linearity, as in signal processing, making it suitable for applications requiring low distortion. Low gm/Id operation typically results in a higher design headroom, allowing for larger output voltage swings which are beneficial in signal processing.

The drawbacks are A lower gm/Id means more current (Id) is needed for a given gm, leading to higher power dissipation. Voltage gain (Av) is also directly tied to gm, lower gm/Id results in reduced intrinsic gain, which may necessitate stages of amplification. The noise figure tends to be higher due to reduced transconductance, potentially degrading the overall performance in noise-sensitive applications.

But we aren't pros, and we really didn't have any specific specifications on our gm/Id ratio. The specific circuit we were building was an amplifier circuit so the intrinsic gain and lower noise from a relatively high gm/Id made sense. The ft we decided on was in the end 46.83GHZ, 7.8 times larger than a UGF of 6GHz. Even though we decided on

wanting a higher gm/Id, the downsides of approaching the edge case, here being 5 times larger than UGF, pushed us to increase the ft a bit.

From the look-up table we extracted the values:

$$g_m = 222.2\mu S \tag{13}$$

$$I_{dunit} = 17.89\mu A \tag{14}$$

$$V_{eff} = 16.9mV \tag{15}$$

We can use these values and a unit transistor to try to improve our amplifier design. We have the width of a unit transistor,

$$W_{unit} = 1\mu m \tag{16}$$

, which we can use in conjunction with the Id from Task 1., 8, and the unit transistor current from our look-up table 6, 14. We can then calculate the width we need for the amplifier transistor with the formula:

$$\begin{aligned} W_{amp} &= \frac{I_d}{I_{unit}} \cdot W_{unit} \\ &= \frac{377\mu A}{17.89\mu A} \cdot 1\mu m \\ &= 24.105\mu m \end{aligned} \tag{17}$$

We can now build our amplifier circuit were the left hand MOSFET circuit, the M1 circuit, is the unit transistor and its current with E0 as the voltage controlled voltage source to ensure 1Av:

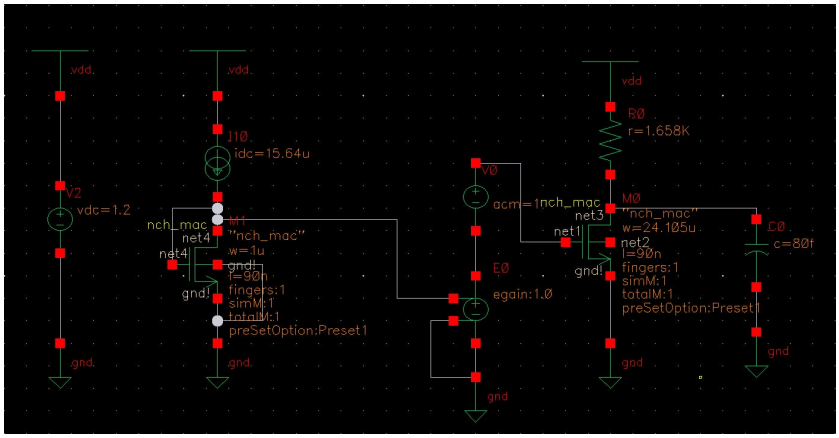

Figure 7: Schematic of the amplifier circuit for Task 6.

The right hand circuit is our amplifier circuit with an AC stimuli for frequency analysis, R_L from 12, C_L of 80 fF and the width of the transistor as we calculated.

Task 6

After doing the DC simulation and AC analysis we got the simulation results

$$g_m = 5.5223mS \tag{18}$$

$$I_d = 457.94\mu A \tag{19}$$

from the results browser from the tool menu, and the frequency response at the output:

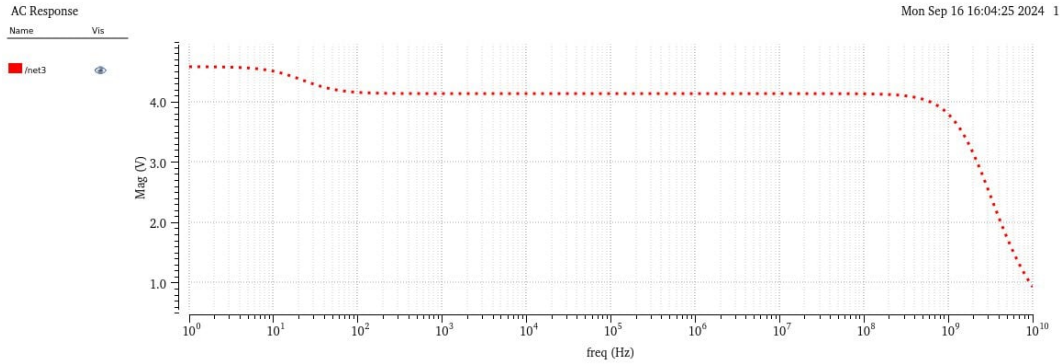

Figure 8: Caption

In retrospect we should have extracted the exact values from the plot and had the y-axis in dB, but by studying the plot we can roughly estimate the values at the critical points. From the start we get an Av of 4.6, which drops down to 4.2 from 10 Hz to 100 Hz. This is only a drop of about 1 dB which can we argued is from the parasitic drain and gate capacitance as we're in saturation during this simulation. We get another linear drop from an Av of 4.2 at 1GHz to 1 at 10 GHz, passing our UGF of 6GHz at Av 1.3. 1 Av is 0dB which is our threshold for when a circuit is unstable. We can then conclude that our circuit works for the desired frequency range.

But there are issues. The simulated g_m value was 80% larger than the calculated one, the current was 20% larger, and the voltage gain was realistically only 4.2 for most of the frequency range, not the 5.0 we tried to achieve. As we mentioned previously the square law model is an idealized approximation that assumes the transistor operates in strong inversion and ignores short-channel effects, channel-length modulation, mobility degradation, velocity saturation, and other second-order effects. As the channel-length modulation is directly proportional to the V_{eff}, and our V_{eff} was 560 mV, 210 mV above a moderate to strong inversion, it's safe to assume that not accounting for it even though

its effect is as strong as it is at that voltage, is a pretty big bottleneck in our calculated circuit.

To improve the general accuracy of the circuit the probable next step would be to do another run of this gm/Id design methodology and change the values to the specifications that we would want. We could also do hand calculations that accounted for the channel-length modulation.

If we instead wanted to increase the accuracy of specific characteristics in the circuit we could e.g. use the g_m from the simulation to calculate another load resistor to increase our voltage gain. We could potentially also do a detailed parasitic analysis, but we doubt that it's effect is comparable to the other factors (inaccuracy in calculations and channel-length modulation).