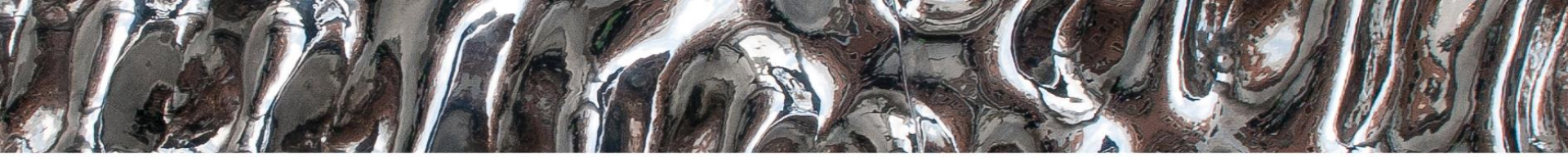


UiO : Department of Informatics
University of Oslo

IN5180 - Analog Microelectronics Design

Advanced MOSFET modelling, passives and EDA tools

Kristian G. Kjelgård

Topics

Body effect

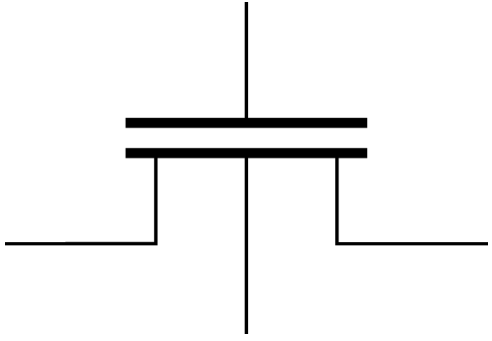
Short channel effects

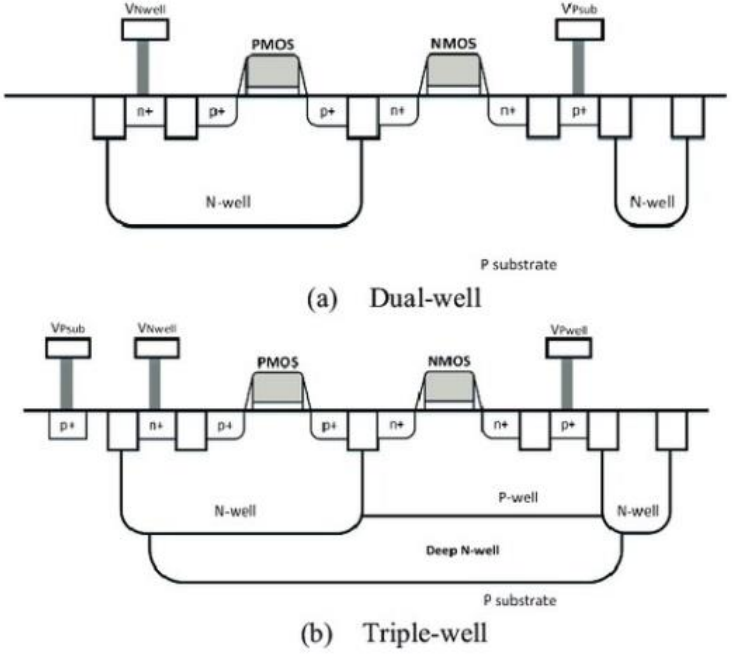
- Mobility Degradation
- Drain Induced Barrier Lowering
- Hot carriers

Passives

EDA tools

The 4th terminal





Body effect

- Back-gate effect, substrate effect

– Current change as V_{SB} is different from zero

– Modeled as change in threshold voltage

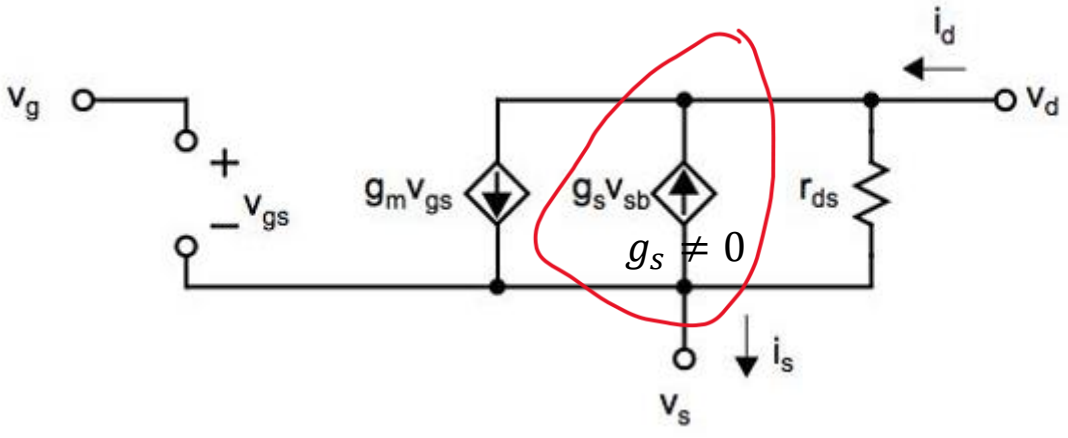
$$V_{tn} = V_{tn0} + \gamma\left(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

– V_{tn0} – zero biased threshold voltage

$$\gamma = \sqrt{\frac{2qN_A K_S \varepsilon_0}{C_{ox}}}$$

ϕ_F - Fermi potential

Body effect – small signal



$$g_s = \frac{\partial I_D}{\partial V_{SB}} = \frac{\partial I_D}{\partial V_{tn}} \frac{\partial V_{tn}}{\partial V_{SB}} = \frac{\gamma g_m}{2\sqrt{V_{SB} + |2\phi_F|}}$$

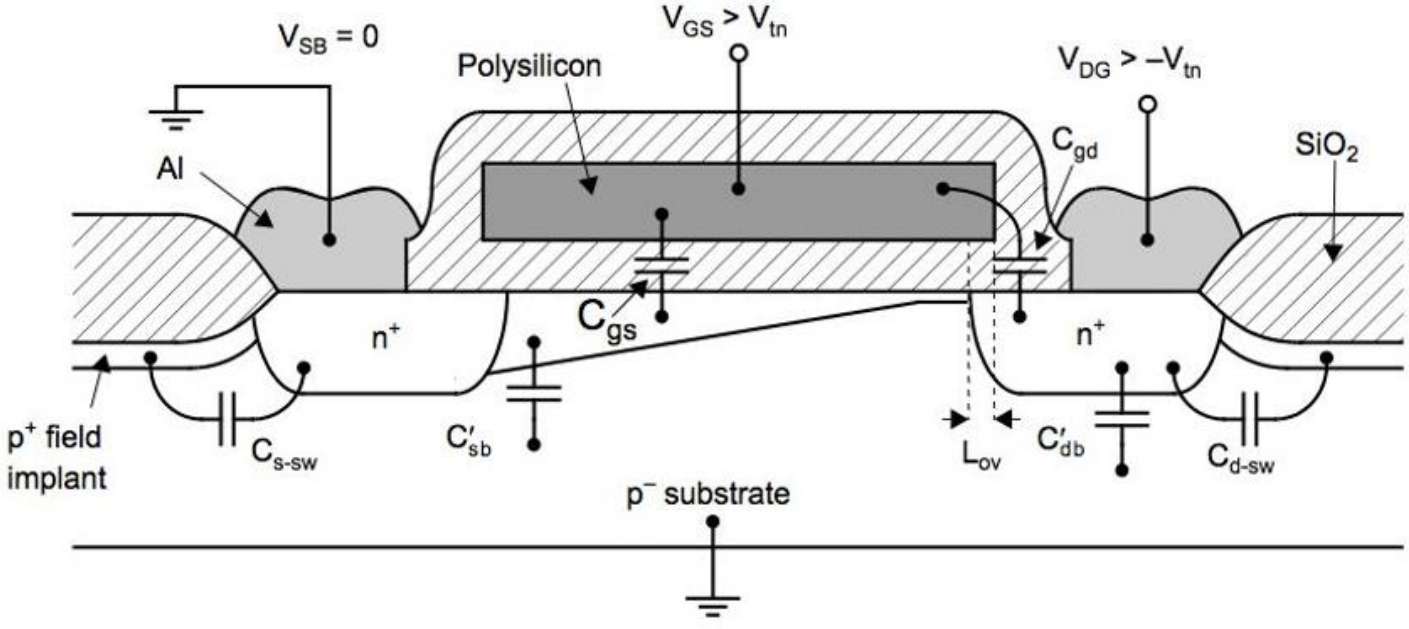
- If bulk connected to source

$$g_s = 0$$

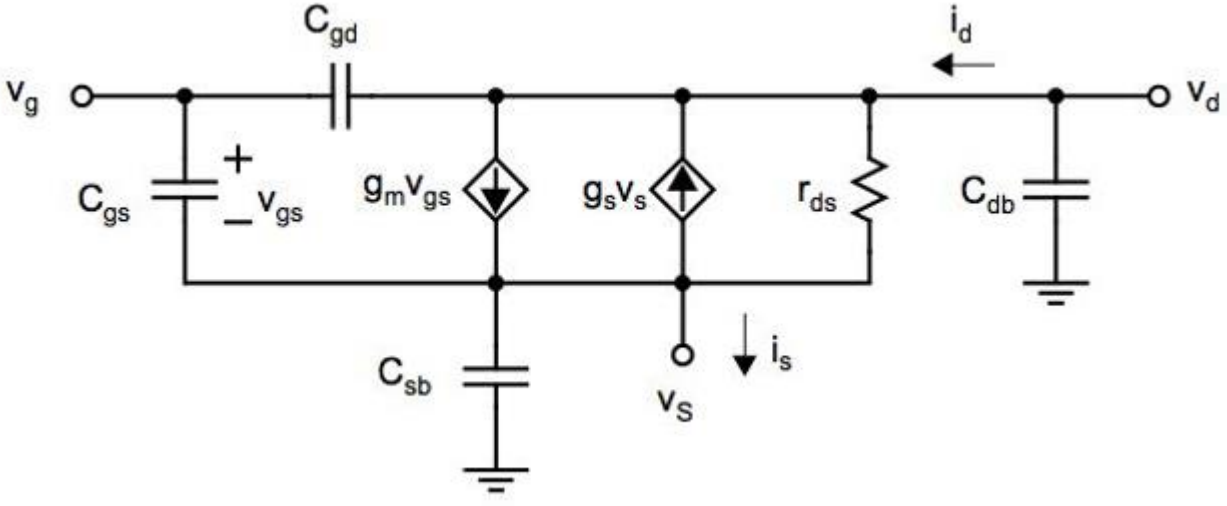
- If Vsb ≠ 0

$$g_s \neq 0$$

X-section with capacitance

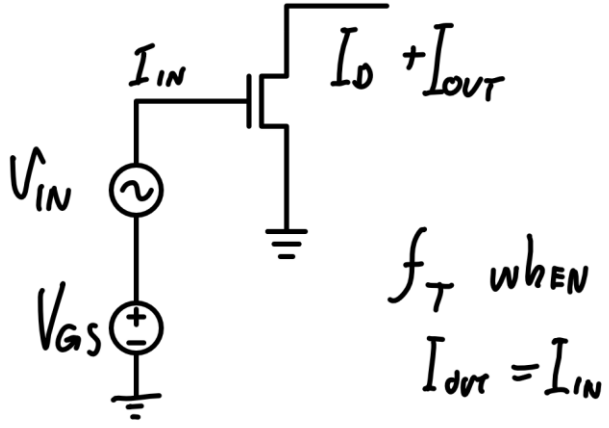


Small signal model with capacitances

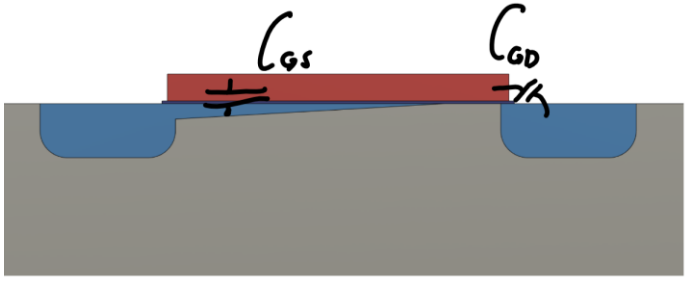


f_T transition frequency - transistor speed

- Higher f_T -> faster digital systems and analog/RF (ie millimetre wave radio / radar systems)



Current gain unity gain frequency



$$f_T \approx \frac{g_m}{2\pi(C_{GS}+C_{GD})}$$

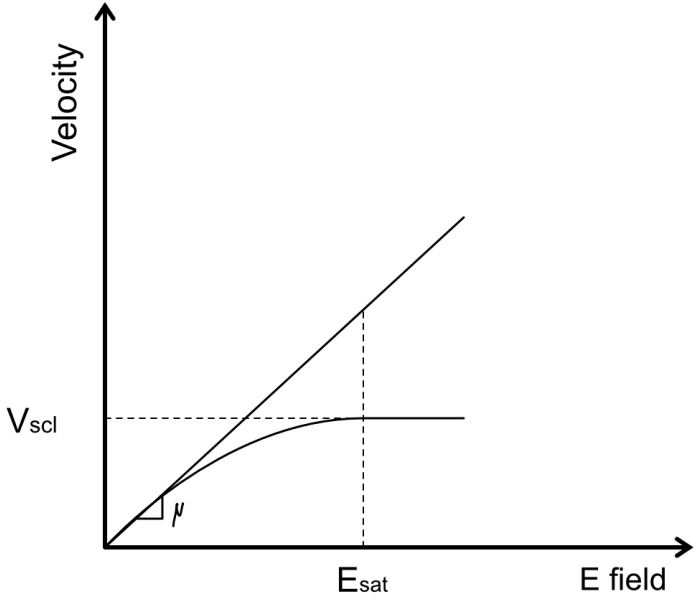
- Lower capacitance and higher Gm with shorter L
- ft proportional to $1/L^2$

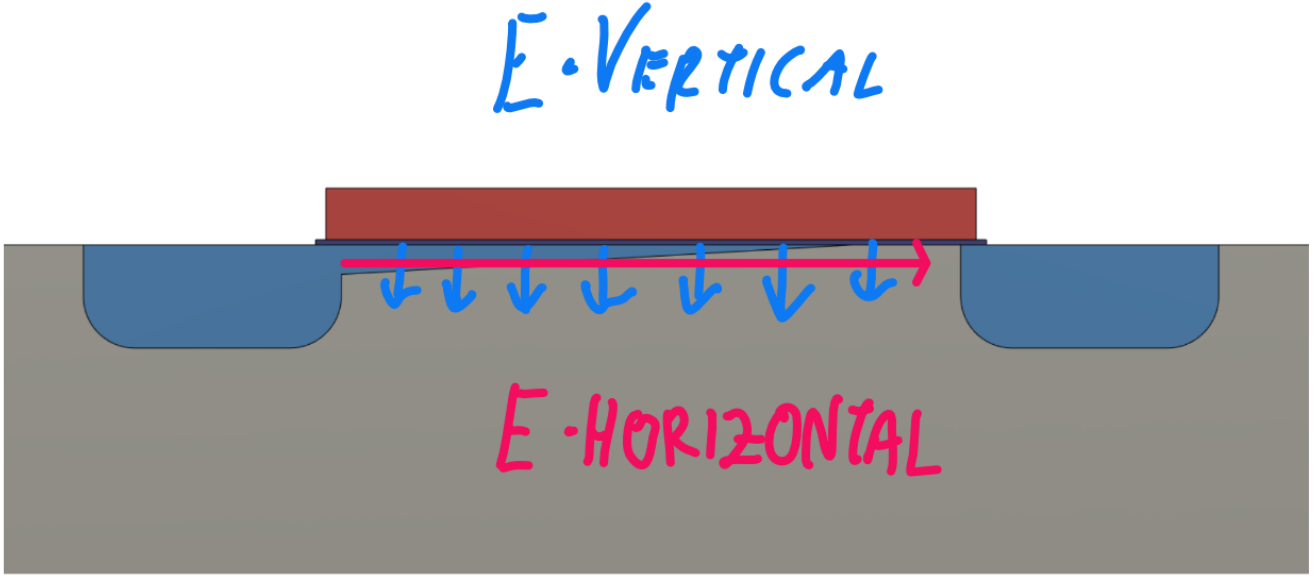
Assumes μ_n constant…

$$f_T \approx \frac{\mu_n C_{ox}\left(\frac{W}{L}\right)V_{EFF}}{2\pi C_{ox} W\left(\frac{2}{3}\right)L} = \frac{3\mu_n V_{EFF}}{4\pi L^2}$$

Mobility degradation - μ_n with high E

- When transistors scale E gets high and mobility degraded
- Velocity of charge carrier limited to 10^7 cm/s
- Affects speed and transconductance




E-VERTICAL
E-HORIZONTAL

$$\mu_{n,eff} = \frac{\mu_n}{\left(1 + (\theta V_{EFF})^m\right)^{1/m}}$$

$V_{EFF} \gg 1/\theta$

↓ MOBILITY DEGRADATION TERM

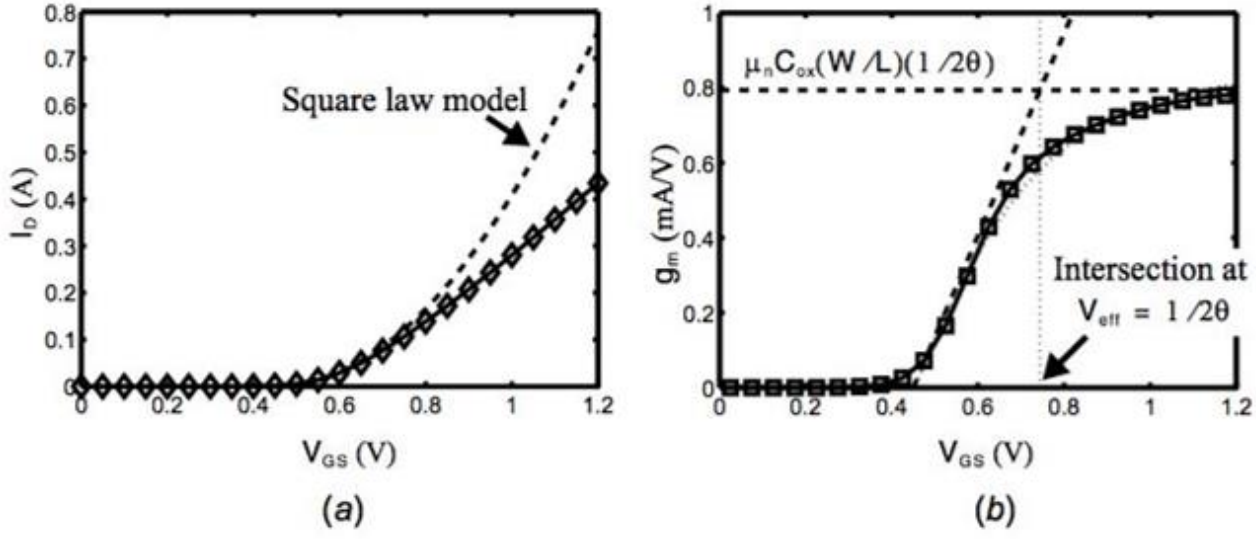
$\frac{1}{\theta V_{EFF}}$

↓ SQUARE LAW

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{V_{EFF}^{\cancel{2}}}{\theta \cancel{V_{EFF}}}$$

High V_{eff} -> less control of channel
Square law -> linear

Implications



- Small-signal transconductance limited
- Reduced available signal swing
- Reduction in intrinsic gain A_i

Scaling of CMOS -> large constraints on analog design

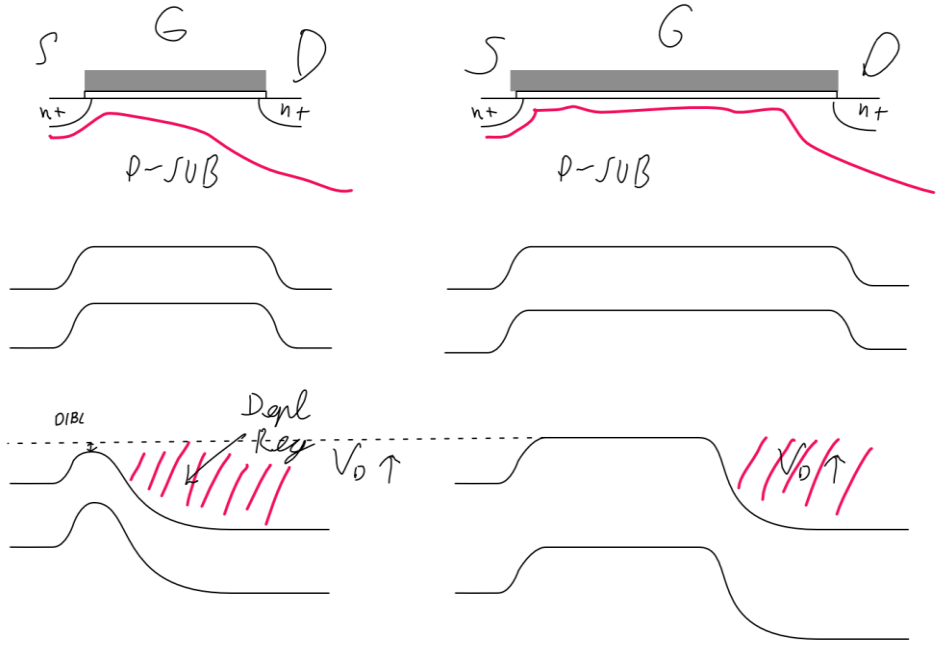
Example

1.25 Make a qualitative sketch of transistor intrinsic gain A_i versus V_{eff} for:

a. Constant device width W

In each case what is the relationship between A_i and V_{eff} in weak-inversion, active mode and under mobility degradation

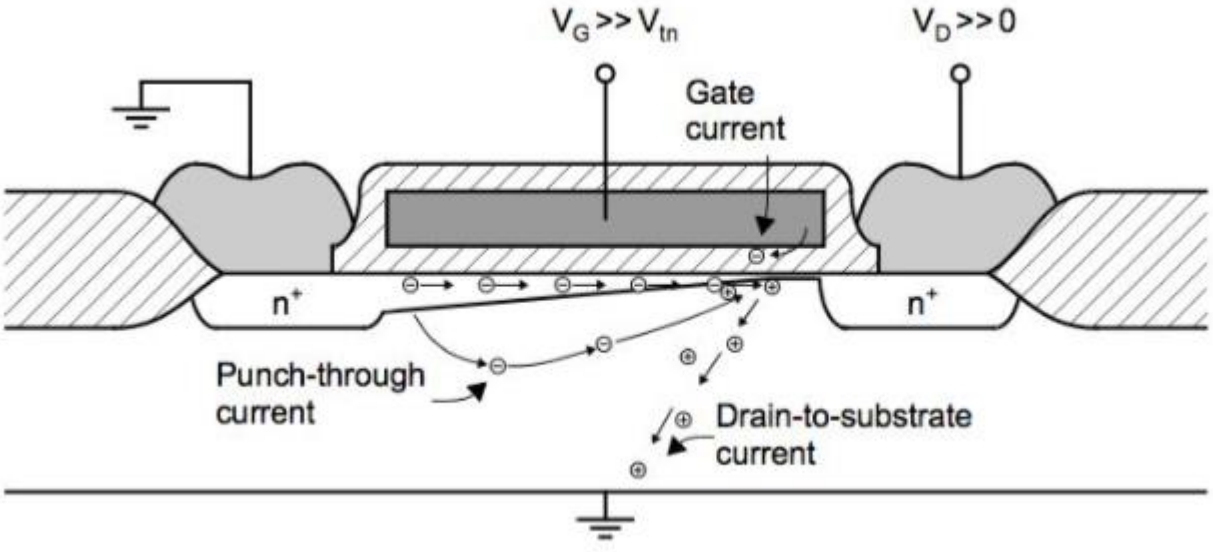
Drain Induced Barrier Lowering (DIBL)



Drain Induced Barrier Lowering (DIBL)

- V_t dependence on V_{ds}
- Current dependent on V_{ds} -> reduced r_{ds}

Hot carriers



High velocity carriers

- E-H pairs -> Drain-to-substrate current
- Gate oxide tunnel
- Electrons in oxide trapped

Leakage Current

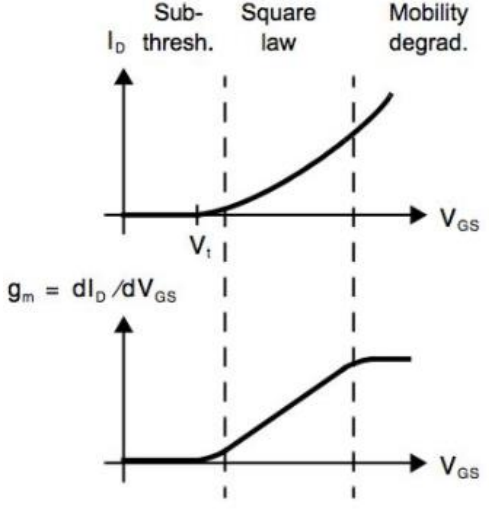
- Gate -> channel quantum-mechanical tunnel

- pn reverse junction leakage

$$I_{in} = \frac{qAn_i x_d}{2\tau_0}$$

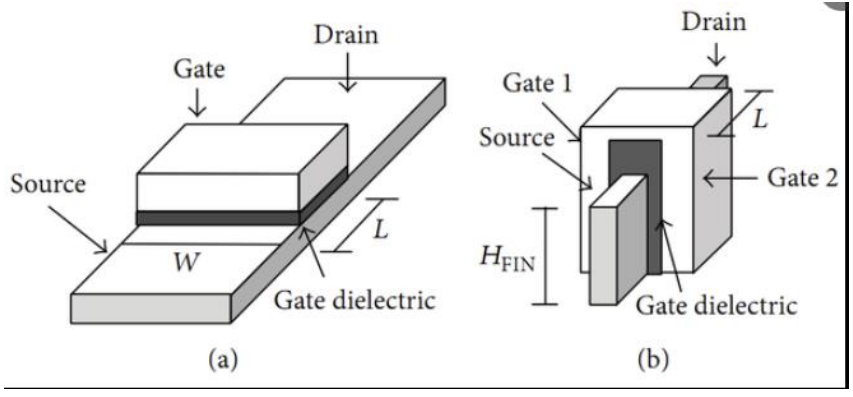
Summary

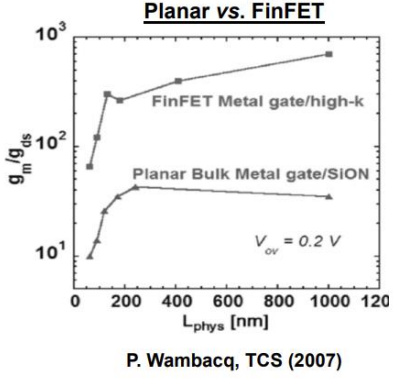
- In modern CMOS technology a large variety of effects gives a non-ideal transistor behaviour
- Basic models used for "intuition" and design ideas
- Non-ideal characteristics very significant
- When to use simulator?



Sub 40 nm technologies -> finfet

- Next generation analog / Radio Frequency SoC in finfet technology?





P. Wambacq, TCS (2007)