Embedded Systems Security'18
Laboratory assignment 1 (must complete)
weeh of Feb. 19

During this class you will get familiar with writing code in VHDL. This is a *hardware description language* allowing to build models of electronic (logic) components of digital systems and verify their workings. Here are the basic steps you will cover today:

- write and run `HelloWorld!` ;
- analyse the code of an *entity* which realises a full-adder;
- anlyse the code of a *testbench* for that adder;
- write and test code for an entity that realises a given logic function.

Assignment 1 Follow steps from **The hello world program** section available at `http://ghdl.readthedocs.io/en/latest/using/QuickStartGuide.html`. Read through the code, try do find analogies to other programming languages you know.

Assignment 2 Try to look for sources of the library `textio` (the code from the previous assignment is using it). Analyse the sources and try to extend the previous code so that it can read a line of text from a keyboard and print it back, like so:

```
[przemek@corsa2 VHDL]$ ./hello_world
Hello world!
hej!
hej!
[przemek@corsa2 VHDL]$
```

Assignment 3 Follow the next steps from the website from **A full adder** section. Again, go through the codes from the first and this assignments. Launch `gtkwave` with the time sequence you just generated (`adder.vcd`). Analyse signals `i0, i1, ci, s, co`. Make sure that you can answer the following questions:

- what is *adder* and how it works?
- what do **entity, architecture, port, component, process** mean?
- how is the full adder tested?

Assignment 4 With all that you've learnt so far, write the code and its testbench for an entity that represents the following logical cirtuit: