Requesting project: External Memory Controller for DDR

The goal of this project is to implement an external memory interface for DDR3 modules using Verilog, simulating realistic memory transactions through a behavioral DDR model. The system emulates how FPGA-based designs communicate with DDR3 memory through a memory controller-like front end. A finite state machine (FSM) issues write and read commands to a DDR3 memory module via a simplified Memory Interface Generator (MIG)-style interface. To verify correctness and functionality, the FSM writes patterned data to memory addresses, reads it back, and compares the results. It also tracks performance by measuring and accumulating the number of clock cycles taken per memory read, enabling calculation of average latency. The interface will support features such as burst read/write support, a register-based front end mimicking an AXI-Lite bus, performance counters to measure throughput and latency, and built-in stress tests to verify stability.

Rather than relying on Xilinx-provided IP cores or vendor-specific simulation environments, this project builds a fully portable behavioral DDR3 model compatible with basic educational tools like Synopsys VCS. The custom memory module includes configurable latency and internal memory storage, responding to read and write requests in a cycle-accurate way. A self-checking testbench drives the system, observes results, and reports test status and timing performance. This setup mimics the essential components of a real DDR interface system, making it an ideal platform for learning memory interfacing, verification, and timing analysis in simulation environments.