Hardware Development of Katmai 24-Bit ADC

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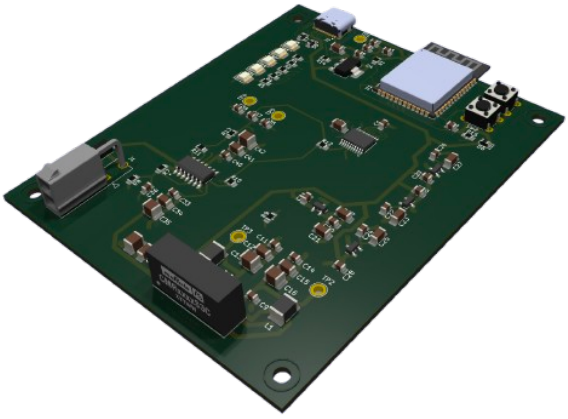

Figure 1. ADC KiCad Rendering

ABSTRACT

The design of the ADC PCB for the Katmai system involved careful selection of components, layout optimization, and implementation of measures to ensure analog signal integrity and stable operation. The board incorporates the ADS131M02 ADC, supported by precision voltage regulation using low-noise regulators and isolated power supplies. Signal integrity was prioritized through the use of differential routing, decoupling capacitors, and filtered input stages. Layout considerations included minimizing trace lengths for high-speed signals and isolating analog and digital domains to reduce interference. Protection measures, such as transient voltage suppressors and robust grounding strategies, were implemented to enhance reliability. These decisions were driven by performance requirements, cost constraints, and modularity, ensuring the PCB meets the demands of high-resolution data acquisition.

Definitions

This section provides definitions for the acronyms and terms specific to the hardware design and assembly described in this document.

- **ESP32-S3:** A low-power, high-performance system-on-chip microcontroller featuring integrated Wi-Fi and Bluetooth, used as the core processor for the ADC system.
- **ADC:** Analog-to-Digital Converter. Converts analog signals from sensors into digital data for processing.
- **USB-C:** Universal Serial Bus Type-C. A compact, reversible connector that supports power delivery and data transfer.
- **OPA4134:** A precision operational amplifier with low noise and high bandwidth, used in the analog signal path.
- **TLV76133:** A low-dropout linear voltage regulator that steps down voltage to power digital circuits.
- **Murata CMR0512S3C:** A DC-DC converter that provides isolated ±12V power for the analog circuitry.
- **REF31xx:** A series of precision voltage reference ICs providing stable reference voltages for ADC and analog circuitry.
- **SMAJ10CA:** A bidirectional transient voltage suppressor diode used for protecting circuits against voltage spikes.
- **DNP:** Do Not Populate. Components that are included in the PCB layout but not installed in the current build, allowing flexibility in future iterations.
- **LED:** Light-Emitting Diode. Used for visual status indicators on the PCB.
- **SPI:** Serial Peripheral Interface. A high-speed communication protocol used between the ESP32 and the ADC.
- **TVS Diode:** Transient Voltage Suppression Diode. Protects sensitive circuits from voltage transients caused by ESD or other sources.

INTRODUCTION

The purpose of this documentation is to detail the design, layout, and testing processes undertaken for the Katmai ADC PCB, which integrates the ADS131M02 ADC with an ESP32-S3 microcontroller. The primary focus was to achieve reliable measurement of differential analog signals while addressing challenges in signal integrity, power management, and communication protocols.

The analog system was designed to meet the ADC's 2.5V differential input requirements, with careful consideration given to voltage regulation and noise minimization. Low-dropout regulators, decoupling capacitors, and differential filter designs were implemented to ensure signal stability. A differential power supply configuration, supported by a Murata CMR0512S3C DC-DC converter, was used to isolate noise between digital and analog domains.

The PCB layout was optimized to reduce noise and interference. Ground planes were separated for analog and digital circuits, while high-speed traces such as SPI and USB were routed to minimize crosstalk and signal degradation. Key design choices included the addition of TVS diodes for protection against transients and maintaining appropriate trace lengths for critical connections.

The testing phase employed tools like oscilloscopes, multimeters, and logic analyzers to validate hardware functionality. Particular focus was given to the enable and reset circuits of the ESP32, as well as the differential input stage of the ADC. Debugging was supported by status LEDs and signal monitoring across key nodes.

This documentation outlines the design rationale, component selection, and troubleshooting methods, providing a comprehensive overview of the PCB development process. It aims to serve as a reference for future projects that require robust ADC integration.

- Analog System Design: Ensuring stable 2.5V differential input and low-noise operation through careful regulator and filter selection.

- PCB Layout: Noise isolation achieved via separated ground planes and optimized routing of high-speed traces, supported by transient protection mechanisms.

- Testing and Debugging: Systematic validation of hardware functionality using oscilloscopes and logic analyzers, focusing on critical circuit nodes and communication protocols.

PIN AND CONNECTION ANALYSIS FOR THE ESP32-S3 WROOM-2 MODULE

The ESP32-S3 WROOM-2 serves as the core processing unit in this ADC design, chosen for its low cost and high functionality, particularly its robust SPI support and integrated wireless capabilities. This section analyzes the connections in the top-left portion of the schematic (ADC v6.pdf) and explains the rationale behind the design decisions.

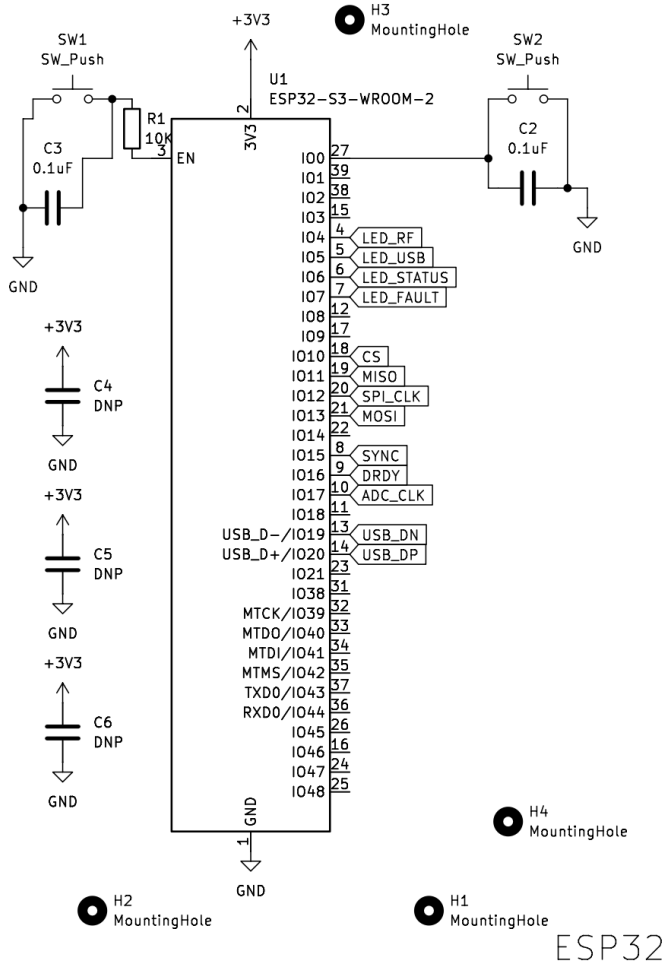

Figure 2. ESP32 Pin Layout

ESP32-S3 WROOM-2 Pin Connections (Figure 2)

The ESP32-S3 WROOM-2 module features numerous GPIO pins, which are utilized for interfacing with the ADC, indicators, and power systems. Key connections are summarized below:

- **Pin IO19 and IO20 (USB_D- and USB_D+):** These pins are configured for USB CDC communication. The differential signals are routed to the USB interface, enabling communication between the ESP32 and a host computer. This connection ensures stable data transfer and debugging capabilities.

- **Pin IO18 (SPI_CLK):** This pin serves as the SPI clock for communication with the ADS131M02 ADC. The ESP32's SPI master configuration provides precise timing control.

- **Pin IO16 (MISO):** Used to receive data from the ADC, this pin ensures reliable data acquisition during operation.

- **Pin IO17 (MOSI):** Configured for transmitting data to the ADC, this pin facilitates configuration commands and control signals.

- **Pin IO15 (SYNC):** This pin handles synchronization and reset signals for the ADC. Proper timing on this pin ensures consistent operation and error-free initialization.
- **Pin IO14 (CS):** The chip select pin for SPI communication is connected to this GPIO, allowing the ESP32 to enable communication with the ADC selectively.
- **Pins IO9 and IO10 (LED Indicators):** These pins control the LED indicators for status visualization. Indicators such as "FAULT" and "STATUS" are used to monitor system health and operational status in real time.
- **EN Pin (Enable):** Connected to a pull-up resistor, this pin ensures proper initialization of the ESP32 during power-on. The pull-up design stabilizes the module's startup.
- **3V3 Pin (Power Supply):** Supplies regulated power to the ESP32, sourced from the onboard TLV76133 LDO. Decoupling capacitors marked as DNP (Do Not Populate) were included in the design near this pin to allow for additional filtering, if needed, during troubleshooting or future iterations.

Rationale for Using the ESP32-S3 WROOM-2

The ESP32-S3 WROOM-2 was selected for this project due to its cost-effectiveness and high performance in embedded applications. Its features include:

- **Dual-core processor:** Provides ample processing power for handling ADC data and communication protocols simultaneously.
- **SPI and USB support:** The module's built-in SPI and USB interfaces simplify hardware integration and reduce the need for external controllers.
- **Low power consumption:** Ideal for battery-operated or energy-sensitive designs.
- **Compact size:** The small form factor allows for efficient PCB layout and minimizes the overall footprint of the design.

Considerations in PCB Layout

Special attention was given to the routing and placement of critical connections:

- Differential USB lines (D+/D-) were routed with controlled impedance to maintain signal integrity.
- Decoupling capacitors marked as DNP were strategically placed near critical power pins to allow for additional noise filtering or stability enhancements, should the need arise during testing or later modifications.
- SPI lines were kept short and shielded where possible to reduce noise and ensure reliable communication.

The ESP32-S3 WROOM-2 module, paired with thoughtful pin utilization and PCB layout considerations, forms the foundation of this ADC design, enabling seamless communication and precise control of the ADC.

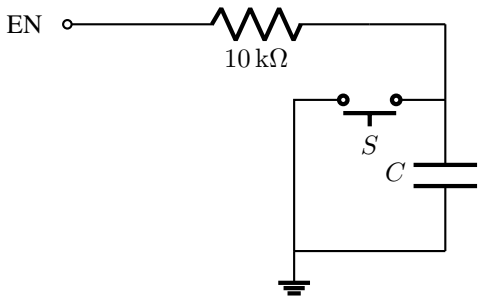

Figure 3. Original Circuit

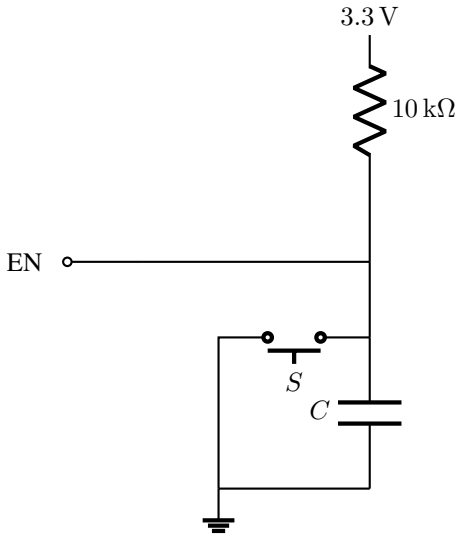

Figure 4. Modified Circuit

NOTE ON EN PIN TOPOLOGY

The topology of the EN (enable) pin was unclear in the ESP32-S3 datasheet and design guidelines. The initial circuit included a resistor in series with a parallel capacitor and switch, but it lacked a pull-up resistor at the EN pin junction. During debugging, the ESP32-S3 failed to initialize correctly, and testing revealed the need for a pull-up resistor to 3.3V at the EN pin junction. Adding this resolved the issue and ensured proper initialization, highlighting the need for clearer documentation in future ESP32 design guidelines. (See Figure 3 and 4)

Selection of the ADS131M02 ADC

The choice of the ADS131M02 ADC for Katmai's NMR register was driven by its combination of high sampling rate and 24-bit resolution, critical for capturing accurate and detailed signals from the NMR coils. This section examines the specific features and design considerations that influenced this decision, as well as how the ADC's specifications align with the system's requirements.

High Sampling Rate:

The ADS131M02 supports sampling rates up to 32 kSPS (kilo-samples per second), which provides sufficient temporal resolution for the frequencies expected in NMR applications.

This capability ensures that even subtle variations in the signal can be captured without aliasing or significant data loss.

24-Bit Resolution:
With its 24-bit resolution, the ADS131M02 offers the precision required to detect and measure low-amplitude signals from the coils. This high resolution enables accurate representation of small variations in the analog signals, which is essential for the sensitivity required in NMR measurements.

Low Noise and Stability:
The ADC's low input-referred noise and built-in offset calibration ensure consistent and reliable data acquisition. These features are particularly important for NMR applications, where signal integrity and stability are paramount for accurate data interpretation.

Integrated Features:
The ADS131M02 integrates key functionalities such as a programmable gain amplifier (PGA), internal clock generation, and flexible data rate options. These features simplify the overall system design by reducing the need for additional external components and ensuring compatibility with Katmai's compact PCB layout.

Synchronization Capabilities:
The ADC's synchronization options allow precise timing control when working with multiple channels or systems. This ensures coherent data acquisition across the NMR coils, which is necessary for analyzing spatial and temporal signal variations.

In conclusion, the ADS131M02 was selected due to its combination of high-resolution sampling, noise performance, and integrated features, all of which align with the stringent requirements of Katmai's NMR system. This ADC provides a robust foundation for capturing high-quality data, facilitating further analysis and experimentation in the application.

SIGNAL PATH AND ANALOG CIRCUIT DESIGN

The circuit depicted integrates various gain and filtering stages to condition and process signals from the NMR coils. Each stage has been designed to meet the requirements of signal integrity and stability for Katmai's NMR register. The following section provides a detailed analysis of the stages, design choices, and their significance.

Input Protection and Attenuation

The input signal from the coils is routed through a transient voltage suppression diode (SMAJ10CA) to protect downstream circuitry from voltage spikes. This diode provides bidirectional clamping, ensuring the safety of sensitive components during transient conditions. Following this, the signal encounters a resistive divider network (R7, R8, and R9) to attenuate the input to levels appropriate for the subsequent operational amplifier (OPA4134). This stage prevents saturation and maintains linearity, crucial for preserving the signal's fidelity.

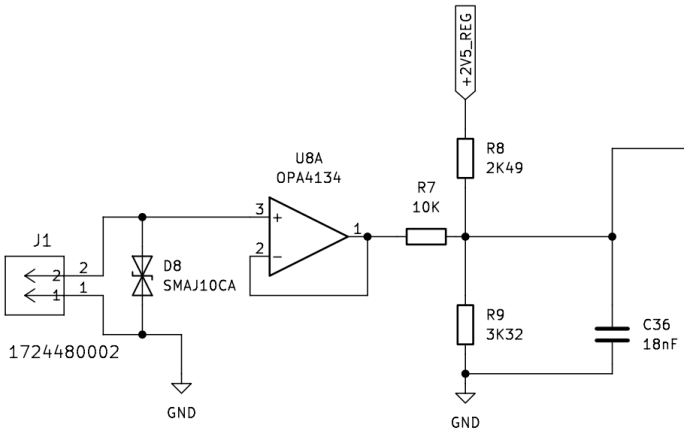

Figure 5. Input and First Gain Stage

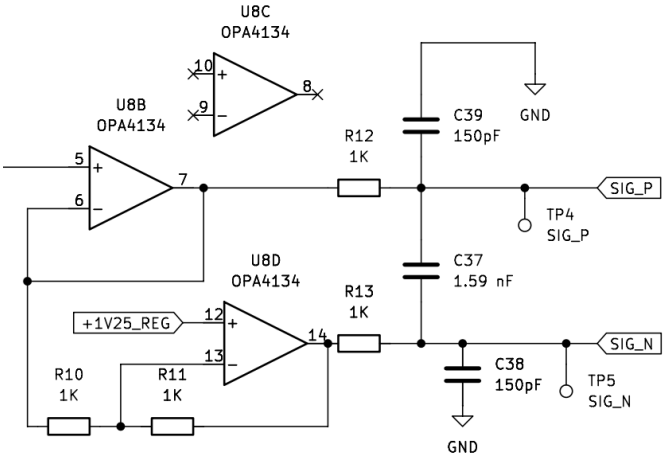

Figure 6. Subsequent Gain Stages

First Gain Stage (Figure 5)

The first operational amplifier (U8A, OPA4134) acts as a non-inverting amplifier, providing initial amplification to the attenuated signal. This stage ensures that low-amplitude signals are boosted to a measurable level while minimizing noise introduction. The choice of the OPA4134 was driven by its low noise characteristics and wide bandwidth, which are essential for handling high-frequency NMR signals with minimal distortion.

Differential Voltage Reference and Stability

A stable differential voltage reference is established using precision resistors (R8 and R9) and capacitors (C36). This reference maintains consistent biasing across the operational amplifiers, ensuring that signal processing remains unaffected by temperature variations or power supply fluctuations. The capacitors in this stage also provide low-pass filtering, reducing high-frequency noise that could interfere with the ADC.

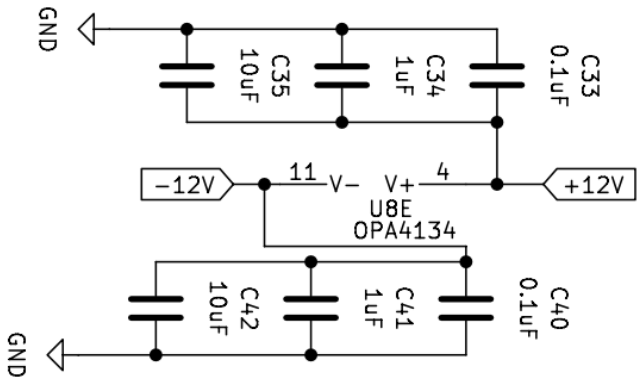

Figure 7. Decoupling on OPAMP Power

Second Gain Stage and Filtering (Figure 6)

The signal is further amplified and filtered through the second operational amplifier (U8B, OPA4134). This stage employs additional resistors (R10 and R12) and capacitors (C39 and C37) to achieve both amplification and low-pass filtering. The filter cutoff frequency has been tuned to match the bandwidth of interest for NMR measurements, effectively attenuating out-of-band noise.

Final Differential Signal Conditioning

The final stage, utilizing U8C and U8D (OPA4134), converts the single-ended signal into a differential format suitable for the ADC input. This stage includes capacitive decoupling (C34, C35) and further filtering to stabilize the signal. The differential configuration enhances noise immunity and signal accuracy, critical for the 24-bit resolution of the ADS131M02 ADC.

Power Supply Decoupling (Figure 7)

To ensure stable operation, the circuit incorporates extensive decoupling capacitors (C33–C42) on the power rails of the operational amplifiers. These capacitors mitigate voltage ripples and transient disturbances, providing clean power to the amplifiers. Proper decoupling is particularly important in this design, as fluctuations in the power supply could introduce noise and compromise the ADC's performance.

Design Rationale:

Each stage of the circuit has been designed to balance performance, stability, and cost-effectiveness. The OPA4134 was selected for its combination of precision, low noise, and affordability. The emphasis on stable voltage references and robust filtering ensures that the signals entering the ADC retain their integrity. The importance of these considerations will be further explored in the next section, which discusses voltage reference stability and its impact on ADC performance.

VOLTAGE REGULATION DESIGN AND COMPONENT SELECTION

The voltage regulation section in the schematic is critical for ensuring stable power delivery to various components of the system. This section details the design choices and the rationale behind the component selection, referring to both the schematic in ADC v6 and the design considerations outlined in the ADC V5 design review.

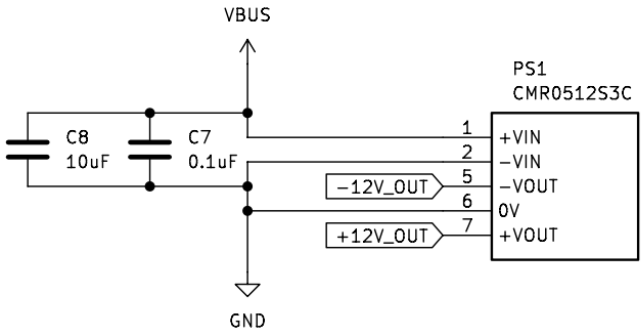

Figure 8. 12V Diffrential Power Conversion

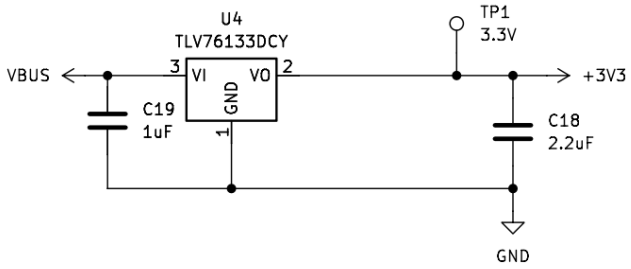

Figure 9. 3.3V Regulation for ESP32

Design Overview

The voltage regulation circuit comprises multiple stages to provide reliable power to the ESP32-S3, ADC, and analog front-end circuitry. These stages include a primary DC-DC converter for dual ±12V supply and several linear regulators for precision voltage rails like 3.3V, 2.5V, and 1.25V. Each regulator was selected to meet specific requirements for current load, voltage stability, and noise characteristics.

Primary DC-DC Converter (Figure 8)

The Murata CMR0512S3C DC-DC converter is employed as the primary voltage source, generating a dual ±12V output. This converter was chosen for its compact size, high efficiency, and ability to provide isolated power, which is essential for minimizing interference between the analog and digital sections. The ±12V output powers the operational amplifiers in the analog front end, ensuring sufficient headroom for accurate signal processing.

3.3V Linear Regulator (Figure 9)

The TLV76133DCY linear regulator is used to step down the 5V input to a 3.3V rail. This rail powers the ESP32-S3 and other digital components. The TLV76133DCY was chosen for its low dropout voltage and ability to supply up to 150mA of current. Decoupling capacitors (e.g., C10, C11, and C12) are placed near the regulator to ensure stability and minimize noise on the 3.3V line.

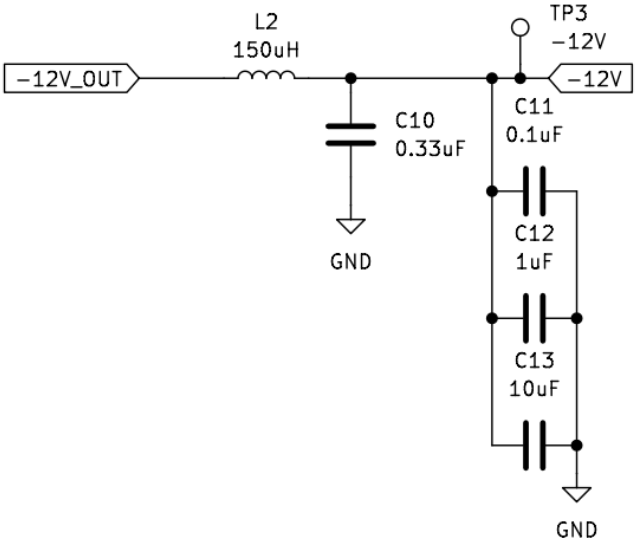

Figure 10. Decoupling for Differential 12V

Voltage References for Precision Rails

Precision voltage references provide the 2.5V, 1.25V, and 3.3V rails required for the ADC and analog circuitry. The selected components include:

- **REF3125AIDBZR (2.5V)**: Provides a stable reference for the ADC's input range. Capacitors such as C29 and C30 are used for decoupling to ensure noise-free operation.
- **REF3112AIDBZR (1.25V)**: Serves as the reference for internal ADC calibration and analog circuitry. Decoupling is similarly implemented with C28 and C31.
- **REF3133AIDBZR (3.3V)**: Used for additional analog circuitry that requires low-noise operation.

These voltage references were selected for their high accuracy, low temperature coefficient, and low output noise, as recommended in the ADC V5 design review.

Decoupling and Filtering

Decoupling capacitors are strategically placed near each regulator and reference IC to minimize voltage ripple and noise. Larger electrolytic capacitors (e.g., C35, 10µF) handle bulk decoupling, while smaller ceramic capacitors (e.g., C20, 0.1µF) manage high-frequency transients. The inductors L1 and L2 (150µH each) further filter noise, particularly on the ±12V rails, enhancing the stability of the power supply to the operational amplifiers.

Design Considerations and Improvements

Our ADC V5 design review highlighted issues such as insufficient current capacity in earlier voltage references and instability under high load conditions. These issues were addressed in the current design by using dedicated linear regulators and references for critical power rails instead of relying on shared sources. The separation of power delivery ensures that voltage-sensitive components, such as the ADC, are not affected by noise or transient loads from the ESP32 or other high-current devices.

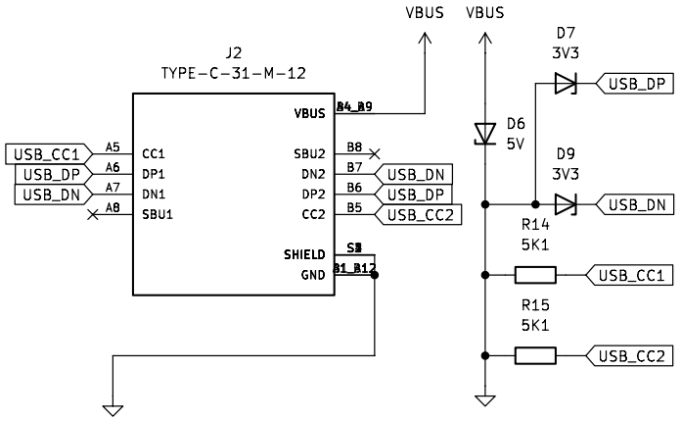

Figure 11. USB Connector

In summary, the voltage regulation circuit is meticulously designed to provide stable, low-noise power for the ADC, ESP32, and analog front end. Component selection focused on ensuring accuracy, stability, and efficiency, addressing the limitations of previous iterations.

USB TYPE-C CONNECTOR DESIGN

The USB Type-C connector (J2) is integral to the system, providing both data transfer and power delivery capabilities. Its selection was driven by its modern design, bidirectional data support, and compatibility with USB 2.0 standards, aligning with the ESP32-S3's requirements and the system's need for compactness.

Key features include differential data lines (USB_DP and USB_DN) routed directly to the ESP32-S3's D+/D- pins, protected by Schottky diodes (D6 and D9) to guard against voltage spikes. Pull-down resistors (R14 and R15, 5.1k) on the USB_CC1 and USB_CC2 lines ensure proper connection initialization as per USB Type-C specifications. For power delivery, VBUS supplies 5V to the system, with diode D7 preventing reverse current flow and stabilizing the input.

COMPONENT PLACEMENT AND LAYOUT ANALYSIS

The PCB layout shown in Figure 12 demonstrates a deliberate arrangement of components to optimize signal integrity, minimize noise, and ensure proper functionality of the system. Each section of the PCB is designed with specific constraints and requirements in mind, balancing performance with manufacturability.

Power Supply and Regulation

The top-right section of the PCB contains the power supply regulation components, including multiple decoupling capacitors and voltage regulators. These components are positioned close to the ESP32-S3 and other critical ICs to minimize power delivery noise and ensure stable voltage lev-

els. The placement of decoupling capacitors near the regulators helps filter out high-frequency noise and provides local charge storage. Additionally, the ground planes in this area are designed to reduce electromagnetic interference (EMI).

ESP32-S3 Placement and Routing

The central portion of the PCB houses the ESP32-S3 microcontroller, positioned strategically to shorten traces to high-speed data lines, such as USB and SPI. Careful routing ensures minimal crosstalk between differential USB signals (DP/DN) and the power delivery traces. The ESP32-S3 is surrounded by optional decoupling capacitors to stabilize its power inputs, while its placement ensures direct connections to the USB Type-C connector for efficient data and power integration.

Analog Signal Path and Filtering

The bottom-left section contains the analog signal processing circuitry, including the OPA4134 operational amplifiers and associated resistors and capacitors. The analog components are deliberately separated from the digital sections of the PCB to reduce noise coupling. The placement ensures the shortest possible trace length for sensitive signal paths, reducing susceptibility to external interference. The differential filtering and gain stages are arranged linearly, optimizing the flow of signals toward the ADC inputs.

USB Type-C Connector and Related Components

The USB Type-C connector is placed in the top-left corner, with nearby pull-down resistors and Schottky diodes for protection. This arrangement minimizes the trace length for VBUS and differential data lines, reducing parasitic capacitance and inductance. The connector's placement at the board's edge simplifies user access and allows straightforward alignment during manufacturing.

Thermal and Mechanical Design

Heat-generating components, such as voltage regulators, are spaced to avoid thermal hotspots. Test points (e.g., TP1–TP5) are distributed across the PCB for easier debugging and measurement during development. Mounting holes at the corners ensure mechanical stability while avoiding interference with critical traces.

Design Rationale

The design prioritizes functional separation to minimize noise and interference. The proximity of capacitors to ICs ensures effective decoupling, while trace lengths are kept short for critical signals like USB and SPI. The placement of analog and digital sections on opposite ends of the board reflects an emphasis on maintaining signal integrity in a mixed-signal environment.

This layout demonstrates a careful balance of electrical, thermal, and mechanical design principles, ensuring robust operation and ease of manufacturing.

BACK LAYER LAYOUT ANALYSIS

The back layer of the PCB, shown in Figure 13, is primarily focused on ground planes, power distribution, and signal

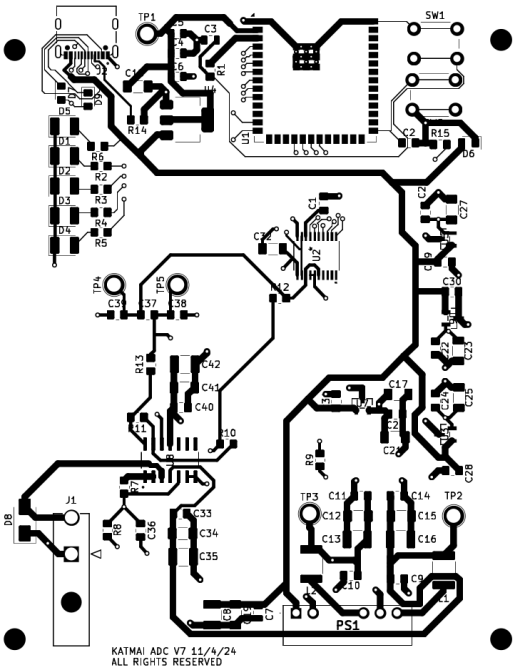

Figure 12. PCB Layout for Katmai ADC showing component placement and routing considerations.

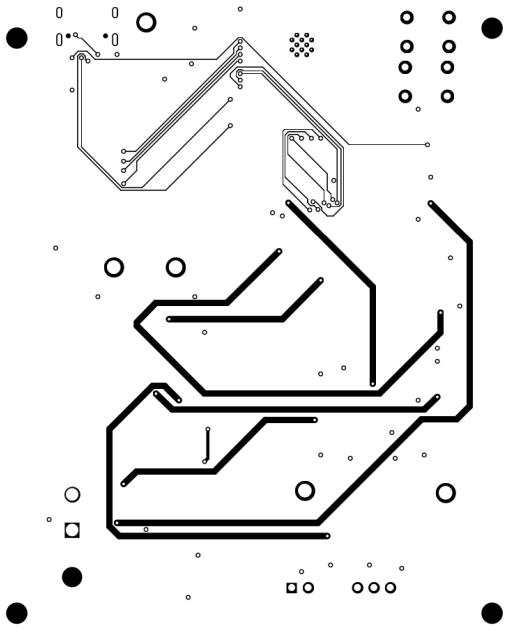

Figure 13. Back of PCB.

routing. This layer complements the front layout by ensuring efficient grounding and mitigating interference between analog and digital sections.

Ground Plane Design

A significant portion of the back layer is dedicated to a continuous ground plane. This design minimizes noise by providing a low-impedance path for return currents, particularly for high-frequency signals. The separation of ground regions between analog and digital sections, as seen on the top and bottom of the layout, reduces the risk of noise coupling. The single connection point between these regions, implemented at a strategic location, prevents ground loops and maintains signal integrity.

Power Delivery and Routing

Thick traces on the back layer indicate the routing of power supply lines, such as VBUS, +3.3V, and ±12V. The width of these traces ensures low resistance, minimizing voltage drops and improving power delivery stability. The positioning of these traces away from sensitive analog signal paths reduces the likelihood of interference.

Signal Routing Considerations

Critical signal lines are routed on the back layer to optimize trace length and reduce crosstalk. Differential signal pairs, such as USB DP/DN and SPI lines, are carefully routed with matched lengths to maintain signal timing and integrity. Where possible, traces are routed over a continuous ground plane to further enhance performance by reducing electromagnetic interference (EMI).

Thermal and Mechanical Features

The back layer incorporates thermal relief patterns around vias and mounting holes to improve solderability and ensure solid mechanical connections. The mounting holes are strategically placed to provide structural stability without interfering with sensitive traces or components.

Design Rationale

The back layer layout prioritizes grounding and power distribution while providing additional routing paths for critical signals. The separation of analog and digital sections aligns with the overall design goal of minimizing noise and ensuring reliable operation in a mixed-signal environment. The careful routing of power and signal lines reflects a deliberate effort to balance electrical performance with manufacturability.

ASSEMBLY AND PARTS SOURCING

The assembly process involved sourcing components from trusted suppliers. Orders for components were placed with Mouser and Digikey, while the blank PCBs were manufactured by JLCPCB. Assembly was performed using a hot air rework station, solder paste, and a circuit microscope to ensure precision and efficiency in component placement and soldering. Each component was placed by hand, which was time-intensive, particularly for small-form-factor components like the ADC. To streamline the process in future iterations, a reflow solder oven and stencil will be used for faster and more consistent assembly.

One of the most challenging tasks was aligning the ADC's small pin package to the PCB solder pads. After multiple attempts, the alignment was achieved successfully. Another challenge was the orientation of the cathode side on LEDs and diodes. Several components, including the 5V zener diode used for USB protection, were initially installed backwards due to an error in the schematic design. This issue was resolved by reversing the installation of the zener diode and reinstalling the incorrectly oriented LEDs.

After assembly, all solder joints were inspected under a microscope to confirm alignment and quality. Additionally, an oscilloscope was used to test for functionality and ensure there were no shorts or connectivity issues. These meticulous steps contribute to a robust and reliable design, minimizing potential debugging challenges in subsequent stages.

REFERENCES

1. Capacitor, 0.47uF, 0805, Quantity: 4.
2. Capacitor, 0.33uF, 0805, Quantity: 2.
3. Capacitor, 10uF, 1210, Quantity: 5.
4. ESP32-S3-WROOM-2, Module, Quantity: 1.
5. Capacitor, 0.1uF, 0805, Quantity: 9.
6. Capacitor, DNP, 0805, Quantity: 3.
7. Zener Diode, 3.3V, 0805, Quantity: 2.
8. Resistor, 3.32kΩ, 0805, Quantity: 1.
9. Capacitor, 18nF, 0805, Quantity: 1.
10. Zener Diode, 5V, 0805, Quantity: 1.
11. Resistor, 1kΩ, 0805, Quantity: 4.
12. Capacitor, 0.1uF, 0805, Quantity: 2.
13. LED, 1210, Quantity: 5.
14. Capacitor, 1uF, 1206, Quantity: 11.
15. Voltage Reference IC, REF3125AIDBZR, SOT-23, Quantity: 1.
16. Connector, USB-C, TYPE-C-31-M-12, Quantity: 1.
17. Resistor, 10kΩ, 0805, Quantity: 2.
18. Resistor, 82Ω, 0805, Quantity: 4.
19. Resistor, 2.49kΩ, 0805, Quantity: 1.
20. Op-Amp, OPA4134, SOIC-14, Quantity: 1.
21. DC-DC Converter, CMR0512S3C, Quantity: 1.
22. Switch, Push Button, 6mm, Quantity: 2.
23. Capacitor, 150pF, 0805, Quantity: 2.
24. Voltage Regulator, TLV76133DCY, SOT-223-3, Quantity: 1.
25. Resistor, 5.1kΩ, 0805, Quantity: 2.
26. Voltage Reference IC, REF3130AIDBZR, SOT-23, Quantity: 1.
27. Capacitor, 1.59nF, 0805, Quantity: 1.
28. Resistor, 200Ω, 0805, Quantity: 1.
29. TVS Diode, SMAJ10CA, SMA, Quantity: 1.
30. Inductor, 150uH, 1812, Quantity: 2.
31. Capacitor, 220nF, 0805, Quantity: 1.
32. Voltage Reference IC, REF3133AIDBZR, SOT-23, Quantity: 1.
33. Capacitor, 2.2uF, 1206, Quantity: 1.
34. Voltage Reference IC, REF3112AIDBZR, SOT-23, Quantity: 1.
35. ADC, ADS131M02IPWR, TSSOP-20, Quantity: 1.