

Fabrication of NMOS Transistors

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Abstract – This report describes the fabrication of diodes, MOSCAPs, and functional NMOS transistors on a single p-Si wafer. 2- and 4-point probe analysis via I-V and C-V measurements were used to characterize device performance and the effect of different device dimensions. For a 1000 μ m length pn diode, a reverse leakage current of -0.0265mA and threshold voltage of 0.3 were found, with an ideality factor of 271. For a 200 μ m gate width by 20 μ m gate length NMOS transistors, we saw rectifying characteristics by I-V measurements and found source - drain current of 5.0×10^{-4} A at gate-source voltage of 0.7 V. We also calculated transconductance to study how the source-drain voltage and dimensions of the channel area affects the device performance.

1. INTRODUCTION

The purpose of this work was to create n-channel metal oxide semiconductor field-effect transistor (NMOS) devices, by building upon the techniques and theory learned in prior experiments. The following describes the theory for fabrication, while the fabrication process and results are described in detail in Sections 2 and 3. Discussion and analysis of the results is detailed in Section 4.

A MOSFET consists of four terminals: the source, drain, gate, and base. These terminals build the transistor itself; they are built during fabrication via the structures of metal-oxide-semiconductor capacitors (MOSCAPS), p-n junctions or diodes, oxide insulator, or exposed substrate of varying length and width. The source and the drain are each highly conductive, n-type regions, opposing the p-type substrate. The semiconducting substrate is separated from these n-type regions by p-n junctions. Between the source and drain is the metal gate, which is separated from the semiconducting substrate by the gate oxide; a full cross-sectional view of these components can be seen in Figure 1.

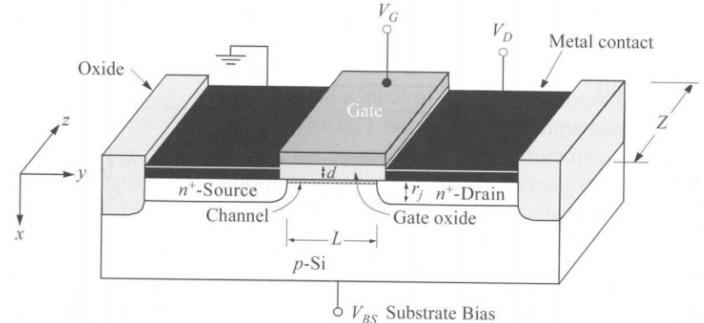


Fig. 1: nMOSFET cross section [1].

The p-n diode, or junction, consists of a semiconductor doped heavily with negative charge carriers on one side, and doped heavily with opposing charge carriers on the other side. Where the two doped regions meet, the charge carriers diffuse into the adjacent doped region, causing positive and negative recombinations. These recombinations eliminate the movement of free carriers for immobile exchange of ions, and creates a region known as the *depletion region*.

Due to the ionized acceptors and donors, the built-in barrier potential prevents the movement of charge until bias is externally applied. The bias may either be forward or reverse bias; a forward bias is defined as external bias that reduces the width of the depletion region, and has increasing current flow with applied voltage. This current increases exponentially as the barrier potential decreases and charge carriers cross the junction. Reverse bias increases the width of the depletion region, but flows current through minority carriers. This allows for a small but limited current, which quickly reaches its saturation, and is referred to as reverse saturation current. The junction behavior is described by the Ideal Diode Equation [2],

$$I = I_0 e^{(\frac{qV}{nkT} - 1)}$$

where I is the diode current, I_0 is the reverse-bias saturation current, V is the applied voltage across the diode, q is electron charge, k is Boltzmann's constant, and n is the ideality factor of the diode. The various bias behaviors modeled by the diode equation are seen as in Figure 2,

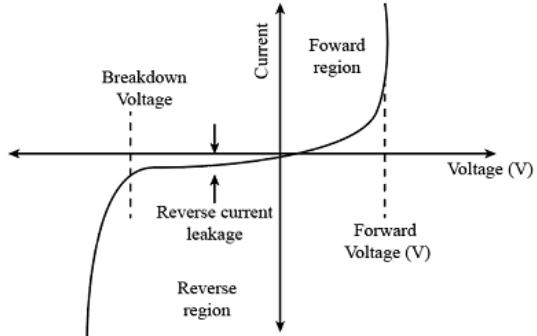


Fig. 2: Diode I-V behavior as modeled by the Shockley Diode Equation [mcallister].

At high reverse bias voltages, breakdown behavior begins to take over – this is caused by two processes; Zener and avalanche breakdown, dependent on the dopant concentration. In each case, the junction ceases to function; however, failure is only permanent in the event of an avalanche breakdown over a thick depletion region. In the case of breakdown, the entire device fails with an essential component lost.

Meanwhile, the MOSCAP, or metal oxide semiconductor capacitor, works at the center of the device. The MOSCAP is also responsible for full operation of the FET (field-effect transistor). It consists of a semiconductor body, or substrate; an insulator film; and a metal electrode, called a gate. In this experiment, these materials are p-type Si, SiO₂, and aluminum, respectively. Figure 3 shows a cross section of the capacitor.

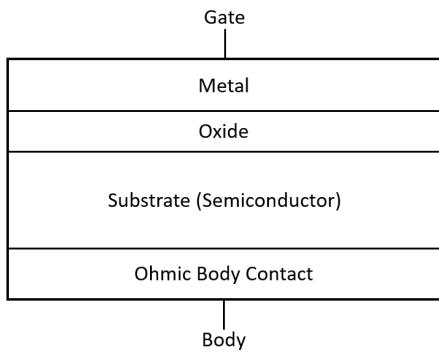


Fig 3: MOSCAP cross section.

The MOSCAP functions due to divergence in work function between the metal and semiconductor. This causes a band bending in the semiconductor region. When the work function of the metal is smaller than that of the semiconductor, it leads to a depletion of holes near the oxide, and is referred to as the depletion layer. This layer is then free of carriers, leaving negatively charged and immobile acceptor ions near the oxide surface. Upon applying a voltage at the gate,

$$V_{FB} = \phi_m - \phi_s$$

Band bending flattens, leading to the “flat-band condition.”

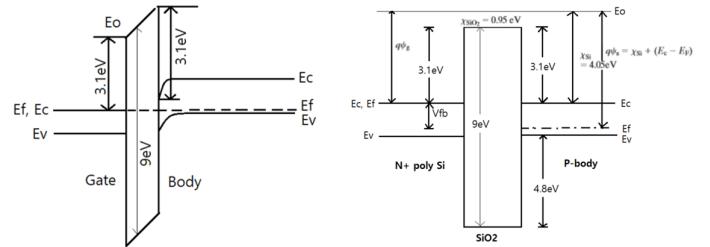


Fig. 4: Band diagrams of the MOS structure when $\phi_m < \phi_s$ (left) and in the flat-band condition (right) [3].

As shown in Fig. 4, the conduction and energy band gaps of the substrate become flat at the oxide interface. At flat-band condition, there is no electric field in the device. For the Al/SiO₂ interface, the applied voltage must be negative. If the magnitude exceeds that of the magnitude necessary for flat-band condition, the direction of band bending changes again (mirroring Fig. 4(a)). Consequently, carriers accumulate near the oxide; this is referred to as accumulation. With a high positive voltage applied, bending bands steeper and similarly to Fig. 4(a), the device enters the inversion region. These regions exhibit specific C-V characteristics which help in analyzing the overall quality and characteristics of the MOSFET.

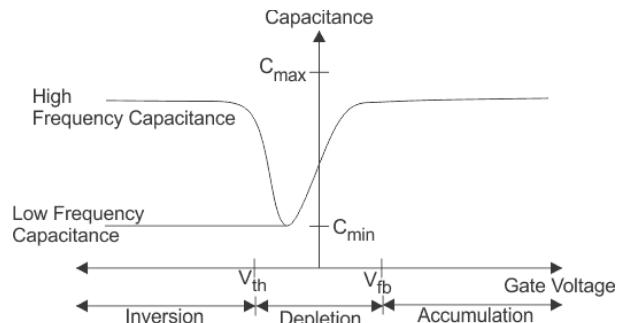


Fig. 5: General C-V characteristics of a capacitor with $\phi_m < \phi_s$ [4].

MOSFETs can otherwise be identified by the sign of their threshold voltage, indicating which of two types the transistor is: depletion or enhancement mode. In depletion mode, the device is turned ON at zero gate-source voltage, and can be turned off with applied negative voltage. In enhancement mode, the device is turned ON by increasing the gate voltage higher than the source.

Other contributors to characterization include analysis of transmission line measurement pads and transconductance calculations. TLM contact patches are areas on the mask designed with specific spacing for measurement, which makes it possible to determine contact resistance, according to the equation:

$$R_T = 2R_C + R_{sheet} \frac{L}{W}, \quad \left(R_{semi} = R_{sheet} \frac{L}{W} \right)$$

Where R_T is total resistance, and R_C is contact resistance. It also indicates the behavior of contacts as Schottky or Ohmic. Transconductance describes the ability of the transistor to produce current with the application of voltage across the gate, and is calculated by,

$$g_m = \frac{\Delta I_D}{\Delta V_g}$$

Which indicates the sensitivity of the transistor. Both 2 and 4 point probe setups were used to determine C-V and I-V characteristics of the fabricated devices, the results of which can be found in the subsequent portion of this report.

2. EXPERIMENTAL

Summary. Transistors and diodes with varying geometries were fabricated using conventional lithography, oxidation, and metal deposition steps. Four lithography steps were performed for three purposes: (1) to expose the source and drain contacts for n-type doping, (2) to pattern windows for the field oxide at the gate contact, (3) to pattern the contacts for the device source, drain and their respective vias. Each fabrication step is described in order and followed by a brief description of IV and CV measurements for device characterization.

1st Lithography: n-Doping Source and Drain.

The purpose of the first lithography step was to expose the source and drain for n-type doping of ohmic contacts. As shown in Fig.6, this required five principal steps including (a) initial oxide growth for isolating different devices on the same wafer, (b) lithography to expose the source and drain, (c) oxide etching down to the contact point for the source and drain, (d) phosphorus diffusion doping of the source and drain, and (e) regrowth of a 300 nm oxide on the contact regions while driving-in the phosphorus dopant. The result in Fig.6(e) are variations in 600 and 300 nm SiO₂ patterned over n-type contacts.

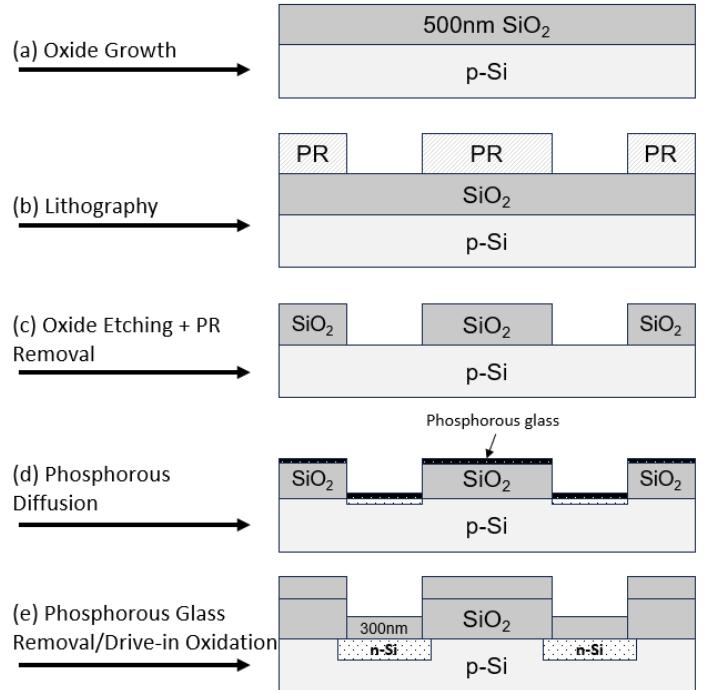


Fig. 6: Schematic of the first lithography step, including (a) the initial silicon wafer , (b) oxide growth, (c) lithography, (d) oxide etching, (e) phosphorus diffusion, (f) phosphor glass removal, and dopant drive-in.

First, two 6-inch diameter boron-doped (100) Si wafers were cleaved into several 2 sq. inch samples along the {110} planes using a diamond scribe. Wafer thickness, sheet resistances, and sheet resistivities were measured using wafer calipers and 4-point probe (4PP) measurements to assess wafer uniformity. Thickness was $553.7 \pm 0.1 \mu\text{m}$, the sheet resistance was $149.8 \pm 0.4 \Omega/\square$, and the resistivity was $8.29 \pm 0.02 \Omega \cdot \text{cm}$ across the wafer. Resistivity was within the manufacturer's expectations ($1-100 \Omega \cdot \text{cm}$). The fact that the thickness was greater than the expected $525 \pm 25 \mu\text{m}$ did not, to our knowledge, impact device fabrication or performance. According to NIST standards [el-kareh], the measured resistivity corresponded to a $\sim 5.5 \times 10^{14} \text{ cm}^{-3}$ carrier density, with $\sim 420 \text{ cm}^2/\text{Vs}$ mobility. This was below the $450 \text{ cm}^2/\text{Vs}$ maximum for pure silicon, as expected.

After triple-rinsing the samples in acetone, isopropyl alcohol, and water, a 10-minute, 80°C piranha clean in a 5:1 parts H₂SO₄:H₂O₂ solution, and a 10 second BHF treatment to remove residual surface oxides, a three-step thermal oxidation was performed at 1020°C , including 10 minutes of dry oxidation first, 70 minutes of wet oxidation second, and a 10 minutes of dry oxidation last to minimize hydrogen impurities at the critical interfaces. The thickness of the oxide was $485 \pm 2 \text{ nm}$ by reflectometry.

Photolithography of the mask layer 1 pattern was performed using standard spin-coating and hard-contact mask alignment steps detailed here. First, samples were solvent cleaned using the triple-rinse procedure mentioned before, then dehydration baked for 3 minutes at 120°C to remove

excess water from the silicon surface. One monolayer of hexamethyldisilane (HMDS) was vapor deposited for 3 minutes to make the SiO_2 surface hydrophobic and prevent photoresist (PR) delamination after spin-coating. Positive PR AZ4100 was spin-coated onto the wafer surface at 4000 RPM for 30s to achieve a steady state $\sim 1.2 \mu\text{m}$ thickness. Samples were then soft-baked for one minute at 95°C to evaporate the solvent in the PR. Exposure to a 90 mJ/cm^2 dose at 5 mW/cm^2 ultraviolet (UV) irradiation for 18 seconds using a hard contact mask aligner was used to chemically inscribe the intended oxide etching pattern. Finally, the patterns were developed for 71 seconds using the 1:4 AZ 400K developer to wash away the pattern onto the photoresist. The results of development on a portion of the 12 transistor array is shown in Fig. 7(a). Features are well-defined to the smallest transistor gate length ($5 \mu\text{m}$), shown in Fig. 7(b), and the surface was visibly clean.

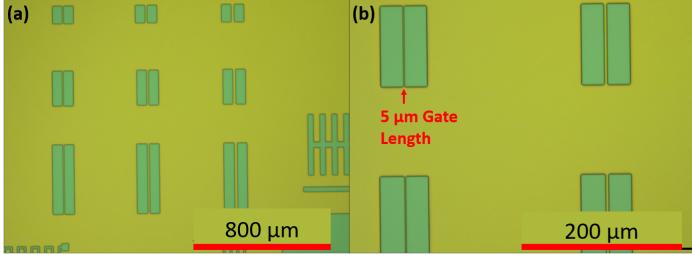


Fig. 7: (a) 5x and (b) 20x micrographs of the 12 transistor array of varied gate lengths and widths. The 20x micrograph shows well-defined features down to the smallest gate length ($5 \mu\text{m}$).

Samples were prepared for oxide etching via a hard bake at 120°C for 5 minutes to evaporate surface H_2O and strengthen the PR from the SiO_2 etching step via heat-induced crosslinking. Following a 2 minute oxygen plasma cleaning step to clear the samples of organic debris using the reactivity of oxygen plasma, we calibrated the etch rate in buffered hydrofluoric acid (BHF) using a reference sample at 1 minute increments, which was found to be around 99.7 nm/min . With a $\sim 500 \text{ nm}$ oxide, the etch time was 6 minutes, which included a 20% overetch to eliminate any residual oxides that would compromise device functionality at the critical interfaces. After etching, samples were rinsed in DI water to prevent excessive sidewall etching. Samples were rinsed in acetone to completely remove the PR.

Fig. 8 summarizes the first lithography and oxide etching steps. First, the PR is exposed and developed (Fig. 8(a)), with two trenches at the sources and drains of the transistors shown in Fig. 7. After etching and photoresist removal, the profile in Fig. 8(b) is achieved, in which the low points are the bare Si wafer and the upward steps are of the oxide. The PR thickness was $1167 \pm 19 \text{ nm}$, while the oxide thickness by DEKTAK was $497 \pm 3 \text{ nm}$ and comparable to $485 \pm 2 \text{ nm}$ measured by reflectometry.

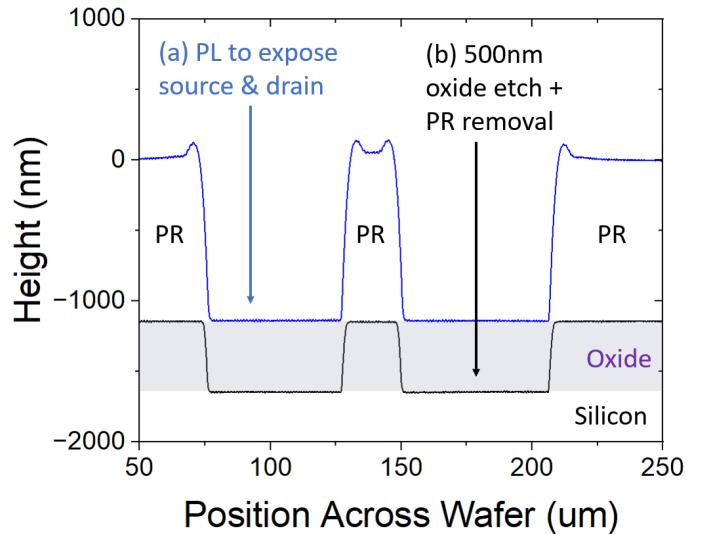


Fig. 8: Depth profiles across the transistor patterns (a) after exposure and development and (b) after the oxide etch and photoresist removal.

The final step was phosphorus predeposition and drive-in oxidation. Samples were placed into a loading tray outfitted with planar PH-1000N phosphorus diffusion sources facing the polished side of the samples. Predeposition occurred at 950°C for 15mins, and was followed by a 30s BHF etch to remove the phosphor glass layer. Successful removal of the glass was demonstrated by water beading on the sample surfaces.

For a sanity check, sheet resistance and resistivity measured from the 4PP method was lost, so the Lab 2 results are referenced here, given identical predeposition procedures. Ignoring parallel resistance from the undoped p-Si, sheet resistance was $25.1 \pm 0.7 \Omega/\square$, yielding a junction depth of $x_j = 9.8 \times 10^{-5} \text{ cm}$ by the manufacturer's technical specifications. This assumes uniform doping. Based on x_j , the resistivity of the doped layer was $(2.5 \pm 0.007) \times 10^{-3} \Omega \cdot \text{cm}$, compared to the base wafer in Table I below.

Table I: Comparison of sheet resistance ρ_s and resistivity ρ before and after predeposition.

Timing	$\rho_s = R [\Omega/\square]$	$\rho = \rho_s \cdot x [\Omega \cdot \text{cm}]$
Before	149.8 ± 0.4	8.29 ± 0.02
After	25.1 ± 0.7	$(2.5 \pm 0.007) \times 10^{-3}$

The results are consistent with $\rho = 1/ne\mu$ from the Drude model, where n is the carrier concentration, e is the fundamental charge, and μ is the carrier mobility. Resistivity increased after phosphorus diffusion due to an increase in activated phosphorus donors (assuming complete doping efficiency). This increased the carrier concentration, which dropped the resistivity/sheet resistance by $\sim 10^3$, shown in Table II. Given that the majority carriers changed from holes to electrons after predeposition, the resulting electron mobility $\sim 97 \text{ cm}^2/\text{Vs}$ was reasonably below the maximum of $1400 \text{ cm}^2/\text{Vs}$. The difference is more

significant due to higher concentrations of ionized impurities, which reduce carrier mobility.

Table II: Comparison of dopant/carrier density n and carrier mobility μ before and after predeposition.

Timing	n (cm^{-3})	$\mu = 1/\rho n e$ (cm^2/Vs)
Before	5.5×10^{14}	~ 420 (holes)
After	$\sim 2 \times 10^{19}$	~ 97 (electrons)
Literature Values	-	≤ 450 (holes) ≤ 1400 (electrons)

The final step was the growth of a 350 nm oxide over the n-doped regions to drive-in the phosphorus doped layer. After the rinsing/piranha/BHF sample cleaning procedure, a 10 minute dry, 38 minute wet, and 10 minute dry oxidation procedure was performed at 1020°C. The oxide thickness was measured to be ~360 nm over the n-doped regions, while the thicknesses of those already oxidized had grown to be 570 ± 14 nm by reflectometry.

2nd Lithography: Growth of Gate Oxide.

The purpose of the second lithography step was to expose the gate region of the bare Si to grow a thin 50 nm oxide as a component of the MOSCAP stack. As shown in Fig.9, this required three principle steps including (a) lithography to expose the gate region of the oxide, (b) oxide etching to expose the bare silicon at the gate, and (c) growth of the 50 nm gate oxide. The results of this step (Fig.9(c)) are approximately the same as in the previous lithography, except that a 50 nm was patterned over the gate regions.

The standard lithography procedure was performed to align and expose the second mask layer pattern onto the samples. Additional steps were taken to ensure that the patterns were aligned within just a few microns of error.

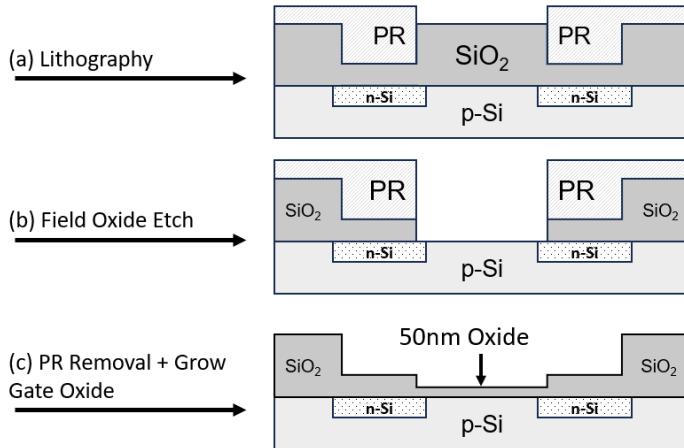


Fig. 9: Schematic the second lithography step, including (a) exposure of the gate region by lithography, (b) etching of the field oxide, and (c) growth of the 50 nm gate oxide.

After a 70s development, we found a misalignment around $\Delta=1\mu\text{m}$ in both directions, shown by the micrograph in Fig.10 and schematically in Fig.11(b).

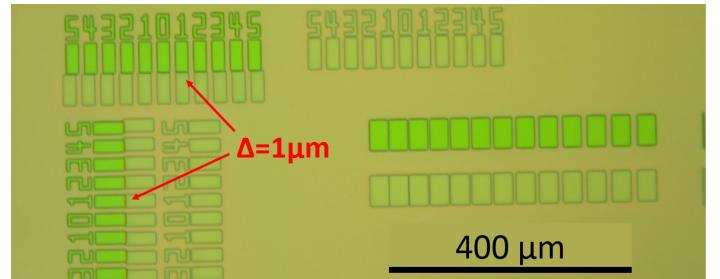


Fig 10. 10x micrograph of Venier patterns indicating a $\Delta = 1\mu\text{m}$ misalignment between mask layer 1 and mask layer 2.

Next, samples were etched to the gate region. After hard-baking to strengthen the photoresist against the buffered HF etchant, the etch rate was calibrated to 122.6 nm/min. The samples were etched for 6 minutes for a thickness of 600 nm, the results of which are shown in Fig.11(c).

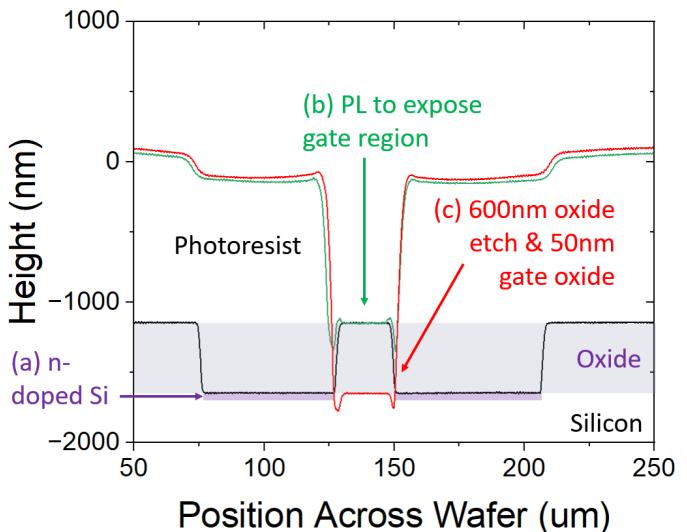


Fig 11. Depth profiles across transistor patterns (a) after phosphorus doping, (b) after photolithography to expose the gate region, and (c) after the oxide etch for the gate oxide growth.

The depth profiles mentioned before in Fig.11(b) and (c) show a difference in 500 nm height after the etch for one sample, corresponding to the oxide thickness. Compared to the initial profile in Fig.11(a), indicated by the n-doped regions, additional thickness needed to be accounted for after the additional drive-in oxidation. The teeth-like features at the bottom corners of the trenches as in Fig.11(c) indicates discontinuities at the Si surface due to uneven consumption of Si during oxidation of selective regions.

Finally, after removing the photoresist in acetone and the piranha/BHF cleaning procedure, the samples underwent another oxidation at 1020°C for 63 minutes. Only dry oxidation was performed this time for a higher purity oxide. The thickness was confirmed to be ~ 51 nm by ellipsometry, as reflectometry was too imprecise for thin oxides.

3rd/4th Lithography: Metal Patterning

The purpose of the final two lithography steps was to expose the source, gate, drain, and vias for metal deposition while ensuring that each component is electrically isolated. Shown in Fig.12, this involved four steps: to (a) perform lithography and expose the source and drain regions, (b) etch to the n-Si layer, (c) spin photoresist on areas where metal is to be removed, and (d) deposit and lift-off ~ 300 nm of aluminum in the appropriate regions.

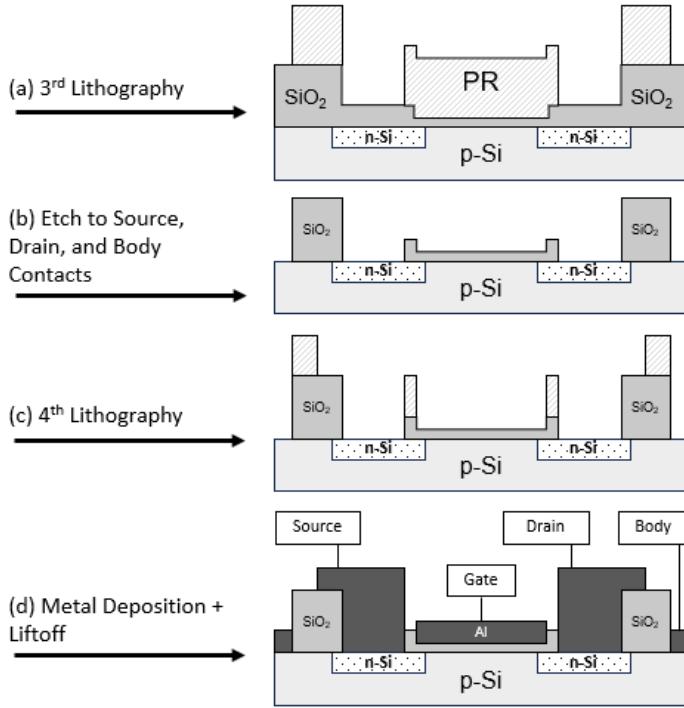


Fig. 12: Schematic of the processes involved in the third and fourth lithography steps, including (a) exposing the contact regions by lithography, (b) etching the oxide to the contact regions, (c) another lithography step to lift-off metal in unwanted areas, (d) metal evaporation and liftoff, and (e) a micrograph of a fabricated transistor.

Following the standard solvent cleaning and spin-coating procedure, samples were aligned and exposed using the same procedure as the 2nd lithography for mask layer 3. After developing, hard baking, and plasma descumming the samples, the micrograph in Fig.13 was obtained, revealing a minor misalignment $\Delta < 1 \mu\text{m}$ in both directions.

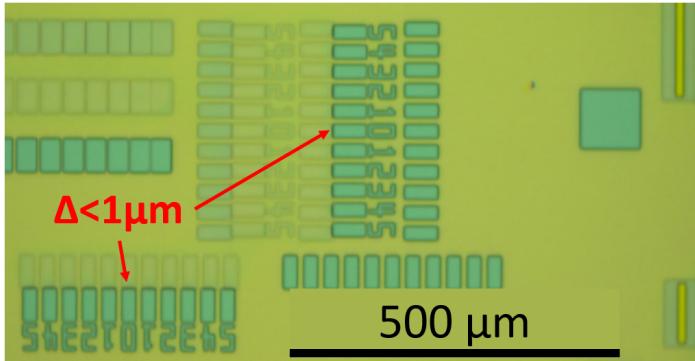


Fig. 13. 10x micrograph of Venier patterns indicating a $\Delta < 1 \mu\text{m}$ misalignment between mask layer 2 and 3.

Next, samples were etched down to the source and drain contacts using the standard oxide etching procedure, preceded by a plasma descum step. To ensure complete etching, an etch time of 8 minutes was used. The etch rate was estimated to be 100 nm/min, with a 600 nm oxide thickness to account for every oxidation step so far. Fig.14(a) shows the results of the etch, including the photoresist before removal. Fig.14(b) shows the height profiles after removing the photoresist.

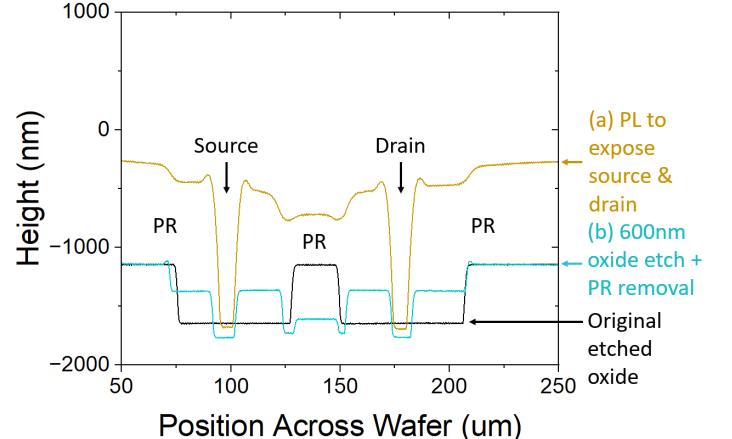


Fig. 14: Depth profiles across transistor patterns (a) photolithography exposing the source and drain, and (b) after the 600 nm oxide etch. The original etched oxide is shown for reference.

For the fourth lithography step of mask layer 4, the standard solvent cleaning and spin-coating procedure was followed, and samples were aligned and exposed using the procedure in the previous lithography step. However, with metal evaporation as the next step samples were soaked in toluene for 5 minutes before development to ensure the deposited metal would be discontinuous as the sidewalls. Samples were developed for an extra 30s compared to normal to account for PR hardening. This time the samples were not hard-baked. After a 1-min plasma descum, the micrographs in Fig.15. were obtained. Similarly to the previous step, both directions showed a minor misalignment $\Delta = 1 \mu\text{m}$ (Fig.15(a)). A micrograph of four transistors in Fig.15(b) shows the pads, contacts, and gate regions where the metal was to be deposited.

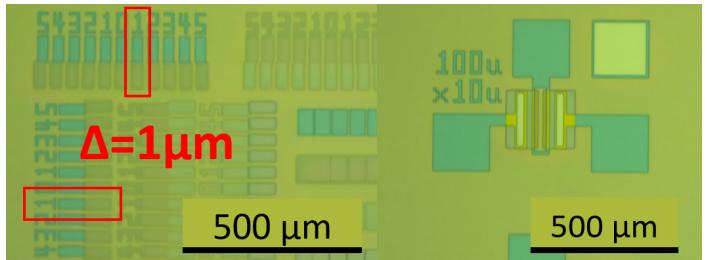


Fig. 15: (a) 10x micrograph of Venier patterns indicating a $\Delta = 1 \mu\text{m}$ misalignment between mask layer 3 and 4, and (b) 5x micrograph showcasing a transistor with $100 \times 10 \mu\text{m}$ gate dimensions.

The resulting pattern at this point is shown in Fig.16(a), in which photoresist remains in the areas

where metal is to be lifted off. These act as insulating regions where different portions of the device are electrically isolated. The source, gate, drain, and vias are exposed, while the remainder of the device is not.

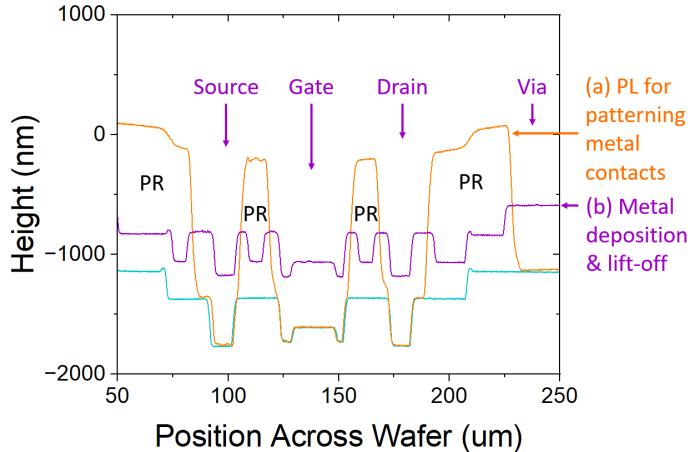


Fig. 16: Depth profiles across transistor patterns (a) photolithography exposing the source and drain, and (b) after the 600 nm oxide etch. The original etched oxide is shown for reference.

Immediately after a 10 second etch in BHF to remove ambient oxide formation, aluminum was deposited onto the samples using electron-beam evaporation and lifted-off, revealing the purple profile in Fig.16(b). The film was lifted-off by immersing the samples in acetone overnight, and afterward repeatedly sonicating for 3 minute segments and aggressive pipetting to rinse away unwanted film. Based on analysis of Fig.16, the metal film thickness was ~ 559 nm, though the thickness differed depending on the deposition location. Smaller features deposited thicker amounts of Al, also with a higher RMSE, shown in Table III.

Table III. Comparison of thickness of evaporated aluminum over the gate, drain, source, and vias of one transistor.

Region	Thickness (nm)	RMSE (nm)
Gate	545	0.06
Drain	566	0.27
Source	586	1.53
Via	541	0.04

After the appropriate amount of aluminum was removed, the following micrographs were obtained and are shown in Fig.17(a) for Vernier patterns and Fig.17(b) for images of the transistor array.

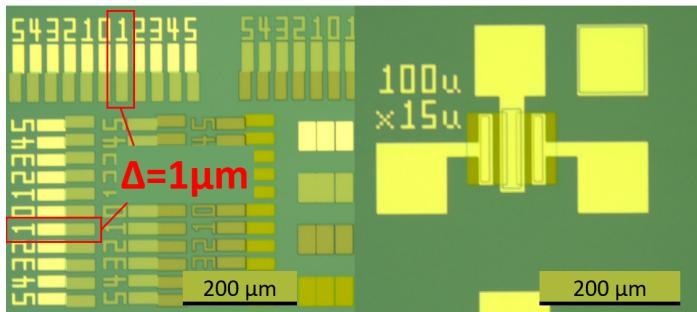


Fig. 17: (a) 10x micrograph of Venier patterns indicating the same $\Delta = 1 \mu\text{m}$ misalignment between mask layer 3 and 4 as in Fig. 16(a), and (b) 5x micrograph showcasing a transistor with $100 \times 15 \mu\text{m}$ gate dimensions. The micrographs are identical to Fig. 16, except that the Al film enhanced the brightness contrast.

The metal was patterned reliably, as the misalignment $\Delta=1\mu\text{m}$ is identical to the micrograph of the same feature in Fig.15(a); the only difference is that the metal film enhanced the brightness contrast.

Electrical Characterization

This final portion of the experiment was dedicated to the demonstration of more complex device characterization. First, the aluminum film, TLM pads, and source-drain contacts were tested using both 2-probe and 4-probe measurements. Second, contact resistances and channel resistances were measured using the 2-point method on the TLM patterns. Third, diodes were measured for IV and CV characteristics using a 2-probe setup to determine the key on, off, and breakdown features. Finally, the IV characteristics of the transistors using a 4-probe setup and CV characteristics of MOSCAPs using a 2-probe setup were performed to determine key on, off, accumulation, and inversion properties. No additional sintering was needed to establish ohmic contacts. Further details are included in the next section.

3. DISCUSSION & ANALYSIS

TLM Characterization

The transmission line method (TLM) was used to calculate the sheet and contact resistance by both 2PP and 4PP measurements by relating the total resistances as a function of TLM pad distance. Fig. 18 plots of the total resistances as a function of TLM pad distances, and shows that the 4PP method reduced both the sheet resistance from the slope and the contact resistances from the intercepts. Contact resistances were 2.865Ω and 0.77Ω for 2PP and 4PP, respectively. Sheet resistances were $20.1\Omega/\square$ and $15.9\Omega/\square$ for 2PP and 4PP, respectively. This is expected; 4PP measurements eliminate contact resistance from the probe itself.

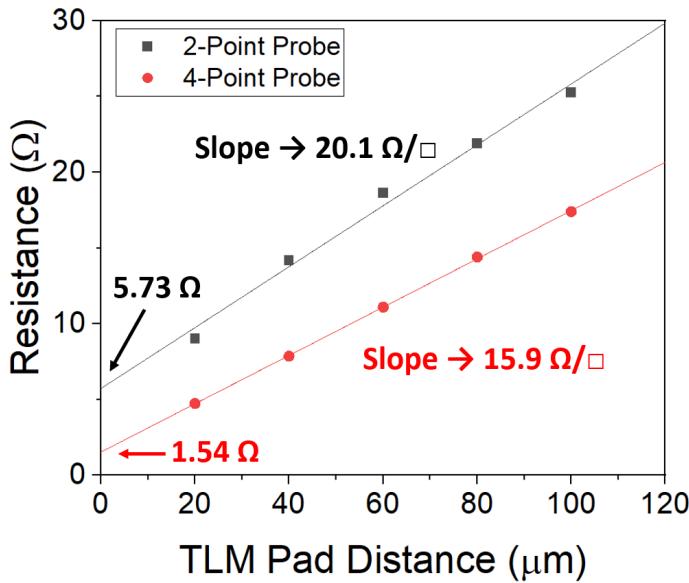


Fig. 18: Resistance versus TLM pad distance for the 2-point probe (black) and 4-point probe (red) tests, showing contact resistance (intercept/2) and sheet resistances (slope $\times 10^3$).

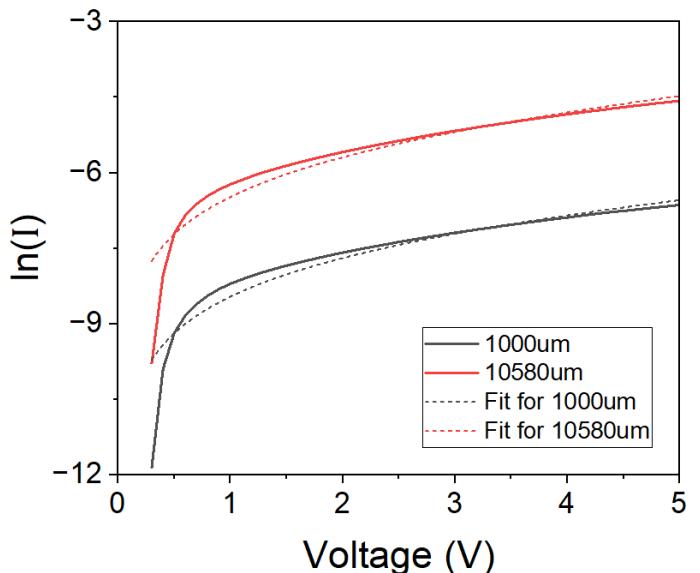


Fig. 19: Ideality calculation from 1000 μm and 10580 μm diode $\ln(I)$ vs bias voltage plots. Parameters I_0 and n (ideality factor) were fitted logarithmically, yielding $n = 271$ for 1000 μm and $n = 214$ for 10580 μm .

Basic Capacitors

Both $100 \times 100 \mu\text{m}$ and $1000 \times 1000 \mu\text{m}$ capacitors were measured for CV curves using a 2PP. The capacitance values of the 1000 μm capacitor returned an open circuit upon repeated measurement, and could not be used to reconfirm gate oxide thickness. However, the 100 μm capacitor returned a CV curve with average capacitance of 0.0262 nF. From the formula,

$$C = \frac{\epsilon_r \epsilon_0 A}{d}$$

with ϵ_0 being the vacuum permittivity, and $\epsilon_r \approx 3.9$ as the dielectric constant of silicon dioxide [campbell], an oxide thickness of 13.19 nm was calculated. This is within range of the intended gate oxide thickness of 50 nm, but falls short of the ideal value. The discrepancy may be due to contamination during mask application, local oxide damage from nearby measurements, or trapped charges at the interfaces between regions.

P-N Diodes

To calculate ideality factor, the natural log of the current was plotted against the bias voltage according to the ideal diode equation, seen in Fig. 19. The data was fitted to parameters I_0 and n , and ideality factor n of 271 and 214 were found for diode lengths of 1000 and 10580 microns, respectively. This value differs **wildly** from the expected range of 1-2. As the diode equation does not account for effects of series resistance, variations in reverse leakage current present, nor ambient light effects, an out-of-range ideality factor is reasonable.

Next, IV curves are shown in Fig. 20 to show the threshold voltages for the 1000 μm and 10580 μm diodes. These were found to be 0.3V for both diode scales, as at the point of maximum curvature, the current for both diodes suddenly increased.

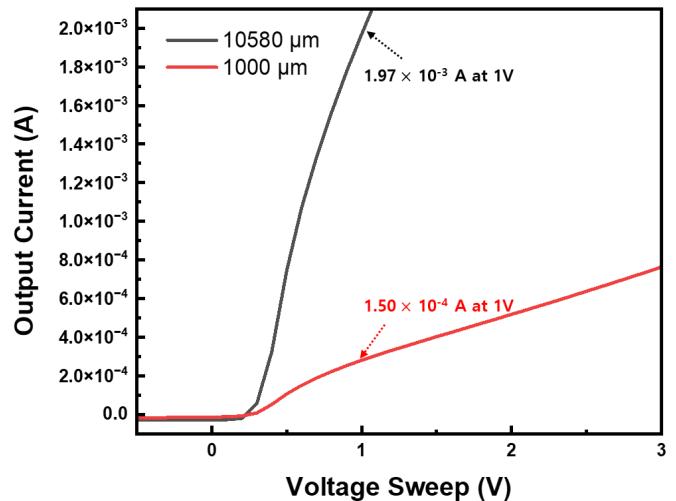


Fig. 20: Graph of IV Curve for a 10580 μm diode vs a 1000 μm diode on our chip, under a voltage sweep from -5 to 5 volts.

The series resistance (resistance in the forward bias ohmic regime) of the larger diode was lower at 481Ω , compared to 3846Ω for the 1000 μm . Thus, resistivity decreased with increasing diode area. The reverse leakage current at -5 V for the 1000 μm and 10580 μm diodes were -0.0265 mA and -0.0354 mA , respectively. For both diodes, reverse bias breakdown down to -20V was not achieved. Reverse saturation currents were roughly 0.03 mA .

I-V Measurements of Transistors

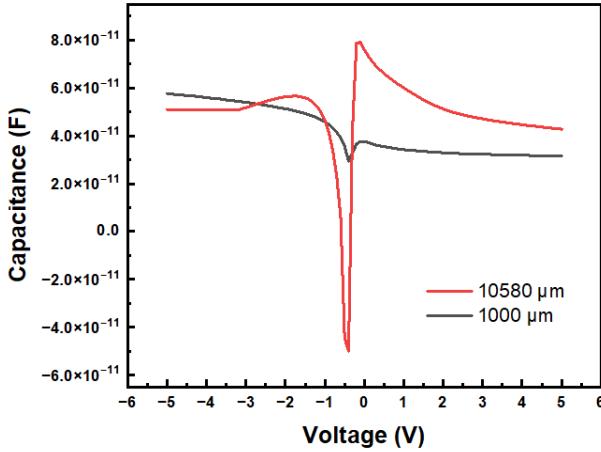


Fig. 21: C-V of 1000 μm and diode 10580 μm from the gate to body.

C-V measurements of the diodes were taken as seen in Fig. 21. The acceptor concentrations $N_a(w)$ were plotted as a function of position in Fig. 22 using formulas relating capacitance, depth, and acceptor concentration below:

$$N_a(w) = -\frac{C^3}{q\epsilon_r \epsilon_0 A^2 \frac{dC}{dw}}$$

$$w = \frac{\epsilon_r \epsilon_0}{C}$$

Knowing the precise area of this device is important to calculating an accurate acceptor profile, and our area of 25 μm by 1000 μm is not trustworthy.

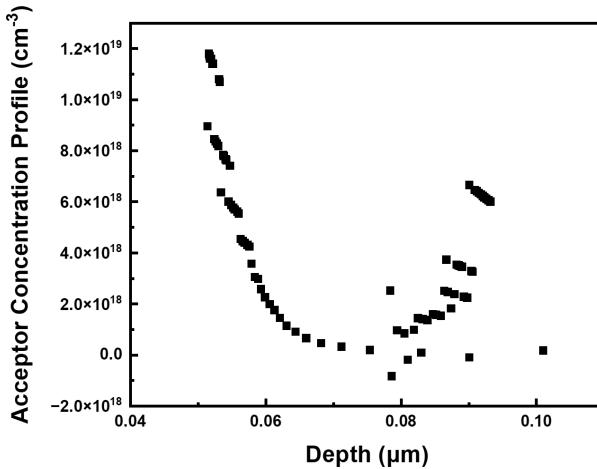


Fig. 22: Acceptor concentration profile of 1000 μm diode.

Acceptor concentration follows a semi-parabolic relationship; concentration decreases exponentially as depth approaches 0.8 μm . This profile is indicative of successful doping near the surface. However, the increasing concentration after the minimum indicates that acceptors were prevalent in high concentration inside the diode.

The purpose of the drain-source current (I_{ds}) vs. drain-source voltage (V_{ds}) measurement is to estimate the pinch-off voltage when gate-source voltage (V_{gs}) is applied, which indicates the formation of a saturated channel layer. If V_{ds} is less than the pinch-off, the slope (dI_{ds}/dV_{ds}) should be high. If V_{ds} exceeds the pinch-off, the slope should decrease and approach zero. [10]

Fig. 23 is the I_{ds} - V_{ds} curve of the transistor with 200 μm channel width and 20 μm channel length. The I_{ds} was measured by sweeping the V_{ds} from 0 to 5 V, increasing V_{gs} in 0.1 volt steps from 0 V to 0.7 V. When $V_{gs} = 0.7$ V was applied, the I_{ds} reached 5.0×10^{-5} A when V_{ds} went higher than 0.65 V, the pinch-off voltage where the channel was completely saturated. Also, I_{ds} was higher when higher V_{gs} was applied, which corresponds to the drain-source current equation of the MOSFET. [1]

$$I_{ds} = \frac{W}{L} \mu_{eff} C_{ox} \frac{(V_{gs} - V_{th})^2}{2}$$

Every I_{ds} - V_{ds} curve had each pinch-off voltage, indicating that the channel layer was successfully formed and saturated in the active layer with increasing the V_{ds} . [10] The dashed curve in Fig. 23. is the plot of pinch-off voltages with V_{gs} from 0 V ~ 0.7 V and the right part is the saturation regime of the channel in the device. Specifically, the pinch-off V_{ds} at $V_{gs} = 0.7$ V was about 0.65 V, which is the minimum V_{ds} that should be applied for I_{ds} - V_{gs} measurement in the saturation regime.

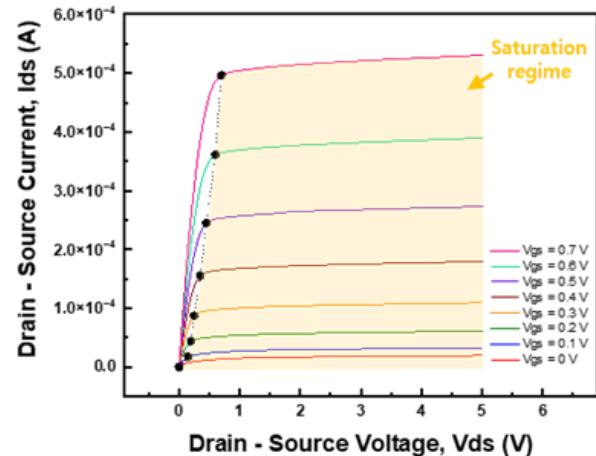


Fig. 23: I_{ds} - V_{ds} curve for MOSFET of 200 $\mu\text{m} \times 20 \mu\text{m}$ channel area with stepping V_{gs} from 0 V to 0.7 V. The dots in each curve are the pinch-off voltages.

The most important purpose for studying I_{ds} - V_{gs} curves in the transistors is to observe the rectifying behavior with low off current and high on current. This allows us to make predictions about the power consumption and switching performance. The curve at $V_{ds} = 0$ V was measured first, and we observed no

rectifying behavior, meaning that there was no leakage current for the malfunctioning of the transistors. When V_{ds} was applied around 0.1 V to 0.5 V (less than pinch-off voltage) the transistor showed rectifying behavior. However, I_{ds} ranged from 1.4×10^{-4} A to 4.8×10^{-4} A at $V_{gs} = 0.7$ V, which is lower than the I_{ds} measured in I_{ds} - V_{ds} curve after V_{ds} exceeds the pinch-off. This result indicates that the channel did not successfully form in the active layer when V_{ds} is less than the pinch-off. And when V_{ds} was applied at 0.7 V which is higher than the pinch-off voltage, the I_{ds} reached around 5.0×10^{-4} A at $V_{gs} = 0.7$ V, similar to the I_{ds} level measured in the saturation regime. And there were no significant changes in the I_{ds} when the higher V_{ds} was applied from 1.0 V to 5.0 V. These results of V_{ds} value being higher than 0.7 V shows that the channel layer was successfully formed and saturated.

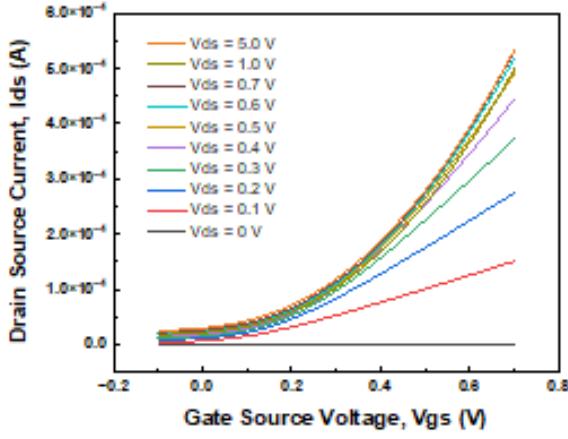


Fig. 24: I_{ds} - V_{gs} curve for MOSFET of $200 \mu\text{m} \times 20 \mu\text{m}$ channel area with stepping V_{ds} from 0 V to 5 V.

Fig. 25. shows the I_{ds} - V_{ds} curve of the transistor with different channel widths and channel lengths to study how the dimensions of the channel affects the device performance. The red curve is the device with shorter channel length of 15 μm than the black curve with the length of 20 μm , and the blue curve with shorter channel width of 100 μm than the black curve with 200 μm length. The I_{ds} was measured to be higher with shorter channel lengths and longer channel widths, which corresponds to the I_{ds} equation in the textbook [1]. The pinch-off voltages in all the three curves were similar at about 0.65 V, which means that the dimensions of the channel layer did not affect the formation and the saturation of the channel.

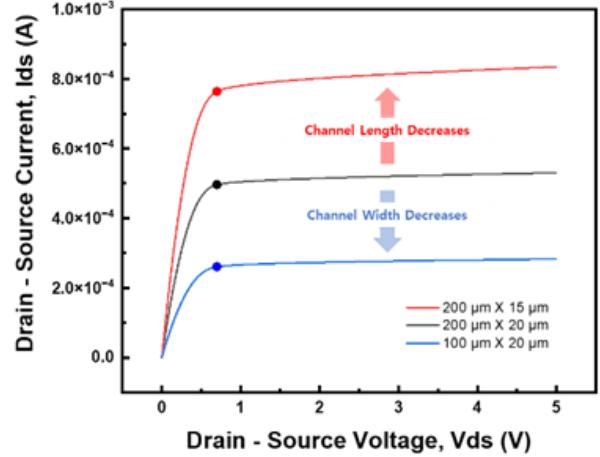


Fig. 25: I_{ds} - V_{ds} curve for MOSFET 0.7 V of V_{gs} applied with different channel width and length.

A useful metric to understand transistor operation is the transconductance ($g = dI_{ds}/dV_{gs}$) with respect to V_{gs} shown in Fig. 26. The increasing nature of the g - V_{gs} relationship means that the device is operating as a transistor, forming the channel in the active layer. Also, the V_{gs} where g is maximum is the voltage that the device is completely saturated. [10] Therefore, finding the tangent line of the I_{ds} - V_{gs} curves on the V_{gs} and calculating voltage on the line where the $I_{ds} = 0$ V gives the ON voltage, which is known as the threshold voltage (V_{th}) [11]. We extracted V_{th} by calculating g and finding when V_{gs} reaches the maximum.

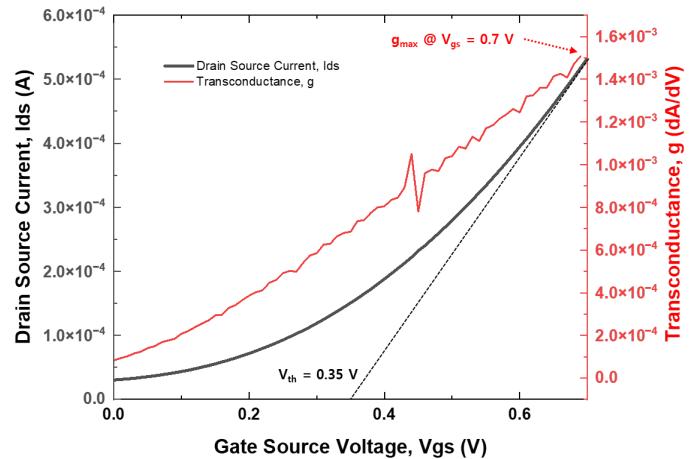


Fig. 26: g - V_{gs} and I_{ds} - V_{gs} curve for MOSFET with of $200 \mu\text{m} \times 20 \mu\text{m}$ channel area at $V_{ds} = 5$ V. The threshold voltage is extracted by extrapolation method at where the transconductance is maximum as shown in the dashed line.

By comparing the V_{th} , we are able to study how the V_{ds} , channel width or channel length affects the performance in the transistors. Fig. 27. shows the difference of V_{th} extracted from the transistors with channel length of 20 μm , with different V_{ds} and channel widths. The black curve in the figure is the V_{th} of the device with channel width of 200 μm . Before the V_{ds} reached the pinch-off, the V_{th} tended to

shift to a positive direction. However, when V_{ds} higher than the pinch-off was applied, V_{th} was maintained around 0.35 V. This result shows that the g was increasing with forming the channel with increasing V_{ds} before it reached the pinch-off voltage. After V_{ds} exceeds the pinch-off, g stopped increasing due to the channel saturation. [10]

Meanwhile, as in the saturation regime of Fig. 27 (a), there was no difference of V_{th} between the transistors with channel widths of 200 μm and 400 μm , which means the width does not affect the g or the channel. Also, as shown in Fig. 27 (b), also there was no difference of V_{th} between the transistors with channel lengths of 10 μm , 15 μm and 20 μm , which indicates that the length also does not affect the g or the channel if channel lengths are higher than certain point. This result corresponds to the pinch-off voltages estimated from the I_{ds} - V_{ds} curve that measured with different channel width and length in the previous paragraph. [1,10]

However, when the channel length was too short like 5 μm which is shown in Fig. 27 (b), the V_{th} tended to shift to the negative direction. This might be due to the shorter channel length than the channel can be formed with a smaller amount of V_{ds} . This result corresponds to the I_{ds} - V_{gs} curve for the transistor with 200 $\mu\text{m} \times 5 \mu\text{m}$ channel area measured at $V_{ds} = 5 \text{ V}$, as described in inset curve of Fig. 27 (b), which showed significantly high I_{ds} of $6.0 \times 10^{-2} \text{ A}$, compared to the devices with longer channel lengths.

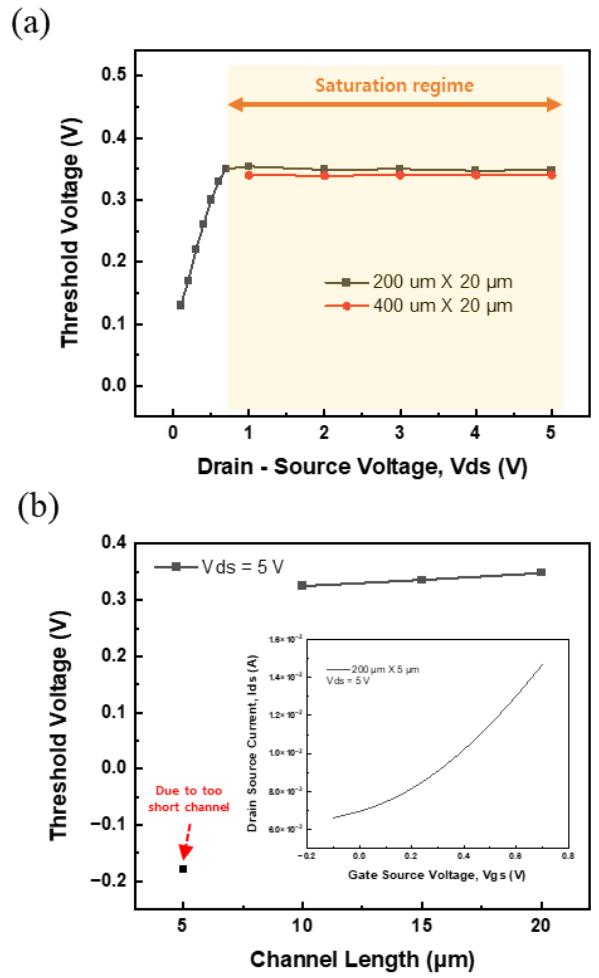


Fig. 27: Difference of V_{th} with (a) different drain voltages and channel widths with the MOSFETs which has channel length of 20 μm , (b) different channel lengths with the MOSFETs which has channel width of 200 μm , inset figure in (b) is the I_{ds} - V_{gs} curve for MOSFET with 200 $\mu\text{m} \times 5 \mu\text{m}$ channel area measured at $V_{ds} = 5 \text{ V}$.

To study the effect of light to the transistors, I_{ds} - V_{gs} characteristics were compared with injecting the light and without the light, which is shown in Fig. 28. When the curve measured without the light, the I_{ds} level was decreased, and V_{th} shifted to the positive direction about 0.06 V. This result implies that the light created some photocurrent in the transistors and it affected the device performance.

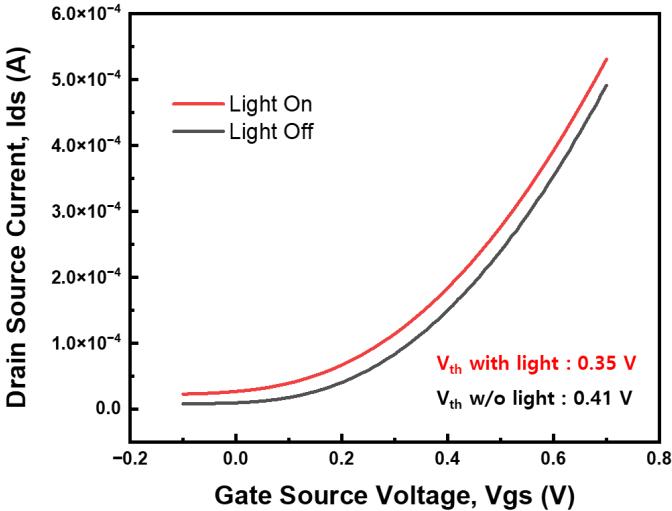


Fig. 28: I_{ds} - V_{gs} curve for MOSFET of $200 \mu\text{m} \times 20 \mu\text{m}$ channel area with light on and off, $V_{ds} = 0.7 \text{ V}$.

Breakdown of Transistors

The breakdown voltage of the MOSFET was measured both qualitatively and quantitatively. Quantitatively, we were able to use the power limited power supply in the clean room to drive one of the internal diodes to 42 V in reverse bias mode. This did not sufficiently heat the material adequately to cause diffusion of the dopants and a breakage of the internal electric field at the PN junction.

We were able to induce sufficient heat with the following method: we held the reverse bias mode of the internal diode at 10V for 5 minutes. This allowed for a sufficient amount of dopant ions to migrate and weakened the internal electric field. After doing this process, we were able to measure breakdown voltage effects as low as in 3 volts. However, this weakened the field effect which is responsible for their operation, and eventually caused our MOSFETs to catastrophically fail.

CV Analysis MOSCAP

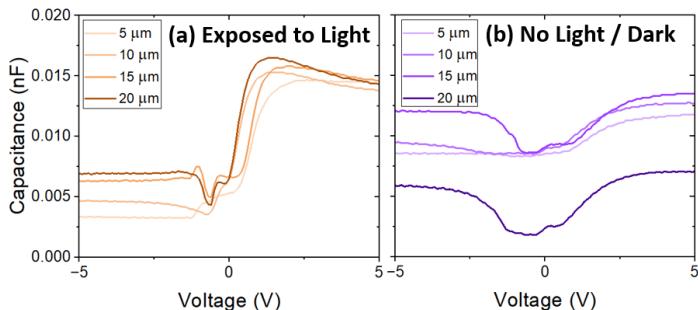


Fig. 29: CV For $400\mu\text{m} \times 5, 10, 15, 20\mu\text{m}$ Gate Body when (a) exposed to room light and (b) with no light / in the dark.

Table IV: Flat band voltages under different optical conditions (rows) and gate lengths (columns).

L_{Gate}	$5 \mu\text{m}$	$10 \mu\text{m}$	$15 \mu\text{m}$	$20 \mu\text{m}$
Light	-1.3 V	-0.8 V	-1.4V	-1.1V
Dark	-1.7V	-2.3 V	-1.7V	-2.5V

In a C-V curve, the flat-band voltage is typically indicated by a transition from the accumulation region, which is the flat part of our CV curve at the negative voltages, to the depletion region (where the curve begins to bend upwards in our CV diagram). From our data of Fig. 29 we can see that we transition into the flat band voltage around -1V on average, while the transition into the flat band voltage for the dark data is around -2V. This has to do with the fact that, in the dark, the transistors are not being exposed to as many photons which would affect the charge carrier generation within the semiconductor. Photons, when absorbed by the semiconductor material, can generate electron-hole pairs. Hence, we expect the charge carrier density to be higher in the light data than in the dark data.

The dark data additionally has a larger depletion region. This is due to the semiconductor surface depleting the majority carriers and hence we expect the capacitance to decrease. Interestingly, in our $20\mu\text{m}$ gate length dark data, the impact of this effect is maximized, as the intensity of light is inversely proportional to the area.

The inversion that occurs with our dark data has a similar voltage to the voltage at the accumulation region. Meanwhile, our MOSCAPs in regular light operation exhibit a difference of roughly 0.010nF between the inversion and accumulation regions. This is due to the interaction of light with the semiconductor material, surface states, and oxide layer, affecting the carrier dynamics and the dielectric properties.

4. CONCLUSION

This work describes the fabrication, characterization, and performance of n-channel MOSFETs, pn diodes, and capacitors at varying device geometries. Transconductance of our NMOS devices was found to increase with increased applied gate voltage, indicating successful transistor function. We also verified the effects of changing gate length, width and application of light to transistor function.

We will work to further control experimental conditions, particularly those related to diffusion and etching, as well as place greater emphasis on measuring factors such as average power dissipation, heat dissipation, frequency response, and other figures of merit which were not discussed currently. In the future, additional testing stages and more

knowledge of device physics will improve the ease of characterization.

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