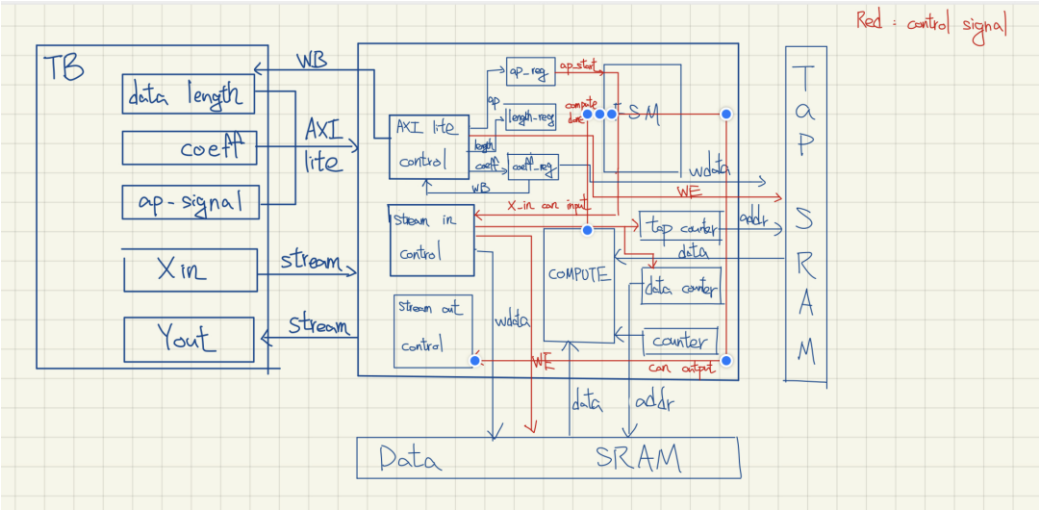
SoC Lab3 report 312510154 符顥瀚

Block Diagram - dataflow & Control signals



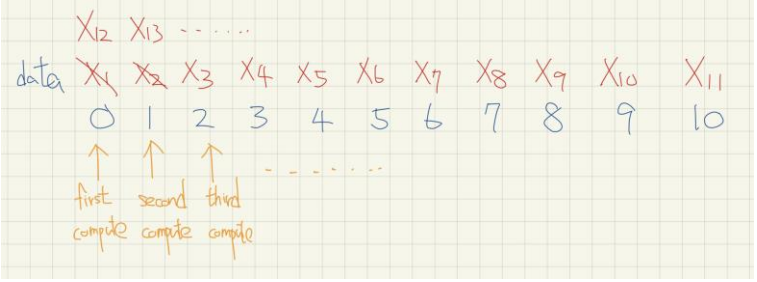
Describe operation

How to receive data-in and tap parameters and place into SRAM

當在 IDLE 時，且 wvalid 有拉起來時，我就讓 wready pull-up 一個 cycle，這時就有 waddr 與 wdata 傳進來，我會先將兩個都存在 reg 裡，再根據 waddr 決定要存到 ap、length 還是 coefficient 的 reg，且我會將 coefficient 的 reg 直接連接到 tap_Di，這樣我只要控制好 WE，WE==1 時就會 WRITE 進 TAP SRAM，而控制 WE 的方法則是當 wvalid 跟 awvalid 都有拉起來過且 waddr!=’h00 和’h10 時(not ap nor length)就可以 pull-up WE。

How to access shiftram and tapRAM to do computation

Tap 的部分比較簡單，我就照順序當做第一個 mult 時候 access tap[0]的 data，第二個 mult 時候 access tap[1]的 data，等到做完所有的 mult，再把 counter 歸零等下一次的 COMPUTE。而 shiftram 我是用像一個循環指標的概念，如下圖我會把 stream-in 的 data 照順序丟到 dataram，當 counter 循環回來第一個的時候就會覆蓋掉原本第一個的 data，然後在 compute 的時候我只要每次都把 counter 往後推一個並且往回數就能做到 fir 的效果。



How ap_done is generated.

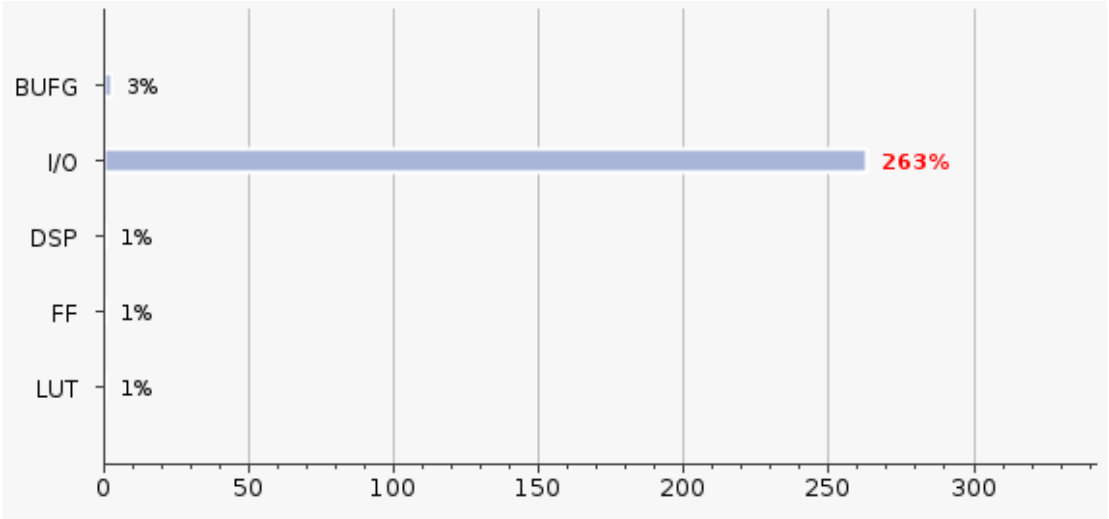
ap_done 只要當 sm_tlast 與 smtvalid、smtready 一起拉起來時就會被我 pull-up，當他被讀到時就會被我變成 0 如下圖

```
else if(ap_signal[1]==1 &&rready&&rvalid&&read_ap) ap_signal <= 32'h0000_0004;
else if(wvalid_HIGH && write_addr == 12'h00 && ap_can_write) ap_signal <= write_data;
else if(sm_tready && sm_tvalid && sm_tlast) ap_signal <= 32'h0000_0006;
else if(curr_state==COMPUTE) ap_signal <= 'h0;
```

FSM

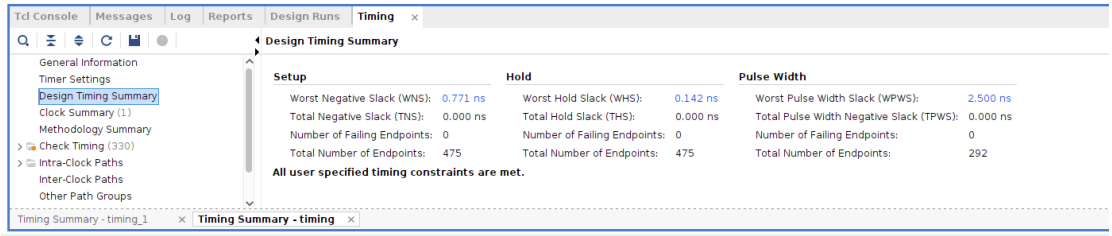
我的 FSM 分得比較簡單，就是 IDLE、INPUT、跟 COMPUTE，IDLE 的時候就是做完 FIR 準備接下一個 data length、coeff 等等，INPUT 的話是調整我的 COUNTER 現在應該要讀 SRAM 的哪個位置，COMPUTE 就開始計算直到 sm_tlast 拉起才回到 IDLE。

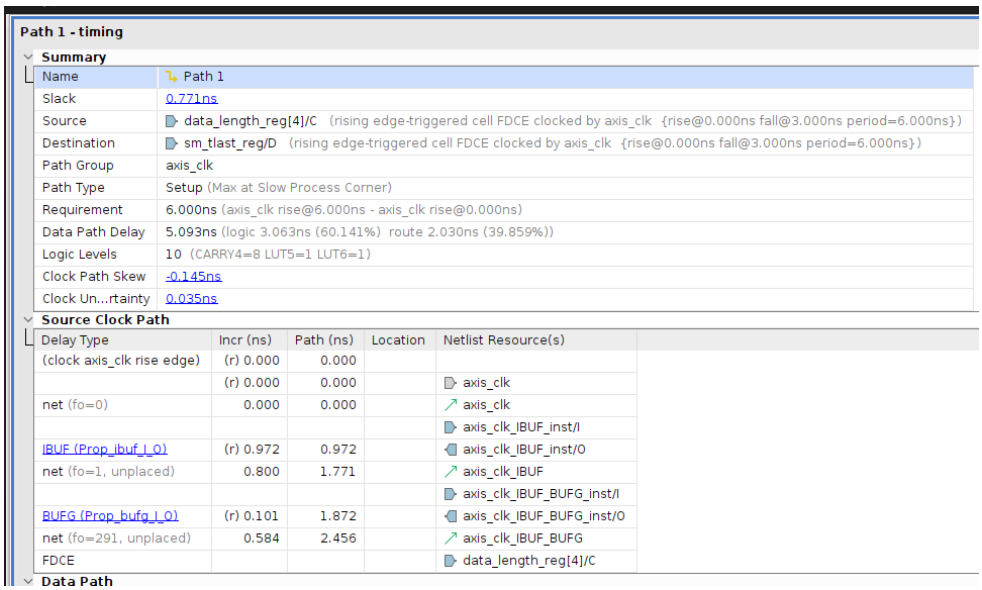
Resource usage: including FF, LUT, BRAM



Timing Report

Name	Waveform	Period (ns)	Frequency (MHz)
axis_clk	{0.000 3.000}	6.000	166.667





Path 1 - timing

Summary

Name	Path 1
Slack	0.771ns
Source	data_length_reg[4]/C (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@3.000ns period=6.000ns})
Destination	sm_tlast_reg/D (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@3.000ns period=6.000ns})
Path Group	axis_clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	6.000ns (axis_clk rise@6.000ns - axis_clk rise@0.000ns)
Data Path Delay	5.093ns (logic 3.063ns (60.141%) route 2.030ns (39.859%))
Logic Levels	10 (CARRY4=8 LUT5=1 LUT6=1)
Clock Path Skew	-0.145ns
Clock Un...rtainty	0.035ns

Source Clock Path

Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
(clock axis_clk rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000		axis_clk
net (fo=0)	0.000	0.000		axis_clk
				axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.972	0.972		axis_clk_IBUF_inst/O
net (fo=1, unplaced)	0.800	1.771		axis_clk_IBUF
				axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	1.872		axis_clk_IBUF_BUFG_inst/O
net (fo=291, unplaced)	0.584	2.456		axis_clk_IBUF_BUFG
FDCE				data_length_reg[4]/C

Data Path

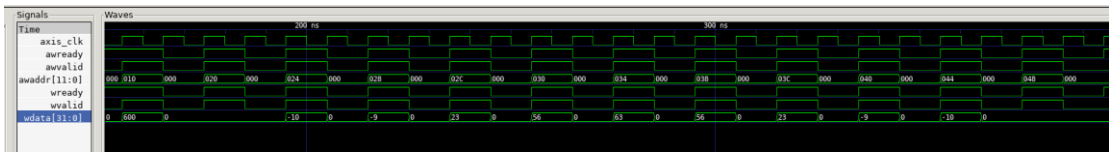
Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)
FDCE (Prop_fdce_C_Q)	(r) 0.478	2.934		data_length_reg[4]/Q
net (fo=3, unplaced)	0.664	3.598		data_length[4]
				sm_tlast_reg_i_34/DI[3]
CARRY4 (Prop_c...4_DI[3]_CO[3])	(r) 0.567	4.165		sm_tlast_reg_i_34/CO[3]
net (fo=1, unplaced)	0.009	4.174		sm_tlast_reg_i_34_n_0
				sm_tlast_reg_i_33/CI
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.117	4.291		sm_tlast_reg_i_33/CO[3]
net (fo=1, unplaced)	0.000	4.291		sm_tlast_reg_i_33_n_0
				sm_tlast_reg_i_21/CI
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.117	4.408		sm_tlast_reg_i_21/CO[3]
net (fo=1, unplaced)	0.000	4.408		sm_tlast_reg_i_21_n_0
				sm_tlast_reg_i_20/CI
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.117	4.525		sm_tlast_reg_i_20/CO[3]
net (fo=1, unplaced)	0.000	4.525		sm_tlast_reg_i_20_n_0
				sm_tlast_reg_i_19/CI
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.117	4.642		sm_tlast_reg_i_19/CO[3]
net (fo=1, unplaced)	0.000	4.642		sm_tlast_reg_i_19_n_0
				sm_tlast_reg_i_14/CI
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.117	4.759		sm_tlast_reg_i_14/CO[3]
net (fo=1, unplaced)	0.000	4.759		sm_tlast_reg_i_14_n_0
				sm_tlast_reg_i_13/CI
CARRY4 (Prop_carry4_CI_O[2])	(r) 0.256	5.015		sm_tlast_reg_i_13/O[2]
net (fo=1, unplaced)	0.905	5.920		sm_tlast1[27]
				sm_tlast_i_5/I1
LUT6 (Prop_lut6_I1_O)	(r) 0.301	6.221		sm_tlast_i_5/O
net (fo=1, unplaced)	0.000	6.221		sm_tlast_i_5_n_0
				sm_tlast_reg_i_2/S[1]
CARRY4 (Prop_c...4_S[1]_CO[2])	(r) 0.574	6.795		sm_tlast_reg_i_2/CO[2]
net (fo=1, unplaced)	0.452	7.247		sm_tlast0
				sm_tlast_i_1/I0
LUT5 (Prop_lut5_I0_O)	(r) 0.302	7.549		sm_tlast_i_1/O
net (fo=1, unplaced)	0.000	7.549		sm_tlast_i_1_n_0
FDCE				sm_tlast_reg/D
Arrival Time		7.549		

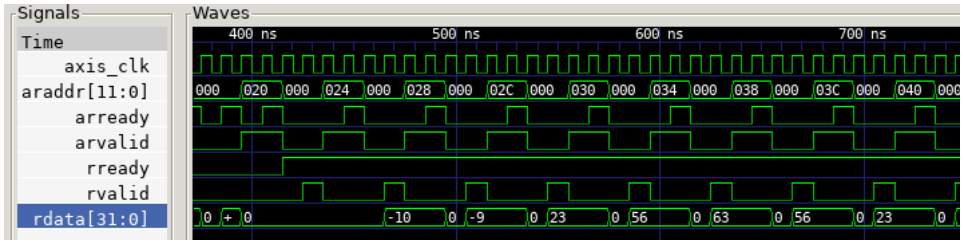
Destination Clock Path

Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)
(clock axis_clk rise edge)	(r) 6.000	6.000		
	(r) 0.000	6.000		axis_clk

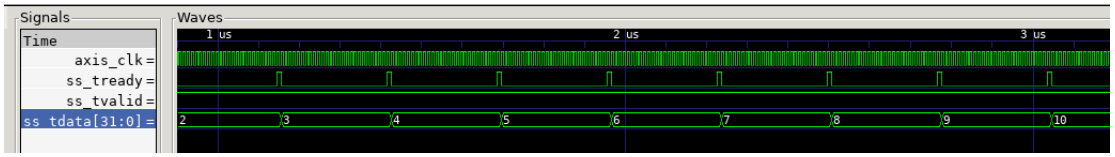
Simulation Waveform

- **Coefficient program, and read back**

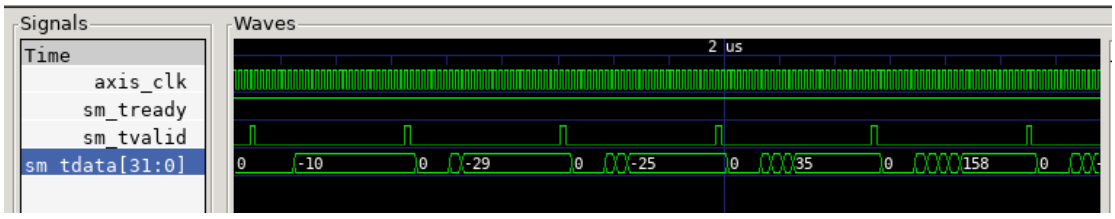




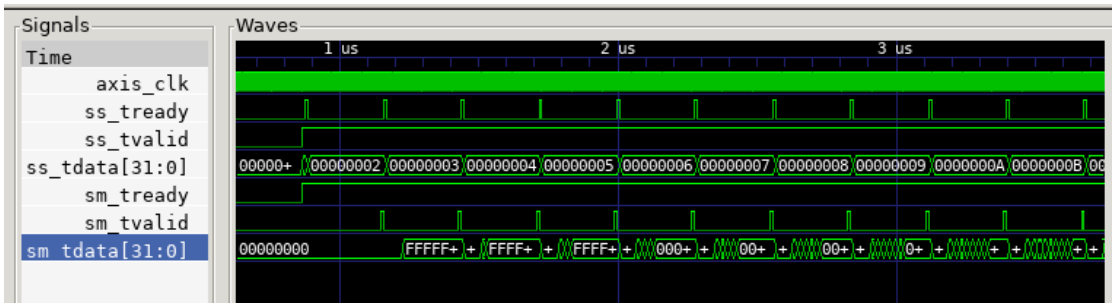
- **Data-in stream-in**



- **Data-out stream-out**

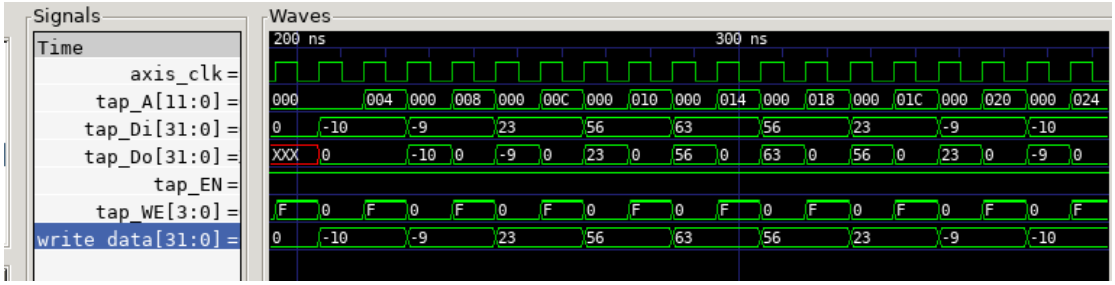


- **stream-in stream-out**

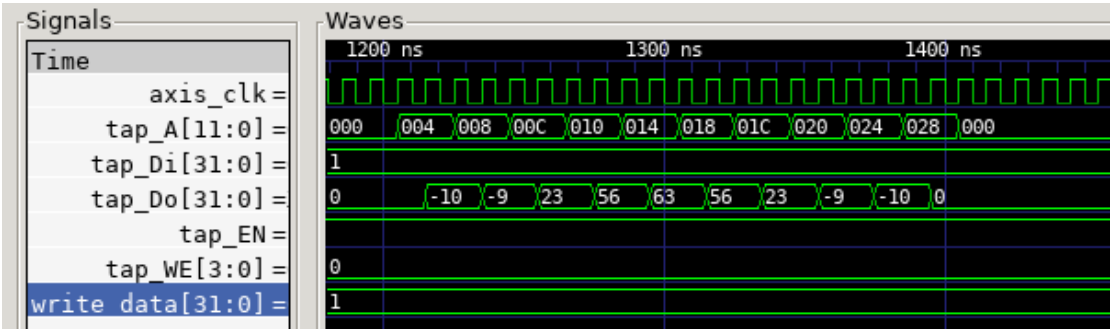


- **RAM access control**

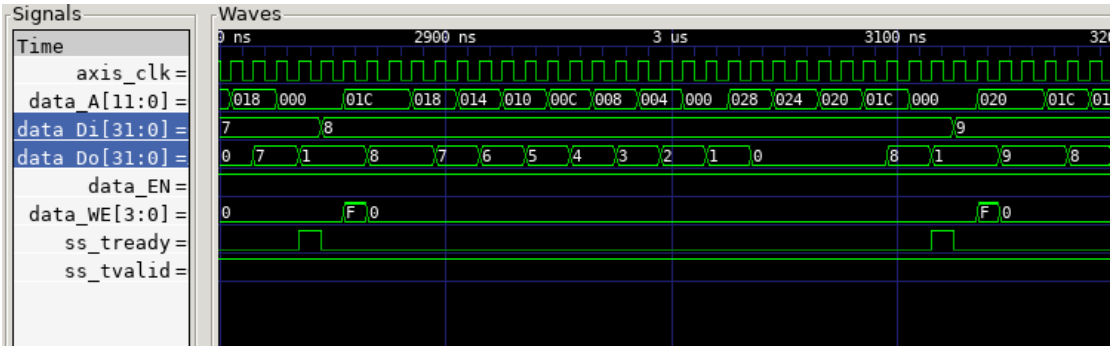
Tap SRAM write



Tap SRAM read

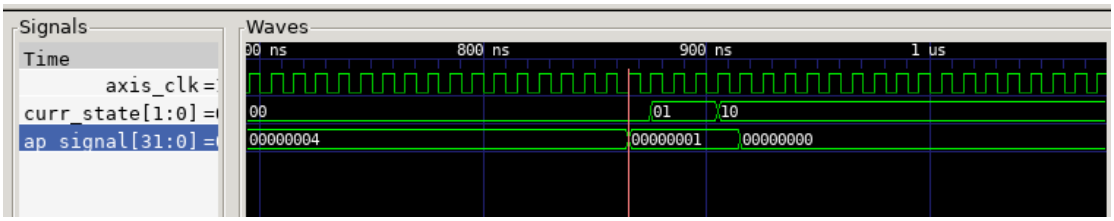


Data SRAM write&read



- **FSM**

When ap->start stream-in



When stream-in complete -> compute