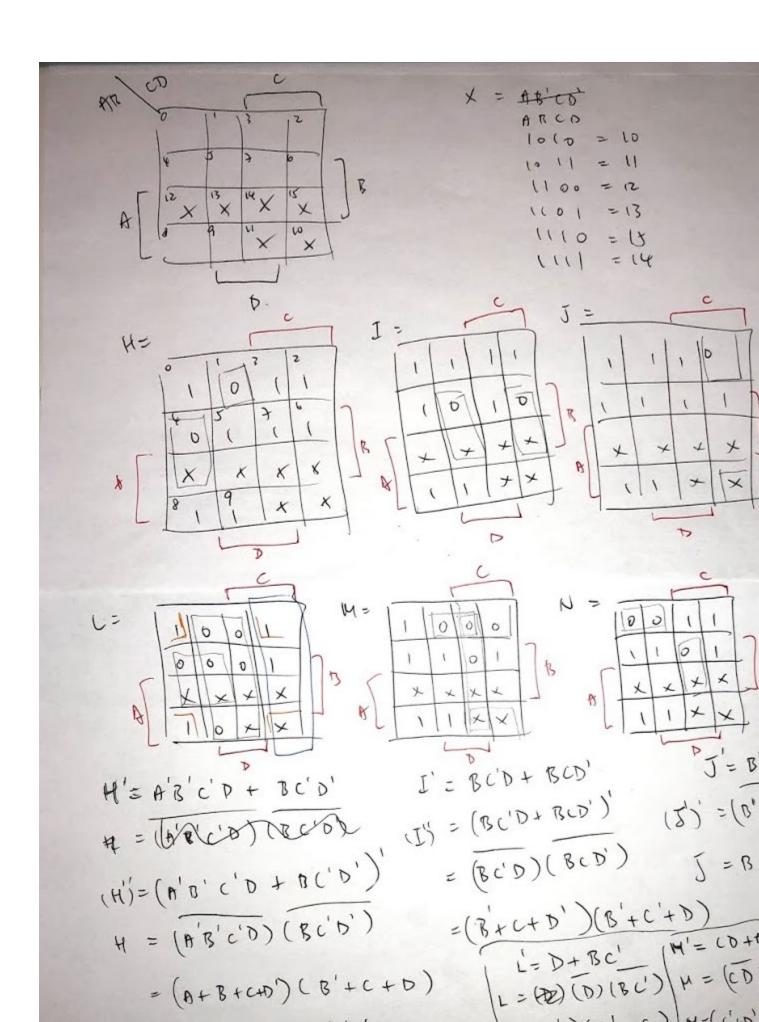
## Andy Lee – 500163559 Lab 4

## Part A

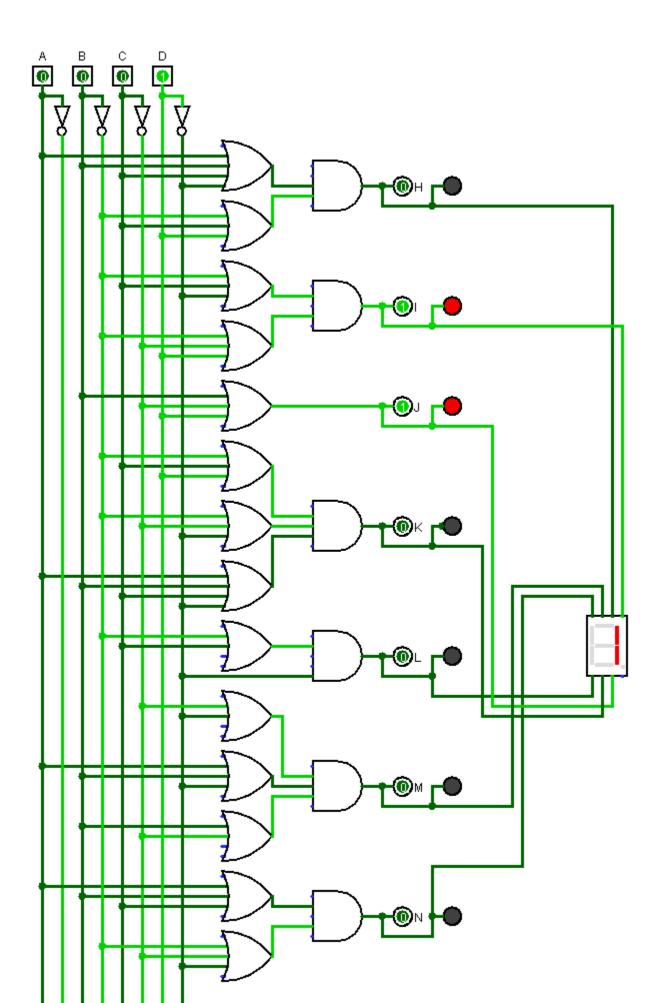
	BCD(8421)	OUTPUTS						
Dec.	ABCD	Н	I	J	K	L	М	N
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
4	0100	0	1	1	0	0	1	1
5	0101	1	0	1	1	0	1	1
6	0110	1	0	1	1	1	1	1
7	0111	1	1	1	0	0	0	0
8	1000	1	1	1	1	1	1	1
9	1001	1	1	1	1	0	1	1
10	1010	Х	Х	Х	Х	Х	Х	Х
11	1011	Х	Х	Х	Х	Х	Х	Х
12	1100	Х	Х	Х	Х	Х	Х	Х
13	1101	Х	Х	Х	Х	Х	Х	Х
14	1110	Х	Х	Х	Х	Х	х	Х
15	1111	Х	Х	Х	Х	Х	Х	Х

```
\begin{split} H &= A'B'C'D' + A'B'CD' + A'B'CD + A'BC'D + A'BCD' + A'BCD + AB'C'D' + AB'C'D \\ I &= A'B'C'D' + A'B'C'D + A'B'CD' + A'B'CD + A'BC'D' + A'BCD + AB'C'D' + AB'C'D \\ J &= A'B'C'D' + A'B'C'D + A'B'CD + A'BC'D' + A'BCD' + A'BCD' + A'BCD + AB'C'D' + AB'C'D \\ K &= A'B'C'D' + A'B'CD' + A'B'CD + A'BC'D + A'BCD' + AB'C'D' + AB'C'D \\ L &= A'B'C'D' + A'B'CD' + A'BCD' + A'BCD' + AB'C'D' \\ M &= A'B'C'D' + A'BC'D' + A'BC'D + A'BCD' + AB'C'D' + AB'C'D \\ N &= A'B'CD' + A'B'CD + A'BC'D' + A'BCD' + AB'C'D' + AB'C'D \\ \end{split}
```



```
H = (A + B + C + D')(B' + C + D)
I = (B' + C + D')(B' + C' + D)
J = (B + C' + D)
K = (B' + C + D)(B' + C' + D')(A + B + C + D')
L = (D')(B' + C)
M = (C' + D')(A + B + D')(B + C')
N = (A + B + C)(B' + C' + D')
```

Using the above we've built BCD decoder and turn it into a component



Part B solution in Logism file.

Utilizing components *full adder* from lab 3, *BCD-decoder* from this lab Part A, *4bit-to-BCD converter*, the final circuit named *Part2-final*.

