

A

Sub Circuits

adc

blame: saleh sabti

File: adc.kicad_sch

lora_module

blame: daniel monahan

File: lora_module.kicad_sch

power_management

blame: manaf alali

File: power_management.kicad_sch

B

B

C

C

D

D

Sheet: /
File: lora_daq_module.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. 9.0.6

Rev:
Id: 1/4

A

A

B

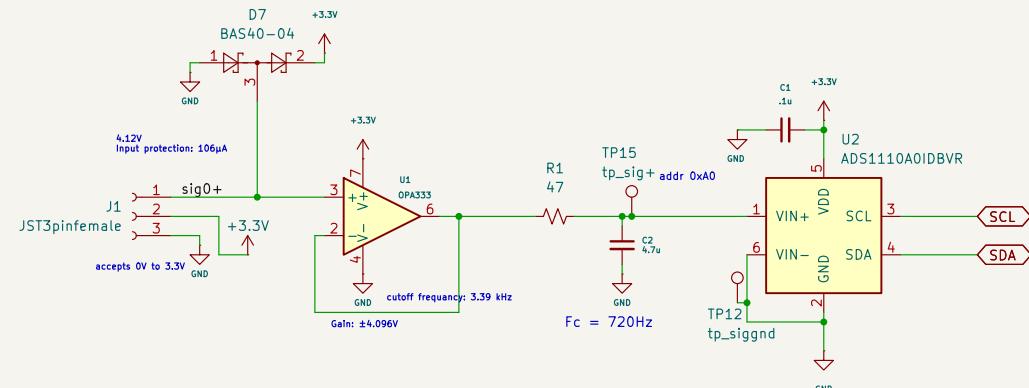
B

C

C

D

D

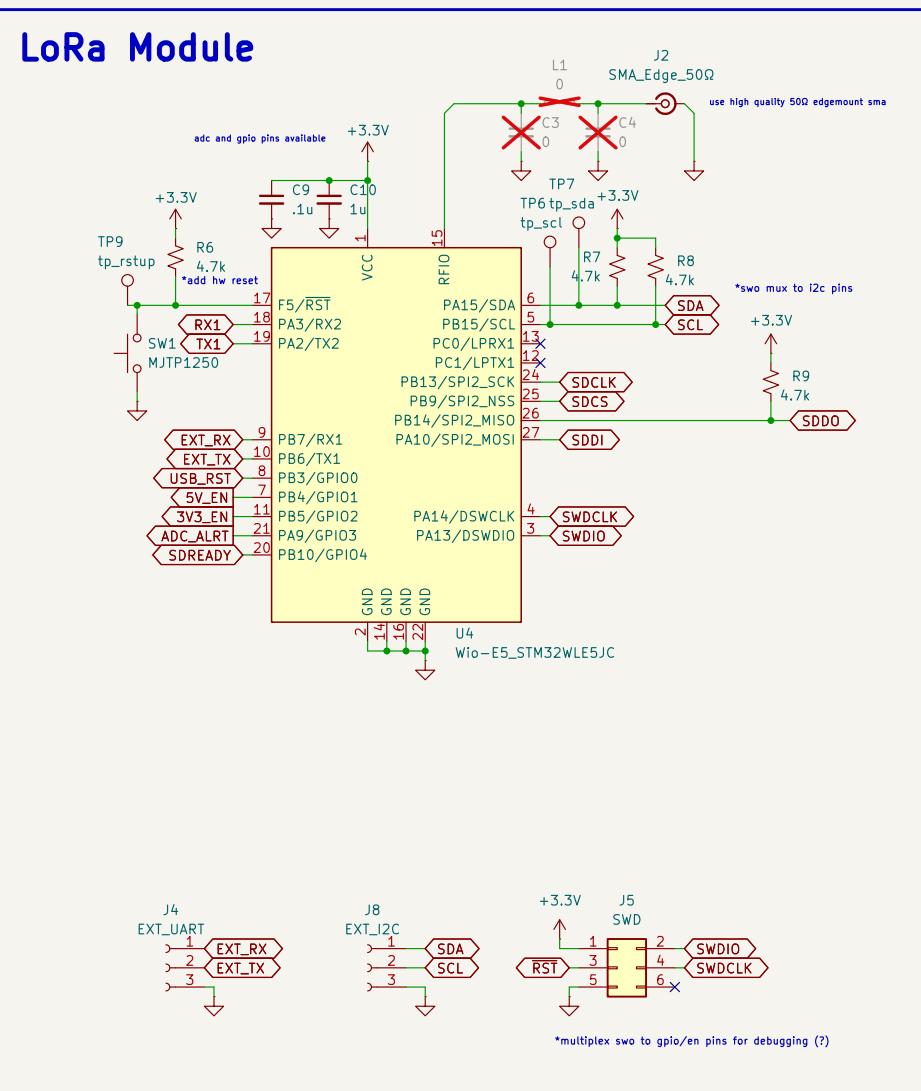
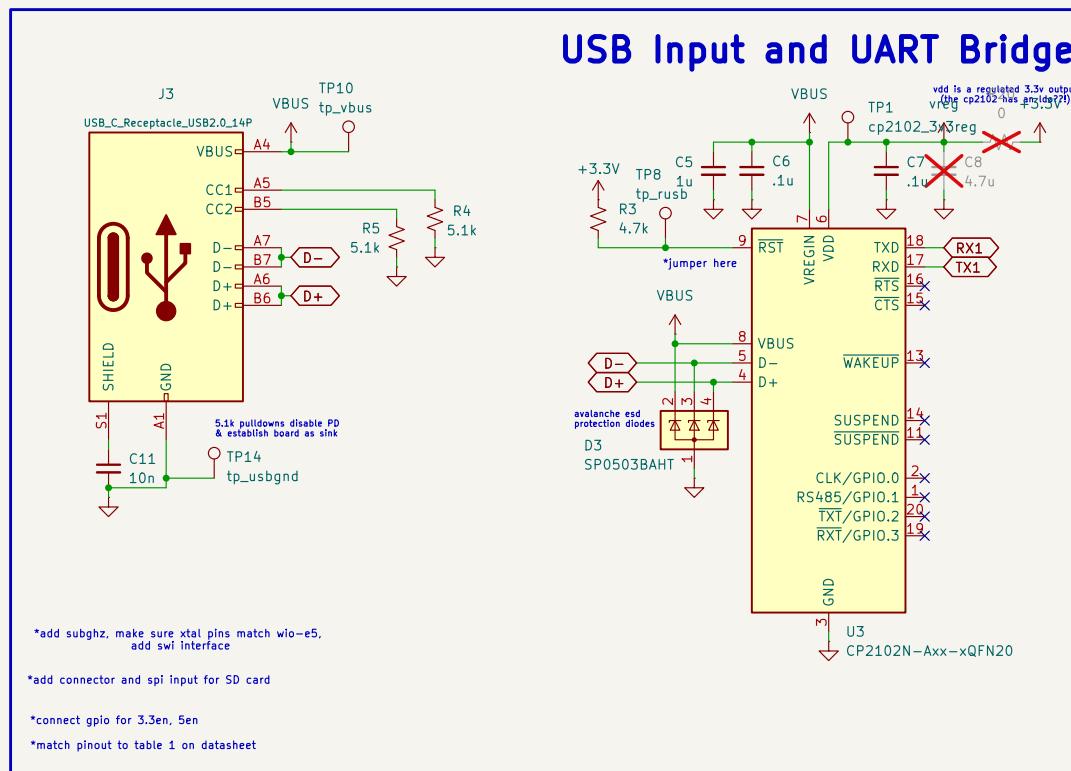


Sheet: /adc/
File: adc.kicad_sch

Title:

Size: A4 | Date:
KiCad E.D.A. 9.0.6

Rev:
Id: 2/4



drawn by daniel monahan
ECE Capstone Team 14 at Portland State University

Sheet: /lora_module/
File: lora_module.kicad_sch

Title: lora module subcircuit

Size: A4 Date: 2025-11-11
KiCad E.D.A. 9.0.6

Rev: rev0
Id: 3/4

