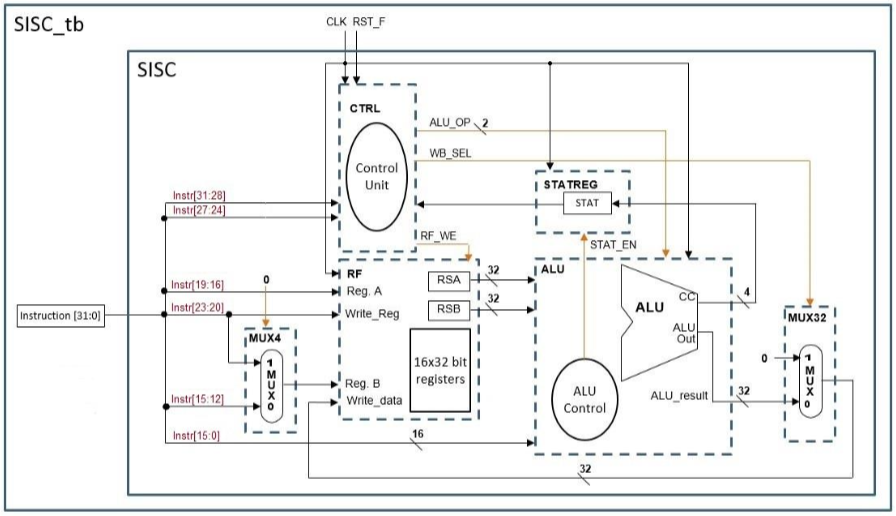
Project Part 1 Description

Team members: Ted Paulsen, Josh Wootonn, Daniel Machlab

**SISC.v**

In SISC.v, we declared all the modules and their connections shown above.

**CTRL.v**

In CTRL.v we created sequential and combinational procedures to determine the next state for the finite state machine. We generated control signals for execute, mem and writeback.