



INSTITUT
POLYTECHNIQUE
DE PARIS



Institute Polytechnique de Paris
École Polytechnique

On the relationship between density of carbon nanotube and the monolayer thickness used for their growth.

Research Project

Daniel Elmaleh
BSc Sebastián Ruiz Gonzalez
Hélène Stefanelli

10/12/2022

1 Abstract

CNTs have been a matter of great interest in the last few years for their versatility. Following a study by the university of Illinois in 2008, a race started to create transistors based on CNTs with the best reproducibility and smaller size. In order to grow SWCNTs one needs to deposit a layer of Al_2O_3 and a catalyst layer of iron Fe before performing a chemical vapor deposition (CVD). In this paper, the effect of varying said iron layer's thickness has been studied. The goal of the experiments thus carried out is to study the effect of this iron layer on the growth of the SWCNT, in particular on their density. The thinner this layer is, a lower density of the SWCNTs on the silicon wafer is expected. This factor is particularly important for the construction of transistors. Indeed, if there is a high SWCNTs density, there is a risk the CNTs will overlap, which will impact the characteristics of the transistors.

2 Introduction

The first transistor was created in the 1940s, and it was about the size of a hand with a depth of about two matchboxes stacked together. It wasn't until the 1950s that the first commercial devices with transistors were released to the market. After this, the transistor has been at the center of technological development, being one of the most important electronic components of all time. In 1965, Gordon Moore stated what came to be known as Moore's law, which states that the number of transistors on a chip would double each year. Since then, this law has held true. However, as we have achieved smaller and smaller transistors, there is an undeniable physical limitation to how small a transistor can get. It was until 2001 that the first nanotransistor was created, and until 2008 that a nanotransistor was created using carbon nanotubes (CNTs).

Since their discovery, CNTs have been regarded as a miracle nanomaterial for their versatility and amazing properties. However, their creation is not a trivial process, and the fact that you need state-of-the-art scientific equipment just to see them makes their creation and characterization much more harder. For more than a decade, there has been a race to try to create a nanotransistor based in CNTs, with a method with high reproducibility and that can be scaled for commercial purposes. That is what has motivated this study.

The growth of CNTs, normally done on a silicon oxide wafer under very specific conditions, is a very delicate and demanding process. Normally, the process requires the deposit of a nanolayer of aluminum oxide, the deposit of a monoatomic catalyst layer, and the actual growth of the CNTs. The conditions by which these steps are conducted will define the density of the CNTs in the wafer, their type and their kind. This study intends to see if there is a direct relationship between the thickness of the catalyst layer (in this case an iron layer) has a direct relation with the density of the CNTs created. This is most important since for the creation of functional nanotransistors the CNTs must be not too dense to reduce the possibility of them getting tangled with each other, as well as semi-conducting and single-walled (SWCNTs).

3 Theoretical framework

3.1 Transistors

In today's electrical devices, the type of transistors used are Metal Oxyde and Silicon Field Effect Transistors (MOSFET). This kind of transistors are composed of two type of doped

silicium. In case of a p doped substrate two areas strongly n doped are created (see Fig.1) in between which a layer of oxyde is provided as insulation. On top of this layer the gate pin is plugged while the first n+ doped area is plugged to the source pin and the second n+ area is plugged to the drain pin. This architecture enables the control of the current between the source and the drain through the gate.

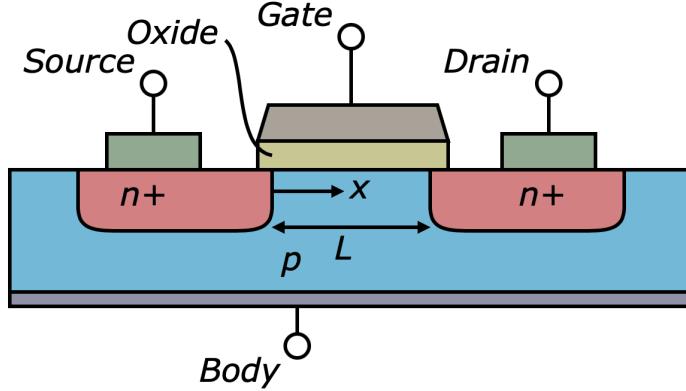


Figure 1: MOSFET transistor

However with the constant down-sizing of transistors the technology is facing strong challenges due to several factors:

- **Material challenges:** With continuous scaling dielectric materials are enable to provide sufficient insulation.
- **Physical challenges:** Due to the always smaller length of the channel between the two strongly doped areas we have now reached a point where quantum physics can apply. Quantum tunneling for instance enables electrons to jump the barrier even if no voltage is applied through the gate.
- **Power-thermal challenges:** The ever-increasing number of transistors integrated per unit-area demands larger power consumption and higher thermal dissipation.
- **Technological challenges:** Incompetency of lithography-based techniques to provide the resolution below the wavelength of the light to manufacture CMOS devices.
- **Economical challenges:** The rising cost of production will make the production of such transistors very expensive.

To tackle those challenges, a possible solution is to use SWCNTs based transistors. SWCNTs are a particularly interesting technology since 2/3 of SWCNTs behave as semiconductors while every MWCNTs are metallic therefore behaving as conductors. Moreover SWCNTs electric conductance is ballistic which means that all electrons that go into one end of the SWCNT come out of the other end almost without scattering.

To create a transistor based on SCNTs we need to connect each extremity to electrodes acting as "gate" and "source". The main requirement is for the CNTs to be single walled and have a diameter of maximum 2 nm, as the band-gap of the CNT is inversely proportionate to the diameter of the CNT. Indeed, if the diameter is too big the SWCNT will behave as a conductor.

3.2 Creation of CNT

3.2.1 Deposition

As it will be explained, the process of creation of CNTs is a long one. The first step consists in the deposition of Al_2O_3 . This layer is used to prevent the catalyst's particles to cluster during the growth of the CNTs by creating an electrical barrier with this layer.

The second step is the deposition of a catalyst layer. The role of this layer is to form clusters which would be used as anchoring points by the carbon atoms, on which they will assemble and begin the growth of the nanotubes (figure 2, (b)).

3.2.2 CVD : Chemical Vapor Deposition

The growth also consists of several steps:

Step 1:

The first step of the growth is, as mentioned above, to create electrical barriers on the wafer to prevent the gathering of the catalyst particles into one major cluster, which would lead the formation of either fewer SWNTs but with wider diameters or Multi-walled carbon nanotubes (MWCNTs). In order to do so, the substrate is heated and hydrogen H_2 is evaporated on the wafer. The increase of temperature activates the Al_2O_3 on the first layer, which leads to the loss of some oxygen atoms when they encounter hydrogen.

Step 2:

The second step of the growth is to continue evaporating H_2 on the wafer, while starting to evaporate methane CH_4 as well. Carbon atoms from the methane will then begin to fixate on the catalyst clusters previously formed and then the CNTs will begin to grow on them (see Fig.2 (b)).

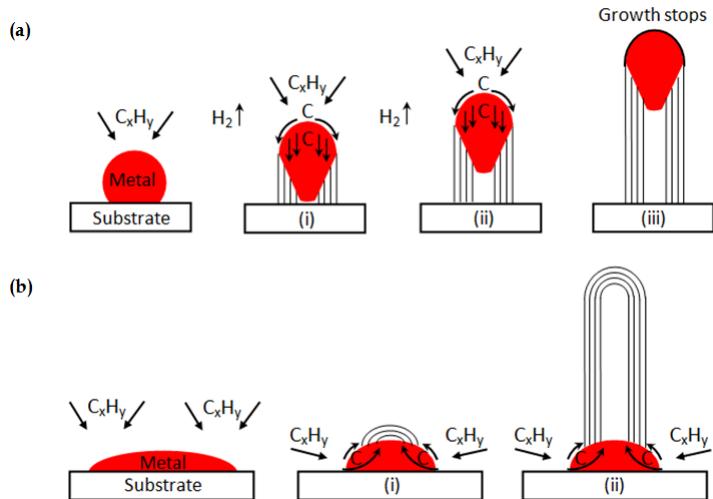


Figure 2: Growth of carbon nanotube (a)tip-growth (b)base-growth

3.3 Characterization Techniques

In order to analyze the results on the CNTs we built, several characterization techniques were used.

3.3.1 Raman Spectroscopy

The first technique used is called Raman Spectroscopy. This technique was used to obtain the characteristics of the nanotube that were created on the silicon wafers. For instance, with the spectrum obtained it is possible to calculate the diameter of the CNTs, if there are CNTs with different diameters and their respective densities, if the predominant species in the wafer are semi-conducting or metallic, and if the nanotube are single-walled or multi-walled. A more precise explanation of how this was calculated is in the section *Experimental results*.

This technique uses diffused light from a laser to identify chemical components by observing their modes of vibration and rotation once they are excited by this light. When one of the lasers used (red or green) encounters a molecule, its emission changes for a specific wavelength and these changes are what is measured by the detector.

3.3.2 Scanning electron microscopy

The other characterization technique used is scanning electron microscopy (SEM). This technique enabled us to have a topographical understanding of the sample while the Raman spectroscopy gave us an understanding of what type of nanotube we had.

This technique uses a beam of electrons that interact with the sample. Once the beam meets the atoms of the sample, they discharge secondary electrons which are then analyzed by the machine. The second electron detector of the machine converts the electron signal into a light signal, thus giving an idea of the topology of the sample.

3.4 Photolithography

Once the CNTs are created and we have made sure they comply with the specified characteristics by the characterization techniques, photolithography was performed in the sample in order to connect the SWCNTs and form functioning transistors.

The first step of photolithography is to treat the wafer with silicium dioxyde SiO_2 in order to remove any impurities. Then, a drop of polymer is placed on top of the wafer to cover it and the polymer is then covered with a photomask. The polymer layer, covered by the photomask, is then exposed to light, which weakens the exposed parts not covered by the photomask. The weakened regions are then washed away, which reveals the silicon wafer and the SWCNTs. Metal is then deposited on the wafer, covered still in some parts by the polymer layer. The final step is the removal of the rest of the polymer and metallic layers, leaving metal on the regions not covered by the photomask, which then form the electrodes of our transistors.

4 Experimental Results

4.1 Experiment description

In our experiment, we have decided to focus the attention on the effect of the Iron (Fe) deposition thickness on a variety of parameters, such as density of CNTs, size of the CNTs (length, diameter), the nature of the CNTs and their shape, and finally to try and utilize them as function transistors.

To do so we had a procedure that consists of 2 main steps for the making of the CNTs, without counting the lithography done to put electrodes over the wafer, and 4 main tools to

check and test our results. Once we could confirm that the potential of the right density, shape, and nature of CNTs were present on the wafer in question, we proceeded to the lithography part which was not done by us, but delegated to THALES laboratories, whom have the appropriate tools.

The first step consists of taking a virgin silicon wafer and depositing on it a layer of Al_2O_3 and a layer of Fe over it. To do so, we had to work under a vacuum of 10^{-9} [Pa], to respect the mean free path of the desired materials we want to deposit. The deposition was done by an evaporation technique, where a beam of electrons excites a crater containing the desired material, which in turn evaporates in the vacuum chamber and hits the wafer. This procedure is done once for the deposition of Al_2O_3 and once for the Fe , on the same wafer. The elements that vary in this first part are the time of exposure to the deposition of each material, the flux of the material going toward the wafer, and the distance from the wafer. We kept all those parameters constant but the time of evaporation of the Al_2O_3 as it affects the thickness of the Al_2O_3 deposited, which is our subject of experiment. Using this empiric formula - $time = (thickness)/(C_{Fe} * flux)$ we were able to calculate the thickness of the Al_2O_3 deposited as a function of time of exposure. The machine used for this part can be seen on Figure 3. Where the chamber on the far right is the final vacuum chamber for the evaporation process. while on the left a handle and a primary vacuum chamber are seen, used to access the sample and achieve a primary vacuum of 10^{-2} [Pa].



Figure 3: Vacuum chamber on the right, handle and primary vacuum chamber on the left

In the second step, we are growing the CNTs on our wafer. To do so we are again putting our wafer in a vacuum chamber, this time of 10^{-7} [Pa] to keep the purity of the gases used. Once in vacuum, we heat up our wafer to 800 degrees C and we start filling the chamber with hydrogen (H_2), which reacts with the surface's oxygen to make the imperfections needed to get the right size of Fe drops. Then we start filling the chamber with both H_2 and CH_4 with a proportion of 2:1 respectively. At this point the CH_4 reacts with the Fe and starts to grow the CNTs. The machine can be seen on Figure ??, where we seen the vacuum chamber, the gases entry and the current and voltage controllers used to control the temperature on the left.

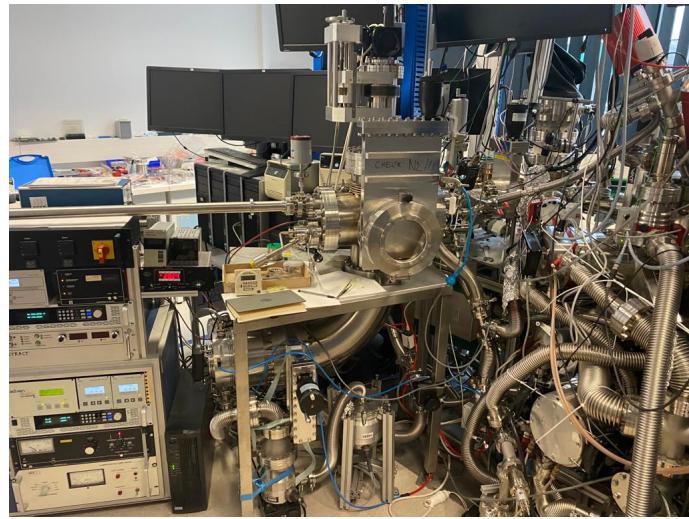


Figure 4: CVD machine with vacuum chamber in the middle, gases entry from above

The 4 different tools we had to check our results were: 1) scanning electron microscopy (SEM), 2) transmission electron microscopy (TEM), 3) Raman spectroscopy, 4) electronical testing for transistor behavior.

The SEM figure 6 was used mainly to see the presence of CNTs and get an idea of their size and density. To use this tool, we put the wafer in a sterile environment and by using gloves we mount the wafer to the SEM handle substrate.



Figure 5: SEM.



Figure 6: SEM sterile environment used to mount the sample to the SEM substrate.

The TEM was used to get more of a 3-D image of the CNTs and get a better understanding of their shape. This technique is used by scratching the wafer's surface in a sterile environment and putting it on a grid specific to the microscope, which lets the electrons pass through its gaps to get an image of the extracted batch of CNTs.

The Raman spectroscopy analysis helped us characterize the CNTs in a quantitative way, giving us information about their existence, the nature of the CNTs, , their size and so on.

For the electrical measurements we used needle connections to connect to the electrodes as drain and source connections (Figure 7), and to the silicon substrate as the gate, which was done by scratching the surface of the wafer to remove the oxidized layer above. The whole machine can be seen on Figure 8.



Figure 7: Needles connected to the wafer's electrodes and silicone itself



Figure 8: Machine used to make electrical measurements on the right, camera and monitor of the needle connections on the left

4.1.1 Electrical Measurements

In the electronics measurements part, we were trying to find functional SWCNTs by detecting a variable resistance behavior, as in a Cmos transistor. To do so, an iterative process of connecting the needles to electrodes on the wafer, plotting its Id-Vgs characteristic through a voltage swipe, proceeding to burn the metallic portion of the CNTs present with a current swipe, re-plotting the Id-Vgs characteristic and so on. After doing this process in different places on the wafer, and trying an alternative of high voltage - high frequency pulses over a few good potential electrodes in order to burn the metallic CNTs, we didn't succeed to find the transistor characteristic we were looking for. Reasons for that could be a too dense CNT population present on the wafer, to many metallic ones present, inter-crossing of the CNTs, or even a too big diameter of the SWCNTs which tend to behave like metallic CNTs due to an inversely proportionate band-gap to diameter relation.

4.2 Results and discussion

Three full silicon oxide wafers where used to try to grow SWCNTs. The parameters used are as follows:

4.2.1 Evaporation:

	1st wafer	2nd wafer	3rd wafer
Aluminum Width (nm)	5 ± 0.1	5 ± 0.1	5 ± 0.1
Closed Shutter flux (μA)	6.5	7.5	7.5
Open Shutter flux (μA)	2	1.8	2.35
Time (s)	153	200	150

	1st wafer	2nd wafer	3rd wafer
<i>Fe</i> Width (nm)	0.49 ± 0.01	0.47 ± 0.01	0.36 ± 0.01
Closed Shutter flux (μA)	500	3	3.12
Open Shutter flux (nA)	70	200	250
Time (s)	210	10 + 60	44

In the table above, for the second wafer, there is an addition. This is due to the fact that two separate evaporation were done, with the same parameters and an interval of 50s between each.

The first wafer was done as a collective effort by the whole class, the second wafer was the first attempt we conducted alone. Both of these wafers showed a very high density of CNTs, bigger than what we wanted, so for the last wafer the *Fe* layer thickness was decreased more dramatically to strive for a minor density. Which, as is stated later, was achieved successfully.

4.2.2 LCVD:

After the deposition process, the wafers were cut in half. After this, the samples were numbered according to the number of the wafer, and which half was used. Samples 1-6 were obtained, however, following the incident of sample number 2, sample number 3 was cut in half again. The numbering of the samples grew by one after this, thus obtaining samples 1-7. The parameters used for the growth of CNTs on each of those samples are as follows:

Sample 1:

- Substrat temperature: 700°C
- Pressure: 2mbar
- Time: 6 min of pure H_2 and 30 min of CH_4 at 10 sccm and H_2 at 20 sccm

Sample 2:

Initially the same parameters as for the 1st halve were used, however, a heater problem made the substrate temperature drop from 700°C to 336°C. As a consequence, the process was unsuccessful and no CNTs grew in this sample.

Rest of the samples:

The same parameters as for the 1st half of wafer 1 were used.

The decision was made to only continue with the analysis of samples 1, 5, and 7 since they were the ones with the most interesting and clear properties.

4.2.3 SEM:

With the use of the electronic microscope viewing the CNTs was possible, thus we were able to get rough estimates of the densities of CNTs in the wafers. The following images were obtained:

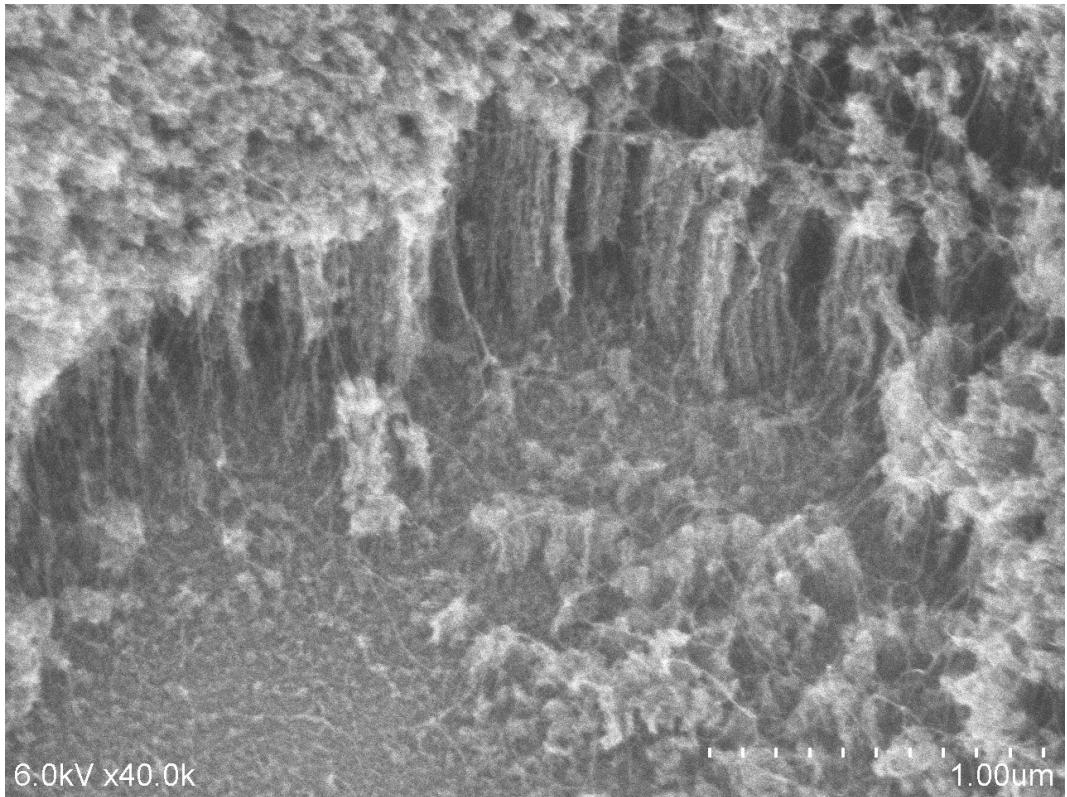


Figure 9: Forrest of carbon nanotubes in sample 1.

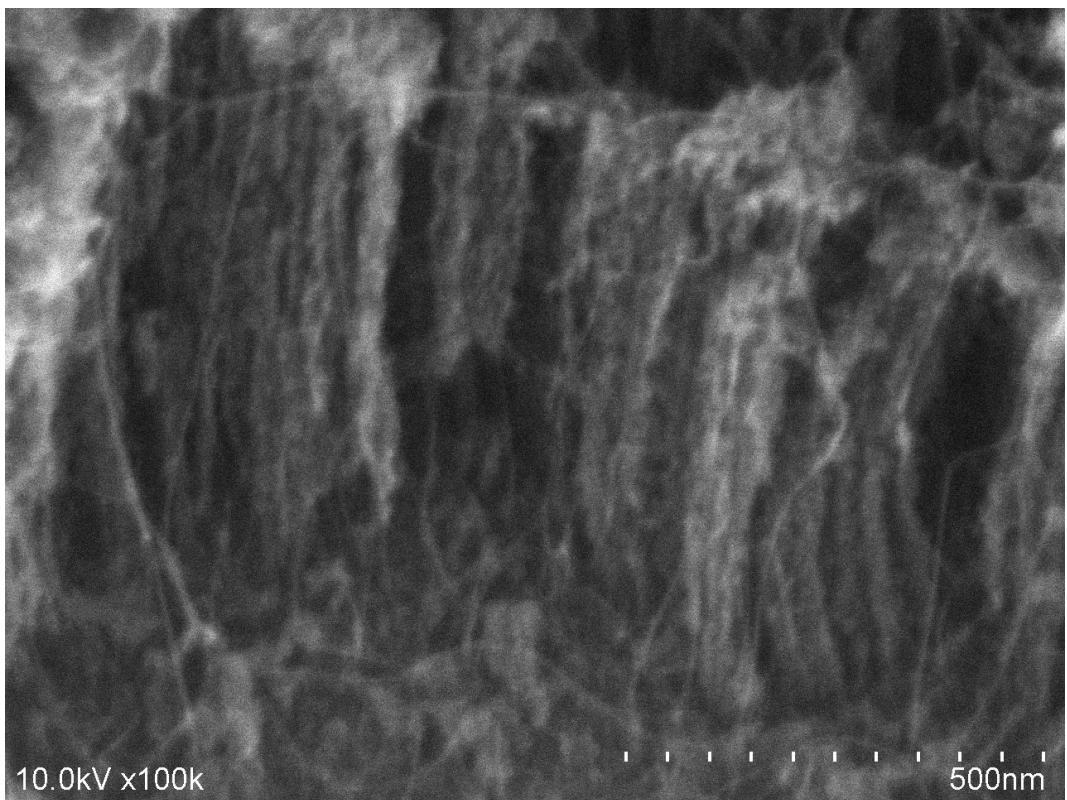


Figure 10: Forrest of carbon nanotubes in sample 1.

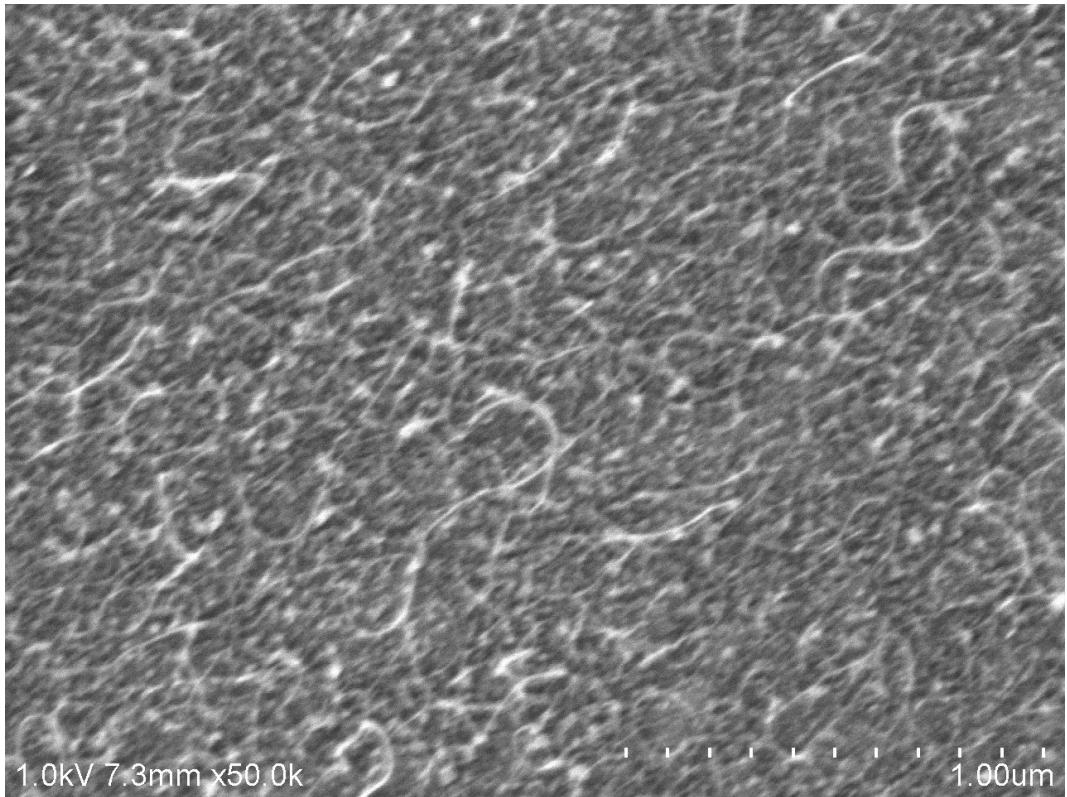


Figure 11: Carbon nanotubes in sample 5.

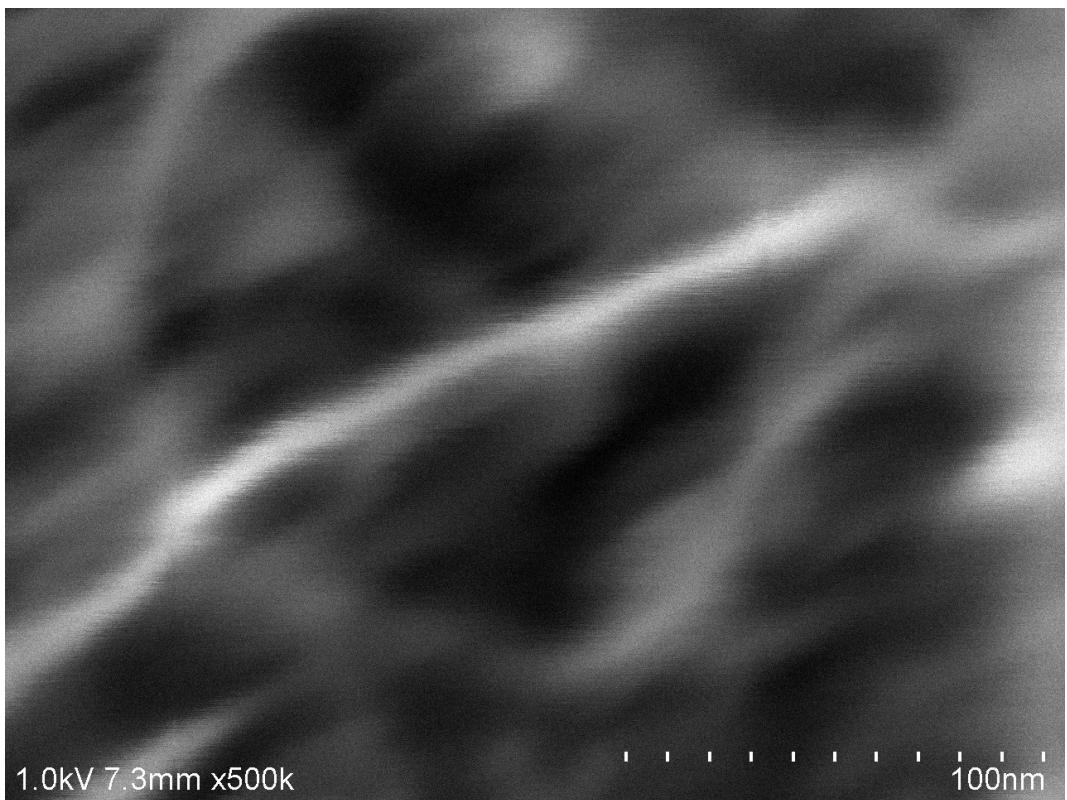


Figure 12: Single stretched carbon nanotube in sample 5.

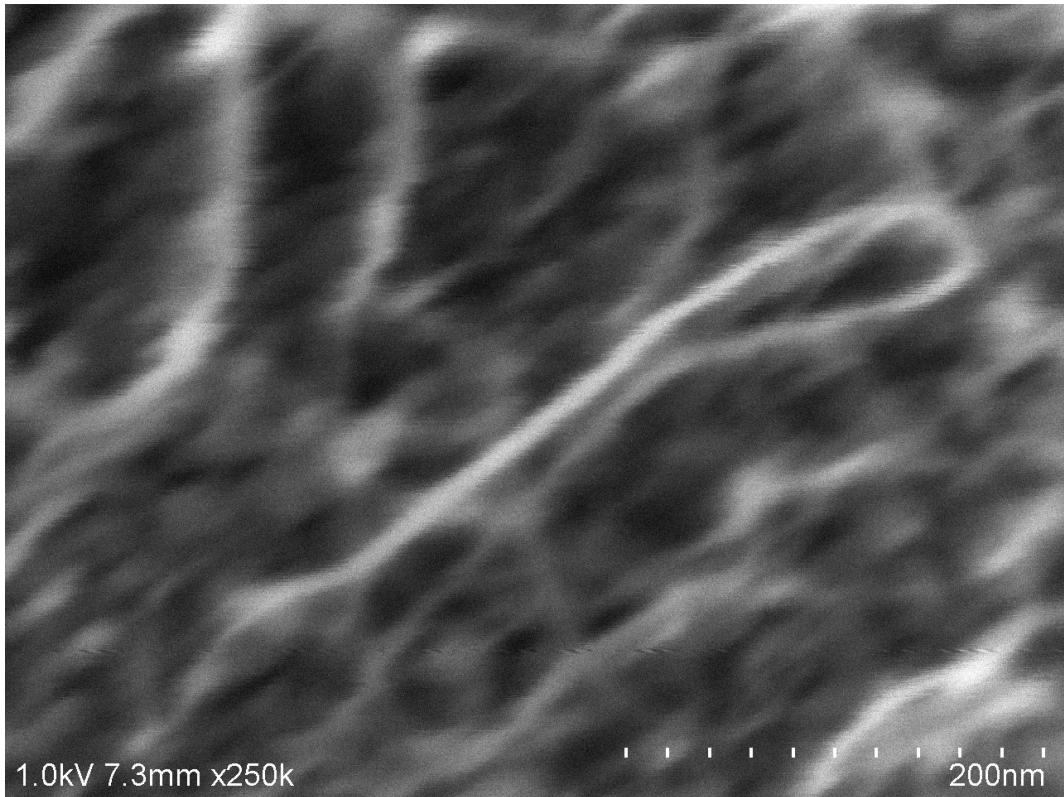


Figure 13: Single tangled carbon nanotube in sample 5.

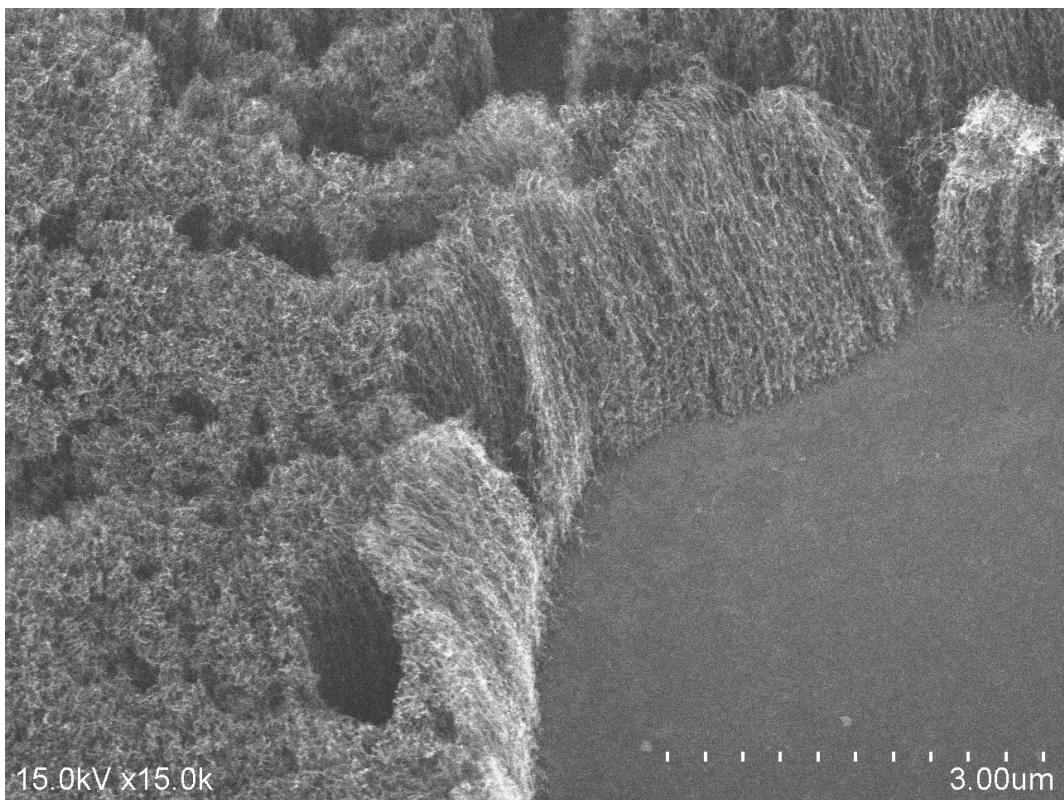


Figure 14: Forrest of carbon nanotubes in sample 7.

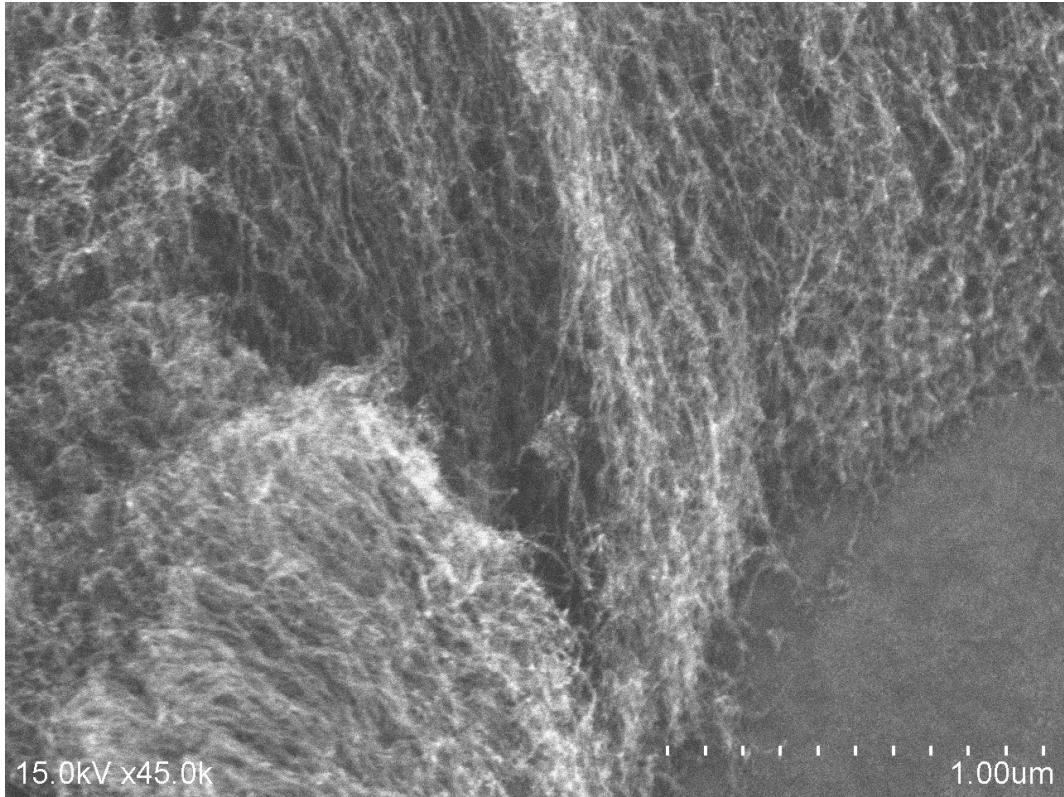


Figure 15: Forrest of carbon nanotubes in sample 7.

It is easy to see that samples 1 and 7 present a forest. While the properties of this forests can be very interesting, specially the one in sample 7, the objective is a lower density of CNTs to maximize the probability of having working transistors, as explained above.

However, sample 5 seems like the perfect candidate to continue the process, since the density seems to be just about right to have some working transistors after the lithography process.

4.2.4 Raman Spectroscopy

With the Raman Spectroscopy we can get a lot of valuable information from our samples, non the less, this study focuses around the radius of the CNTs, their type (conductor, semiconductor, etc.), and their kind (single-walled, double-walled, multi-walled).

The spectrometer has two lasers; green (532 nm) and red (633 nm). Comparing three positions on our wafers with each laser, to find the best densities, we get the following results:

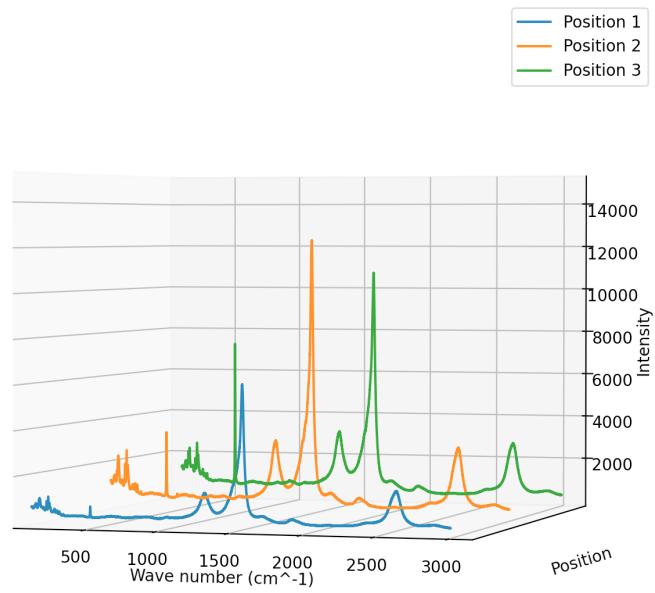


Figure 16: spectrum of 3 positions in sample 1, with the green laser.

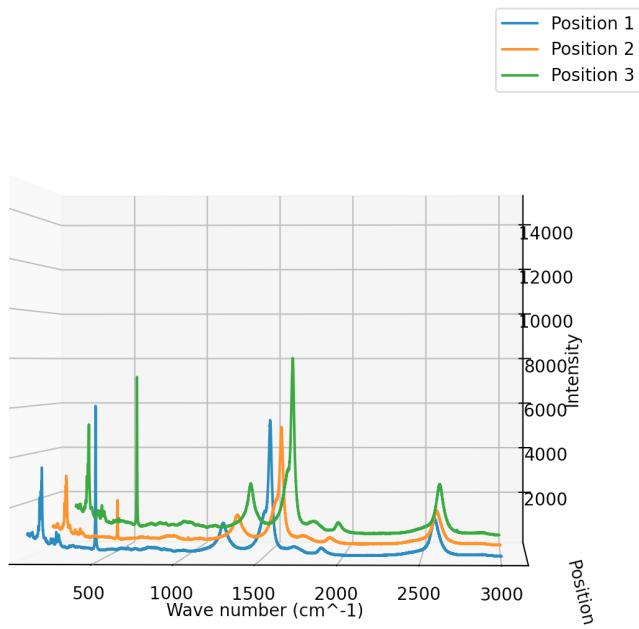


Figure 17: spectrum of 3 positions in sample 1, with the red laser.

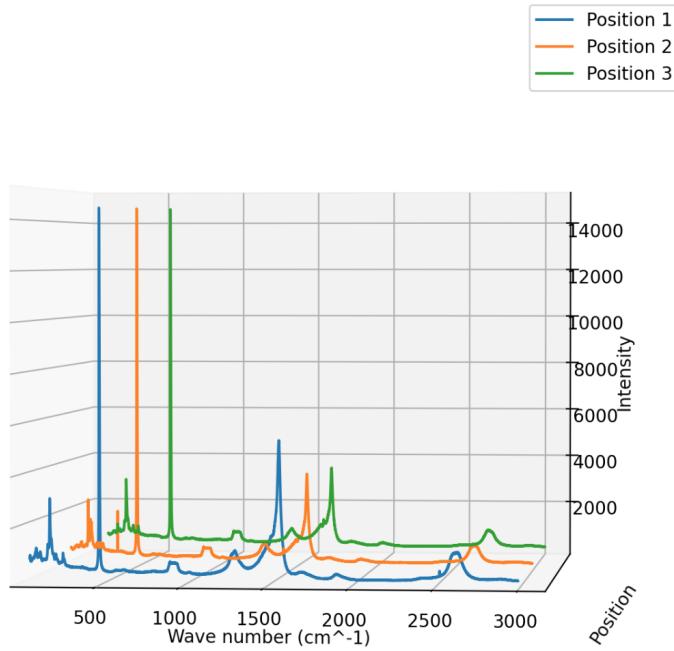


Figure 18: spectrum of 3 positions in sample 5, with the green laser.

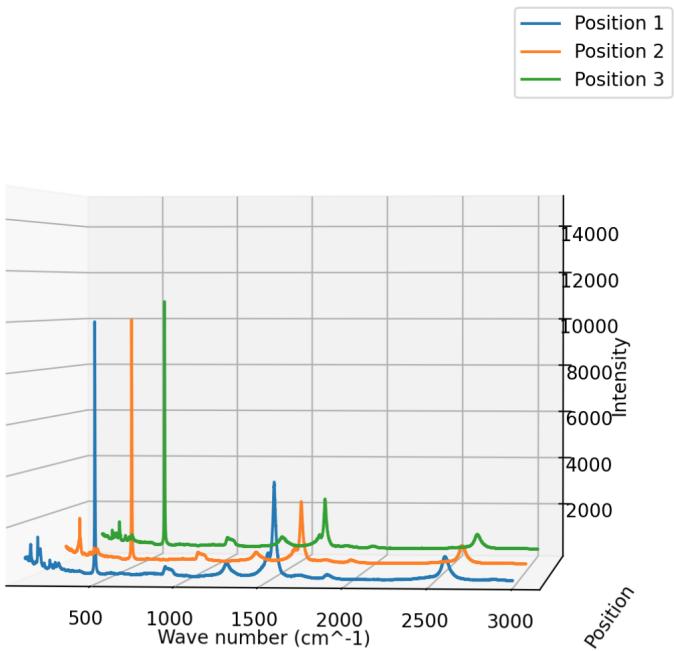


Figure 19: spectrum of 3 positions in sample 5, with the red laser.

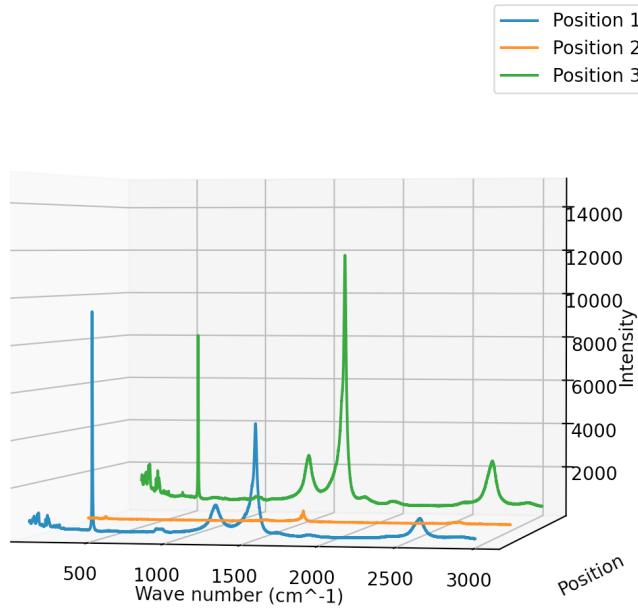


Figure 20: spectrum of 3 positions in sample 7, with the green laser.

Figure 21: spectrum of 3 positions in sample 7, with the red laser.

By comparing the respective spectra, we chose to analyse the spectra with the highest and lowest peaks only (including the samples from both lasers), in order to have the characteristics of the CNTs on the most and least populated parts of the wafer.

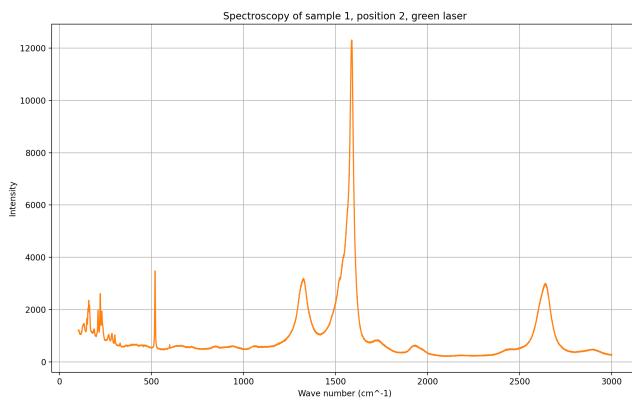


Figure 22: spectrum of sample 1, position 2, green laser.

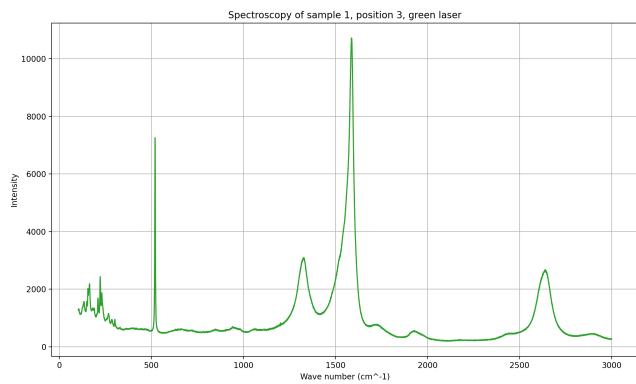


Figure 23: spectrum of sample 1, position 3, green laser.

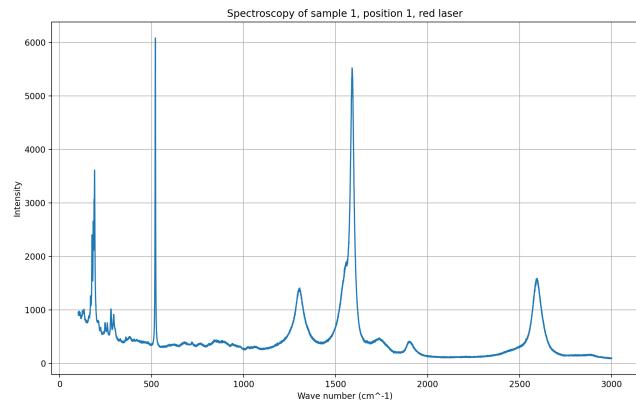


Figure 24: spectrum of sample 1, position 1, red laser.

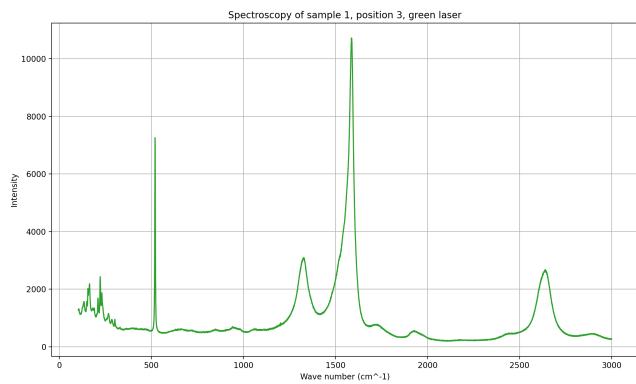


Figure 25: spectrum of sample 1, position 3, red laser.

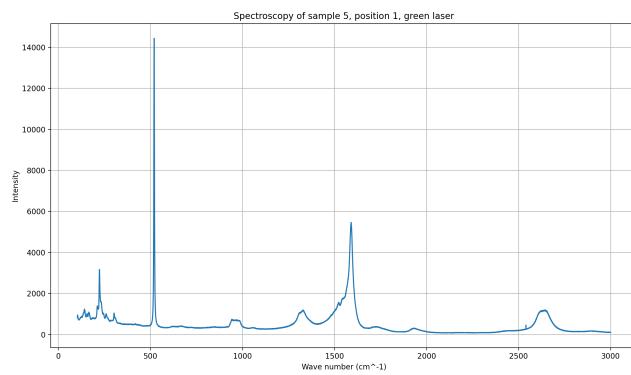


Figure 26: spectrum of sample 5, position 1, green laser.

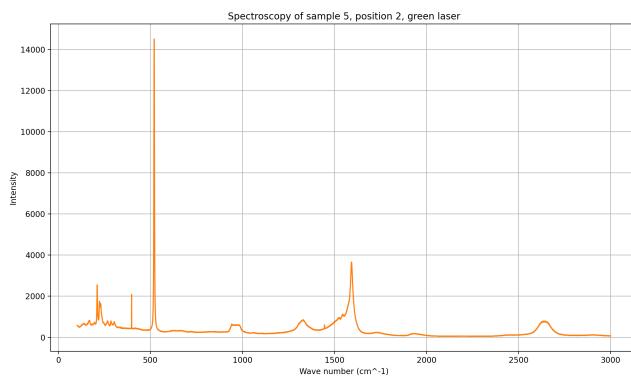


Figure 27: spectrum of sample 5, position 2, green laser.

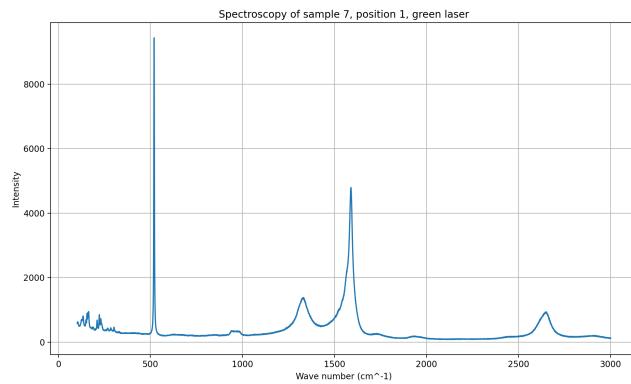


Figure 28: spectrum of sample 7, position 1, green laser.

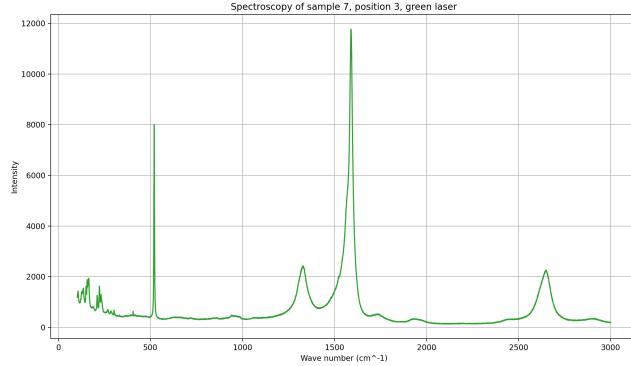


Figure 29: spectrum of sample 7, position 3, green laser.

For the first sample, 2 spectra for each laser were chosen because it was the only sample whose both results for the different lasers, showed the maximum and minimum peaks at different positions for each laser.

The radii were calculated the same way as in the paper by S. Forel and co-workers³, where they used the formula:

$$\omega = 248/d \quad (4.2.1)$$

Where d is the diameter of the CNTs and ω is the wave number at which there is a peak (peak frequency). Once we have the radii of the CNTs, and by comparing¹ the results from the red laser with the results from the green one we can see what type of CNTs we have (metallic or semi conducting). Finally, by analyzing² the D and G bands from the graphs, namely the D/G ratio, we can also estimate the predominant kind of CNTs we have (single-walled, double-walled or multi-walled).

From these results we can conclude that we have CNTs with the following characteristics:

	Sample 1	Sample 5	Sample 7
Radius (nm) $\pm 0.01\text{nm}$	0.8 - 1.3	0.8 - 1.4	1.0 - 1.5
CNT predominant type	Semi-conducting	Semi-conducting	Metallic
CNT predominant kind	2 single-walled	single-walled	double-walled

However, the biggest CNTs density for the three samples were for CNTs with radius of 1.1 nm in our three cases, whose peaks are clearly visible in figures 17-24.

4.2.5 Electrical measurements

As stated above, only sample 5 had an appropriate CNT density to build transistors with, so only this sample underwent the process of photolithography. However, after finishing this process, we proceeded to make electrical measurements. Unfortunately, no transistor was found that gave any of the desired measurements, which means no working transistor was found.

As a matter of fact, no transistor was found that after measured yielded the desired electrical properties. With only one final sample that made it to the final state it is hard to target the reason for this. The main hypotheses for this result are that the density of CNTs was not low enough, or the CNTs were too long, thus making the transistors to not behave as expected, but this is outside the scope of the current study.

5 Conclusion

It is clear that there exists a relationship between the CNT density and the catalyst monolayer thickness. As that thickness grows, even by a small amount, the density of the CNTs grew dramatically, quickly rendering the samples useless for the creation of nanotransistors. The best thickness, yielded by our results is around 0.35 nm for an atomic iron monolayer. It is also worth noting that the method of growth of the CNTs was very successful since the three samples measured presented a notorious majority of CNTs with the same radius, and in two samples we achieved a majority of semi-conducting and single-walled CNTs. This points to the fact that reproducibility for this results can be achieved if the same steps are followed carefully.

6 Bibliografía

1. Costa, S. Borowiak-Palen, E, Kruszynska, Marta, Bachmatiuk, A. Kalenczuk, Ryszard. (2008). Characterization of carbon nanotubes by Raman spectroscopy. Materials Science-Poland. 26.
2. del Corro, Elena Gonzalez, Jesus Taravillo, Mercedes Flahaut, Emmanuel Garcia Baonza, Valentin. (2008). Raman Spectra of Double-Wall Carbon Nanotubes under Extreme Uniaxial Stress. Nano Letters. 8. 10.1021/nl080760o.
3. Gaudin, S. (2007) The transistor: The most important invention of the 20th century?, Computerworld. Computerworld. Available at: <https://www.computerworld.com/article/2538123/the-transistor--the-most-important-invention-of-the-20th-century-.html> (Accessed: December 11, 2022).
4. Michael Anissimov Last Modified Date: December 03 and Michael Anissimov Michael is a longtime EasyTechJunkie contributor who specializes in topics relating to paleontology (2022) What is a nanotransistor?, EasyTechJunkie. Available at: <https://www.easytechjunkie.com/what-is-a-nanotransistor.htm> (Accessed: December 11, 2022).
5. Salomé Forel, Alice Castan,c Hakim Amara, Ileana Florea,a Frédéric Fossard,b Laure Catala,c Christophe Bichara,d Talal Mallah,c Vincent Huc,c Annick Loiseau,b and Costel-Sorin Cojocaru. Tuning bimetallic catalysts for a selective growth of SWCNTs. Nanoscale, 10.1039/C8NR09589B.
6. Staff, E.D.N. (2001) Bell Labs claims first Nanotransistor, EDN. Available at: <https://www.edn.com/bell-labs-claims-first-nanotransistor/> (Accessed: December 11, 2022).
7. image transistor MOSFET: https://commons.wikimedia.org/wiki/File:Lateral_mosfet.svg
8. image growth SWCNT : <https://www.researchgate.net/figure/Growth-mechanism-of-carbon-nanotubefig4281751127>
9. Raman spectroscopy: <https://youtu.be/ILLRQsbW1nQ>
10. SEM: <https://youtu.be/a0G7iyz4McM>
11. SWCNTs transistors: <https://youtu.be/mf5wPBpnRnQ>