Daniel Wang **Electrical Engineering Student**

https://github.com/danielmutong

Vancouver, BC

danielmutong@yahoo.ca | 6047215501

EDUCATION

University of British Columbia **Sep, 2018 – Apr, 2023**

Bachelor of Applied Science – Electrical Engineering

Relevant Courses: System Software Engineering, Digital Design, Introduction to Microcomputers, Signals and Systems, Data Structures and Algorithms, Circuit Analysis, Vector Calculus

EXPERIENCE

Intel Corporation (Programmable Solutions Group), Software/Hardware Intern **Starting Jan 2021**

FPGA Silicon Architecture, Memory and Interconnect Performance Modeling Team **San Jose, USA**

- Will be working with **C++** (**SystemC** library) to model **RTL** designs (**Verilog**) for simulation of Intel's next generation **FPGAs**

UBC Baja SAE, Embedded Software Developer **Sep, 2019 – Present**

Electronic Continuous Variable Transmission **Vancouver, Canada**

- Implementing a Multiple-Input Single-Output control system for Electronic-CVT on off-road race vehicle using **C++**
- Used **QEMU** to simulate a **STM-32** running the control system in a **multi-threaded** environment using **FreeRTOS**
- Tuning PID controller that relates engine RPM and throttle position to torque conducted unit tests with **Google Test**
- Coded a GUI interface with **Python Tkinter** library to adjust parameters for testing

TECHNICAL PROJECTS

Autonomous Driving Car Using FPGA for Hardware Acceleration **Apr, 2020 – Present**

https://www.youtube.com/watch?v=-NW3qeaB6Hw

- Developed a mathematical lane detection algorithm with **C++** and **OpenCV**, tuned a PID controller for steering
- Wrote **Verilog** for image manipulations to allow for hardware acceleration on **FPGA**, resulted in 92% image size reduction
- Designing interface which allows the **FPGA** to communicate with an **ARM** processor running the autonomous driving software
- Implemented **YOLOv3** model with **TensorFlow** for car detection

Automatic Ski Reservation Bot **Dec, 2020**

- Coded a script with **Python Selenium** and **Schedule** to reserve ski tickets from local ski hill website at midnight release

Hardware Acceleration for Convolutional Neural Network **Nov, 2020 – Dec, 2020**

- Wrote **Verilog** for hardware direct memory access and matrix calculations, used memory-mapped Avalon bus interface protocols
- Connected hardware to Nios 2 soft processor to accelerate CNN code written in **C** (MNIST dataset), implemented on **FPGA**

ARC4 Decryption Circuit **Oct, 2020 – Nov, 2020**

- Designed circuit with **System Verilog** to decipher an ARC4 cipher in parallel (50% faster than software methods), verified with **C++**
- Employed extensive use of on-chip memory blocks on the **DE1-SOC** and wrote extensive test benches for > 95% code coverage

Formula 1 Pitstop Simulation **Oct, 2020 – Nov, 2020**

- Developed a concurrent **multi-threaded, multi-process** program in **C++** to simulate a Formula 1 race, had 25+ threads, 3 processes
- Utilized semaphores, mutexes, and FIFOs to allow for inter-thread/inter-process communication and synchronization

Reduced Instruction Set Computer (RISC) **Oct, 2019 – Nov, 2019**

- Designed a RISC with **Verilog** capable of running simple **ARM Assembly** instructions and implemented on **FPGA**
- Included an FSM to control the Datapath, ALU, interactions with memory and I/O, and supports branching instructions

TECHNICAL SKILLS

Programming Languages: C/C++ • Python • ARM Assembly • MATLAB

Hardware Skills: Verilog/System Verilog • SystemC • FPGA • PCB Design • Quartus • Modelsim

Computer Skills: Linux • Multi-threaded • Object-Oriented • Embedded Systems

Software: OpenCV • TensorFlow • Git • GCC/GDB • QEMU • UML • FreeRTOS • Google Test • Eclipse