V_{CCINT} operating range from the data sheet = 3%;

Assumed DC tolerance = 1%;

Therefore, allowable AC ripple = 3% – 1% = 2%.

The target impedance is calculated using the 2% AC ripple along with the current estimates from XPE for the above resource utilization to arrive at the capacitor recommendations. The equation for target impedance is:

$$Z_{target} = \frac{\text{VoltageRailValue} \times \frac{\%\ \text{Ripple}}{100}}{\text{StepLoadCurrent}} \qquad \textit{Equation 1-1}$$

V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} capacitors are listed as the quantity per device, while V_{CCO} capacitors are listed as the quantity per I/O bank. Device performance at full utilization is equivalent across all devices when using these recommended networks.

Table 1-2 through Table 1-9 do not provide the decoupling networks required for the GTY or GTH transceiver power supplies. For this information, refer to the *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 6] or the *UltraScale Architecture GTY Transceivers User Guide* (UG578) [Ref 7].

RECOMMENDED: *Refer to the UltraScale Architecture Schematic Review Checklist (XTP344) [Ref 8] and UltraScale+ FPGA and Zynq UltraScale+ MPSoC Schematic Review Checklist (XTP427) [Ref 18] for a comprehensive checklist for schematic review which complements this user guide.*

Note: The capacitor values and part numbers have been updated taking into account the latest product offerings from various vendors because some of the part numbers from the previous versions of this user guide have reached end of life. The new guidelines also incorporate capacitors with a wider temperature range (X6S) compared to the previous part numbers, while moving away from a combination of tantalum/ceramic capacitors to solely ceramic capacitors across the entire frequency range. The prior capacitor tables and specifications are still valid for existing designs, but for new designs, the current tables and specifications are recommended.

Recommended Decoupling Capacitor Quantities for Kintex UltraScale and Virtex UltraScale Devices

Table 1-2 and Table 1-3 show the recommended decoupling capacitor quantities for Kintex UltraScale and Virtex UltraScale devices.

Table 1-2: **Kintex UltraScale Devices Decoupling Capacitor Recommendations**

	V_{CCINT}/V_{CCINT_IO} (1)				V_{CCBRAM}		V_{CCAUX}/V_{CCAUX_IO} (2)		HRIO/HPIO (3) (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCKU025-FFVA1156	1	4	1	1	1	1	1	1	1	1
XCKU035-FBVA676	1	5	1	1	1	1	1	1	1	1
XCKU035-SFVA784	1	5	1	1	1	1	1	1	1	1

Table 1-2: **Kintex UltraScale Devices Decoupling Capacitor Recommendations *(Cont'd)***

	V_{CCINT}/V_{CCINT_IO}[1]				V_{CCBRAM}		V_{CCAUX}/V_{CCAUX_IO}[2]		HRIO/HPIO[3] (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCKU035-FBVA900	1	5	1	1	1	1	1	1	1	1
XCKU035-FFVA1156	1	5	1	1	1	1	1	1	1	1
XCKU040-FBVA676 XQKU040-RBA676	1	5	1	1	1	1	1	1	1	1
XCKU040-SFVA784 XQK040-RFA1156	1	5	1	1	1	1	1	1	1	1
XCKU040-FBVA900	1	5	1	1	1	1	1	1	1	1
XCKU040-FFVA1156	1	5	1	1	1	1	1	1	1	1
XCKU060-FFVA1156 XQKU060-RFA1156	1	5	1	1	1	1	1	1	1	1
XCKU060-FFVA1517	1	5	1	1	1	1	1	1	1	1
XCKU085-FLVA1517	2	6	1	1	1	1	1	1	1	1
XCKU085-FLVB1760	2	6	1	1	1	1	1	1	1	1
XCKU085-FLVF1924	2	6	1	1	1	1	1	2	1	1
XCKU095-FFVA1156 XQKU095-RFA1156	1	5	1	1	1	1	1	1	1	1
XCKU095-FFVC1517	1	5	1	1	1	1	1	1	1	1
XCKU095-FFVB1760	1	5	1	1	1	1	1	1	1	1
XCKU095-FFVB2104	1	5	1	1	1	1	1	2	1	1
XCKU115-FLVA1517	2	7	2	2	1	1	1	1	1	1
XCKU115-FLVD1517 XQKU115-RLD1517	2	7	2	2	1	1	1	1	1	1
XCKU115-FLVB1760	2	7	2	2	1	1	1	1	1	1
XCKU115-FLVD1924	2	7	2	2	1	1	1	1	1	1
XCKU115-FLVF1924 XQKU115-RLF1924	2	7	2	2	1	1	1	2	1	1
XCKU115-FLVA2104	2	7	2	2	1	1	1	2	1	1
XCKU115-FLVB2104	2	7	2	2	1	1	1	2	1	1

Notes:

1. Assumes combined V_{CCINT}/V_{CCINT_IO} plane or combined $V_{CCINT}/V_{CCINT\_IO}/V_{CCBRAM}$ plane.
2. V_{CCAUX} and V_{CCAUX_IO} must share the same plane on the PCB.
3. The 47 µF capacitor can be combined at one per every four shared HRIO/HPIO banks.

Table 1-3: **Virtex UltraScale Devices Decoupling Capacitor Recommendations**

	V_{CCINT}/V_{CCINT_IO}[1]				V_{CCBRAM}		V_{CCAUX}/V_{CCAUX_IO}[2]		HRIO/HPIO[3] (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCVU065-FFVC1517	1	5	1	1	1	1	1	1	1	1
XCVU080-FFVC1517	1	5	1	1	1	1	1	1	1	1
XCVU080-FFVD1517	1	5	1	1	1	1	1	1	1	1
XCVU080-FFVB1760	1	5	1	1	1	1	1	1	1	1
XCVU080-FFVA2104	1	5	1	1	1	1	1	2	1	1
XCVU080-FFVB2104	1	5	1	1	1	1	1	2	1	1
XCVU095-FFVC1517	1	5	1	1	1	1	1	1	1	1
XCVU095-FFVD1517	1	5	1	1	1	1	1	1	1	1
XCVU095-FFVB1760	1	5	1	1	1	1	1	1	1	1
XCVU095-FFVA2104	1	5	1	1	1	1	1	2	1	1
XCVU095-FFVB2104	1	5	1	1	1	1	1	2	1	1
XCVU095-FFVC2104	1	5	1	1	1	1	1	1	1	1
XCVU125-FLVD1517	2	6	1	1	1	1	1	1	1	1
XCVU125-FLVB1760	2	6	1	1	1	1	1	1	1	1
XCVU125-FLVA2104	2	6	1	1	1	1	1	2	1	1
XCVU125-FLVB2104	2	6	1	1	1	1	1	2	1	1
XCVU125-FLVC2104	2	6	1	1	1	1	1	2	1	1
XCVU160-FLGB2104	2	7	2	2	1	1	1	2	1	1
XCVU160-FLGC2104	2	7	2	2	1	1	1	2	1	1
XCVU190-FLGB2104	3	7	3	1	1	1	1	2	1	1
XCVU190-FLGC2104	3	7	3	1	1	1	1	2	1	1
XCVU190-FLGA2577	3	7	3	1	1	1	1	2	1	1
XCVU440-FLGB2377	5	11	7	17	1	2	2	4	1	1
XCVU440-FLGA2892	5	11	7	17	1	2	2	4	1	1

Notes:

1. Assumes combined V_{CCINT}/V_{CCINT_IO} plane or combined $V_{CCINT}/V_{CCINT\_IO}/V_{CCBRAM}$ plane.
2. V_{CCAUX} and V_{CCAUX_IO} must share the same plane on the PCB.
3. The 47 µF capacitor can be combined at one per every four shared HRIO/HPIO banks.

Recommended Decoupling Capacitor Quantities for Kintex UltraScale+ and Virtex UltraScale+ Devices

Table 1-4 and Table 1-5 show the recommended decoupling capacitor quantities for Kintex UltraScale+ and Virtex UltraScale+ devices, including 58G-enabled devices and HBM devices.

Table 1-4: **Kintex UltraScale+ FPGAs Decoupling Capacitor Recommendations**

	V_{CCINT}/V_{CCINT_IO}[1]				V_{CCBRAM}/V_{CCINT_IO}[2]		V_{CCAUX}/V_{CCAUX_IO}[3]		HDIO/HPIO[4] (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCKU3P-SFVB784	1	4	1	1	1	1	1	1	1	1
XCKU3P-FFVA676	1	4	1	1	1	1	1	1	1	1
XCKU3P-FFVB676	1	4	1	1	1	1	1	1	1	1
XCKU3P-FFVD900	1	4	1	1	1	1	1	1	1	1
XCKU5P-SFVB784 XQKU5P-FFRB784	1	5	1	1	1	1	1	1	1	1
XCKU5P-FFVA676	1	5	1	1	1	1	1	1	1	1
XCKU5P-FFVB676 XQKU5P-FFRB676	1	5	1	1	1	1	1	1	1	1
XCKU5P-FFVD900	1	5	1	1	1	1	1	1	1	1
XCKU9P-FFVE900	1	5	1	1	1	1	1	1	1	1
XCKU11P-FFVD900	1	5	1	1	1	1	1	1	1	1
XCKU11P-FFVA1156	1	5	1	1	1	1	1	1	1	1
XCKU11P-FFVE1517	1	5	1	1	1	1	1	1	1	1
XCKU13P-FFVE900	1	5	1	1	1	1	1	1	1	1
XCKU15P-FFVA1156 XQKU15P-FFRA1156	1	5	1	1	1	1	1	1	1	1
XCKU15P-FFVE1517 XQKU15P-FFRE1517	1	5	1	1	1	1	1	1	1	1
XCKU15P-FFVA1760	1	5	1	1	1	1	1	1	1	1
XCKU15P-FFVE1760	1	5	1	1	1	1	1	1	1	1

Notes:

1. Connect V_{CCINT} and V_{CCINT_IO} together on the PCB for -3, -2, and -1 speed grades.
2. Connect V_{CCBRAM} and V_{CCINT_IO} together on the PCB for -2L and -1L speed grades.
3. V_{CCAUX} and V_{CCAUX_IO} must share the same plane on the PCB.
4. The 470 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Table 1-5: **Virtex UltraScale+ FPGAs Decoupling Capacitor Recommendations**

	V_{CCINT}/V_{CCINT_IO}[1]				V_{CCBRAM}/V_{CCINT_IO}[2]		V_{CCAUX}/V_{CCAUX_IO}[3]		HRIO/HPIO[4] (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCVU3P-FFVC1517 XQVU3P-FFRC1517	1	5	1	1	1	1	1	1	1	1
XCVU5P-FLVA2104	2	6	1	1	1	1	2	2	1	1
XCVU5P-FLVB2104	2	6	1	1	1	1	2	2	1	1
XCVU5P-FLVC2104	2	6	1	1	1	1	2	2	1	1
XCVU7P-FLVA2014 XQVU7P-FLRA2104	2	7	2	2	1	1	2	2	1	1
XCVU7P-FLVB2104 XQVU7P-FLRB2104	2	7	2	2	1	1	2	2	1	1
XCVU7P-FLVC2104	2	7	2	2	1	1	2	2	1	1
XCVU9P-FLGA2104	3	8	3	4	1	2	2	2	1	1
XCVU9P-FLGB2104	3	8	3	4	1	2	2	2	1	1
XCVU9P-FLGC2104	3	8	3	4	1	2	2	2	1	1
XCVU9P-FSGD2104	3	8	3	4	1	2	2	2	1	1
XCVU9P-FLGA2577	3	8	3	4	1	2	2	2	1	1
XCVU11P-FLGF1924	4	9	4	8	1	2	1	2	1	1
XCVU11P-FLGB2104	4	9	4	8	1	2	1	2	1	1
XCVU11P-FLGC2104 XQVU11P-FLRC2104	4	9	4	8	1	2	1	2	1	1
XCVU11P-FSGD2104	4	9	4	8	1	2	1	2	1	1
XCVU11P-FLGA2577	4	9	4	8	1	2	1	2	1	1
XCVU13P-FHGA2104	5	11	6	16	1	2	2	2	1	1
XCVU13P-FHGB2104	5	11	6	16	1	2	2	2	1	1
XCVU13P-FHGC2104	5	11	6	16	1	2	2	2	1	1
XCVU13P-FIGD2104	5	11	6	16	1	2	2	2	1	1
XCVU13P-FLGA2577	5	11	6	16	1	2	2	2	1	1
XCVU13P-FSGA2577	5	11	6	16	1	2	2	2	1	1

Notes:

1. Connect V_{CCINT} and V_{CCINT_IO} together for -3, -2, and -1 speed grades.
2. Connect V_{CCBRAM} and V_{CCINT_IO} together for -2L and -1L speed grades.
3. V_{CCINT}, V_{CCINT_IO}, and V_{CCBRAM} can be tied together if all three rails are operated at the same voltage.
4. One 47 µF capacitor is required for up to four HP/HR I/O banks when powered by the same voltage.

Table 1-6: **Virtex UltraScale+ FPGAs Decoupling Capacitor Recommendations for 58G Enabled Devices**

	V_{CCINT} or $V_{CCINT}/V_{CCBRAM}/V_{CCINT\_IO}/V_{CCINT\_GT}$[1][2]				$V_{CCBRAM}/V_{CCINT\_IO}/V_{CCINT\_GT}$[1][2]		V_{CCAUX}/V_{CCAUX_IO}[3]		HPIO[4] (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCVU27P-FIGD2104	3	9	4	8	1	2	1	2	1	1
XCVU27P-FSGA2577	3	9	4	8	1	2	1	2	1	1
XCVU29P-FIGD2104	4	10	6	15	1	2	2	2	1	1
XCVU29P-FSGA2577	4	10	6	15	1	2	2	2	1	1

Notes:

1. For non -2LE devices, combine V_{CCINT}, V_{CCBRAM}, V_{CCINT_IO}, and V_{CCINT_GT} to the same plane on the PCB.
2. For -2LE devices, V_{CCINT} is standalone. Combine V_{CCBRAM}, V_{CCINT_IO}, and V_{CCINT_GT} to the same plane on the PCB.
3. V_{CCAUX} and V_{CCAUX_IO} must share the same plane on the PCB.
4. The 47 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Table 1-7: **Virtex UltraScale+ FPGAs Decoupling Capacitor Recommendations for HBM Devices**

	V_{CCINT} or $V_{CCINT}/V_{CCBRAM}/V_{CCINT\_IO}$[1]				V_{CCBRAM}/V_{CCINT_IO}		V_{CCAUX}/V_{CCAUX_IO}[2]		HPIO[3] (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCVU31P-FSVH1924	1	5	1	1	1	2	1	1	1	1
XCVU33P-FSVH2104	1	5	1	1	1	2	1	1	1	1
XCVU35P-FSVH2104	2	7	2	2	1	2	1	1	1	1
XCVU35P-FSVH2892	2	7	2	2	1	2	1	1	1	1
XCVU37P-FSVH2892	3	9	4	8	1	2	2	2	1	1

Notes:

1. V_{CCINT} can be standalone or combined with V_{CCBRAM} and V_{CCINT_IO} on the same plane.
2. V_{CCAUX} and V_{CCAUX_IO} must share the same plane on the PCB.
3. The 47 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Table 1-8: **Decoupling Capacitor Recommendations for Virtex UltraScale+ Device HBM Rails**

	V_{CC_HBM}			$V_{CC\_IO\_HBM}$			V_{CCAUX_HBM}	
	100 µF	47 µF	10 µF	100 µF	47 µF	10 µF	47 µF	10 µF
VU31P, VU33P, VU35P, VU37P	1	1	2	1	1	1	1	1

Notes:

1. These recommendations are per stack.
2. Step load assumptions for V_{CC_HBM} and $V_{CC\_IO\_HBM}$ are approximately 2.5A per stack per rail for VU31P, VU33P, VU35P, and VU37P.

Recommended Decoupling Capacitor Quantities for Zynq UltraScale+ Devices

Table 1-9 shows the recommended decoupling capacitor quantities for Zynq UltraScale+ devices.

Table 1-9: **Zynq UltraScale+ MPSoC Decoupling Capacitor Recommendations**

	V_{CCINT}/V_{CCINT_IO} (1)				V_{CCBRAM}/V_{CCINT_IO} (2)		V_{CCAUX}/V_{CCAUX_IO} (3)		HDIO/HPIO (4) (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
CG Devices										
XCZU2CG-SBVA484	1	4	1	1	1	1	1	1	1	1
XCZU2CG-SFVA625	1	4	1	1	1	1	1	1	1	1
XCZU2CG-SFVC784	1	4	1	1	1	1	1	1	1	1
XCZU3CG-SFVC484	1	4	1	1	1	1	1	1	1	1
XCZU3CG-SFVA625	1	4	1	1	1	1	1	1	1	1
XCZU3CG-SFVC784	1	4	1	1	1	1	1	1	1	1
XCZU4CG-SFVC784	1	4	1	1	1	1	1	1	1	1
XCZU4CG-FBVB900	1	4	1	1	1	1	1	1	1	1
XCZU5CG-SFVC784	1	4	1	1	1	1	1	1	1	1
XCZU5CG-FBVB900	1	4	1	1	1	1	1	1	1	1
XCZU6CG-FFVC900	1	5	1	1	1	1	1	1	1	1
XCZU6CG-FBVB1156	1	5	1	1	1	1	1	1	1	1
XCZU7CG-FBVB900	1	5	1	1	1	1	1	1	1	1
XCZU7CG-FFVC1156	1	5	1	1	1	1	1	1	1	1
XCZU7CG-FFVF1517	1	5	1	1	1	1	1	1	1	1
XCZU9CG-FFVC900	1	5	1	1	1	1	1	1	1	1
XCZU9CG-FBVB1156	1	5	1	1	1	1	1	1	1	1
EG Devices										
XCZU2EG-SBVA484	1	4	1	1	1	1	1	1	1	1
XCZU2EG-SFVA625	1	4	1	1	1	1	1	1	1	1
XCZU2EG-SFVC784	1	4	1	1	1	1	1	1	1	1
XCZU3EG-SFVC484 XQZU3EG-SFRA484	1	4	1	1	1	1	1	1	1	1
XCZU3EG-SFVA625	1	4	1	1	1	1	1	1	1	1
XCZU3EG-SFVC784 XQZU3EG-SFRC784	1	4	1	1	1	1	1	1	1	1
XCZU4EG-SFVC784	1	4	1	1	1	1	1	1	1	1

Table 1-9: **Zynq UltraScale+ MPSoC Decoupling Capacitor Recommendations *(Cont'd)***

	V_{CCINT}/V_{CCINT_IO}[1]				V_{CCBRAM}/V_{CCINT_IO}[2]		V_{CCAUX}/V_{CCAUX_IO}[3]		HDIO/HPIO[4] (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCZU4EG-FBVB900	1	4	1	1	1	1	1	1	1	1
XCZU5EG-SFVC784	1	4	1	1	1	1	1	1	1	1
XCZU5EG-FBVB900	1	4	1	1	1	1	1	1	1	1
XCZU6EG-FFVC900	1	5	1	1	1	1	1	1	1	1
XCZU6EG-FBVB1156	1	5	1	1	1	1	1	1	1	1
XCZU7EG-FBVB900	1	5	1	1	1	1	1	1	1	1
XCZU7EG-FFVC1156	1	5	1	1	1	1	1	1	1	1
XCZU7EG-FFVF1517	1	5	1	1	1	1	1	1	1	1
XCZU9EG-FFVC900 XQZU9EG-FFRC900	1	5	1	1	1	1	1	1	1	1
XCZU9EG-FBVB1156 XQZU9EG-FFRB1156	1	5	1	1	1	1	1	1	1	1
XCZU11EG-FFVC1156 XQZU11EG-FFRC1156	1	5	1	1	1	1	1	1	1	1
XCZU11EG-FFVB1517	1	5	1	1	1	1	1	1	1	1
XCZU11EG-FFVF1517	1	5	1	1	1	1	1	1	1	1
XCZU11EG-FFVC1760 XQZU11EG-FFRC1760	1	5	1	1	1	1	1	1	1	1
XCZU15EG-FFVC900 XQZU15EG-FFRC900	1	5	1	1	1	1	1	1	1	1
XCZU15EG-FBVB1156 XQZU15EG-FFRB1156	1	5	1	1	1	1	1	1	1	1
XCZU17EG-FFVB1517	1	5	1	1	1	1	1	1	1	1
XCZU17EG-FFVC1760	1	5	1	1	1	1	1	1	1	1
XCZU17EG-FFVD1760	1	5	1	1	1	1	1	1	1	1
XCZU17EG-FFVE1924	1	5	1	1	1	1	1	1	1	1
XCZU19EG-FFVB1517 XQZU19EG-FFRB1517	1	5	1	1	1	1	1	1	1	1
XCZU19EG-FFVC1760 XQZU19EG FFRC1760	1	5	1	1	1	1	1	1	1	1
XCZU19EG-FFVD1760	1	5	1	1	1	1	1	1	1	1
XCZU19EG-FFVE1924	1	5	1	1	1	1	1	2	1	1
EV Devices										
XCZU4EV-SFVC784	1	4	1	1	1	1	1	1	1	1

Table 1-9: **Zynq UltraScale+ MPSoC Decoupling Capacitor Recommendations *(Cont'd)***

	V_{CCINT}/V_{CCINT_IO}[1]				V_{CCBRAM}/V_{CCINT_IO}[2]		V_{CCAUX}/V_{CCAUX_IO}[3]		HDIO/HPIO[4] (per bank)	
	330 µF	100 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
XCZU4EV-FBVB900	1	4	1	1	1	1	1	1	1	1
XCZU5EV-SFVC784 XQZU5EV-SFRC784	1	4	1	1	1	1	1	1	1	1
XCZU5EV-FBVB900 XQZU5EV-FFRB900	1	4	1	1	1	1	1	1	1	1
XCZU7EV-FBVB900 XQZU7EV-FFRB900	1	5	1	1	1	1	1	1	1	1
XCZU7EV-FFVC1156 XQZU7EV-FFRC1156	1	5	1	1	1	1	1	1	1	1
XCZU7EV-FFVF1517	1	5	1	1	1	1	1	1	1	1
RFSoC Devices										
See Chapter 3, PCB Guidelines for Zynq UltraScale+ RFSoCs.										

Notes:

1. Connect V_{CCINT} and V_{CCINT_IO} together on the PCB for -3, -2, and -1 speed grades.
2. Connect V_{CCBRAM} and V_{CCINT_IO} together on the PCB for -2L and -1L speed grades.
3. V_{CCAUX} and V_{CCAUX_IO} must share the same plane on the PCB.
4. The 47 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Table 1-10: **Zynq UltraScale+ MPSoC PS Decoupling Capacitor Recommendations**

$V_{CC\_PSINTFP}$		$V_{CC\_PSINTLP}$		V_{CC_PSAUX}		V_{CC_PSPLL}		$V_{CC\_PSINTFP\_DDR}$		V_{CCO_PSIOx}[1] (Each)		V_{CC_PSBATT}		V_{CCO_PSDDR}	
100 µF	10 µF	100 µF	10 µF	100 µF	10 µF	100 µF	10 µF	100 µF	10 µF	100 µF	10 µF	100 µF	10 µF	100 µF	10 µF
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes:

1. The 100 µF capacitor can be combined at one per every four shared V_{CCO_PSIO} banks.
2. For PS_MGTRAVCC and PS_MGTRAVTT use one 10 µF capacitor each. See Chapter 4, PCB Guidelines for the PS Interface in the Zynq UltraScale+ MPSoC.

Capacitor Specifications

Table 1-11 lists capacitor specifications that were used when determining the PCB decoupling tables in this chapter. Alternate devices can be used to fit particular design requirements, with simulations to ensure suitability.

Table 1-11: **Recommended PCB Capacitor Specifications and Placement Guidelines**

Nominal Value (µF)	Case Size	Temp/Change (%)	Manufacturer	Manufacturer Part Number	Ideal Placement to FPGA/MPSoC[1]
330	1210	X6S	Murata	GRM32EC80E337ME05	1–4″
100	0805	X6S	Murata	GRM21BC80G107ME15	0.5–3″

Table 1-11: **Recommended PCB Capacitor Specifications and Placement Guidelines *(Cont'd)***

Nominal Value (µF)	Case Size	Temp/Change (%)	Manufacturer	Manufacturer Part Number	Ideal Placement to FPGA/MPSoC(1)
47	0603	X6S	Murata	GRM188C80E476ME05	0.5–2″
10	0402	X6S	Murata	GRM155C80J106ME11D	0–1″(2)

Notes:

1. Ideal placement is to minimize spreading inductance from capacitor to FPGA/MPSoC.
2. Xilinx recommends placing the 0402 capacitors directly under the FPGA footprint on the oppose site of the board. This minimizes spreading inductance and result in maximum efficiency.

$V_{CC\_PSDDR\_PLL}$ Supply

$V_{CC\_PSDDR\_PLL}$ is a 1.8V nominal supply that provides power to the PLL used for the PS DDR controller. It can be powered separately or derived from the V_{CC_PSAUX} supply. If powered by V_{CC_PSAUX}, $V_{CC\_PSDDR\_PLL}$ must be filtered through a 120Ω @ 100 MHz, size 0603 ferrite bead and a 10 µF or larger, size 0603 decoupling capacitor. In both cases, a 1.0 µF 0201 or 10 µF 0402 capacitor must be placed near the $V_{CC\_PSDDR\_PLL}$ BGA via.

The PCB construction of the $V_{CC\_PSDDR\_PLL}$ power supply must be carefully managed. The recommended connection between the 0603 capacitor and the $V_{CC\_PSDDR\_PLL}$ BGA ball is a planelet with a minimum width of 80 mil (2 mm) and a length of less than 3,000 mil (76 mm). If a planelet cannot be used, a trace with a maximum impedance of 40Ω and a length of less than 2,000 mil (50.8 mm) must be used. The 0201 or 0402 capacitor should be placed a close as possible to the FPGA, along with the shortest possible trace length. Figure 1-1 shows an example of the filtering and local capacitor circuit used when $V_{CC\_PSDDR\_PLL}$ is derived from V_{CC_PSAUX}.

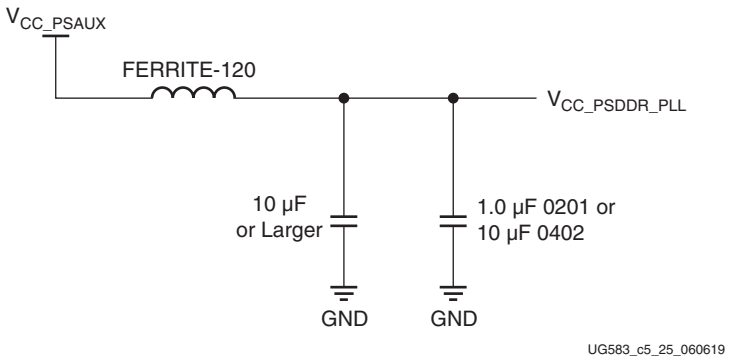

Figure 1-1: **Connecting $V_{CC\_PSDDR\_PLL}$**

Figure 1-2 shows an example of the layout of the same filtering circuit.

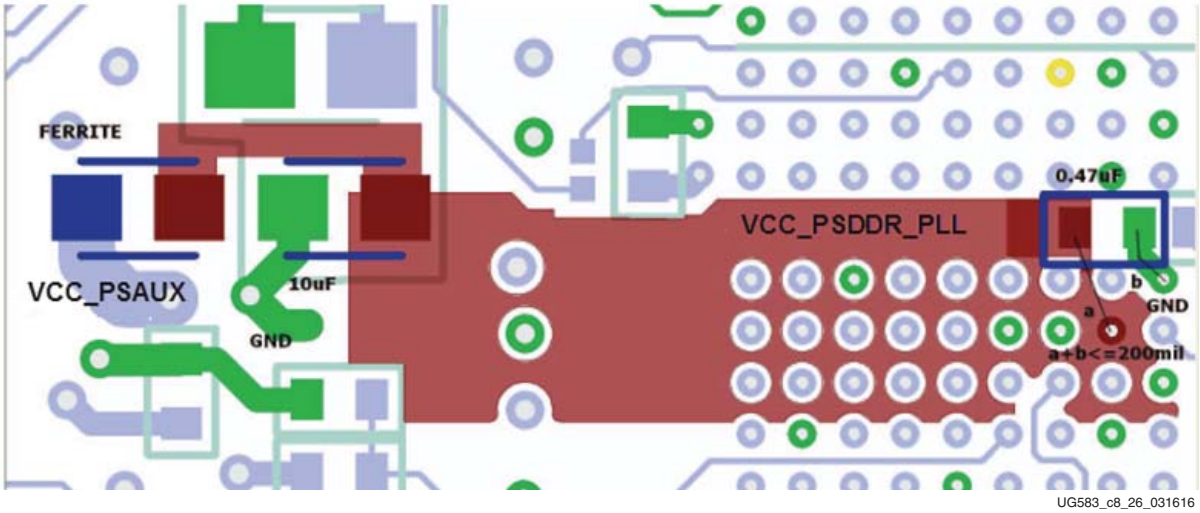

Figure 1-2: **Filtering Circuit Layout**

The recommended components are:

- Ferrite bead: Murata BLM18SG121TN1
- 10 µF (or larger) capacitor: Murata GRM188C80E476ME05
- 1.0 µF 0201 or 10 µF 0402 capacitor: Murata GRM155C80J106ME11D

Video Codec Unit (MPSoC EV Devices Only)

V_{CCINT_VCU} is a 0.90V rail that provides power to the video codec unit (VCU) within Zynq UltraScale+ MPSoC EV devices. V_{CCINT_VCU} must be powered as a standalone power rail and cannot be combined with any other power rails.

If the VCU is not going to be used, the V_{CCINT_VCU} pins can be grounded to reduce leakage current.