AWR1243 Single-Chip 77- and 79-GHz FMCW Transceiver

1 Device Overview

1.1 Features

- FMCW Transceiver
  - Integrated PLL, Transmitter, Receiver, Baseband, and A2D
  - 76- to 81-GHz Coverage With 4 GHz Available Bandwidth
  - Four Receive Channels
  - Three Transmit Channels (Two Can be Used Simultaneously)
  - Ultra-Accurate Chirp Engine Based on Fractional-N PLL
  - TX Power: 12 dBm
  - RX Noise Figure:
    - 15 dB (76 to 77 GHz)
    - 16 dB (77 to 81 GHz)
  - Phase Noise at 1 MHz:
    - –94 dBc/Hz (76 to 77 GHz)
    - –91 dBc/Hz (77 to 81 GHz)
- Built-in Calibration and Self-Test
  - Built-in Firmware (ROM)
  - Self-calibrating System Across Frequency and Temperature
- Host Interface
  - Control Interface With External Processor Over SPI
  - Data Interface With External Processor Over MIPI D-PHY and CSI2 V1.1
  - Interrupts for Fault Reporting
- ASIL B Capable
- AECQ100 Qualified
- AWR1243 Advanced Features
  - Embedded Self-monitoring With No Host Processor Involvement
  - Complex Baseband Architecture
  - Option of Cascading Multiple Devices to Increase Channel Count
  - Embedded Interference Detection Capability
- Power Management
  - Built-in LDO Network for Enhanced PSRR
  - I/Os Support Dual Voltage 3.3 V/1.8 V
- Clock Source
  - 40.0-MHz Crystal With Internal Oscillator
  - Supports External Oscillator at 40 and 50 MHz
- Easy Hardware Design
  - 0.65-mm Pitch, 161-Pin 10.4 mm × 10.4 mm Flip Chip BGA Package for Easy Assembly and Low-Cost PCB Design
  - Small Solution Size
- Supports Automotive Temperature Operating Range

1.2 Applications

- Automated Highway Driving
- Automatic Emergency Braking
- Adaptive Cruise Control

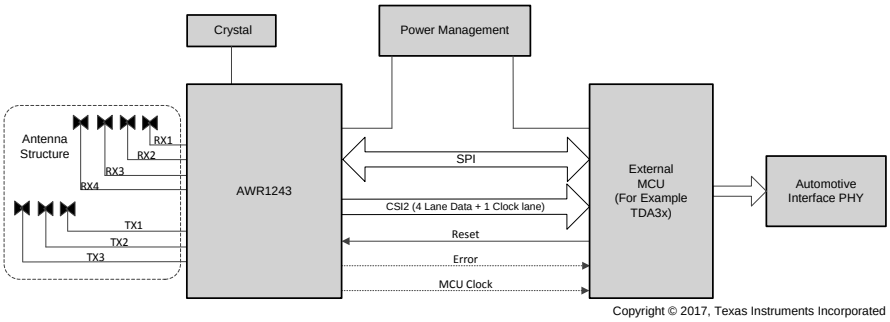

Figure 1-1. Radar Sensor for Automotive Applications

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1.3 Description

The AWR1243 device is an integrated single-chip FMCW transceiver capable of operation in the 76- to 81-GHz band. The device enables unprecedented levels of integration in an extremely small form factor. AWR1243 is an ideal solution for low power, self-monitored, ultra-accurate radar systems in the automotive space.

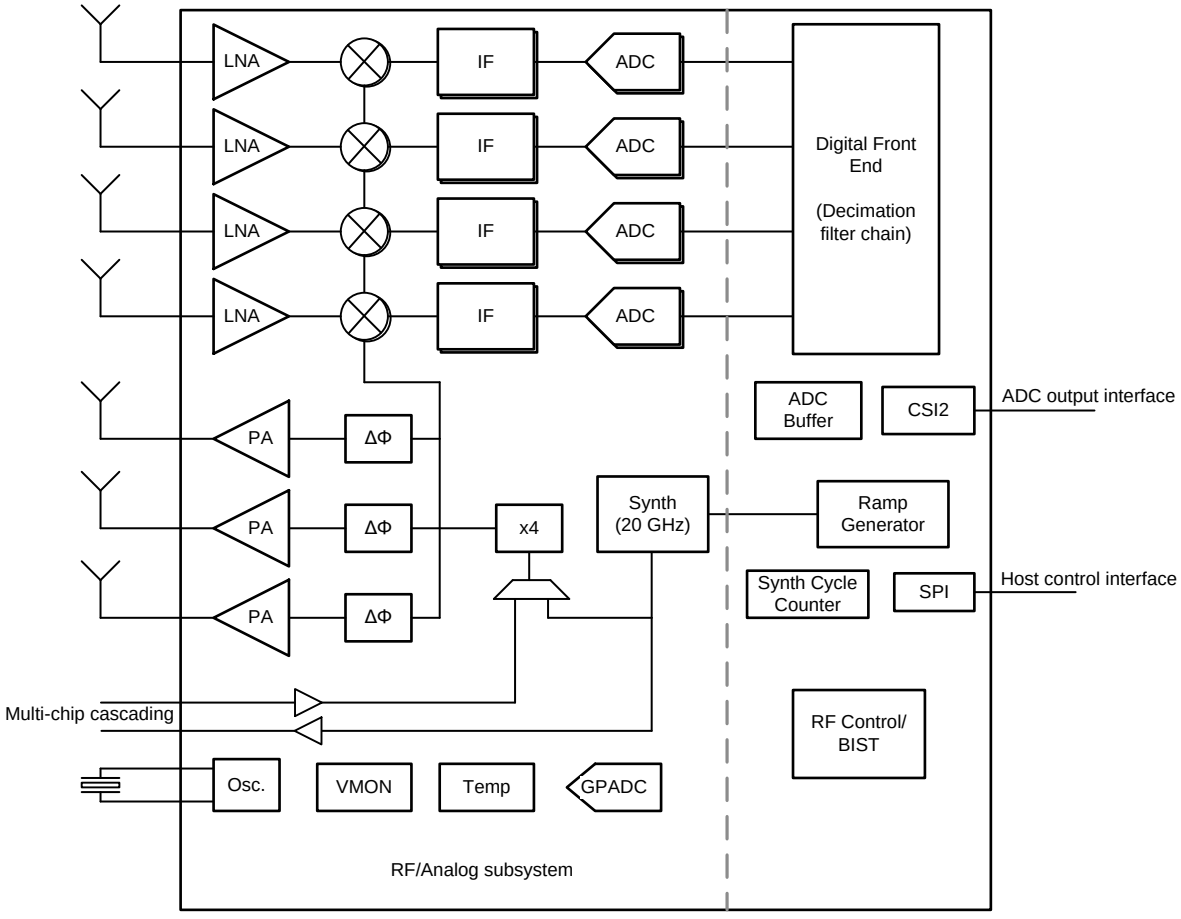
The AWR1243 device is a self-contained FMCW transceiver single-chip solution that simplifies the implementation of Automotive Radar sensors in the band of 76 to 81 GHz. It is built on TI's low-power 45-nm RFCMOS process, which enables a monolithic implementation of a 3TX, 4RX system with built-in PLL and A2D converters. Simple programming model changes can enable a wide variety of sensor implementation (Short, Mid, Long) with the possibility of dynamic reconfiguration for implementing a multimode sensor. Additionally, the device is provided as a complete platform solution including reference hardware design, software drivers, sample configurations, API guide, and user documentation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
X1243BIGABL (Tray)	FCBGA (161)	10.4 mm × 10.4 mm

(1) For more information, see Section 9, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram



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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2017	*	Initial Release

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3 Device Comparison

Table 3-1. Device Features Comparison

FUNCTION		AWR1243	AWR1443	AWR1642
Number of receivers		4	4	4
Number of transmitters		3	3	2
On-chip memory		—	576KB	1.5MB
ASIL		B-Capable	—	B-Capable
Max interface (MHz)		15	5	5
Max real sampling rate (Msps)		37.5	12.5	12.5
Processor				
MCU (R4F)		—	Yes	Yes
DSP (C674x)		—	—	Yes
Peripherals				
Serial Peripheral Interface (SPI) ports		1	1	2
Quad Serial Peripheral Interface (QSPI)		—	Yes	Yes
Inter-Integrated Circuit (I^2C) interface		—	1	1
Controller Area Network (DCAN) interface		—	Yes	Yes
CAN FD		—	—	Yes
Trace		—	—	Yes
PWM		—	—	Yes
Hardware In Loop (HIL/DMM)		—	—	Yes
GPADC		—	Yes	Yes
LVDS/Debug		Yes	Yes	Yes
CSI2		Yes	—	—
Hardware accelerator		—	Yes	—
1-V bypass mode		Yes	Yes	Yes
Cascade (20-GHz sync)		Yes	—	—
JTAG		—	Yes	Yes
Product status(1)	PRODUCT PREVIEW (PP), ADVANCE INFORMATION (AI), or PRODUCTION DATA (PD)	AI	AI	AI

(1) ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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3.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.

Automotive mmWave Sensors TI's automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI's scalable sensor portfolio enables design and development of ADAS system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.

Companion Products for AWR1243 Review products that are frequently purchased or used in conjunction with this product.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pin locations for the 161-pin FCBGA package. Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5 show the same pins, but split into four quadrants.

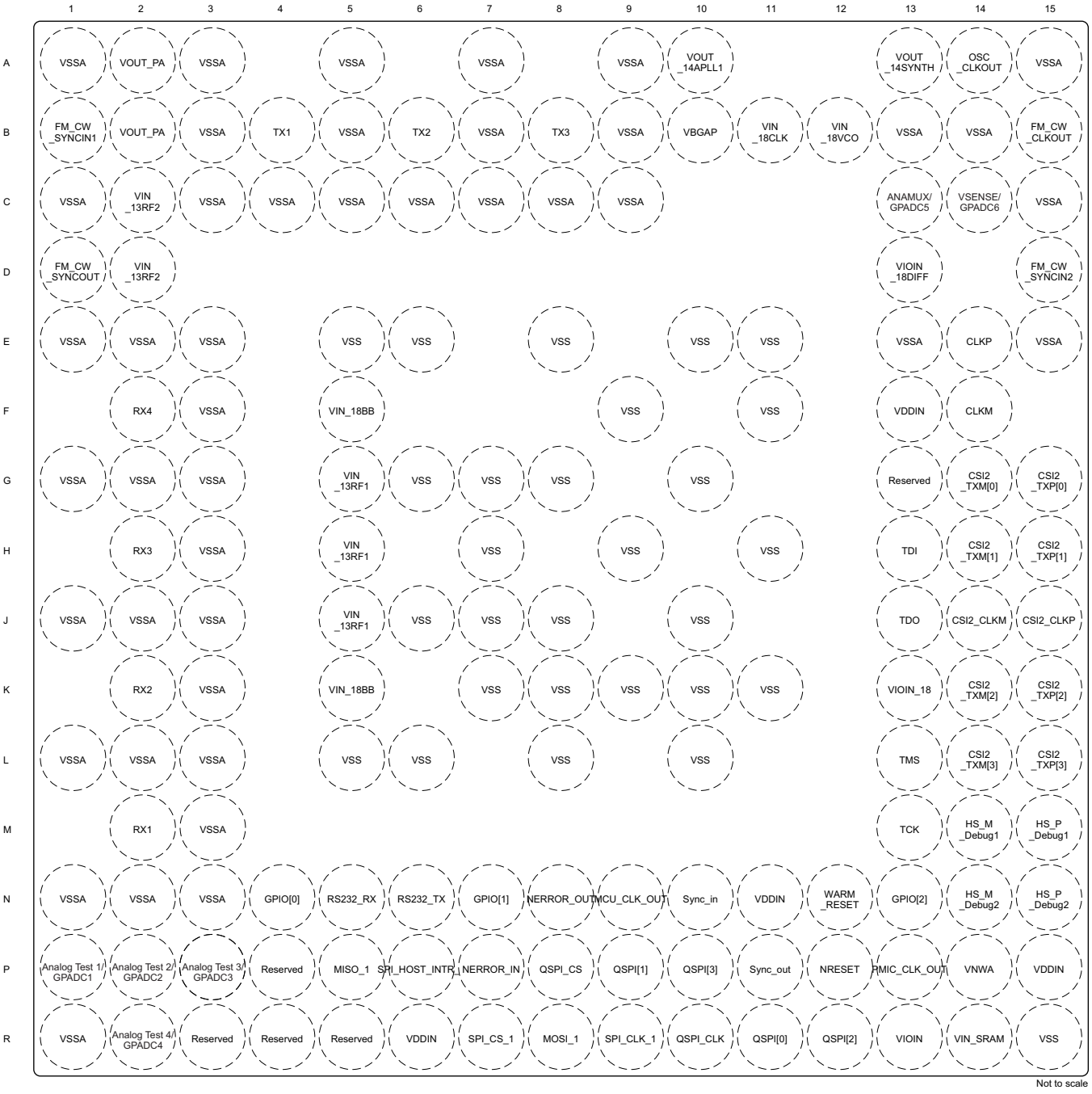

Figure 4-1. Pin Diagram

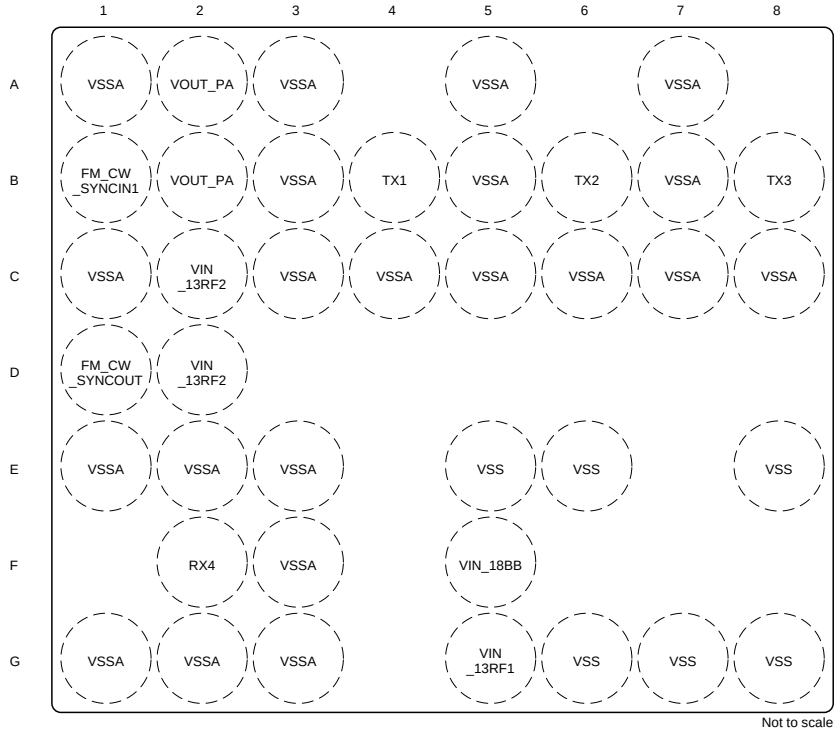

Figure 4-2. Top Left Quadrant

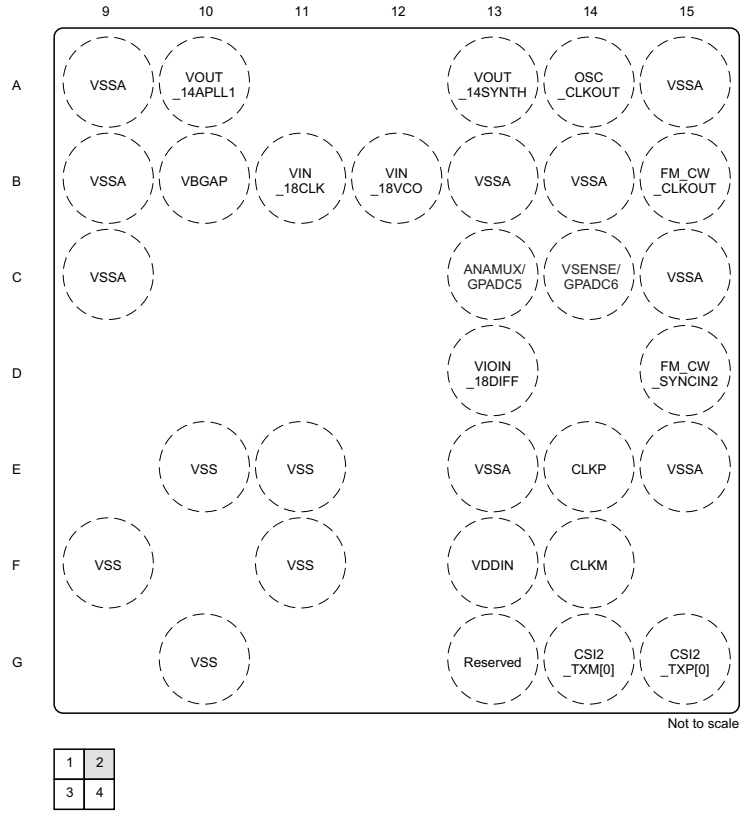

Figure 4-3. Top Right Quadrant

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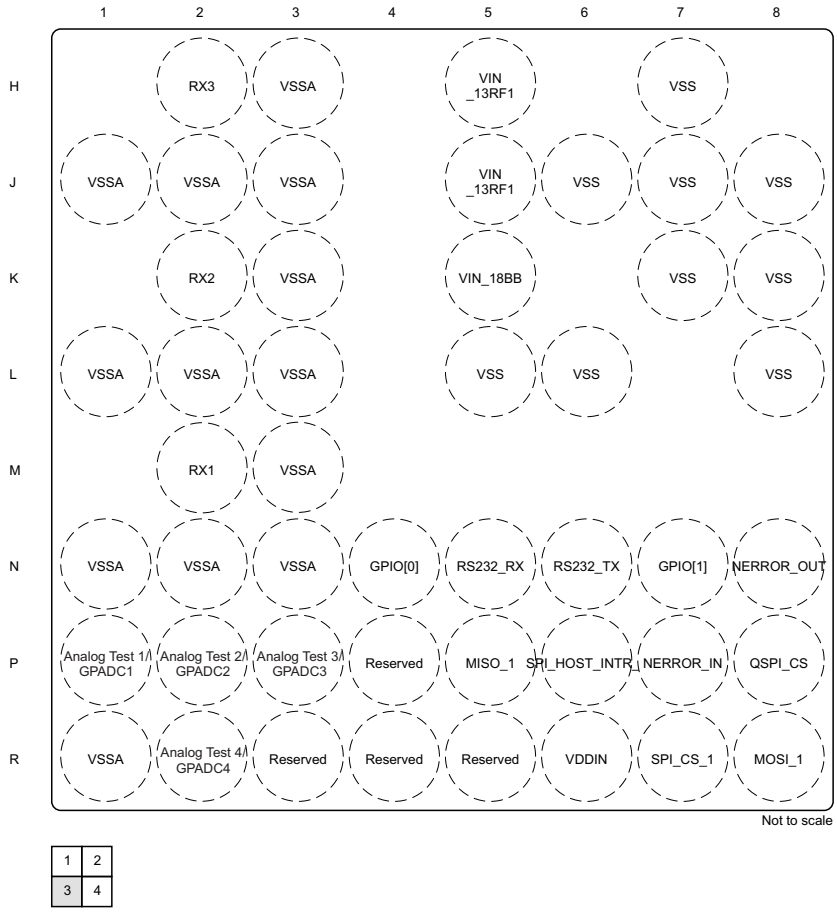

Figure 4-4. Bottom Left Quadrant

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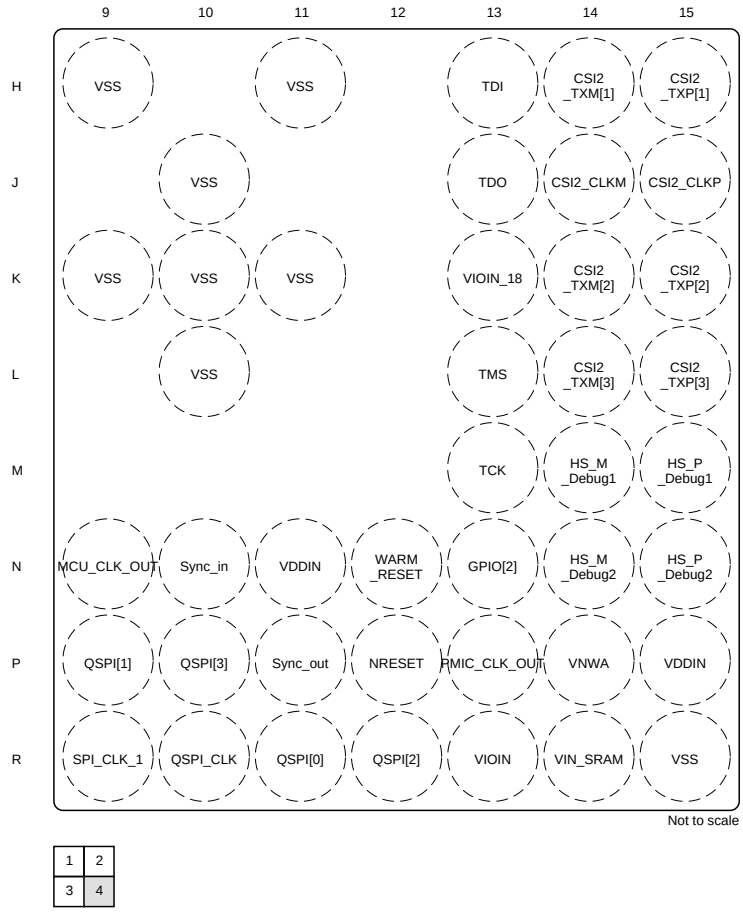

Figure 4-5. Bottom Right Quadrant

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4.2 Signal Descriptions

Table 4-1 lists the pins by function and describes that function.

Table 4-1. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
Transmitters	TX1	B4	O	Single-ended transmitter1 o/p
	TX2	B6	O	Single-ended transmitter2 o/p
	TX3	B8	O	Single-ended transmitter3 o/p
Receivers	RX1	M2	I	Single-ended receiver1 i/p
	RX2	K2	I	Single-ended receiver2 i/p
	RX3	H2	I	Single-ended receiver3 i/p
	RX4	F2	I	Single-ended receiver4 i/p
CSI2 TX	CSI2_TXP[0]	G15	O	Differential data Out – Lane 0
	CSI2_TXM[0]	G14	O	
	CSI2_CLKP	J15	O	Differential clock Out
	CSI2_CLKM	J14	O	
	CSI2_TXP[1]	H15	O	Differential data Out – Lane 1
	CSI2_TXM[1]	H14	O	
	CSI2_TXP[2]	K15	O	Differential data Out – Lane 2
	CSI2_TXM[2]	K14	O	
	CSI2_TXP[3]	L15	O	Differential data Out – Lane 3
	CSI2_TXM[3]	L14	O	
	HS_DEBUG1_P	M15	O	Differential debug port 1
	HS_DEBUG1_M	M14	O	
	HS_DEBUG2_P	N15	O	Differential debug port 2
	HS_DEBUG2_M	N14	O	
Chip-to-chip cascading synchronization signals	FM_CW_CLKOUT	B15	O	20-GHz single-ended output. Modulated waveform
	FM_CW_SYNCIN1	B1	I	20-GHz single-ended input. Only one of these pins should be used. Multiple instances for layout flexibility.
	FM_CW_SYNCIN2	D15	I	
	FM_CW_SYNCOUT	D1	O	20-GHz single-ended output for onboard loopback if desired
System synchronization	SYNC_OUT	P11	O	Low-frequency synchronization signal output
	SYNC_IN	N10	I	Low-frequency synchronization signal input
SPI control interface from external MCU (default slave mode)	SPI_CS_1	R7	I	SPI chip select
	SPI_CLK_1	R9	I	SPI clock
	MOSI_1	R8	I	SPI data input
	MISO_1	P5	O	SPI data output
	SPI_HOST_INTR_1	P6	O	SPI interrupt to host
	RESERVED	R3, R4, R5, P4		
Reset	NRESET	P12	I	Power on reset for chip. Active low
	WARM_RESET	N12	IO	Open-drain fail-safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.
Safety	NERROR_OUT	N8	O	Open-drain fail-safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.
	NERROR_IN	P7	I	Fail-safe input to the device. Error output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by firmware

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Table 4-1. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
JTAG	TMS	L13	I	JTAG port for standard boundary scan
	TCK	M13	I	
	TDI	H13	I	
	TDO	J13	O	
Reference oscillator	CLKP	E14	I	CLKP is the Input and CLKM is the Output to drive crystal
	CLKM	F14	O	
Reference clock	OSC_CLKOUT	A14	O	Reference clock output from clocking subsystem after cleanup PLL. Can be used by slave chip in multichip cascading
Band-gap voltage	VBGAP	B10	O	
Power supply	VDDIN	F13,N11,P15, R6	POW	1.2-V digital power supply
	VIN_SRAM	R14	POW	1.2-V power rail for internal SRAM
	VNWA	P14	POW	1.2-V power rail for SRAM array back bias
	VIOIN	R13	POW	I/O supply (3.3-V or 1.8-V): All CMOS I/Os would operate on this supply.
	VIOIN_18	K13	POW	1.8-V supply for CMOS IO
	VIN_18CLK	B11	POW	1.8-V supply for clock module
	VIOIN_18DIFF	D13	POW	1.8-V supply for CSI2 port
	Reserved	G13	POW	No connect
	VIN_13RF1	G5,J5,H5	POW	1.3-V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board
	VIN_13RF2	C2,D2	POW	
	VIN_18BB	K5,F5	POW	1.8-V Analog baseband power supply
	VIN_18VCO	B12	POW	1.8-V RF VCO supply
	VSS	E5,E6,E8,E10, E11,F9,F11,G 6,G7,G8,G10, H7,H9,H11,J6, J7,J8,J10,K7,K 8,K9,K10,K11, L5,L6,L8,L10, R15	GND	Digital ground
	VSSA	A1,A3,A5,A7,A 9,A15,B3,B5,B 7,B9,B13,B14, C1,C3,C4,C5, C6,C7,C8,C9, C15,E1,E2,E3, E13,E15,F3,G 1,G2,G3,H3,J1 ,J2,J3,K3,L1,L 2,L3, M3,N1,N2,N3, R1	GND	Analog ground
Internal LDO output/inputs	VOUT_14APLL1	A10	O	
	VOUT_14SYNTH	A13	O	
	VOUT_PA	A2,B2	O	
External clock out	PMIC_CLK_OUT	P13	O	Dithered clock input to PMIC
	MCU_CLK_OUT	N9	O	Programmable clock given out to external MCU or the processor
General-purpose I/Os	GPIO[0]	N4	IO	General-purpose IO
	GPIO[1]	N7	IO	General-purpose IO
	GPIO[2]	N13	IO	General-purpose IO

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Table 4-1. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
QSPI for Serial Flash(1)	QSPI_CS	P8	O	Chip-select output from the device. Device is a master connected to serial flash slave.
	QSPI_CLK	R10	O	Clock output from the device. Device is a master connected to serial flash slave.
	QSPI[0]	R11	IO	Data IN/OUT
	QSPI[1]	P9	IO	Data IN/OUT
	QSPI[2]	R12	IO	Data IN/OUT
	QSPI[3]	P10	IO	Data IN/OUT
Flash programming and RS232 UART(1)	RS232_TX	N6	O	UART pins for programming external flash in preproduction/debug hardware.
	RS232_RX	N5	I	
Test and Debug output for preproduction phase. Can be pinned out on production hardware for field debug	Analog Test1 / GPADC1	P1	IO	GP ADC channel 1
	Analog Test2 / GPADC2	P2	IO	GP ADC channel 2
	Analog Test3 / GPADC3	P3	IO	GP ADC channel 3
	Analog Test4 / GPADC4	R2	IO	GP ADC channel 4
	ANAMUX / GPADC5	C13	IO	GP ADC channel 5
	VSENSE / GPADC6	C14	IO	GP ADC channel 6

(1) This option is for development/debug in preproduction phase. Can be disabled by firmware pin mux setting.

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5 Specifications

5.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VDDIN	1.2 V digital power supply	–0.5	1.4	V
VIN_SRAM	1.2 V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2 V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	–0.5	2	V
VIN_18CLK	1.8 V supply for clock module	–0.5	2	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	–0.5	2	V
VIN_13RF1	1.3 V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board.	–0.5	1.45	V
VIN_13RF2		–0.5	1.45	V
VIN_13RF1 (1-V LDO bypass mode)	Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	–0.5	1.4	V
VIN_13RF2 (1-V Internal LDO bypass mode)		–0.5	1.4	V
VIN_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VIN_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot)		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	125	ºC
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±250	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Power-On Hours (POH)[1]

OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	JUNCTION TEMPERATURE (T_j)	POWER-ON HOURS [POH] (HOURS)
100% duty cycle	1.2	–40°C	600 (6%)
		75°C	2000 (20%)
		95°C	6500 (65%)
		105°C	900 (9%)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

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5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	3.15	3.3	3.45	V
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIOIN_18DIFF	1.8 V supply for CSI2 port	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board	1.23	1.3	1.36	V
VIN_13RF2		1.23	1.3	1.36	V
VIN_13RF1 (1-V Internal LDO bypass mode)	Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	0.95	1	1.05	V
VIN_13RF2 (1-V Internal LDO bypass mode)	Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	0.95	1	1.05	V
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
V_{IH}	Voltage Input High (1.8 V mode)	1.17			V
	Voltage Input High (3.3 V mode)	2.25			
V_{IL}	Voltage Input Low (1.8 V mode)			0.63	V
	Voltage Input Low (3.3 V mode)			0.8	
V_{OH}	High-level output threshold (I_{OH} = 6 mA)	85%*VIOIN			mV
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)			350	mV
CLKP,CLKM	Voltage Input High	0.96			V
	Voltage Input Low			0.24	

5.5 Power Supply Specifications

Table 5-1 describes the four rails from an external power supply block of the AWR1243 device.

Table 5-1. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, CSI2	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode)	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM

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Table 5-2 lists tolerable ripple specifications for 1.3-V (1.0-V) and 1.8-V supply rails.

Table 5-2. Ripple Specifications

FREQUENCY (kHz)	RF RAIL		VCO/IF RAIL
	1.0 V (INTERNAL LDO BYPASS) (μV_{RMS})	1.3 V (μV_{RMS})	1.8 V (μV_{RMS})
137.5	7.76	648.73	83.41
275	5.83	76.48	21.27
550	3.44	22.74	11.43
1100	2.53	4.05	6.73
2200	11.29	82.44	13.39
4200	13.65	93.35	19.70
6600	22.91	117.78	29.63

5.6 Power Consumption Summary

Table 5-3 and Table 5-4 summarize the power consumption at the power terminals.

Table 5-3. Maximum Current Ratings at Power Terminals

PARAMETER	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
Current consumption	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			500	mA
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V rail			2000	
	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail			850	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail			50	

Table 5-4. Average Power Consumption at Power Terminals

PARAMETER	CONDITION		DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption	1.0-V internal LDO bypass mode	1TX, 4RX	Sampling: 16.66 MSps complex Transceiver, 40-ms frame time, 512 chirps, 512 samples/chirp, 8.5-µs interchirp time (50% duty cycle) Data Port: MIPI-CSI-2		1.73		W
		2TX, 4RX			1.88		
	1.3-V internal LDO enabled mode	1TX, 4RX			1.92		
		2TX, 4RX			2.1		

ADVANCE INFORMATION

5.7 RF Specification

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Noise figure	76 to 77 GHz		15		dB
		77 to 81 GHz		16		
	1-dB compression point			–5		dBm
	Maximum gain step			48		dB
	Gain range			24		dB
	Gain step size			2		dB
	IQ gain mismatch			1		dB
	IQ phase mismatch			2		degree
	IF bandwidth(1)				15	MHz
	A2D sampling rate (real)				37.5	Msps
	A2D sampling rate (complex)				18.75	Msps
	A2D resolution			12		Bits
Transmitter	Output power			12		dBm
	Amplitude noise			–145		dBc/Hz
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				100	MHz/µs
	Phase noise at 1-MHz offset	76 to 77 GHz		–94		dBc/Hz
		77 to 81 GHz		–91		

(1) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)

HPF1	HPF2
175, 235, 350, 700	350, 700, 1400, 2800

The filtering performed by the baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

Figure 5-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

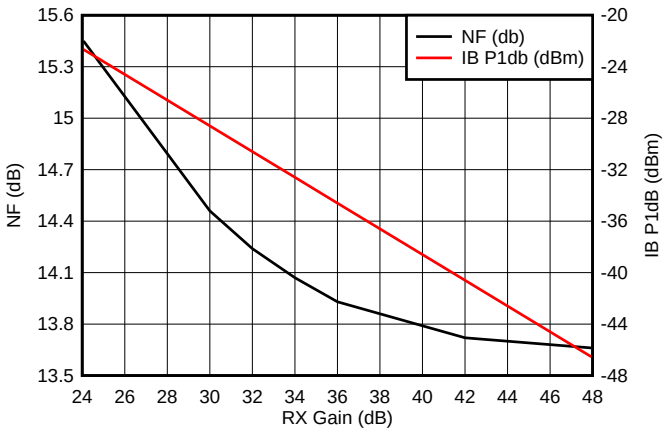


Figure 5-1. Noise Figure, In-band P1dB vs Receiver Gain

Table 5-5 describes the CSI-2 DPHY electrical specifications.

ADVANCE INFORMATION

Table 5-5. CSI-2 DPHY Electrical Specification

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
HSTX Driver					
$\|V_{OD}\|$	HS transmit differential voltage(1)	140	200	270	mV
V_{CMTX}	HS transmit static common-mode voltage(1)	150	200	250	mV
$\|\Delta V_{OD}\|$	VOD mismatch when output is Differential-1 or Differential-0			10	mV
$\|\Delta V_{CMTX(1,0)}\|$	VCMTX mismatch when output is Differential-1 or Differential-0			5	mV
V_{OHHS}	HS output high voltage(1)			360	mV
Z_{OS}	Single-ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch			10%	
LPTX Driver					
V_{OL}	Thevenin output low level	–50		50	mV
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V
Z_{OLP}	Output impedance of LP transmitter	110			Ω

(1) Value when driving into differential load impedance anywhere in the range from 80 to 125 Ω.

5.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161](1)

THERMAL METRICS(2)		°C/W(3) (4)
$R\Theta_{JC}$	Junction-to-case	4.92
$R\Theta_{JB}$	Junction-to-board	6.57
$R\Theta_{JA}$	Junction-to-free air	22.3
$R\Theta_{JMA}$	Junction-to-moving air	N/A(1)
Psi_{JT}	Junction-to-package top	4.92
Psi_{JB}	Junction-to-board	6.4

(1) N/A = not applicable
(2) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(3) °C/W = degrees Celsius per watt.
(4) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

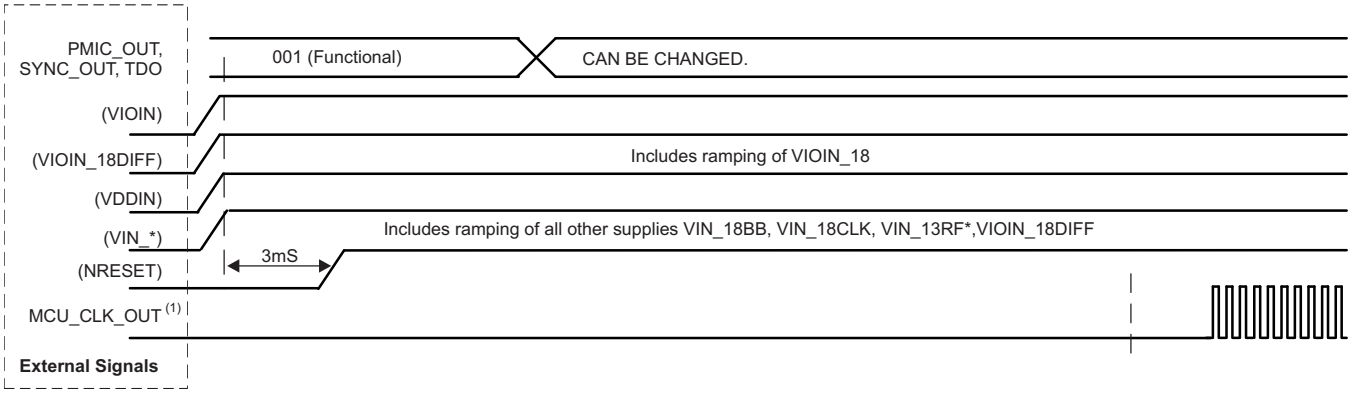
A junction temperature of 125ºC is assumed.

ADVANCE INFORMATION

5.9 Timing and Switching Characteristics

5.9.1 Power Supply Sequencing and Reset Timing

The AWR1243 device expects all external voltage rails to be stable before reset is deasserted. Figure 5-2 describes the device wake-up sequence.



(1) MCU_CLK_OUT in autonomous mode, where AWR1243 application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

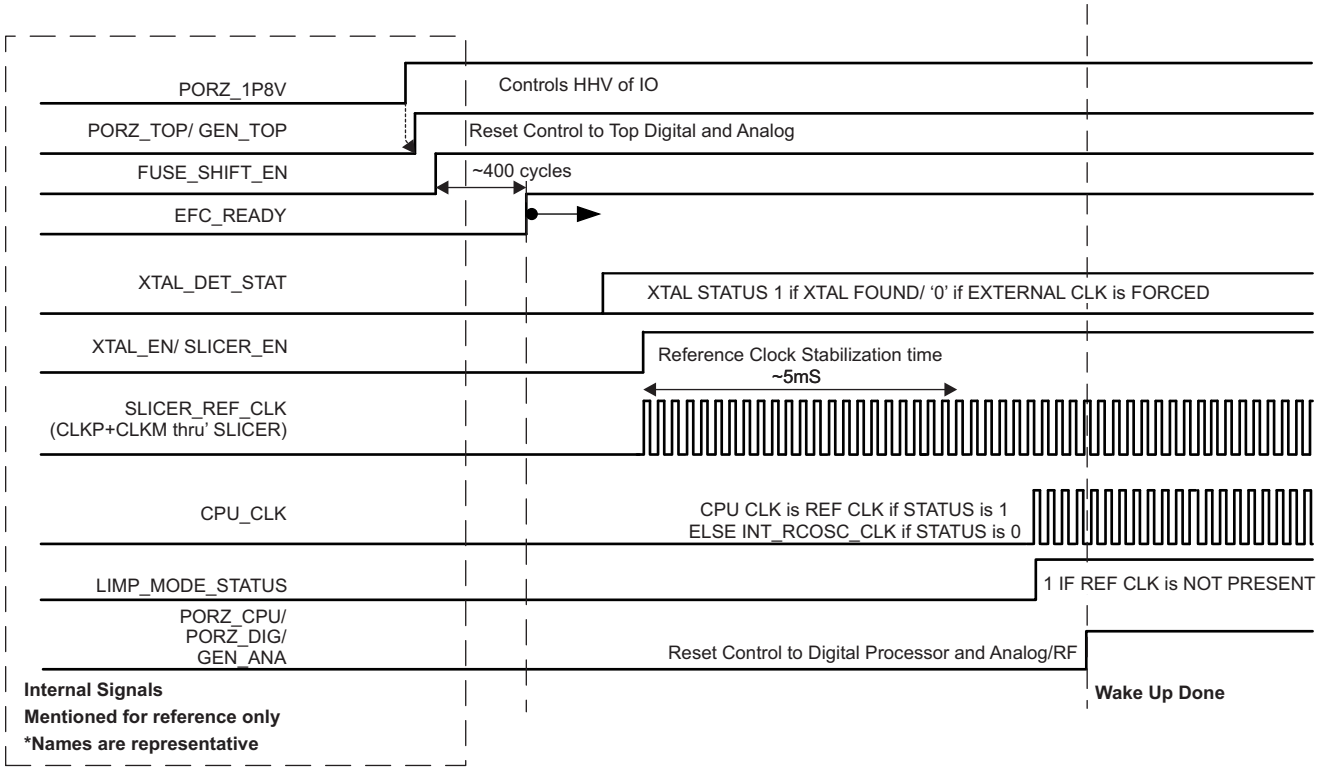


Figure 5-2. Device Wake-up Sequence

5.9.2 Input Clocks and Oscillators

5.9.2.1 Clock Specifications

An external crystal is connected to the device pins. Figure 5-3 shows the crystal implementation.

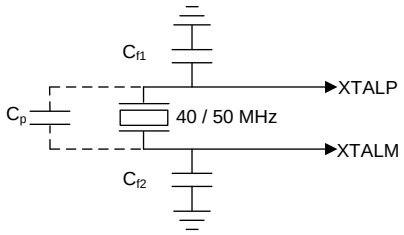


Figure 5-3. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-3, should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

Table 5-6 lists the electrical characteristics of the clock crystal.

Table 5-6. Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40, 50		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		150	ºC
Frequency tolerance	Crystal frequency tolerance(1)(2)	–50		50	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

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5.9.3 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

5.9.3.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Table 5-8 and Table 5-9 assume the operating conditions stated in Table 5-7. Table 5-8, Table 5-9, and Figure 5-4 describe the timing and switching characteristics of the MibSPI transmit and receive RAM organization.

Table 5-7. SPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 5-8. SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK	25			ns
2	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	10			ns
3	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	10			ns
4	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	ns
5	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			ns

(1) The mode of operation is mode 0 (clock polarity = 0 ; clock phase = 0).

Table 5-9. SPI Slave Mode Timing Requirements (SPICLK = input, SPISIMO = input, and SPISOMI = output)

NO.			MIN	TYP	MAX	UNIT
1	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	3			ns
2	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	0			ns

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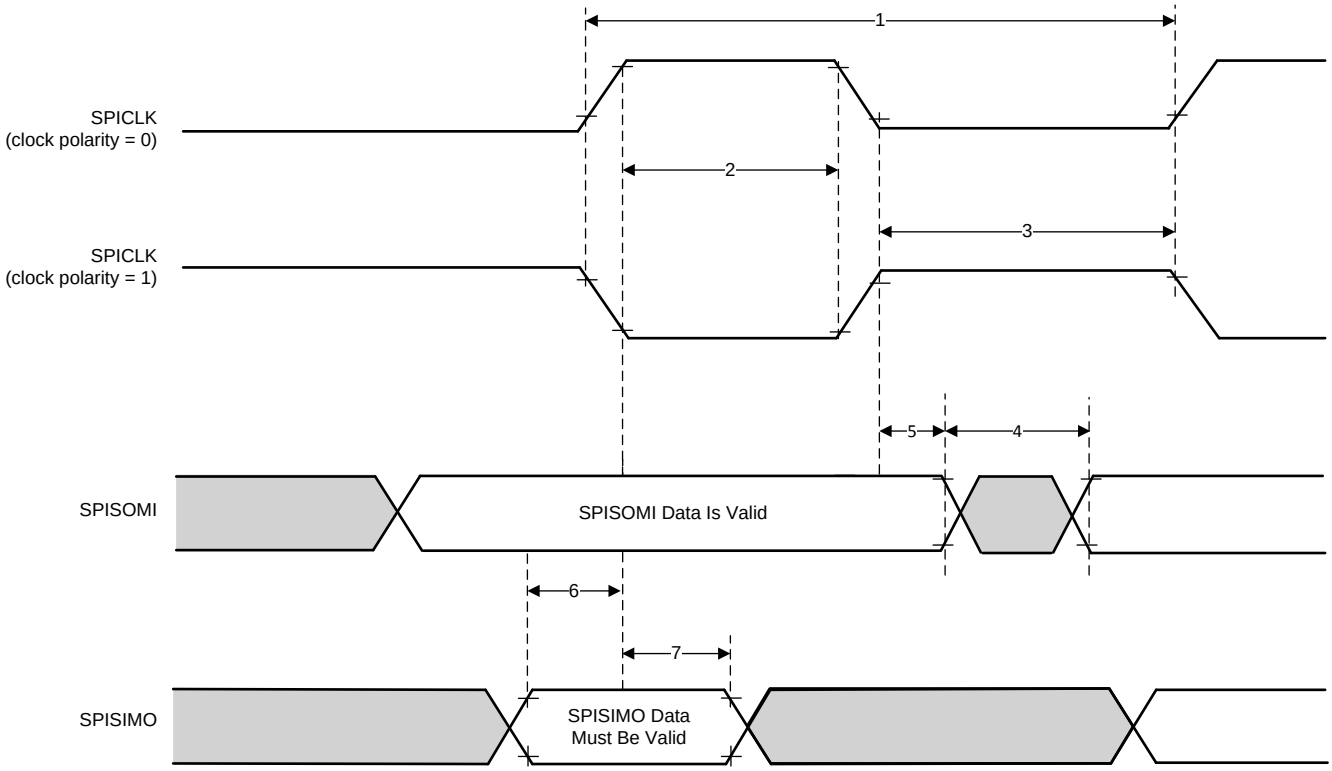

Figure 5-4. SPI Slave Mode External Timing

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5.9.3.2 Typical Interface Protocol Diagram (Slave Mode)

1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 5-5 shows the SPI communication timing of the typical interface protocol.

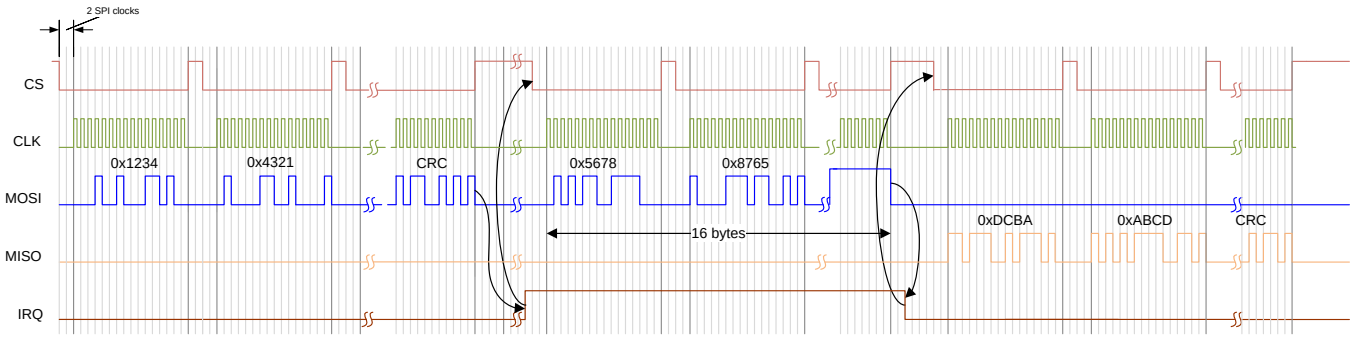

Figure 5-5. SPI Communication

5.9.4 General-Purpose Input/Output

Table 5-10 lists the switching characteristics of output timing relative to load capacitance.

Table 5-10. Switching Characteristics for Output Timing versus Load Capacitance (C_L)(1)(2)

PARAMETER		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.878	3.013	ns
			C_L = 50 pF	6.446	6.947	
			C_L = 75 pF	9.43	10.249	
t_f	Max fall time		C_L = 20 pF	2.827	2.883	ns
			C_L = 50 pF	6.442	6.687	
			C_L = 75 pF	9.439	9.873	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.307	3.389	ns
			C_L = 50 pF	6.77	7.277	
			C_L = 75 pF	9.695	10.57	
t_f	Max fall time		C_L = 20 pF	3.128	3.128	ns
			C_L = 50 pF	6.656	6.656	
			C_L = 75 pF	9.605	9.605	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

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5.9.5 Camera Serial Interface (CSI)

The CSI is a MIPI D-PHY compliant interface for connecting this device to a camera receiver module. This interface is made of four differential lanes; each lane is configurable for carrying data or clock. The polarity of each wire of a lane is also configurable. Table 5-11, Figure 5-6, Figure 5-7, and Figure 5-8 describe the clock and data timing of the CSI.

Table 5-11. CSI Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
HPTX						
$HSTX_{DBR}$	Data bit rate	(1 or 2 data lane PHY)	150		900	Mbps
		(4 data lane PHY)	150		600	
f_{CLK}	DDR clock frequency	(1 or 2 data lane PHY)	75		450	MHz
		(4 data lane PHY)	75		300	
$\Delta_{VCMTX(LF)}$	Common-level variation from 75 to 450 MHz of CSI2 clock frequency		–50		50	mVpeak
t_R and t_F	20% to 80% rise time and fall time		150			ns
					0.3	UI
LPTX DRIVER						
t_{RLP} and t_{FLP}	15% to 85% rise time and fall time				25	ns
t_{EOT} (1)	Time from start of THS-TRAIL period to start of LP-11 state				105 + 12*UI	ns
$\delta V/\delta t_{SR}$ (2)(3)(4)	Slew rate. C_{LOAD} = 0 to 5 pF				500	mV/ns
	Slew rate. C_{LOAD} = 5 to 20 pF				200	
	Slew rate. C_{LOAD} = 20 to 70 pF				100	
C_{LOAD} (2)	Load capacitance		0		70	pF
DATA-CLOCK Timing Specification						
UINOM	Nominal unit interval (1, 2, or 3 data lane PHY)		1.11		13.33	ns
	Nominal unit interval (4 data lane PHY)		1.67		13.33	
UIINST,MIN	Minimum instantaneous Unit Interval (1, 2, or 3 data lane PHY)		1.033	0.975*UINOM – 0.05		ns
	Minimum instantaneous Unit Interval (4 data lane PHY)		1.131			
TSKEW[TX]	Data to clock skew measured at transmitter		–0.15		0.15	UIINST, MIN
CSI2 TIMING SPECIFICATION						
$T_{CLK-MISS}$	Time-out for receiver to detect absence of clock transitions and disable the clock lane HS-RX.				60	ns
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated data lane has transitioned to lp mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.		60 ns + 52*UI			ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter before any associated data lane beginning the transition from LP to HS mode.		8			ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the clock lane LP-00 line state immediately before the HS-0 line state starting the HS transmission.		38		95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any clock lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.		95		300	ns

(1) With an additional load capacitance CCM of 0 to 60 pF on the termination center tap at RX side of the lane
(2) While driving C_{LOAD}. Load capacitance includes 50 pF of transmission line capacitance, and 10 pF each for TX and RX.
(3) When the output voltage is from 15% to 85% of the fully settled LP signal levels
(4) Measured as average across any 50 mV segment of the output signal transition

Table 5-11. CSI Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$T_{CLK-TERM-EN}$	Time for the clock lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN		38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state before starting the clock.	300			ns
$T_{D-TERM-EN}$	Time for the data lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN		35 ns + 4*UI	ns
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLKTRAIL}$, to the start of the LP-11 state following a HS burst.			105 ns + n*12*UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission	40 + 4*UI		85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any data lane HS transitions, starting from the beginning of $T_{HSPREPARE}$. The HS receiver shall ignore any data lane transitions before the minimum value, and he HS receiver shall respond to any data lane transitions after the maximum value.	85 ns + 6*UI		145 ns + 10*UI	ns
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the data lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI) (5)(6)			ns
T_{LPX}	Transmitted length of any low-power state period	50 (7)			ns

(5) If a > b then max(a, b) = a, otherwise max(a, b) = b.
(6) Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode
(7) T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

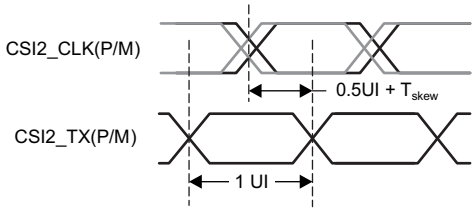

Figure 5-6. Clock and Data Timing in HS Transmission

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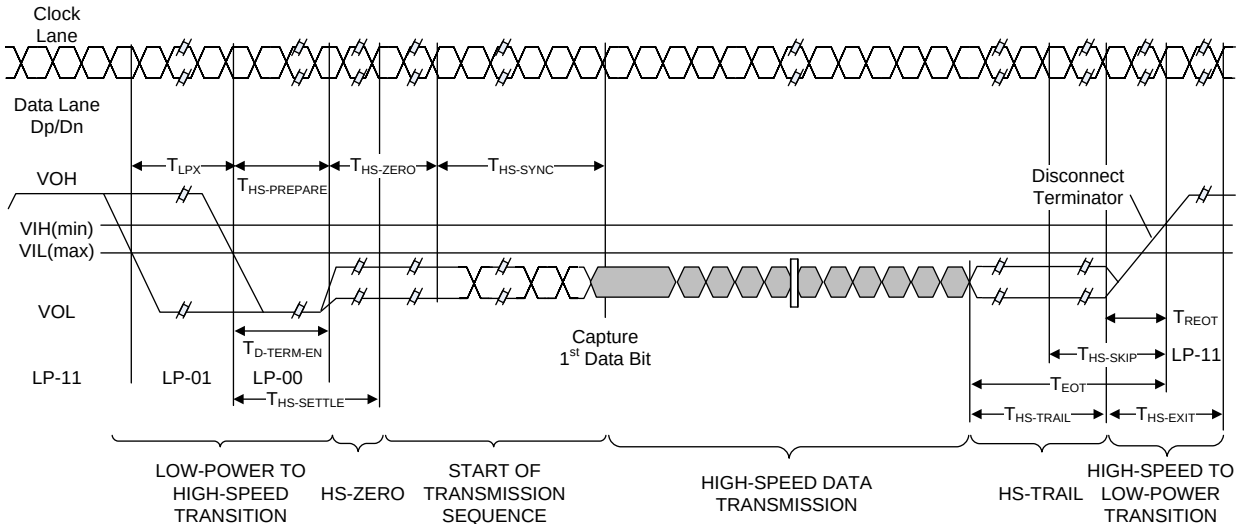


Figure 5-7. High-Speed Data Transmission Burst

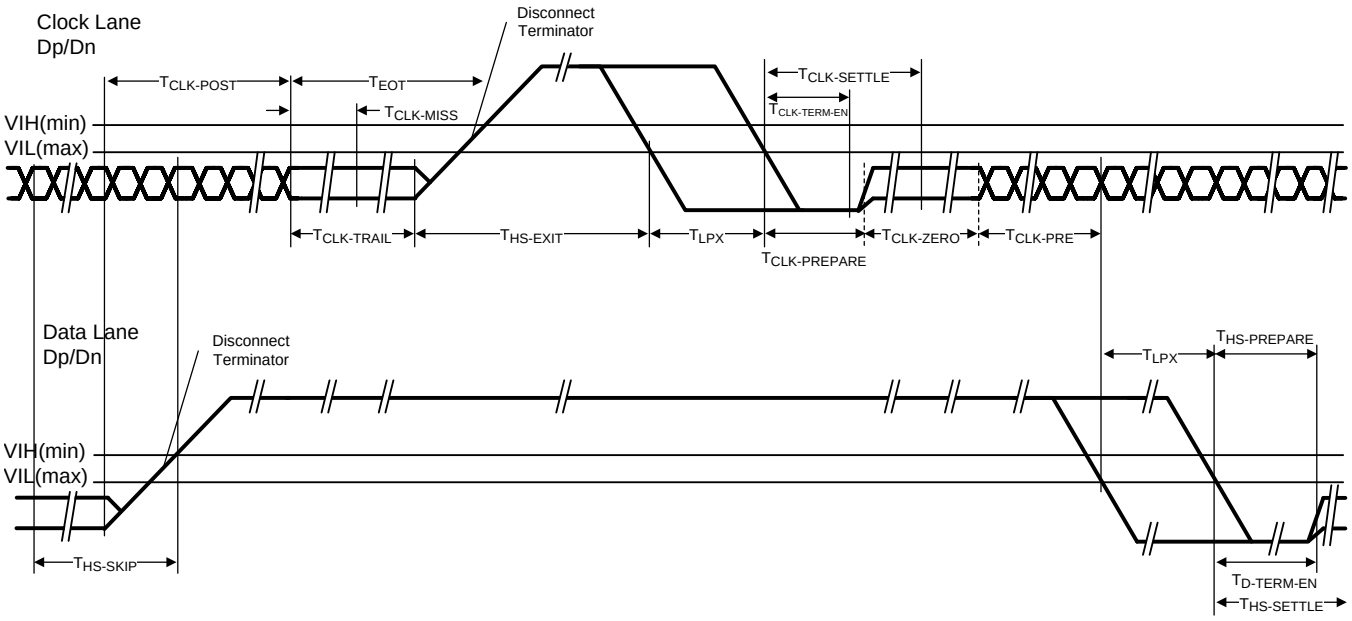


Figure 5-8. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

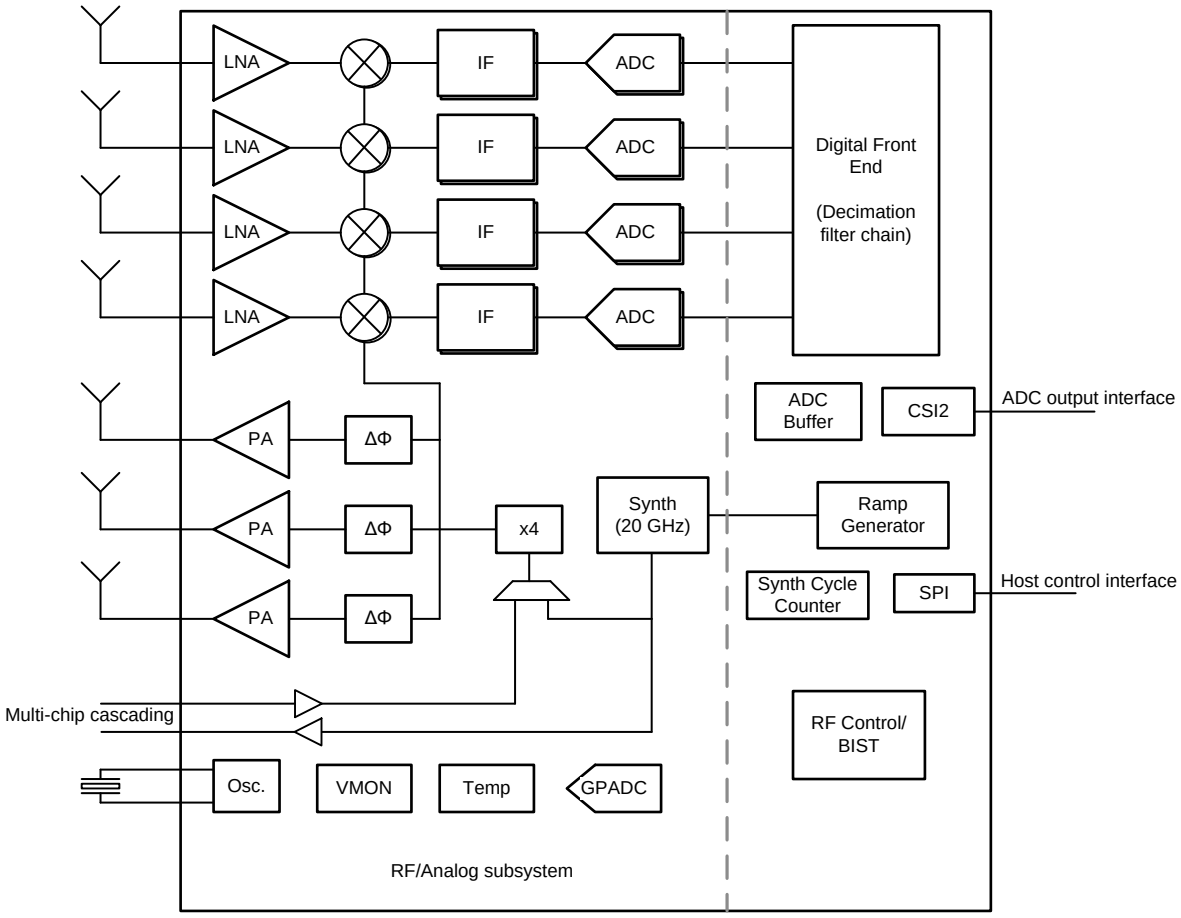
ADVANCE INFORMATION

6 Detailed Description

6.1 Overview

The AWR1243 device is a single-chip highly integrated 77-GHz transceiver and front end that includes three transmit and four receive chains. The device can be used in long-range automotive radar applications such as automatic emergency braking and automatic adaptive cruise control. The AWR1243 has extremely small form factor and provides ultra-high resolution with very low power consumption. This device, when used with the TDA3X or TD2X, offers higher levels of performance and flexibility through a programmable digital signal processor (DSP); thus addressing the standard short-, mid-, and long-range automotive radar applications.

6.2 Functional Block Diagram



6.3 Subsystems

6.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

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6.3.1.1 Clock Subsystem

The AWR1243 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76- to 81-GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The output of the RF synthesizer is available at the device pin boundary for multichip cascaded configuration. The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 6-1 describes the clock subsystem.

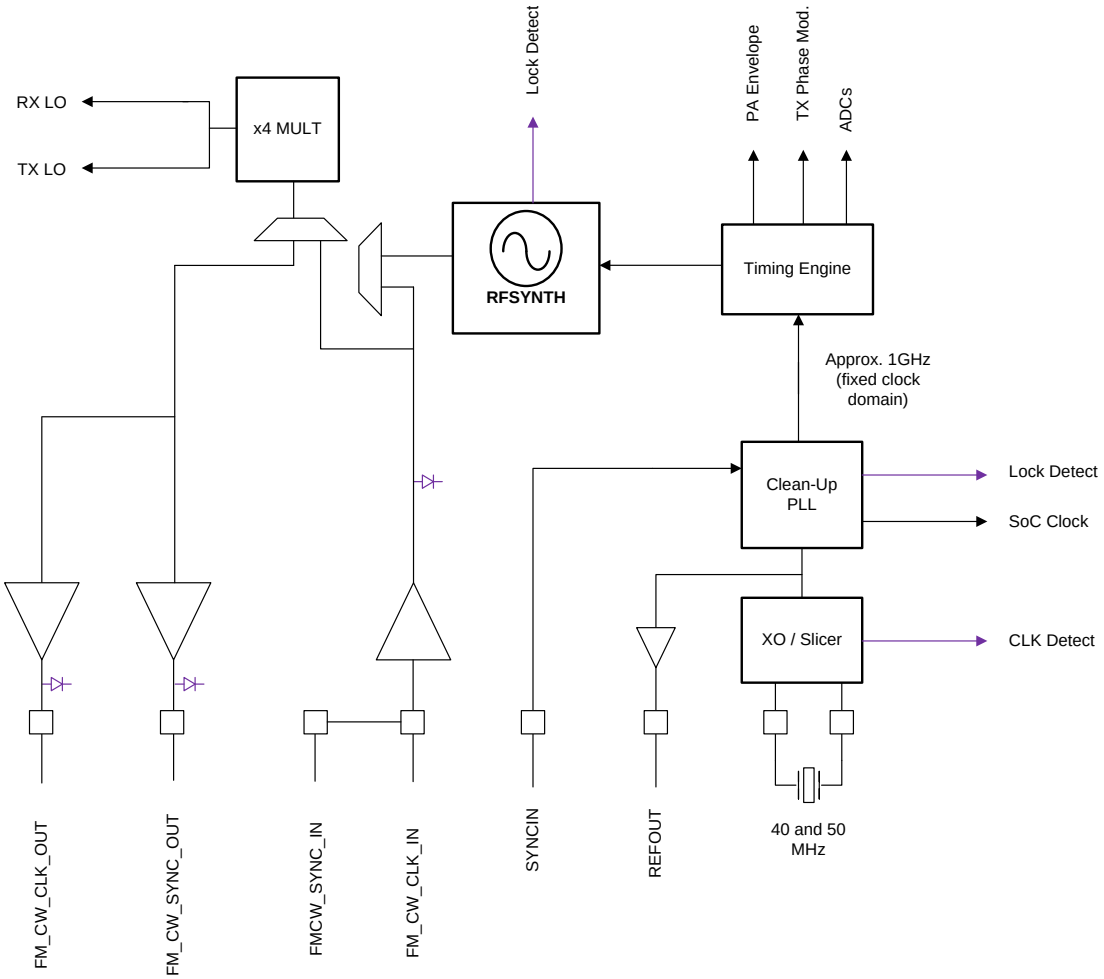


Figure 6-1. Clock Subsystem

6.3.1.2 Transmit Subsystem

The AWR1243 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. A maximum of two transmit chains can be operational at the same time. However all three chains can be operated together in a time-multiplexed fashion. The device supports binary phase modulation for MIMO radar and interference mitigation.

Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 6-2 describes the transmit subsystem.

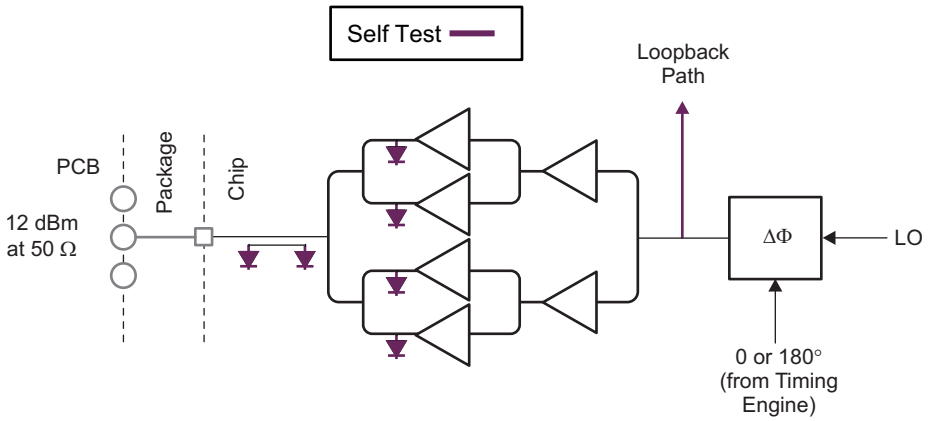


Figure 6-2. Transmit Subsystem (Per Channel)

6.3.1.3 Receive Subsystem

The AWR1243 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the AWR1243 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The AWR1243 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 350 kHz and can support bandwidths up to 15 MHz.

Figure 6-3 describes the receive subsystem.

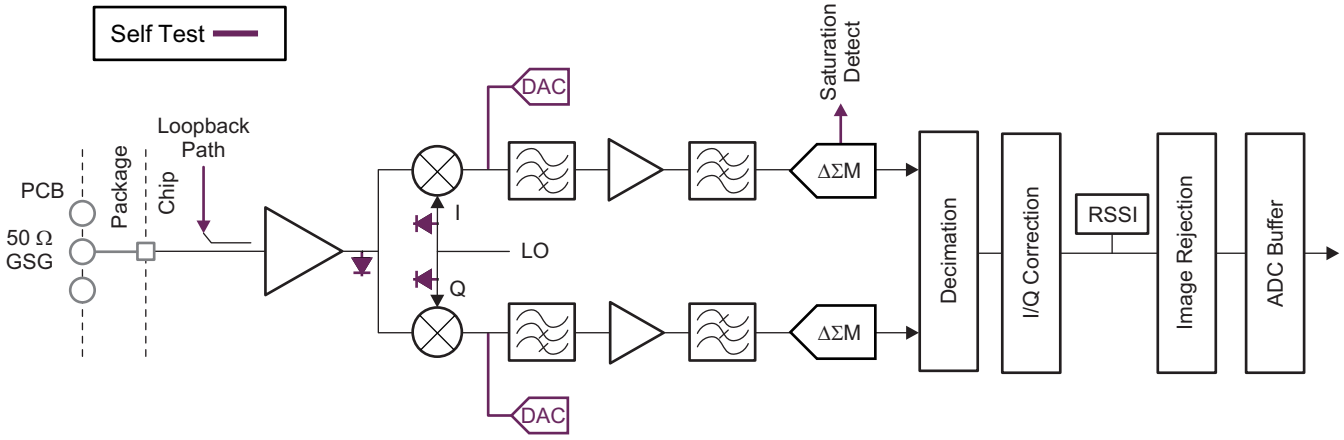


Figure 6-3. Receive Subsystem (Per Channel)

ADVANCE INFORMATION

6.3.2 Host Interface

The AWR1243 device communicates with the host radar processor over the following main interfaces:

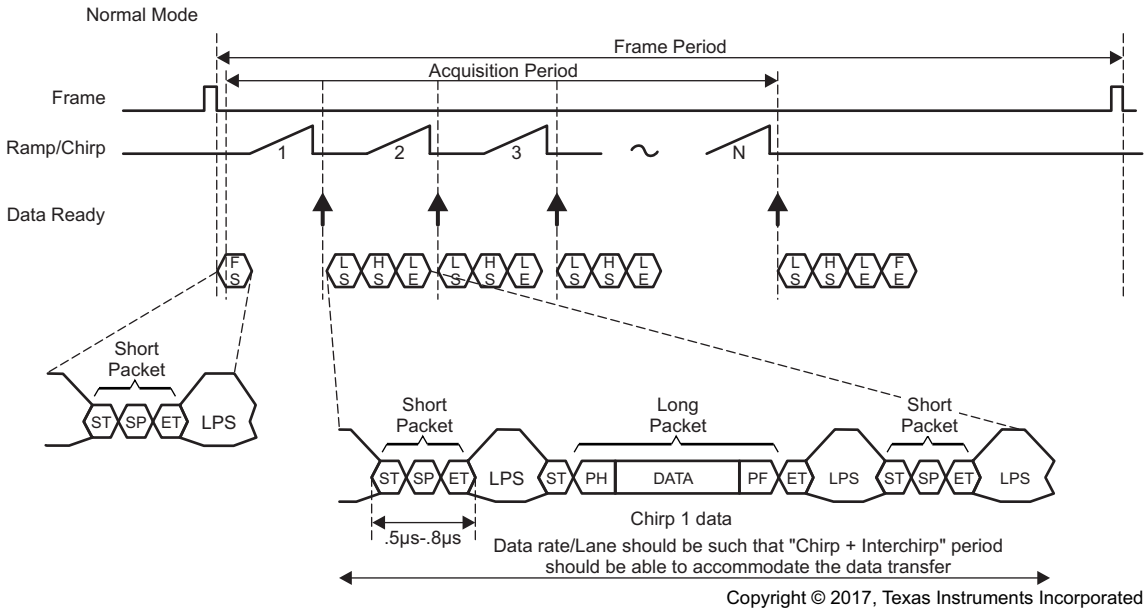
- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (slave) for host control. All radio control commands (and response) flow through this interface.
- Data – High-speed serial port following the MIPI CSI2 format. Four data and one clock lane (all differential). Data from different receive channels can be multiplexed on a single data lane to optimize board routing. This is a unidirectional interface used for data transfer only.
- Reset – Active-low reset for device wakeup from host
- Out-of-band interrupt
- Error – Used for notifying the host in case the radio controller detects a fault

6.4 Other Subsystems

6.4.1 A2D Data Format Over CSI2 Interface

The AWR1243 device uses MIPI D-PHY / CSI2-based format to transfer the raw A2D samples to the external MCU. This is shown in Figure 6-4.

- Supports four data lanes
- CSI-2 data rate scalable from 150 Mbps to 900 Mbps per lane (If four lanes are used simultaneously then the maximum data rate supported is 600 Mbps per lane)
- Virtual channel based
- CRC generation



Frame **S**tart – CSi2 VSYNC Start Short Packet
Line **S**tart – CSI2 HSYNC Start Short Packet
Line **E**nd – CSI2 HSYNC End Short Packet
Frame **E**nd – CSi2 VSYNC End Short Packet

Figure 6-4. CSI-2 Transmission Format

The data payload is constructed with the following three types of information:

- Chirp profile information
- The actual chirp number
- A2D data corresponding to chirps of all four channels
  - Interleaved fashion
- Chirp quality data (configurable)

The payload is then split across the four physical data lanes and transmitted to the receiving D-PHY. The data packet packing format is shown in Figure 6-5

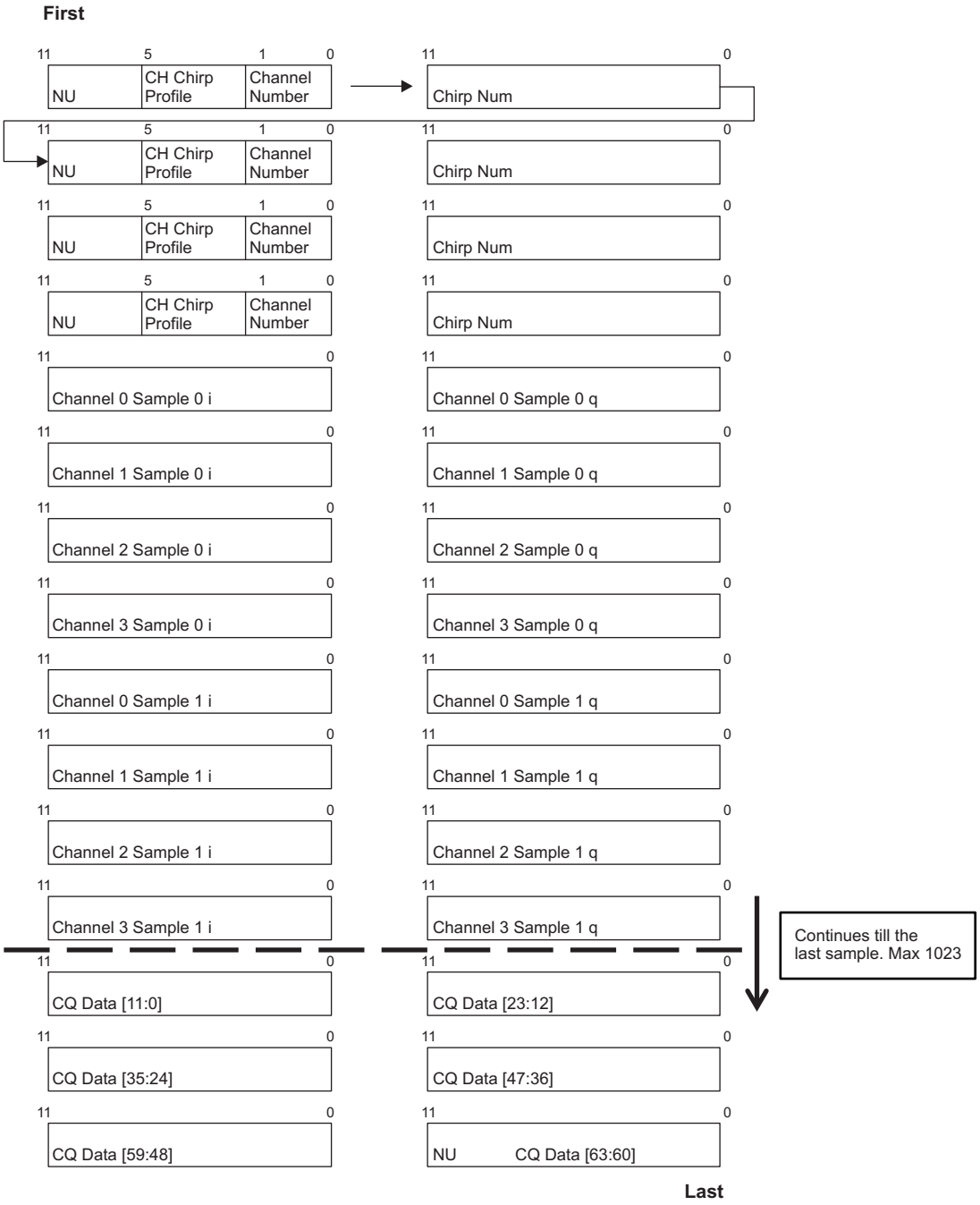


Figure 6-5. Data Packet Packing Format for 12-Bit Complex Configuration

ADVANCE INFORMATION

7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

A typical application addresses the standard short-, mid-, long-range, and high-performance imaging radar applications with this radar front end and external programmable MCU. Figure 7-1 shows a short-, medium-, or long-range radar application.

7.2 Short-, Medium-, and Long-Range Radar

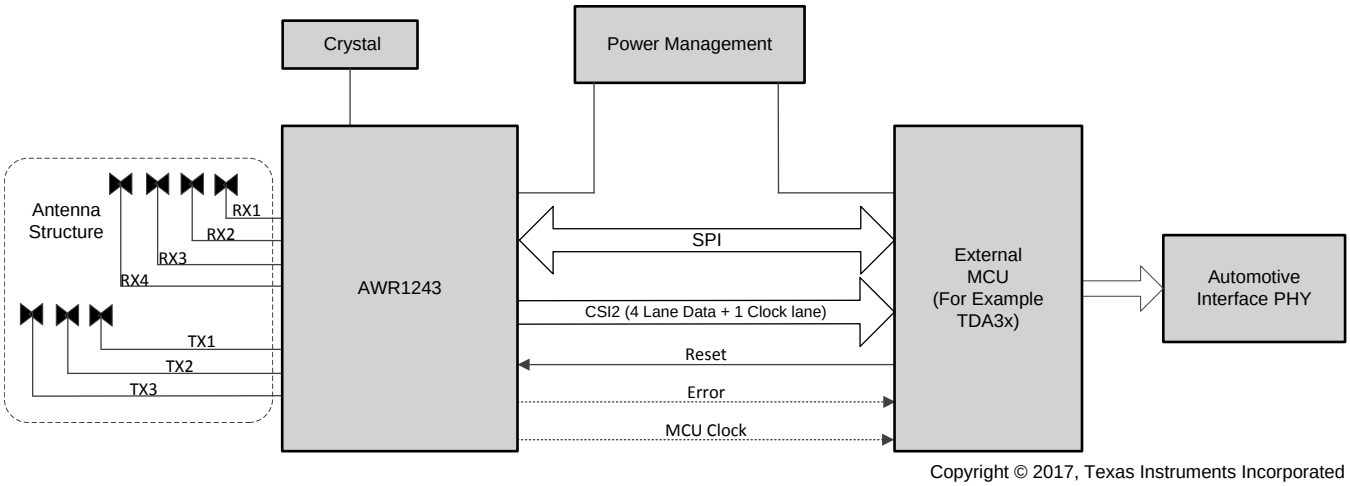


Figure 7-1. Short-, Medium-, and Long-Range Radar

7.3 Reference Schematic

Figure 7-2 and Figure 7-3 show the reference schematic and low-noise LDO circuitry for the AWR1243 device.

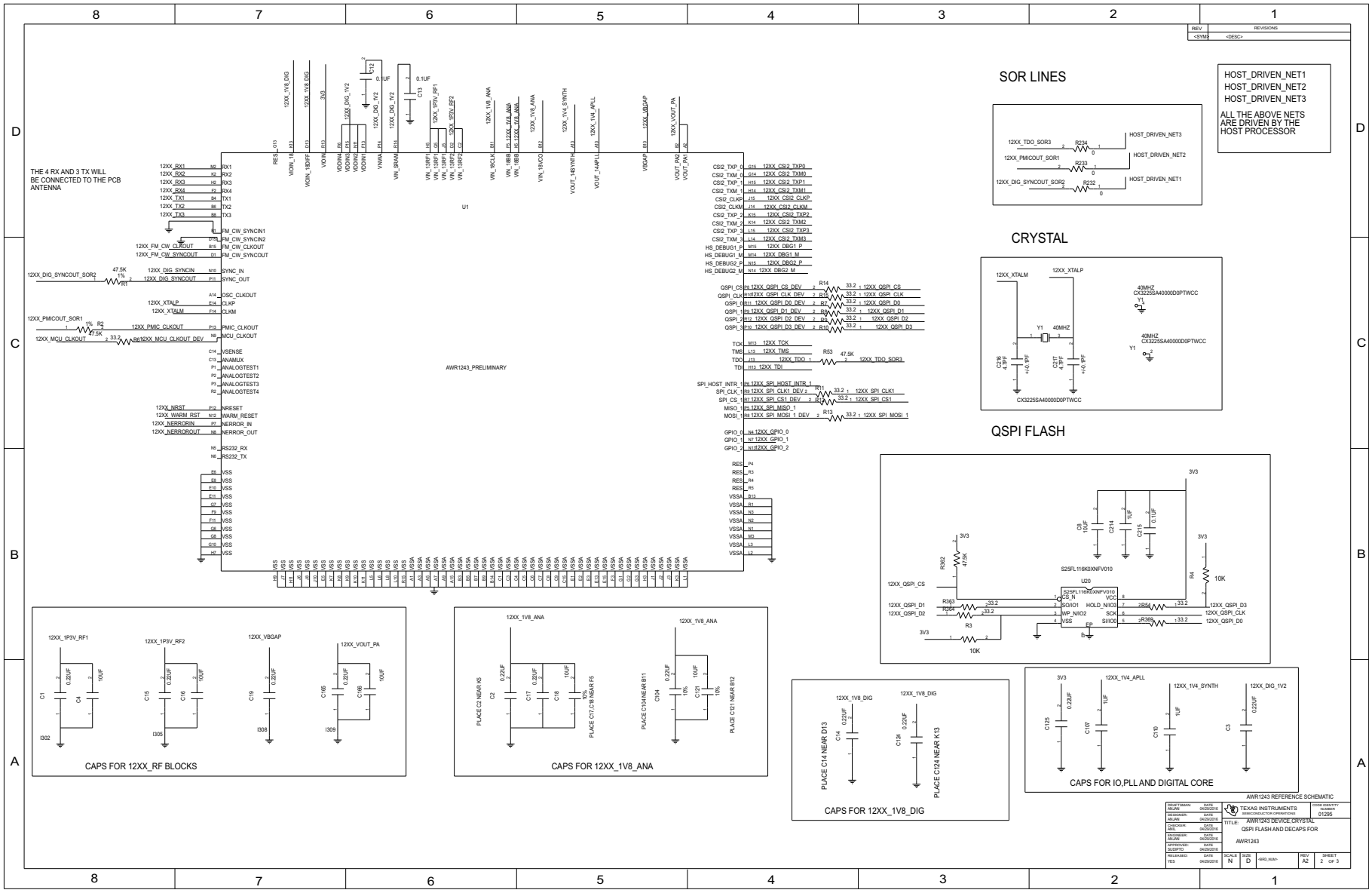


Figure 7-2. AWR1243 Reference Schematic

ADVANCE INFORMATION

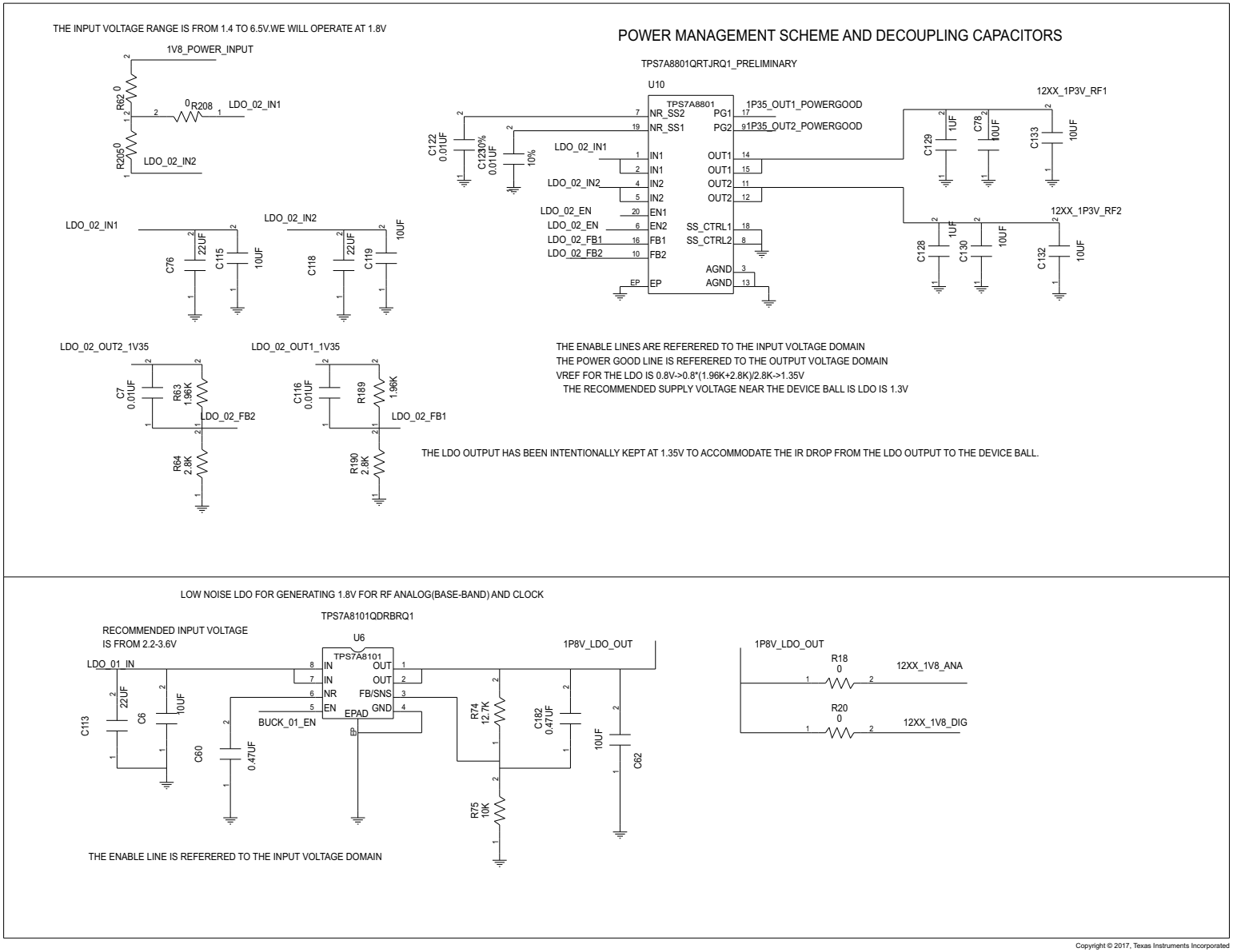


Figure 7-3. AWR1243 Low-Noise LDO Circuitry

7.4 Layout

The top layer routing, top layer closeup, and bottom layer routing are shown in Figure 7-4, Figure 7-5, and Figure 7-6, respectively.

7.4.1 Layout Guidelines

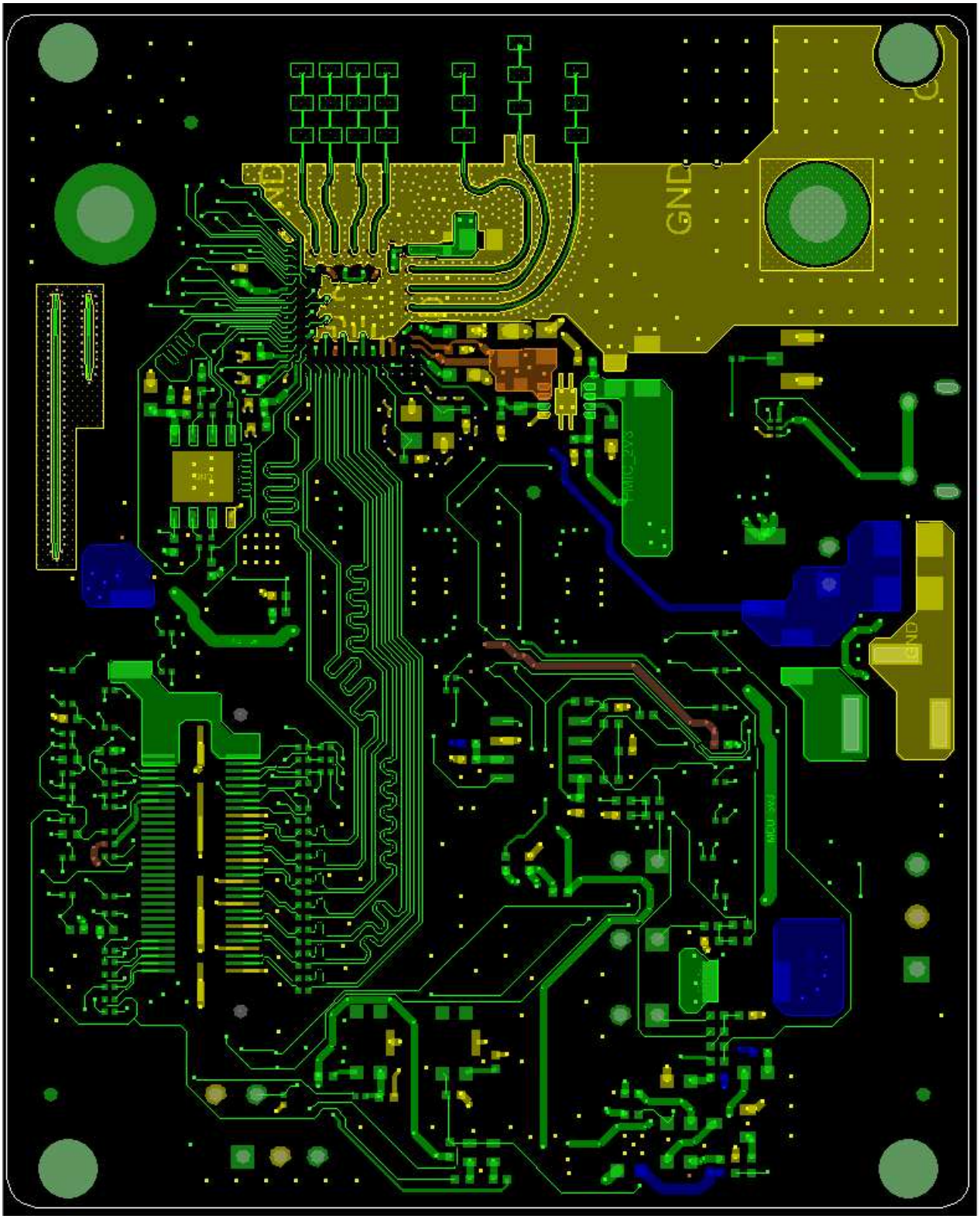


Figure 7-4. Top Layer Routing

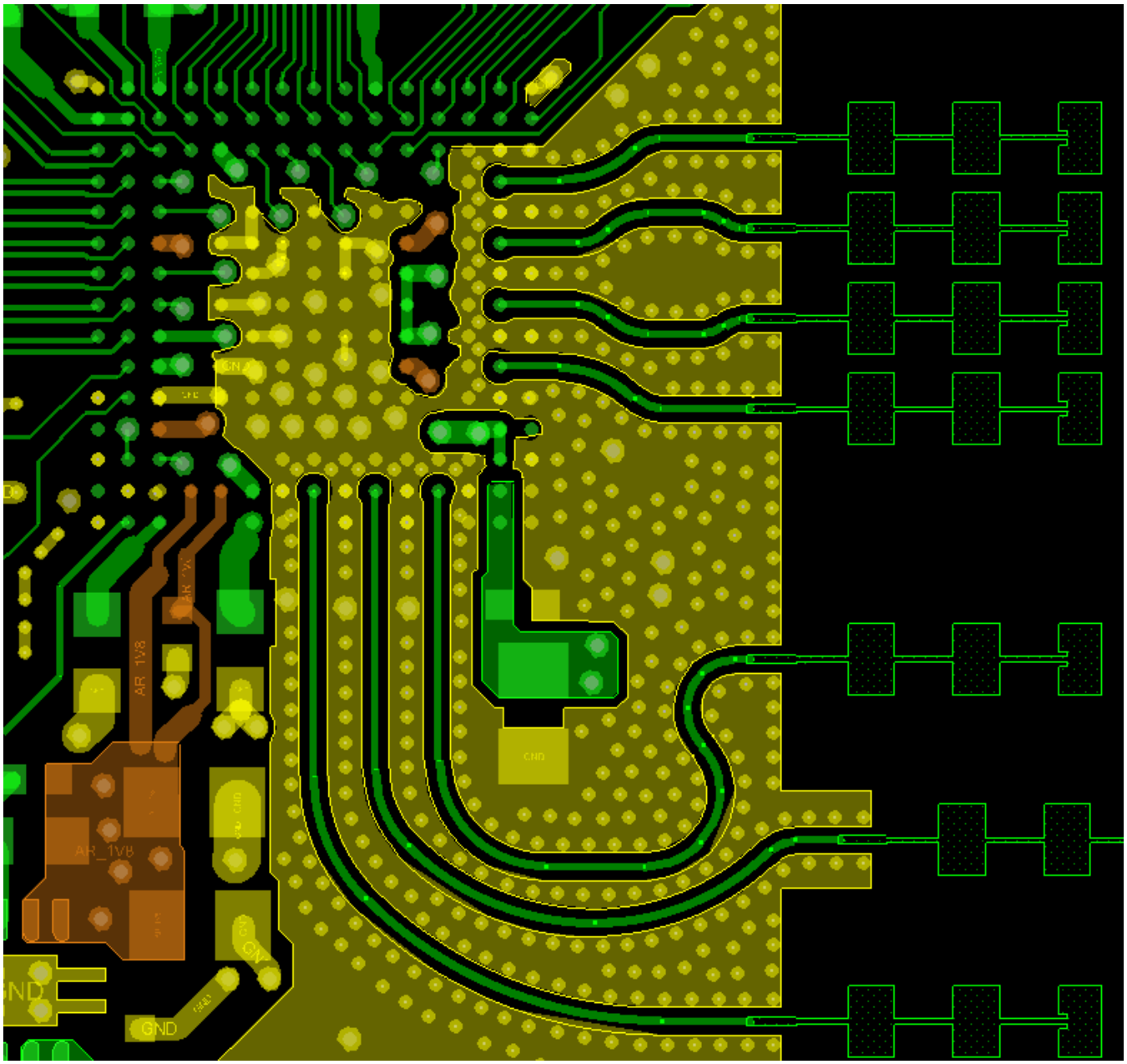


Figure 7-5. Top Layer Routing Closeup

ADVANCE INFORMATION

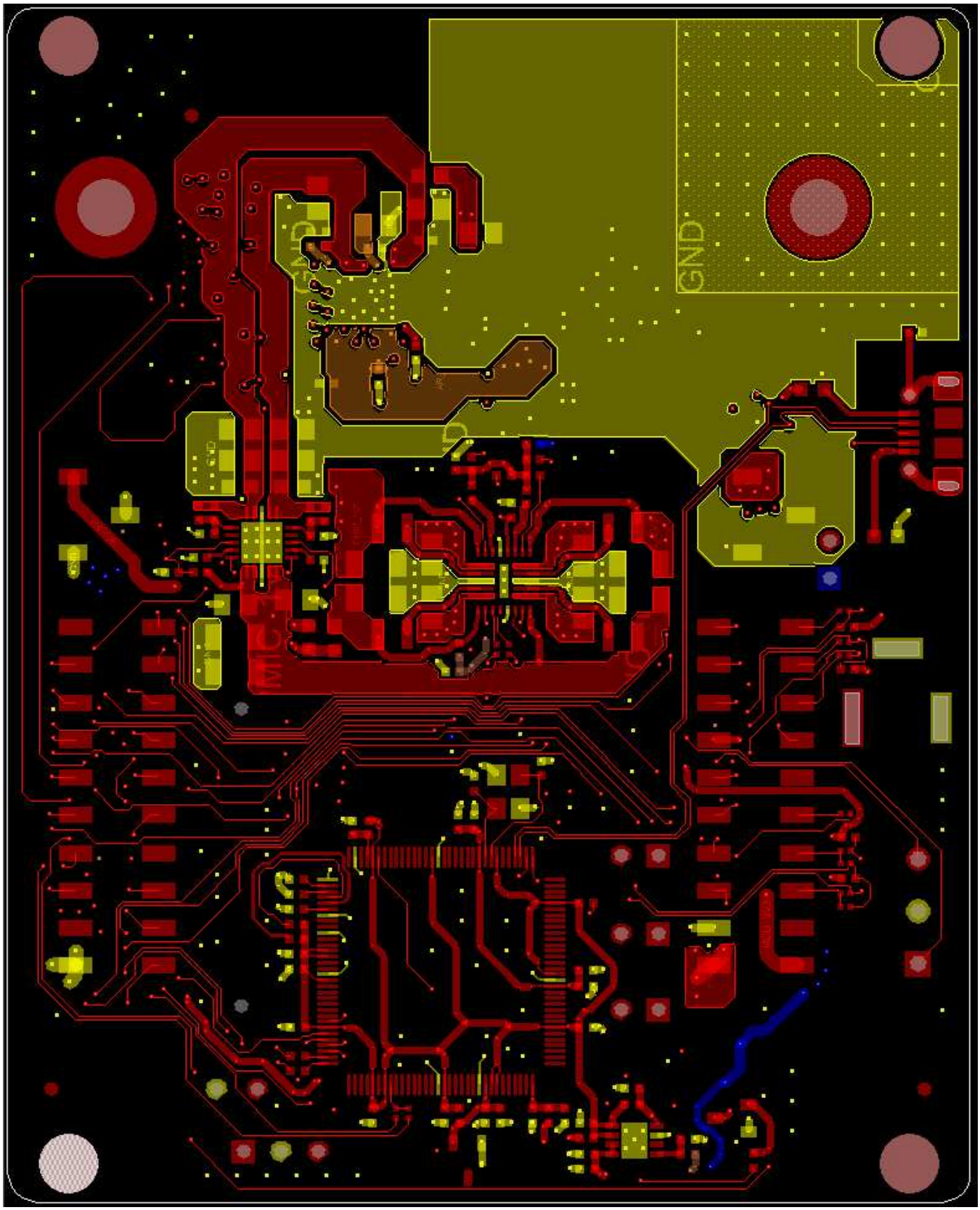
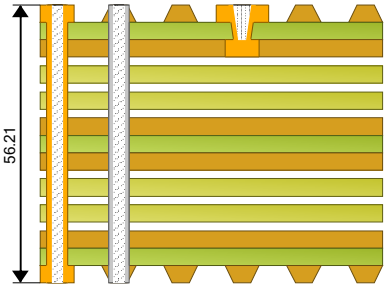


Figure 7-6. Bottom Layer Routing

7.4.2 Stackup Details



Layer	Stack up	Description	Type	Base Thickness	Processed Thickness	εr	Copper Coverage
1				0.689	2.067		100.000
		Rogers 4835 4mil coreH/1 Low Pro	Rogers 4835	4.000	4.000	3.480	
2				1.260	1.260		73.000
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.830	3.700	
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.830	3.700	
3				1.260	1.260		69.000
		Iteq IT180A 28 mil core 1/1	FR4	28.000	28.000	4.280	
4				1.260	1.260		48.000
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.691	3.700	
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.691	3.700	
5				1.260	1.260		72.000
		Iteq IT180A 4 mil core 1/H	FR4	4.000	4.000	3.790	
6				0.689	2.067		100.000

ADVANCE INFORMATION

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AWR1243*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161), the temperature range (for example, blank is the default commercial temperature range). Figure 8-1 provides a legend for reading the complete device name for any *AWR1243* device.

For orderable part numbers of *AWR1243* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *AWR1243 Device Errata Silicon Revision 1.0 and 2.0*.

ADVANCE INFORMATION

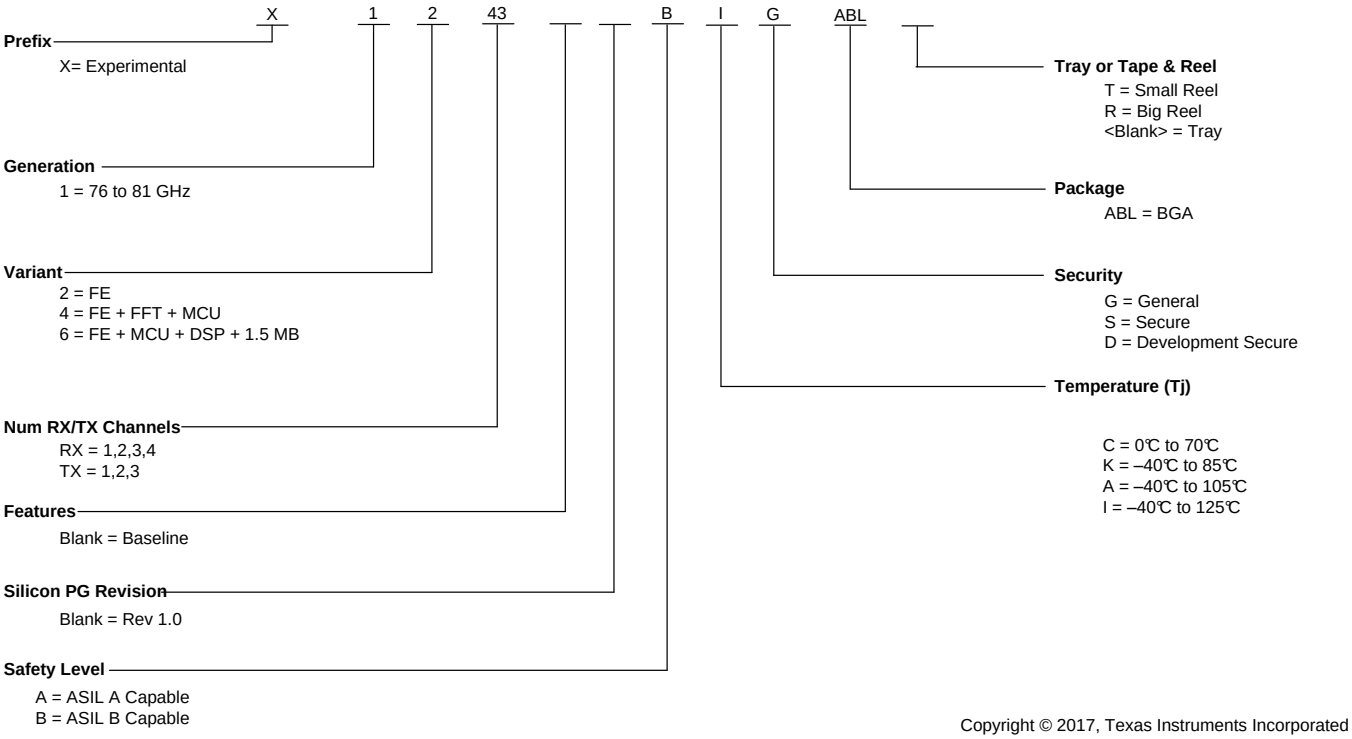


Figure 8-1. Device Nomenclature

8.2 Tools and Software

Models

AWR1243 BSDL Model Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

AWR1x43 IBIS Model IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

AWR1243 Checklist for Schematic Review, Layout Review, Bringup/Wakeup A set of steps in spreadsheet form to select system functions and pinmux options. Specific EVM schematic and layout notes to apply to customer engineering. A bringup checklist is suggested for customers.

8.3 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (AWR1243). In the upper right-hand corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

Errata

AWR1243 Device Errata Describes known advisories, limitations, and cautions on silicon and provides workarounds.

ADVANCE INFORMATION

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

CAUTION

The following package information is subject to change without notice.

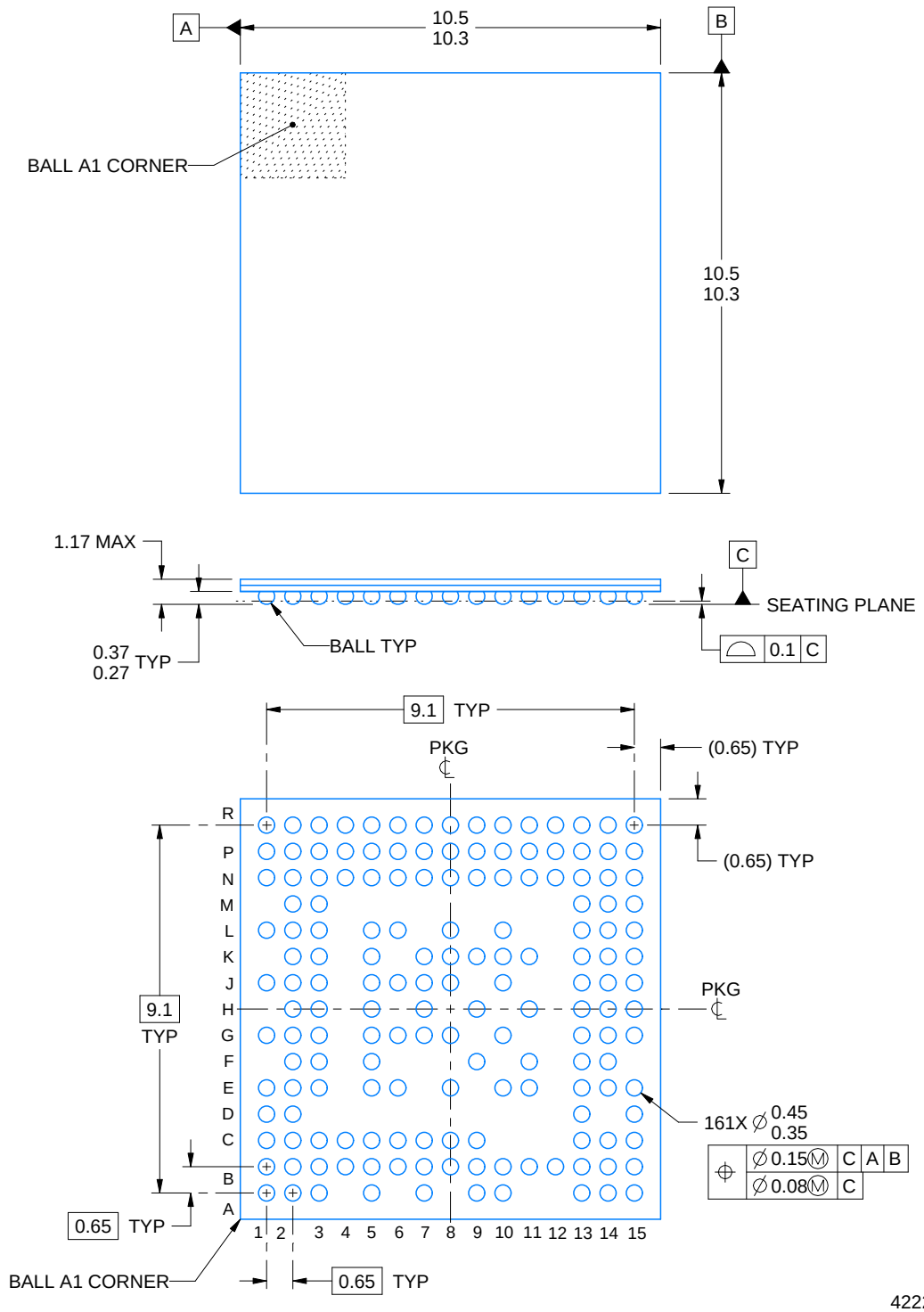
ADVANCE INFORMATION

PACKAGE OUTLINE

ABL0161A

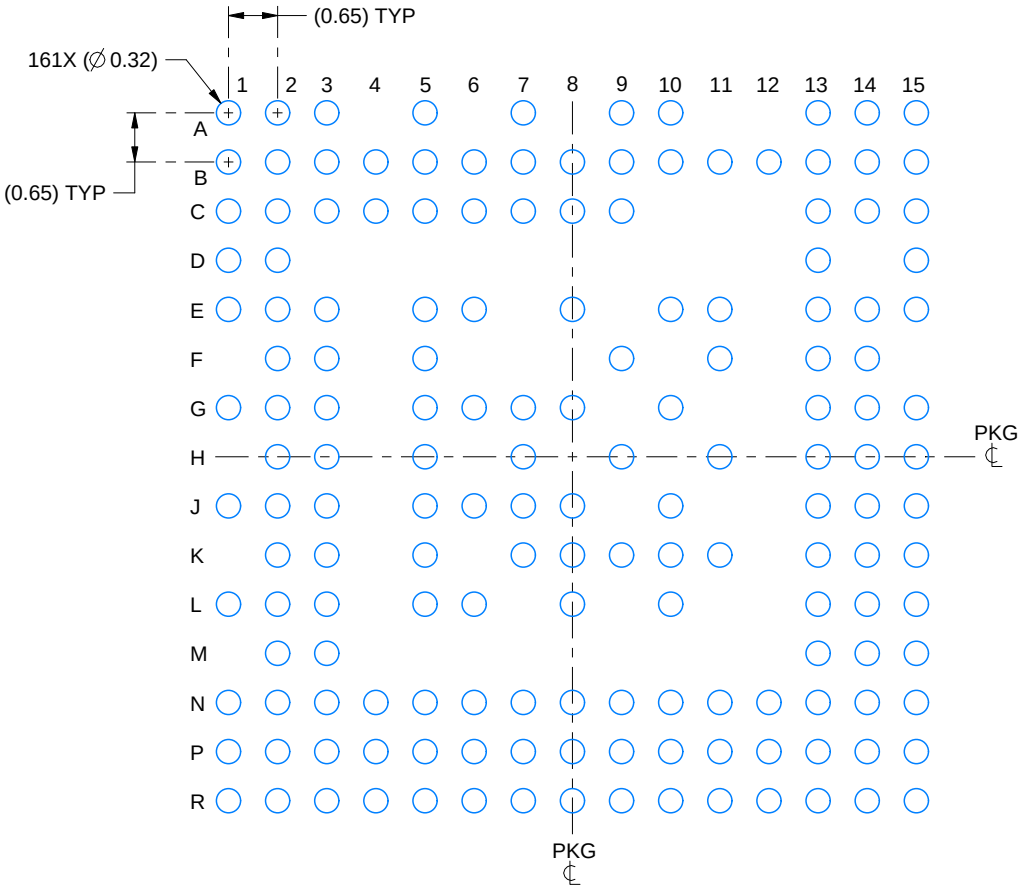
FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY

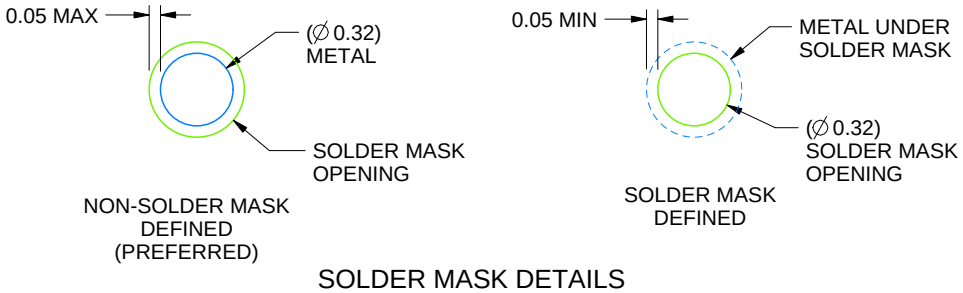


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:10X

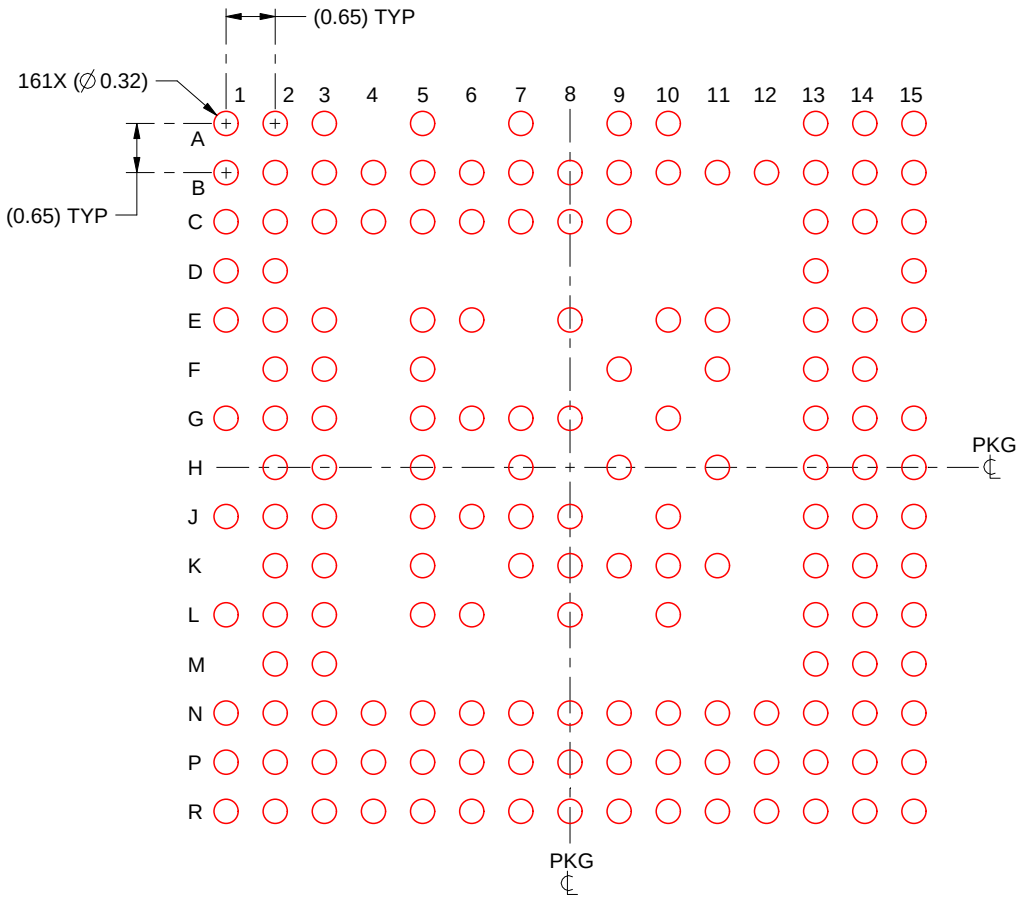


SOLDER MASK DETAILS
NOT TO SCALE

4222493/B 10/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4222493/B 10/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AWR1243FBIGABLQ1	PREVIEW	FC/CSP	ABL	161	1	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 125	AWR1243 IG 964FC C 964FC ABL	
AWR1243FBIGABLRQ1	PREVIEW	FC/CSP	ABL	161	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 125	AWR1243 IG 964FC C 964FC ABL	
X1243BIGABL	ACTIVE	FC/CSP	ABL	161	1	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265