AN88619

PSoC® 4 Hardware Design Considerations

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Software Version: N/A

Related Documentation: For a complete list, click here.

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN88619.

AN88619 shows you how to design a hardware system around a PSoC® 4 device. Subjects include package selection, power, clocking, reset, I/O usage, programming and debugging interfaces, and analog module design tips. Also included are instructions on how to use PSoC Creator™ to configure the device for the hardware environment.

Contents

1 Introduction

PSoC 4 is a powerful, programmable microcontroller with an ARM® Cortex™-M0 CPU. It provides capability and flexibility for analog and digital applications beyond what traditional MCUs offer.

PSoC 4100, 4200, 4100M and 4200M are four families of PSoC 4 that have balanced analog and digital performance. This application note documents considerations for hardware design, including package, power, clocking, reset, I/O use, programming, debugging, and design tips for analog modules for these family of devices. In addition, it discusses good board layout techniques, which are particularly important for precision analog applications.

The PSoC 4 device must be configured to work in its hardware environment, which is accomplished through the use of PSoC Creator.

This application note assumes that you have some basic familiarity with PSoC 4 devices and the PSoC Creator integrated design environment (IDE). If you are new to PSoC 4, refer to AN79953 – Getting Started with PSoC 4. If you are new to PSoC Creator, see the PSoC Creator home page.

2 Package Selection

One of the first decisions you must make for your PCB is which package you will use. Several considerations drive this decision, including the number of PSoC device pins required, PCB and product size, PCB design rules, and thermal and mechanical stresses.

PSoC 4100/4200 devices are available in three packages: 44-TQFP, 40-QFN, and 28-SSOP. Following are some package selection criteria:

- **44-TQFP:** This package provides 36 I/O pins. It is easier to route signals due to a large pitch and the open area below the part. Disadvantages are a larger package and lower mechanical stability.
- **40-QFN:** This package provides 34 I/O pins. It is much smaller than the other two packages. The central exposure pad gives the package the best heat dispersion performance and mechanical stability. Disadvantages are that it is more difficult to route signals due to the center pad. For more information, see AN72845 – Design Guidelines for QFN Packaged Devices.
- **28-SSOP:** This package provides 24 I/O pins and has the same advantages and disadvantages as the 44-TQFP package.

  PSoC 4100M/4200M devices are available in 64-TQFP (both 0.5-mm and 0.8-mm pitch), 48-TQFP, and 68QFN packages.

- 64-TQFP: This package provides 51 I/O pins .It is easier to route signals due to a large pitch and the open area below the part. Disadvantages are a larger package and lower mechanical stability.
- 48-TQFP: This package provides 38 I/O pins. It is smaller than 64-TQFP, but still provides better routability than QFN parts.
- 68-QFN: This package provides 55 I/O pins. It is much smaller than the other two packages. The central exposure pad gives the package the best heat dispersion performance and mechanical stability. Disadvantages are that it is more difficult to route signals due to the center pad.

As a design reference, see the knowledge base article KBA89265, which contains PSoC 4 schematics and PCB libraries. Please note that you may need to adjust or modify the libraries slightly when you apply them in your hardware design. Cypress takes no responsibility for issues related to use of the libraries.

3 Power

PSoC 4 can be powered by a single supply with a wide voltage range, from 1.71 V to 5.5 V. As listed in Table 1, it has separate power domains for analog and digital modules. V_{DDA} is the analog power supply pin, V_{SSA} is the analog ground pin, V_{DDD} and V_{CCD} are the digital power supply pins, V_{DDIO} is the power supply for I/Os, and V_{SS} is the digital ground pin. Note that V_{DDIO} is only available in certain device families / packages. I/Os are powered from V_{DDD} for devices without a V_{DDIO} pin.

Table 1. PSoC 4 Power Domains

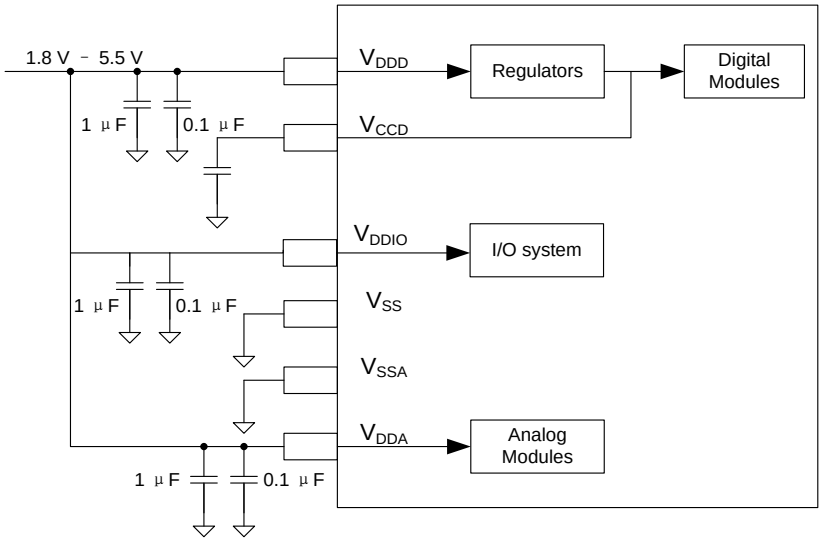
Power Domain	Associated Pins
Analog	V_{DDA}, V_{SSA}
Digital	V_{DDD}, V_{CCD}, V_{SS}
I/O	V_{DDIO}

Note: In the 28-SSOP package, V_{DDA} and V_{DDD} are combined into a single V_{DDD} pin, and V_{SSA} and V_{SS} are combined into a single V_{SS} pin.

3.1 Power Pin Connections

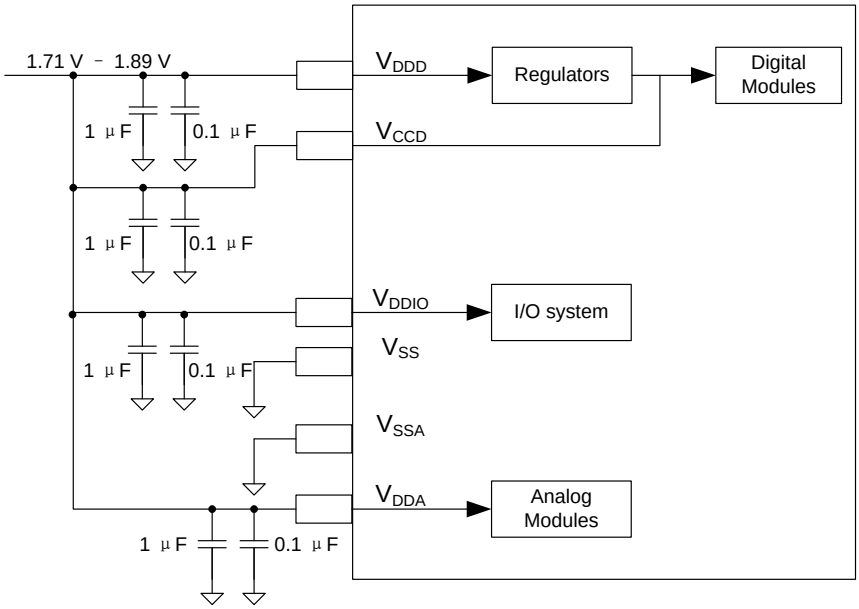
PSoC 4 devices can be powered in regulated or unregulated mode. Power pin connections for these two modes are illustrated in Figure 1 and Figure 2 on page 3. In regulated mode, the internal regulators convert V_{DDD} input to the power supply for the digital domain. Voltages at the V_{DDD} pins can be from 1.8 V to 5.5 V. Outputs of the regulators are also routed to V_{CCD}. Do not connect any external load to V_{CCD} except a capacitor, as Figure 1 shows.

Figure 1. PSoC 4 Single Power Supply Rail for Analog and Digital: Regulated Mode



You can also power PSoC 4100/4200 in unregulated mode, as Figure 2 shows. Note that certain packages have more than one V_{DDD}, V_{DDA}, and V_{DDIO} pin. Each pin must have its own decoupling capacitors. The V_{CCD} pin is directly powered. Its power must be kept within 1.71 V to 1.89 V. The V_{DDD} pins must be tied to the V_{CCD} pin. The unused regulators can be disabled by setting the EXT_VCCD bit in the PWR_CONTROL register to reduce power consumption. For more information, refer to the PSoC 4 device datasheets, Architecture Technical Reference Manual (TRM), and Registers TRM.

Figure 2. PSoC 4 Single Power Supply Rail for Analog and Digital: Unregulated Mode



In both modes, to suppress power supply noise, connect one 0.1-µF and one 1-µF ceramic decoupling capacitor to each power supply pin. The PCB trace between the pin and the capacitors should be as short as possible. For more information, see Appendix A – PCB Layout Tips.

Note: It is a good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (V_{DDD}, V_{DDA}, V_{DDIO}, or V_{CCD} in Figure 1 and Figure 2) is a significant percentage of the rated working voltage.

You can use a single power supply rail for digital power and analog power, which helps to simplify the power design in your board. To get better analog performance in a mixed-signal circuit design, use separate power supply rails for the digital power and the analog power. In this case, the voltage at the V_{DDA} pin must always be greater than or equal to the voltage at the V_{DDD} pin. For more mixed-signal circuit design techniques, see AN57821 – PSoC Mixed-Signal Circuit Board Layout Considerations

Proper use and layout of capacitors and ferrite beads help to improve EMC performance. For more information, see AN80994 – PSoC 3, PSoC 4, and PSoC 5LP EMC Best Practices and Recommendations.

The Cypress PSoC 4 kit web pages (CY8CKIT-042, CY8CKIT-049, and CY8CKIT-044) provide schematics and bills of material (BOMs) that give good examples of how to incorporate PSoC 4 into board schematics. For more information, see Related Documents.

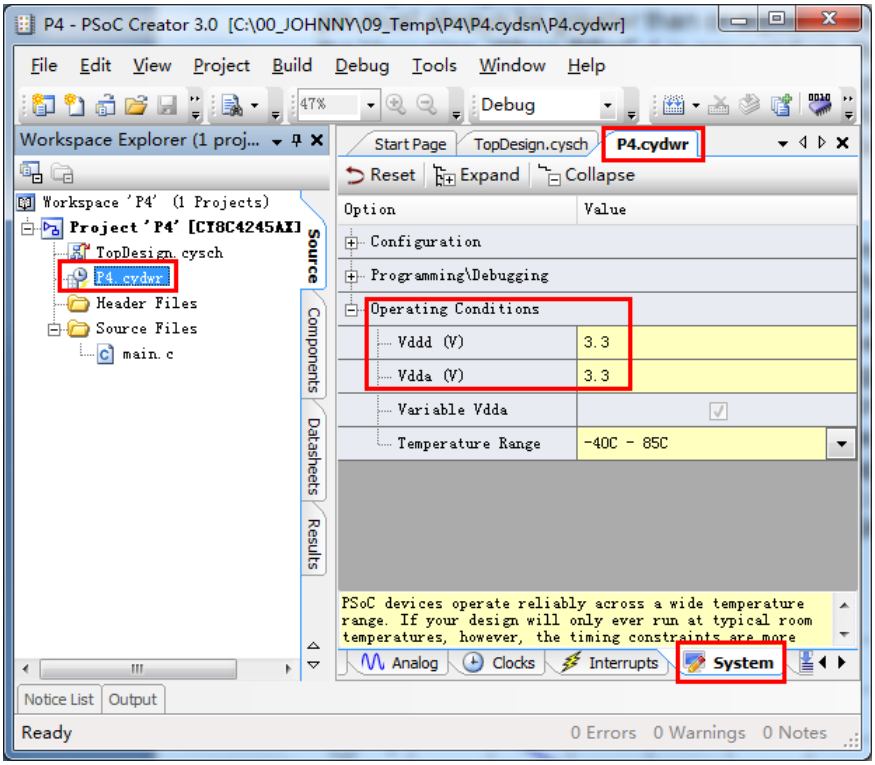
3.2 Power Ramp-Up Considerations

As mentioned previously, if you use separate power rails for the analog and digital power domains, the voltage at the V_{DDA} pin must always be greater than or equal to the voltage at the V_{DDD} pin. When PSoC 4 is powered up, the voltage at the V_{DDA} pin must be present prior to or concurrent with the voltage at the V_{DDD} pin. The maximum allowed voltage ramp rate for any power pin is 67 mV/µs.

3.3 PSoC Creator Settings for Device Power

PSoC Creator automatically configures Components for optimal performance for the voltages applied to the power pins. To do so, it needs to know the value of these voltages. The **System** tab in the PSoC Creator project's Design-Wide Resources (DWR) window is used for this purpose. To open the DWR window, double-click the *.cydw*" file in the project navigator, as Figure 3 shows.

Figure 3. Device Power Settings in PSoC Creator



3.4 Thermal Considerations

Thermal considerations are important in the hardware design processes, such as package selection and PCB layout. PSoC 4 targets low-power applications, as it consumes no more than 0.2 W. The maximum power consumption is low enough that thermal considerations are unlikely.

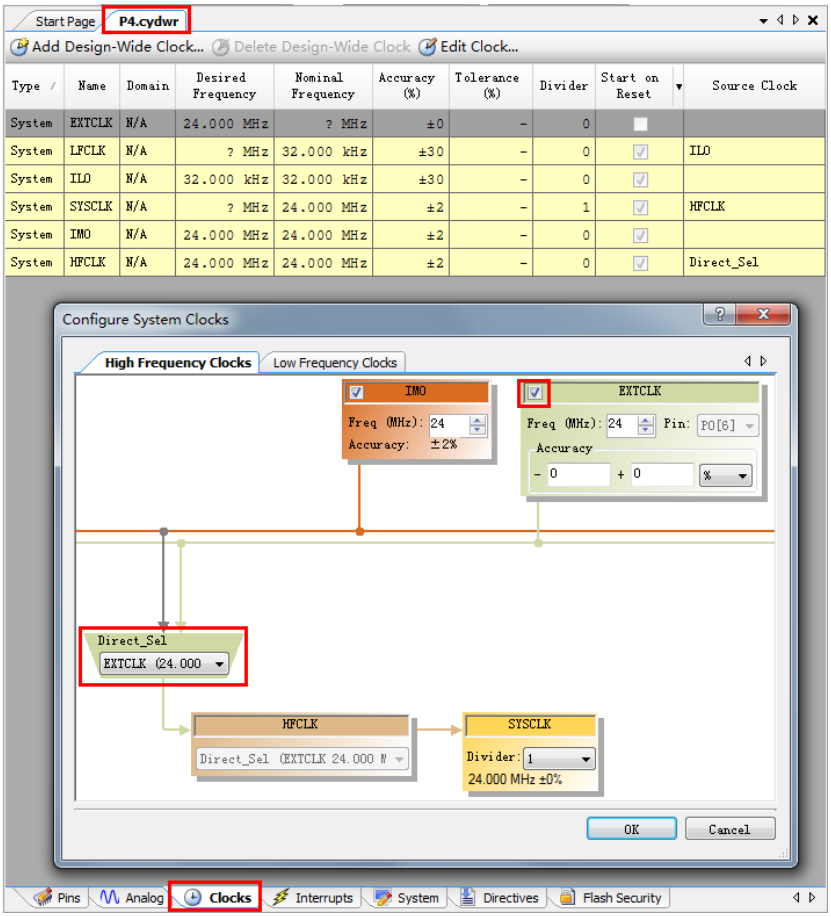
4 Clocking

PSoC 4100/4200 has two oscillators: an internal main oscillator (IMO), which drives the high-frequency clock (HFCLK), and an internal low-speed oscillator (ILO), which drives the low-frequency clock (LFCLK). PSoC 4100M/4200M series devices provide an additional watch crystal oscillator (WCO) that can provide an alternative, high-accuracy clock for the LFCLK.

The IMO is rated at ±2 percent accuracy. If you need better accuracy, you can bring in a precision clock via pin P0[6] to drive the HFCLK. The external clock's frequency can be up to 48 MHz. Its duty cycle must be from 45 percent to 55 percent; a square-wave clock is recommended. PSoC 4100, 4200, 4100M, and 4200M does not support an external crystal connection.

To use the external clock, you must configure system clocks to enable external clock input (EXTCLK), enter the external clock frequency, and select it as HFCLK's source in the **Clocks** tab in the DWR window. Double-click any row in the table of clocks to open the **Configure System Clocks** dialog, as Figure 4 shows.

Figure 4. External Clock Settings in PSoC Creator IDE for PSoC 4100/4200



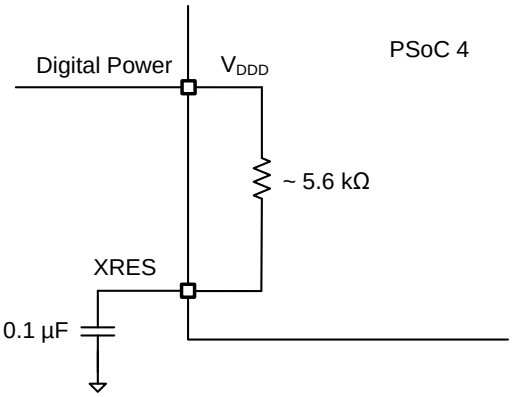
Using HFCLK as the source, internal prescalers and dividers generate clocks for the ARM Cortex-M0 core, analog modules, and digital modules. LFCLK is directly used to drive the watchdog timer (WDT). If necessary, you can output LFCLK and SYSCLK (see Figure 4) via the PSoC 4 I/O pins (except Ports 4, 5, 6, or 7).

5 Reset

PSoC 4 has a reset pin, XRES, which is active LOW. XRES is internally pulled up to V_{DDD} via a 5.6-kΩ resistor; you do not need an external pull-up resistor for XRES.

You can connect a capacitor to the XRES pin, as Figure 5 shows, to filter out glitches and give the reset signal better noise immunity. A typical capacitance is 0.1 µF.

Figure 5. XRES Pin Connection



6 Programming and Debugging

PSoC 4 supports serial wire debug (SWD) interfaces for device programming and debugging. For programming or debugging, you can use the built-in debugger of CY8CKIT-042 and CY8CKIT-044, or connect PSoC 4 to a debugger such as CY8CKIT-002 MiniProg3 via a 10-pin or 5-pin connector (pin maps are shown in Figure 6). For a 10-pin connector, Samtec FTSH-105-01-L-DV-K (surface mount) or FTSH-105-01-L-D-K (through hole) is recommended. For a 5-pin connector, Molex 22-23-2051 is recommended. Similar parts are available from other vendors.

Figure 6. SWD Connector Pin Maps for MiniProg3

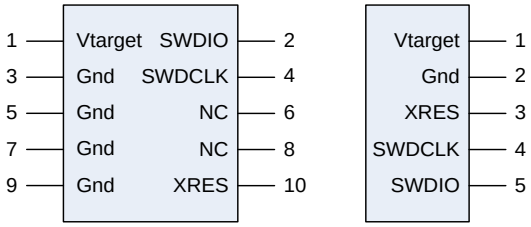
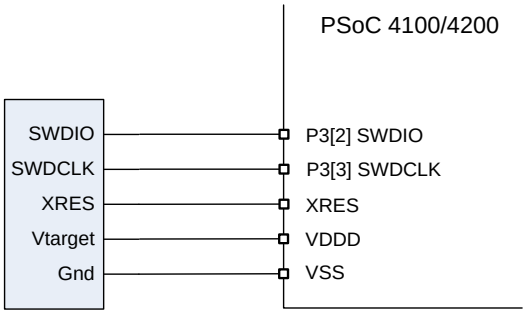


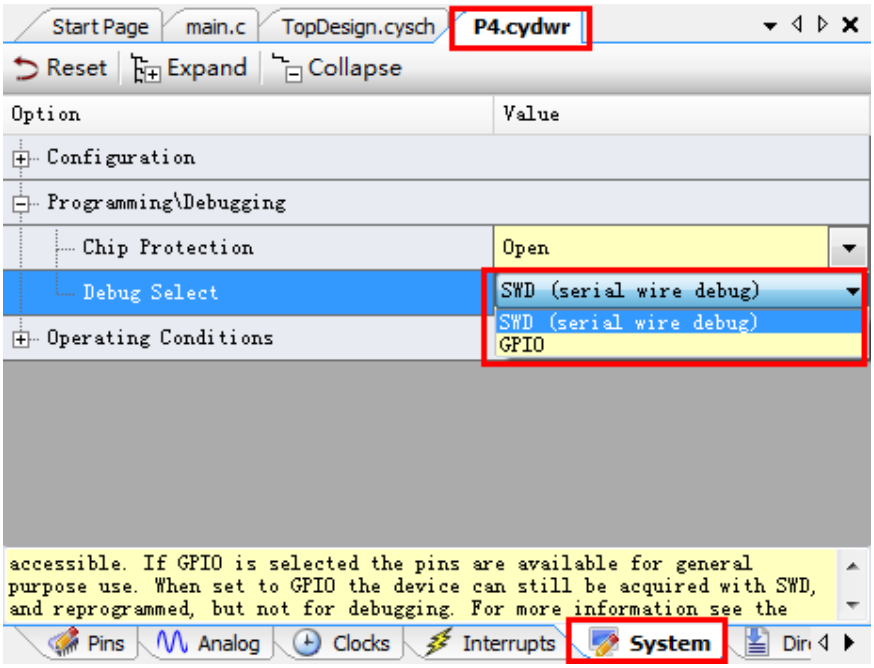
Figure 7 shows the SWD connections.

Figure 7. SWD Connections to PSoC 4100/4200



If you want to use P3[3:2] as the SWD interface for run-time debugging, select **SWD (serial wire debug)** from the **Debug Select** pull-down list in the **System** tab of the DWR window, as Figure 8 shows. Note that if the pins are used as SWD, they cannot be used as GPIOs.

Figure 8. PSoC Creator Debugging Settings



7 GPIO Pins

PSoC 4 provides flexible GPIO pins. Each pin has 4-mA source current or 8-mA sink current capability. The maximum total source and sink current for all GPIO pins is 200 mA.

All GPIO pins can be controlled by firmware. Most of them also have alternative connections to PSoC 4 peripherals. Different components have different dedicated or fixed pins for their terminals. With dedicated pins, you get the best performance when the peripheral is connected to its own dedicated pin or pins. However, for flexibility, you can connect the peripheral to other pins, at the cost of using some internal routing resources.

If a peripheral has fixed pins, then you can connect it only to those pins.

7.1 I/O Pin Selection

When you design a hardware system based on PSoC 4, you should assign the GPIO pins in the following sequence.

1. System function pins
   a. SWD: If you need run-time debugging, use P3[3:2].
   b. External clock: If you need to use an external clock, use P0[6].
   c. Wakeup: This pin is used to wake up PSoC 4 from the Stop low-power mode. If you need this feature, use P0[7]. For more information, see AN86233 – PSoC 4 Low-Power Modes and Power Reduction Techniques.
2. Analog pins
   a. SAR ADC: All the Port 2 pins are used as multichannel inputs to the SAR ADC. Furthermore, if you want a higher ADC clock than 3 MHz or you need to apply an external reference, reserve P1[7] for an external bypass capacitor connection. See SAR ADC Acquisition Time for details.

      Port 2 pins are dedicated pins for the SAR ADC. Through the internal analog bus, you can also route signals from the other pins (except Port 4 pins) to the ADC. P1[7] is a fixed pin for the ADC's reference bypass capacitor connection.

b. Low-power comparator: PSoC 4 has two comparators that can work in the Hibernate low-power mode. Each comparator has two fixed pins, as Table 2 shows.

Table 2. Pin List for Low-Power Comparators

Components	Terminals	GPIO Pin
Low-Power Comparator 0	Noninverting Input	P0[0]
	Inverting Input	P0[1]
Low-Power Comparator 1	Noninverting Input	P0[2]
	Inverting Input	P0[3]

c. Continuous Time Block mini (CTBm): The CTBm module is composed of two opamps. The opamps have dedicated pins for their noninverting inputs and fixed pins for their inverting inputs and outputs, as Table 3 shows.

If you use an opamp as a comparator, you can route the digital output to other GPIO pins (except Port 4).

Table 3. Pin List for CTBm Opamps

Components	Terminals	GPIO Pin
Op Amp 0	Noninverting Input	P1[0]
		P1[6]
	Inverting Input	P1[1]
	Output	P1[2]
Op Amp 1	Noninverting Input	P1[5]
		P1[7]
	Inverting Input	P1[4]
	Output	P1[3]
Op Amp 2 (PSoC 4100M/4200M only)	Noninverting Input	P5[0]
	Inverting Input	P5[1]
	Output	P5[2]
Op Amp 3 (PSoC 4100M/4200M only)	Noninverting Input	P5[5]
	Inverting Input	P5[4]
	Output	P5[3]

d. CapSense®: When you use this module, note that there are two fixed pins. You must connect a reservoir capacitor (C_{MOD}) to P4[2] in all cases and the other reservoir capacitor (C_{SH_TANK}) to P4[3] in some cases. See the PSoC 4 CapSense Design Guide for details. In PSoC 4100M/4200M, you also have the option of using P5[0] and P5[1] as C_{MOD} and C_{SH_TANK}. You can connect any other pin to a CapSense sensor.

3. Digital pins

a. Timer/Counter Pulse-Width Modulator (TCPWM): PSoC 4100/4200 has four TCPWM blocks. PSoC 4100M/4200M has eight TCPWM blocks. Each TCPWM can output two complementary PWM signals. All these signals are routed to dedicated GPIO pins via high-speed paths, Refer to the device datasheet to learn more about these dedicated pins.

You can also route these signals via an internal digital connection to other GPIO pins (except for Ports 4, 5, 6, or 7).

b. Serial Communication Block (SCB): PSoC 4100/4200 has two SCBs, and PSoC 4100M/4200M has four SCBs. Each SCB can be configured as SPI, I^2C, or UART. Each SCB has fixed pins for its terminals. Refer to the device datasheet to learn more about these dedicated pins.

Unlike TCPWM, the SCB terminals are routed to fixed pins and cannot be routed to any other GPIO pin. You must follow the dedicated pin assignments when using the SCBs.

If your system needs a serial communication interface with a more flexible GPIO pin assignment, you can use a Universal Digital Block (UDB) to implement it. See the PSoC 4 Architecture TRM for details.

For an overview of the pin map, refer to the PSoC 4100 Family Datasheet, PSoC 4200 Family Datasheet, PSoC 4100M Family Datasheet, or PSoC 4200M Family Datasheet

7.2 Port 4, 5, 6, and 7 GPIO Pins

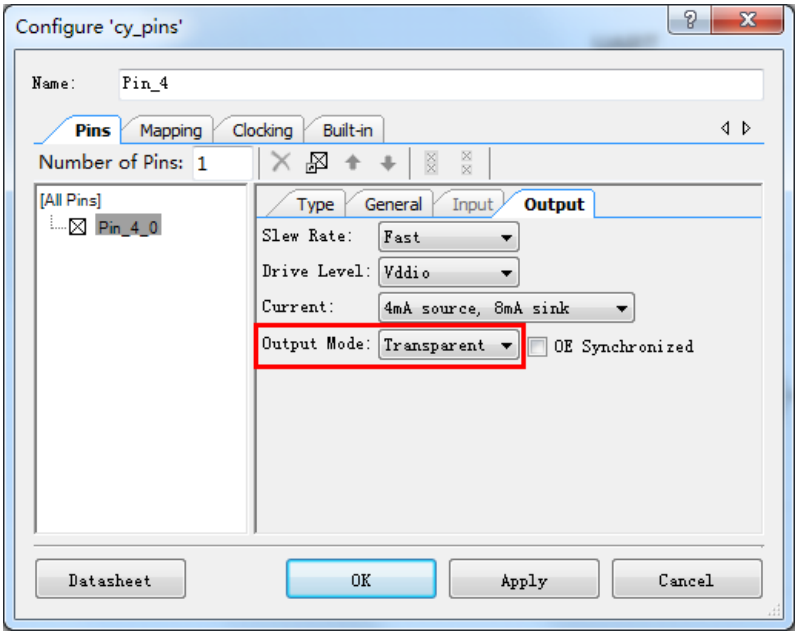
In PSoC 4, Ports 4, 5, 6, and 7 are different from the other three ports in that they have only four GPIO pins. You can use these pins as SCB pins, CapSense pins, dedicated TCPWM pins, Segment LCD pins, or firmware pins.

To achieve a balance between cost and performance, consider the following regarding these ports in the hardware design:

1. You cannot use these GPIO pins for some analog purposes, including SAR ADC and low-power comparators.
2. You cannot route a digital signal to these GPIO pins. For example, you cannot route digital signals of a UDB-based Component or TCPWM to Port 4 GPIO pins.

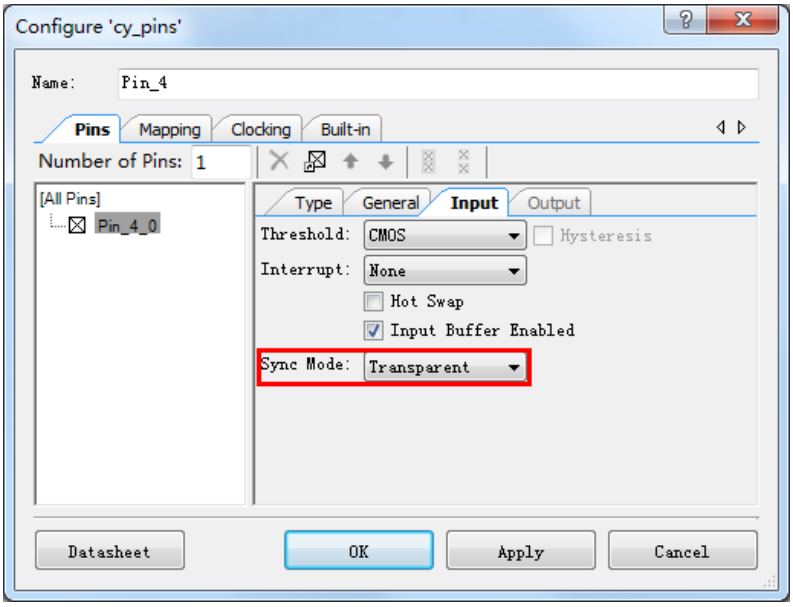
   Note: In PSoC 4100/4200 devices, if P4[2] or P4[3] is used to connect C_{MOD} or C_{SH_TANK}, you cannot route a digital output signal to P3[6] or P3[7].
3. You can use these GPIO pins for firmware. However, the synchronization feature will not be available.
   a. For example, if you want to use a Port 4 GPIO pin for output firmware, select **Transparent** in the **Output Mode** list, as Figure 9 shows.

Figure 9. Port 4 GPIO Pin Output Setting



   b. If you use a Port 4 GPIO pin for input firmware, select **Transparent** in the **Sync Mode** list, as Figure 10 shows.

Figure 10. Port 4 GPIO Pin Input Setting

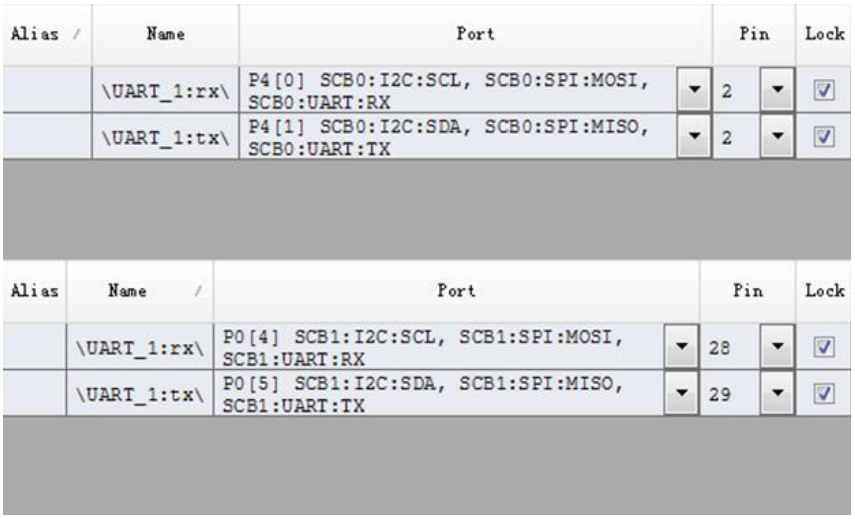


8 Component Placement

In PSoC Creator, you can place Components into device physical blocks in several ways. For Components with fixed pins, assign the Component terminals to the appropriate pin. Following is an example of the UART (SCB mode) Component placement in a PSoC 4200 device, where the SCB implements a UART.

In Figure 11, there are two pin settings for the UART tx and rx terminals. If you select P4[0] and P4[1], the UART is placed on SCB_0; if you select P0[4] and P0[5], the UART is placed on SCB_1. You can configure these pins in the Pin Editor by clicking the **Pins** tab in the DWR window.

Figure 11. SCB Component Placement by Pin Selection

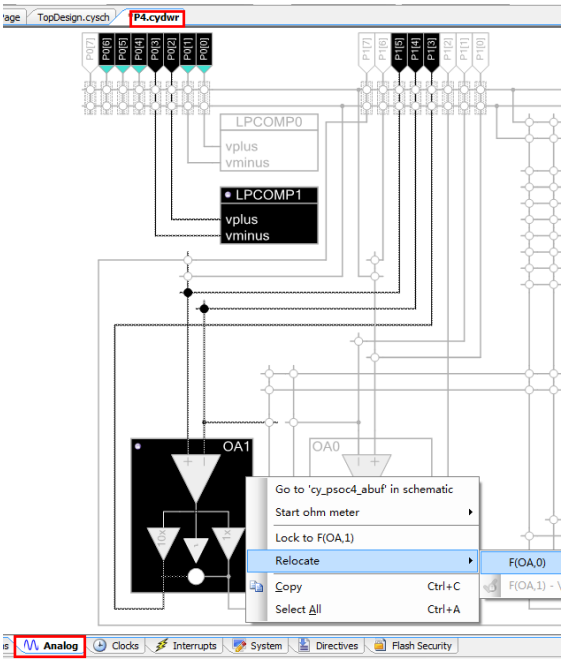


Analog Components can be placed using the Analog Device Editor. Click the **Analog** tab in the DWR window to open it. Figure 12 shows an example of Opamp Component placement.

Right-click the opamp (OAx) to relocate the Component to another available hardware slot. The pins change automatically when the Component is relocated.

The third method to place Components is to use the Directive Editor. Select **Topics** in the PSoC Creator Help menu and search “directive” to get more information.

Figure 12. Opamp Component Placement



9 Analog Module Design Tips

Analog design is always challenging. Using the PSoC 4 analog modules involves several hardware design considerations.

9.1 SAR ADC

PSoC 4 has a 12-bit differential SAR ADC, with a sampling rate up to 1 Msps. As mentioned in I/O Pin Selection, Port 2 pins are dedicated for SAR ADC multichannel inputs. They provide the lowest parasitic path resistance and capacitance. You can also route the signals from other pins to the SAR ADC using the internal analog bus, but doing so will introduce high switch resistance (R_{SW} in Figure 14 on page 12) and additional parasitic capacitance.

PSoC 4 also has an internal precision reference of 1.024 V ±1 percent. You can use other internal references, including V_{DDA} and V_{DDA} / 2, to extend the SAR ADC’s input range. However, note that the accuracy of V_{DDA} and V_{DDA} / 2 as references depends on your power system design, and it probably cannot be better than the internal reference. When you use the internal reference or V_{DDA} / 2 as your reference, a bypass capacitor on P1[7] can help you run the SAR ADC at a faster clock. See Table 4. for details.

Table 4. References for SAR ADC

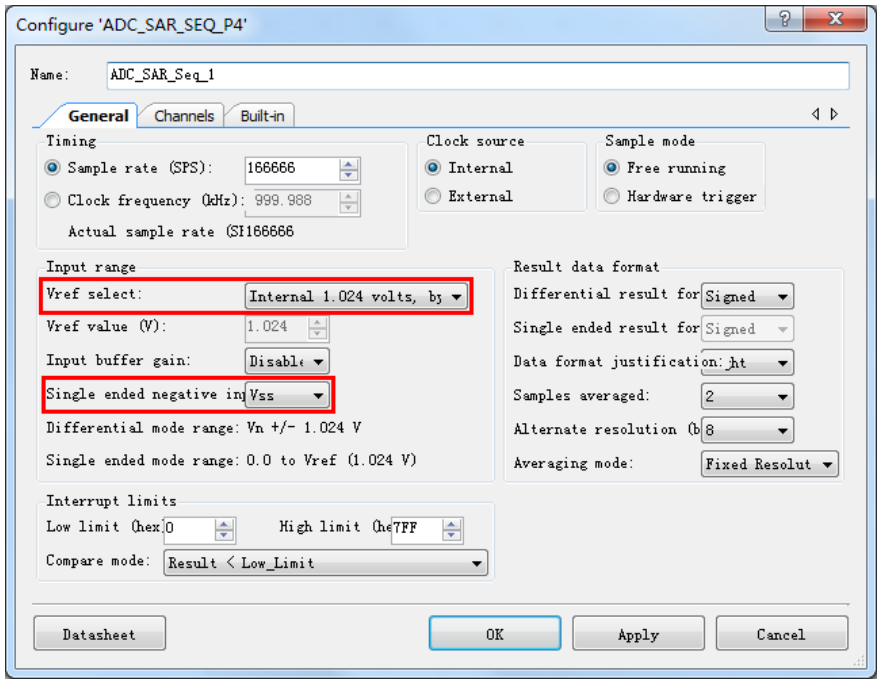
References	Bypass Capacitor at P1[7]	Maximum Component Clock Frequency
Internal 1.024 V	Optional	3 MHz
V_{DDA} / 2	Optional	3 MHz
V_{DDA}	Optional	18 MHz
Internal 1.024 V, bypassed	Mandatory	18 MHz
V_{DDA} / 2, bypassed	Mandatory	18 MHz
External V_{ref}	Mandatory	18 MHz

If you need a reference with a higher accuracy or a specific voltage value, you can connect a custom external reference and a bypass capacitor to P1[7].

The SAR ADC is differential physically. When you select single-ended input mode, you must select the connection for the negative input. There are three options: V_{SS}, V_{REF}, and an external pin. The SAR ADC's input range is affected by the selection as well as by the value of the reference voltage. See the chapter "SAR ADC" in the PSoC 4100/4200 Architecture TRM for more information.

You can select the reference and the negative input connection in the **General** tab of the ADC_SAR_SEQ_P4 Component customizer dialog, as Figure 13 shows.

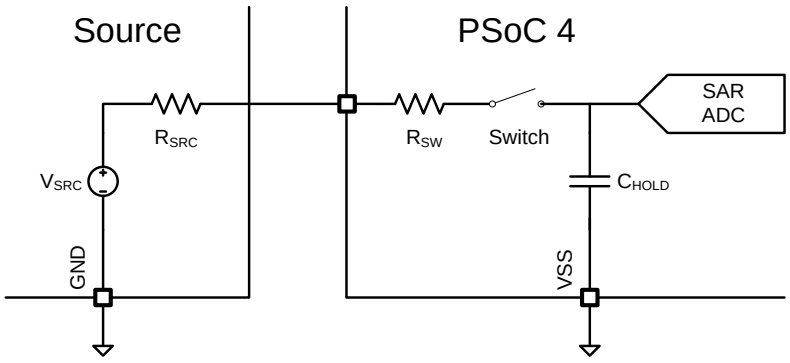
Figure 13. SAR ADC Reference and Negative Input Settings



9.1.1 SAR ADC Acquisition Time

Another parameter of concern is the SAR ADC acquisition time, which depends on your hardware design, as Figure 14 shows.

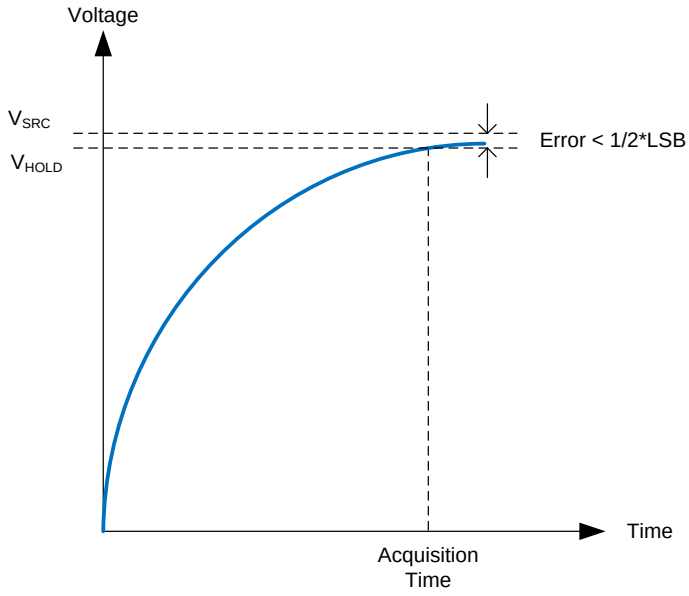
Figure 14. Equivalent Sample and Hold Circuit of PSoC 4 SAR ADC



V_{SRC} is the sampled signal source, and R_{SRC} is its output resistance. R_{SW} is the resistance of the path from a dedicated pin to the SAR ADC input, which is about 2.2 kΩ. C_{HOLD} is the sample and hold capacitance, which is about 10 pF.

Figure 15 shows how C_{HOLD} is charged during acquisition time. During acquisition time, the switch in Figure 14 is on. Assuming that C_{HOLD} is charged from 0, the acquisition time is the time required to charge C_{HOLD} to a voltage level (V_{HOLD}) such that the error (V_{SRC} – V_{HOLD}) is less than the ADC's resolution.

Figure 15. C_{HOLD} Charging Process



If the error is smaller than half the ADC's resolution (1/2 * LSB), it should be okay. The error can be related to the acquisition time in the following equation:

$$Error = V_{SRC} \cdot e^{-\frac{t_{ACQ}}{\tau}} = V_{SRC} \cdot e^{-\frac{t_{ACQ}}{(R_{SRC}+R_{SW})\cdot C_{HOLD}}}$$

Here, t_{ACQ} is the acquisition time, while τ is the charging time constant.

PSoC 4100/4200 provides a 12-bit differential ADC. If V_{REF} is the reference voltage, the resolution can be expressed in the following equation:

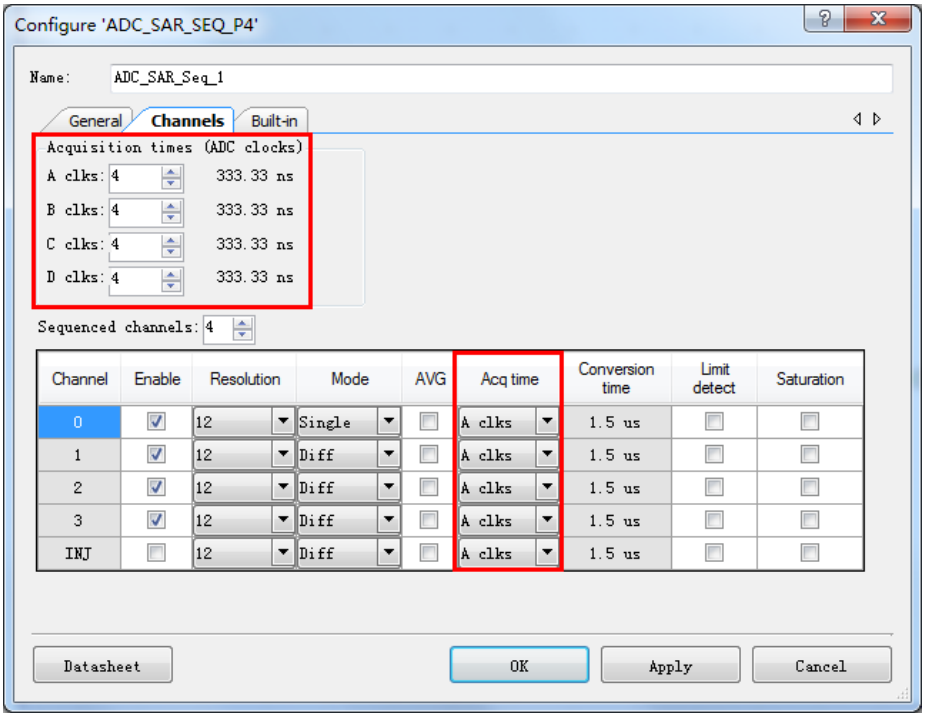
$$LSB = \frac{2V_{REF}}{2^{12}}$$

This example assumes that the negative input is connected to V_{REF}, so that V_{SRC} has an input range from 0 to 2 V_{REF}. If the acquisition time is 9 * (R_{SRC} + R_{SW}) * C_{HOLD}, the error can be expressed as follows:

$$Error = V_{SRC} \cdot e^{-9} \approx \frac{V_{SRC}}{8013} < \frac{2V_{REF}}{8013} \approx \frac{1}{2} \cdot \frac{2V_{REF}}{2^{12}} = \frac{1}{2} \cdot LSB$$

This equation shows that you should choose an acquisition time that is longer than 9 * (R_{SRC} + R_{SW}) * C_{HOLD} to make the error less than 1/2 * LSB of the 12-bit ADC. Select the acquisition time in the **Channels** tab of the ADC_SAR_SEQ_P4 Component customizer dialog, as Figure 16 on page 14 shows. Note that when you select the number of ADC clocks, the corresponding acquisition time is automatically calculated. See the ADC_SAR_SEQ_P4 Component datasheet for details.

Figure 16. SAR ADC Acquisition Time Settings



In conclusion, pay attention to the output resistance of the sampled signal source, R_{SRC}, and the resistance introduced by PCB traces in your ADC hardware design. These determine the acquisition time and therefore the sampling rate.

9.2 Opamps

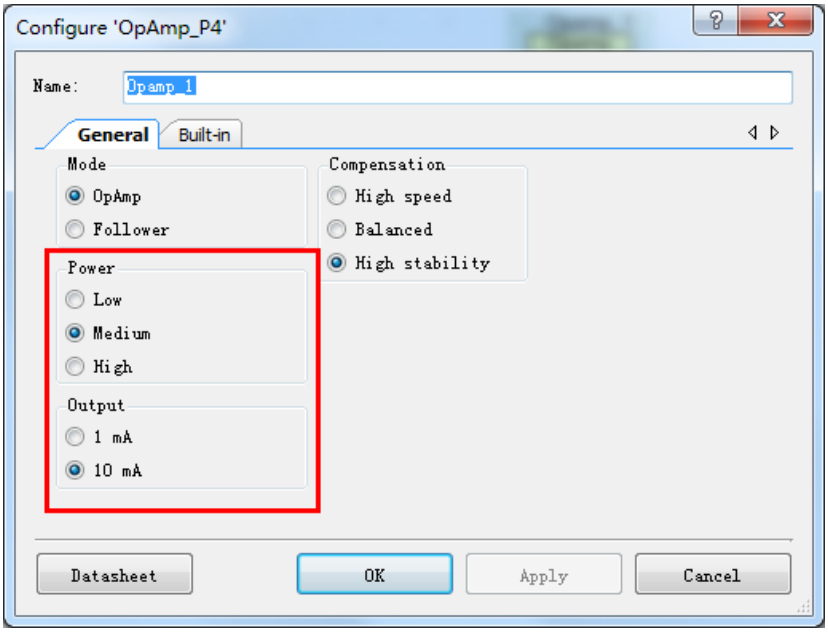
Each CTBm block in PSoC 4 provides two opamps, which facilitate your analog signal chain design. You can configure each opamp as an amplifier, a follower, or a comparator, as shown in Figure 17.

You can configure the power mode and output drive capability in the **General** tab of the OpAmp_P4 customizer dialog, as Figure 17 shows. The opamps have three power modes. For each power mode, the opamp has a different input offset voltage, gain bandwidth (GBW) product, and operating current. See the device datasheet for the specific values.

You should take into account the relation between bandwidth and gain. For example, the highest GBW, 6 MHz, occurs in the high-power mode. In this case, if the bandwidth of a signal to be amplified is 60 kHz, then the gain cannot be higher than 100 or the amplified signal will be distorted.

If you route an opamp output terminal to a pin for external use, select **10 mA** for the output drive capability. If you route the output terminal for internal use, for example to an input of the SAR ADC, select **1 mA** instead.

Figure 17. OpAmp_P4 Component Settings



9.3 Comparators

PSoC 4 provides as many as six comparators. Four comparators are implemented using the opamps in the CTBm module, and the other two are the low-power comparators. All of the comparators' outputs can be routed to PSoC 4 UDB resources. This helps you leverage the outputs flexibly. For example, you can invert an output's logic value. PSoC 4 provides three speed modes for each comparator. For each mode, the comparator has a different output slew rate and operating current. See the device datasheet for the specific values.

The low-power comparators can monitor external analog voltage levels in low-power modes. For more information, see the device datasheet.

When an analog signal's voltage is divided by a resistor network before it is input into a comparator, take the input resistance of the comparator into account. You can get the comparator's input resistance from the device datasheet.

9.4 CapSense

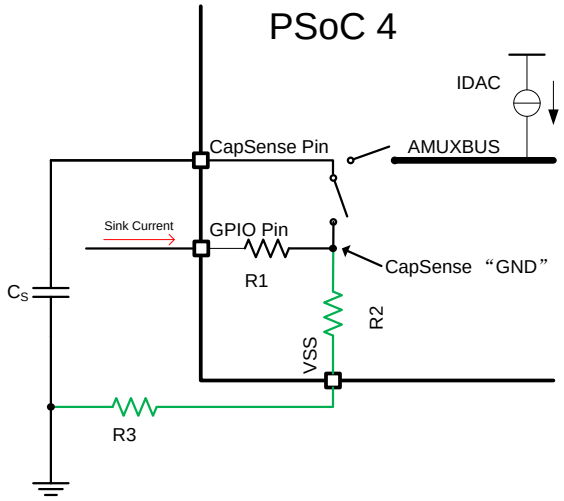
You can connect any PSoC 4 pin to a CapSense sensor except P4[2] or P5[1], which are reserved for C_{MOD}. When you need to use a shield electrode for waterproofing or proximity features, you may also need to reserve P4[3] or P5[1] for C_{SH_TANK}. If the parasitic capacitance of the shield is less than 200 pF, it is optional to use C_{SH_TANK}; otherwise, it is mandatory.

Values for C_{MOD} and C_{SH_TANK} are usually 2.2 nF. The value may be higher if the parasitic capacitance of the sensors is higher.

CapSense detects a finger touch by a tiny variation in the sensor's capacitance (less than 1 pF). It is very sensitive to both signal and noise. Note the PCB layout tips for CapSense. Refer to the PSoC 4 CapSense Design Guide for more details.

Pins with a large sink current that are close to CapSense pins can introduce an offset to the CapSense module's "GND." Figure 18 illustrates a switch circuit for CapSense in IDAC source mode. R1 and R2 represent the resistances of PSoC 4 internal traces, and R3 represents the resistance of a PCB trace. A shared return path of sink current and CapSense current is composed of R2 and R3. The closer a pin with a large sink current is to the CapSense pin, the more the sink current that flows through the return path, generating a greater offset.

Figure 18. Sharing Return Path



This offset is undesirable and may cause fluctuations in the CapSense reading and possible false triggers. Offset compensation can be done in firmware, but it is strongly recommended that you remove the offset in the hardware design instead. Keep pins with a large sink current as far as possible from the CapSense pins (best practice is by more than three pins). In addition, pay attention to the return path in your PCB. See AN57821 – PSoC 3, PSoC 4, and PSoC 5LP Mixed-Signal Circuit Board Layout Considerations for more details on mixed-signal circuit design.

9.5 Current DACs (IDACs)

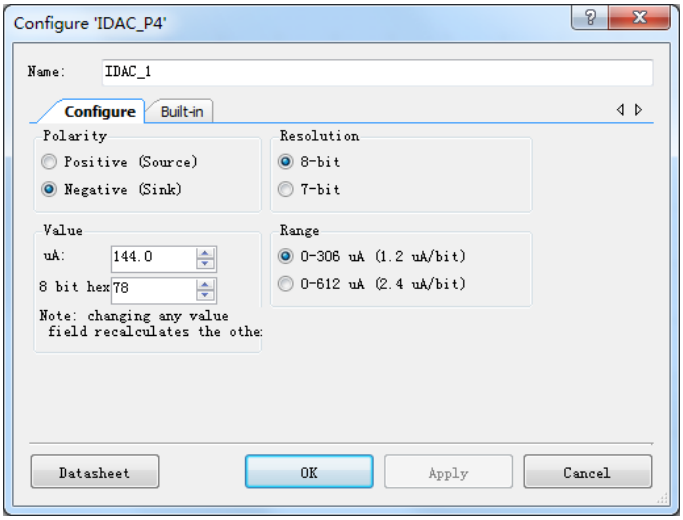
PSoC 4100/4200 provides two IDACs: one 8-bit and the other 7-bit. PSoC 4100M/4200M provides four IDACs: two 8-bit and two 7-bit. See the device datasheethttp://www.cypress.com/?id=4749&rtID=107 for the electrical specifications. There are two gain options for each IDAC. Table 5. gives the detailed resolutions and capabilities for each IDAC and gain option.

Table 5. IDAC Resolutions and Output Current Capabilities

	4X Gain		8X Gain	
	Step (µA/Bit)	**Output Capability (µA)**	**Step (µA/Bit)**	**Output Capability (µA)**
8-Bit IDAC	1.2	306	2.4	612
7-Bit IDAC	1.2	152.4	2.4	304.8

You can set up the IDACs in the **Configure** tab of the IDAC_P4 Component customizer dialog, as Figure 19 shows.

Figure 19. IDAC Settings



Through two internal analog buses, you can route IDAC outputs to any two different pins (except Port 4 GPIO pins).

Note: CapSense requires one or two IDACs. Ensure that the intended IDACs are not used by CapSense.

10 Summary

PSoC 4 provides a flexible solution for designing digital and analog applications. This application note documented the considerations that you need to keep in mind when you build a hardware system around PSoC 4. You can use the Appendix B – Schematic Checklist to quickly check your hardware design.

11 Related Documents

- AN79953 – Getting Started with PSoC 4
- AN72845 – Design Guidelines for QFN Packaged Devices
- AN86233 – PSoC 4 Low-Power Modes and Power Reduction Techniques
- AN80994 – PSoC 3, PSoC 4, and PSoC 5LP EMC Best Practices and Recommendations
- AN57821 – PSoC 3, PSoC 4, and PSoC 5LP Mixed-Signal Circuit Board Layout Considerations
- PSoC 4 CAD Resources
- PSoC 4 Device Datasheets
- PSoC 4 Technical Reference Manuals
- PSoC 4 CapSense Design Guide

Cypress PSoC 4 kit schematics are good examples of how to incorporate PSoC into board schematics. It may be helpful to review the following Cypress kit schematics:

- CY8CKIT-042 - PSoC 4200 Pioneer Kit
- CY8CKIT-044 – PSoC 4200M Pioneer Kit
- CY8CKIT-049 4xxx – PSoC 4100/4200 Prototyping Kit

Note: On the kit web page, scroll to the link *Board Design Files (Schematic, Layout, Gerber, BOM).zip*.

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12 Appendix A – PCB Layout Tips

Note: Before beginning a PCB layout for PSoC, it is a good idea to look at AN57821 – PSoC Mixed-Signal Circuit Board Layout Considerations. Appendix A of that application note shows example PCB layouts and schematics for various PSoC packages.

Note: Cypress PSoC 3, PSoC 4, and PSoC 5LP kit schematics provide good examples of how to incorporate PSoC into board schematics. For more information, see Related Documents.

There are many classic techniques for designing PCBs for low noise and EMC. Some of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multilayer PCB with separate layers dedicated to the V_{SS} and V_{DD} supplies. This gives good decoupling and shielding effects. Separate fills on these layers should be provided for V_{SSA}, V_{SSD}, V_{DDA}, V_{DDIO} and V_{DDD}.

  To reduce cost, a two-layer or even a single-layer PCB can be used. In that case, you must have a good layout for all V_{SS} and V_{DD}.

- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using two-layer or single-layer PCBs.

  The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI.

- **Decoupling:** The standard decoupler for external power is a 100-µF capacitor. Supplementary 0.1-µF capacitors should be placed as close as possible to the V_{SS} and V_{DD} pins of the device to reduce high-frequency power supply ripple.

  Generally, you should decouple all sensitive or noisy signals to improve the EMC performance. Decoupling can be both capacitive and inductive.

- **Component position:** Separate the circuits on the PCB according to their EMI contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components.

- **Signal routing:** When designing an application, the following areas should be closely studied to improve the EMC performance:
  - Noisy signals. For example, signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

  To increase the EMC performance, keep the trace lengths as short as possible and isolate the traces with V_{SS} traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces.

For more information, several references are available:

- *The Circuit Designer's Companion*, *Second Edition, (EDN Series for Design Engineers),* by Tim Williams
- *PCB Design for Real-World EMI Control (The Springer International Series in Engineering and Computer Science),* by Bruce R. Archambeault and James Drewniak
- *Printed Circuits Handbook* (McGraw Hill Handbooks), by Clyde Coombs
- *EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple*, by Mark I. Montrose
- *Signal Integrity Issues and Printed Circuit Board Design*, by Douglas Brooks

13 Appendix B – Schematic Checklist

The answer to each item in the following checklist should be Yes (Y) or Not Applicable (N.A.). For example, if you choose unregulated mode for the PSoC 4100/4200 device in your application, you can mark all the items of "Power (regulated mode)" as N.A.

Catalog	Item	Y / N / N.A.	Remark
Power	Is the voltage at the V_{DDA} pin always greater than or equal to the voltages at the V_{DDD} pins?		
Power (regulated mode)	Are the power supply pin connections made in accordance with Figure 1?		
	Are the 0.1-µF and 1-µF capacitors connected to each V_{DDD}, V_{DDIO}, or V_{DDA} pin?		
	Are the voltages (including ripples) at the V_{DDD} and V_{DDA} pins in the range of 1.8 V to 5.5 V?		
	Is the V_{CCD} pin connected to a 0.1-µF capacitor and no other external load?		
Power (unregulated mode)	Are the power supply pin connections made in accordance with Figure 2?		
	Are the 0.1-µF and 1-µF ceramic decoupling capacitors connected to each V_{CCD}, V_{DDD}, and V_{DDA} pin?		
	Are the voltages (including ripples) at the V_{DDD} and V_{DDA} pins in the range of 1.71 V to 1.89 V?		
Clocking	Is the external clock connected to P0[6]?		
	Is the external clock's frequency less than or equal to 48 MHz (including tolerance)?		
	Is the external clock's duty cycle from 45 percent to 55 percent?		
Reset	Is the reset pin connection made in accordance with Figure 6?		
Programming and debugging	Is the SWD connector's pin map in accordance with one of the pin maps in Figure 8?		
	Are the SWDIO and SWDCLK pins connected to P3[2] and P3[3] respectively?		
GPIO pins	Is the assignment of your GPIO pins done in the sequence described in I/O Pin Selection?		
	Is any GPIO pin's sink current smaller than 8 mA?		
	Is any GPIO pin's source current smaller than 4 mA?		
	Is the GPIO pins' total source current or sink current smaller than 200 mA?		
	Are Port 4,5,6,7 pins used according to Port 4, 5, 6, and 7 GPIO Pins?		
Low-power comparators	Is the assignment of the low-power comparators' fixed pins in accordance with Table 2?		
CTBm	Is the assignment of the CTBm's fixed pins in accordance with Table 3?		
SCB	Is the assignment of the SCB's fixed pins in accordance with the device datasheet?		
SAR ADC	Is the connection of the P1[7] bypass capacitor in accordance with Table 4. ?		
	Is the acquisition time of each SAR ADC channel enough to keep the error less than 1/2 LSB?		
CapSense	Are the pins with strong sink current kept away from the CapSense pins (the space is more than three pins)?		
	Is C_{MOD} connected to P4[2] / P5[0]?		
	Is C_{SH_TANK} connected to P4[3] / P5[1]?		
IDAC	Is the IDAC not being used by CapSense?		

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4293447	JOZH	02/27/2014	New application note
*A	4517949	JOZH	10/07/2014	Changed the title to "PSoC® 4100/4200 Hardware Design Considerations - AN88619" to address only PSoC 4100/4200 devices. Corrected names and links for reference documents. Added the latest references. Added the link for PSoC 4100/4200 SCH and PCB libraries.
*B	4701455		03/25/2015	Added a table to illustrate the differences between PSoC 4100 and PSoC 4200. Added TQFP-48 descriptions. Added variable VDDA introduction. Added routed clock introduction in "Clocking" section. Updated PSoC Creator Component snapshot per PSoC Creator 3.1.
*C	4772693	NIDH	05/26/2015	Updated for PSoC 4100M/4200M device Updated template Changed the title

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