**ECE 385**

Spring 2021

Experiment #5

**Simple Computer SLC-3.2 in SystemVerilog**

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ABF – Friday

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**Part 1:** **Introduction:** In this lab, we built the SLC-3, a simple “computer”, in SystemVerilog. The computer operates in an FSM cycle of Fetch🡪Decode🡪Execute🡪Fetch🡪… In each cycle, the computer fetches an instruction from memory, decodes it with the Instruction Sequencer/Decoder (IDSU) Unit, then executes the instruction. The computer then recurses through the cycle continuously. The computer contains several modules that make up its structure: the aforementioned IDSU, the Program Counter (PC), Instruction Register (IR), Memory Address Register (MAR), Memory Data Register (MDR), Status Register (nzp), an 8x16-bit general register file, and a 16-bit Arithmetic Logic Unit (ALU).

**Part 2: Written Description and Diagrams of SLC-3:**

**a. Further Summary of Operation**

b. Describe in words how the SLC-3 performs its functions. You should describe the Fetch-Decode-Execute cycle as well as the various instructions the processor can perform.

c. Block Diagram of slc3.sv

d. This diagr4am should represent the placement of all your modules in the slc3.sv. Please only include the slc3.sv diagram and not the RTL view of every module (this can go into the individual module descriptions).

e. Written Description of all .sv modules

i. A guide on how to do this was shown in the Lab 2.2 report outline.

f. Description of the operation of the ISDU (Instruction Sequence Decoder Unit)

i. Named ISDU.sv, this is the control unit for the SLC-3. Describe in words how the ISDU controls the various components of the SLC-3 based on the current instruction.

ii. If you prefer to, you can lump this section into the module description section under ISDU.sv.

g. State Diagram of ISDU

**Part 3: Simulations of SLC-3 Instructions:**

a. Simulate the completion of all 6 test programs, I/O Test 1, I/O Test 2, Self-Modifying Code, XOR, Multiplier and Sort.

b. Annotations for the above simulations, should include at a minimum, start of the test program, any user input (for example, entering the numbers in the multiplier test), and reading the expected result.

**Part 4: Post-Lab Questions:**

a. Fill out the Design Resources and Statistics table from Post-Lab question one

b. Answer all the post-lab questions. As usual, they may be in their own section or dispersed into the appropriate sections in the rest of the report.

**Part 5: Conclusion:**

a. Discuss functionality of your design. If parts of your design did not work, discuss what could be done to fix it.

b. Was there anything ambiguous, incorrect, or unnecessarily difficult in the lab manual or given materials which can be improved for next semester? You can also specify what we did right, so it doesn’t get changed.