NAND3

VDD = 2.0 V

temperature = 25°C

NMOS: W/L = 2160n/360n

PMOS: W/L = 1440n/360n

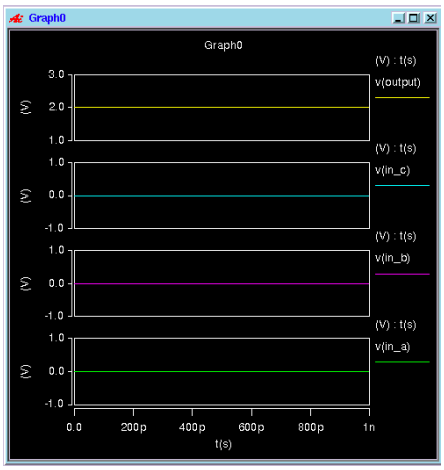
input nodes: in_a, in_b, in_c

output node: output

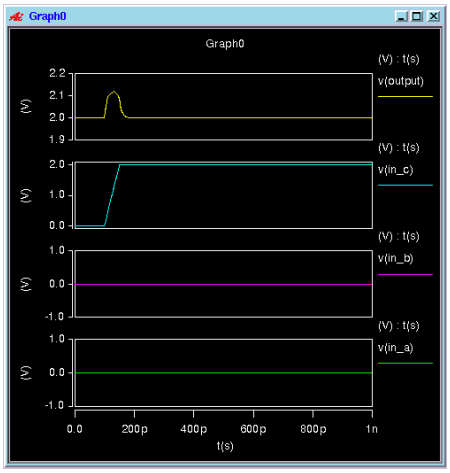
voltage source for input nodes: piecewise linear(pwl)

CASES: logic 0-> 0V; logic1->2.0V

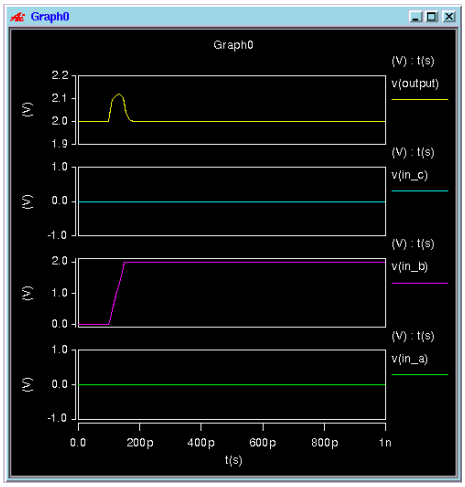
1. (a,b,c) = (0,0,0) -> (abc)' = 1



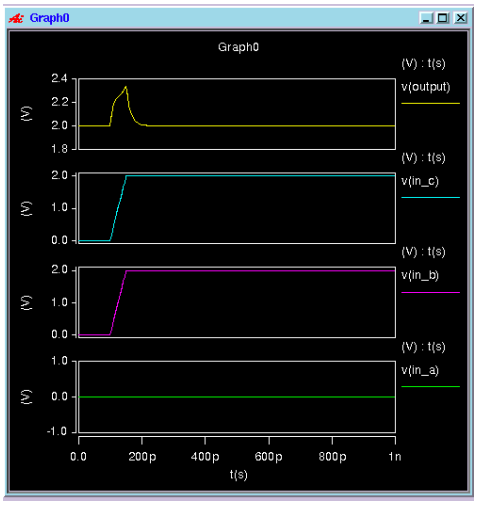
2. (a,b,c) = (0,0,1) -> (abc)' = 1



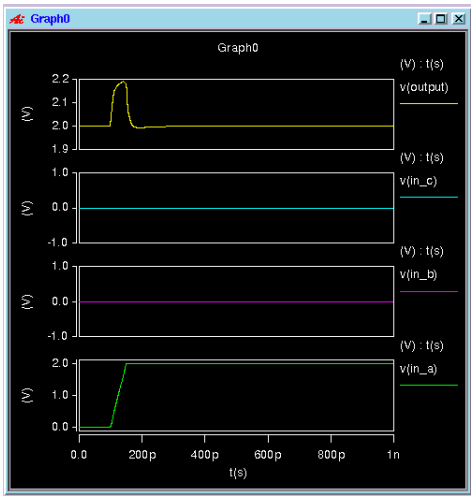
3. (a,b,c) = (0,1,0) -> (abc)’ = 1



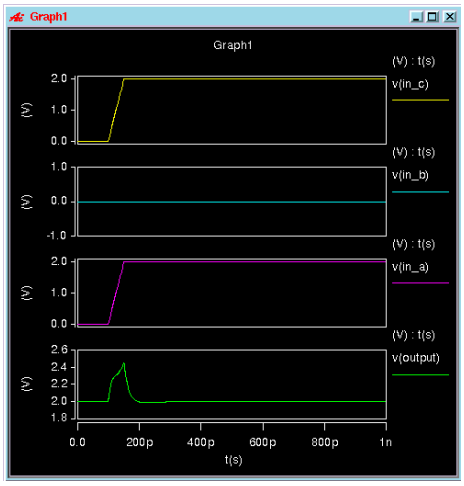
4. (a,b,c) = (0,1,1) -> (abc)’ = 1



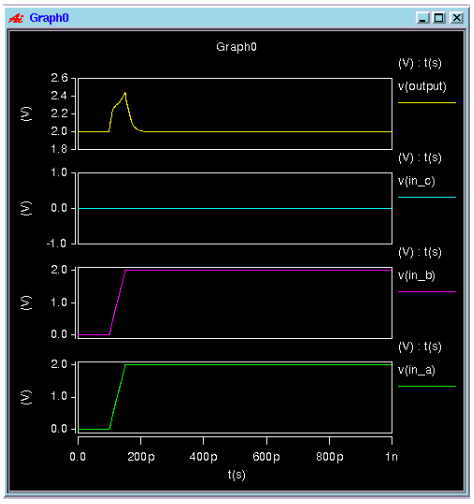
5. (a,b,c) = (1,0,0) -> (abc)’ = 1



6. (a,b,c) = (1,0,1) -> (abc)’ = 1



7. (a,b,c) = (1,1,0) -> (abc)’ = 1



8. (a,b,c) = (1,1,1) -> (abc)’ = 0