Integrated Circuit Design
Homework #4 Logic Synthesis with Design Compiler

Report

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I. 證明電路中沒有Latch的截圖

```
Inferred memory devices in process
        in routine LCD_CTRL line 335 in file
                '/home/raid7_2/userb05/b05030/ICD2019/HW4/lcd_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|        y_reg        | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|        y_reg        | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
|      GRID_reg       | Flip-flop |  40   |  Y  | N  | Y  | N  | N  | N  | N  |
|     IROM_A_reg      | Flip-flop |   6   |  Y  | N  | Y  | N  | N  | N  | N  |
|      IRB_D_reg      | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
|      IRB_A_reg      | Flip-flop |   6   |  Y  | N  | Y  | N  | N  | N  | N  |
|      busy_reg       | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
|      done_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|      _cmd_reg       | Flip-flop |   3   |  Y  | N  | Y  | N  | N  | N  | N  |
|   _cmd_valid_reg    | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|   state_ctrl_reg    | Flip-flop |   2   |  Y  | N  | Y  | N  | N  | N  | N  |
|     counter_reg     | Flip-flop |   6   |  Y  | N  | N  | Y  | N  | N  | N  |
|     counter_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|        x_reg        | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|        x_reg        | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
|   DATA_TABLE_reg    | Flip-flop |  512  |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

II. Report 截圖

① report_timing

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : LCD_CTRL
Version: N-2017.09-SP2
Date   : Tue May  7 11:05:42 2019
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: counter_reg_4_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: IROM_EN_reg
            (falling edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  LCD_CTRL           tsmc13_wl10           slow

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.50       0.50
  counter_reg_4_/CK (DFFRX2)               0.00       0.50 r
  counter_reg_4_/QN (DFFRX2)               0.61       1.11 r
  U11260/Y (NAND3X1)                       0.38       1.49 f
  U11297/Y (NOR2X4)                        0.55       2.05 r
  U10160/Y (NAND2XL)                       0.17       2.21 f
  U7700/Y (BUFX2)                          0.33       2.54 f
  U11771/Y (OAI21XL)                       0.49       3.03 r
  IROM_EN_reg/D (DFFNSRX1)                 0.00       3.03 r
  data arrival time                                   3.03

  clock clk (fall edge)                    5.00       5.00
  clock network delay (ideal)              0.50       5.50
  clock uncertainty                       -0.10       5.40
  IROM_EN_reg/CKN (DFFNSRX1)               0.00       5.40 f
  library setup time                       0.01       5.41
  data required time                                  5.41
  -----------------------------------------------------------
  data required time                                  5.41
  data arrival time                                  -3.03
  -----------------------------------------------------------
  slack (MET)                                         2.38
```

② report_area

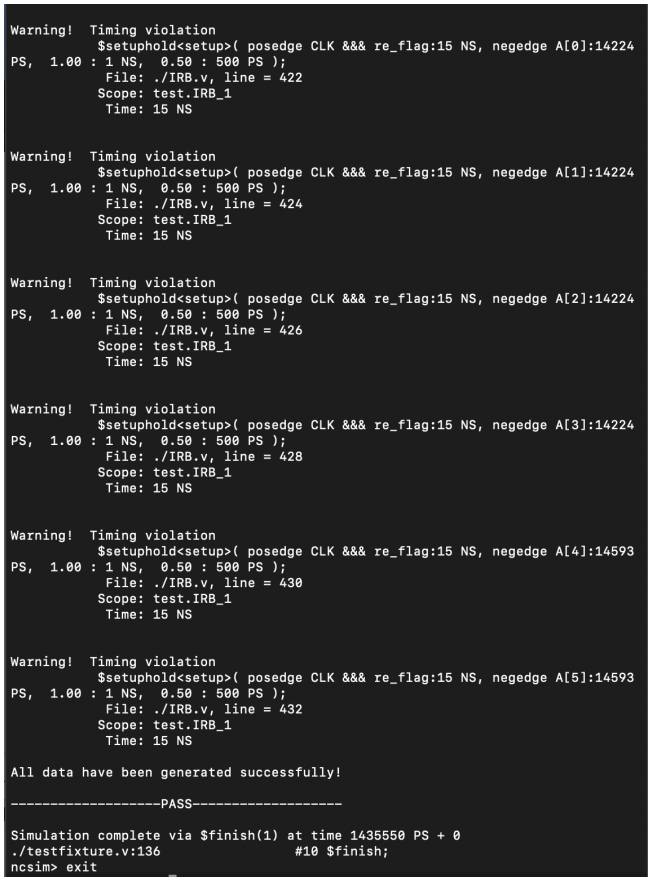
```
[b05030@cad17 HW4]$ more area.report

****************************************
Report : area
Design : LCD_CTRL
Version: N-2017.09-SP2
Date   : Tue May  7 11:05:42 2019
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.
db)

Number of ports:                         38
Number of nets:                       13336
Number of cells:                      13124
Number of combinational cells:        12530
Number of sequential cells:             594
Number of macros/black boxes:             0
Number of buf/inv:                     2263
Number of references:                    84

Combinational area:            104466.482604
Buf/Inv area:                   13273.667846
Noncombinational area:          19209.475166
Macro/Black Box area:               0.000000
Net Interconnect area:        1919362.783447

Total cell area:               123675.957771
Total area:                   2043038.741218
1
```

③ report_power

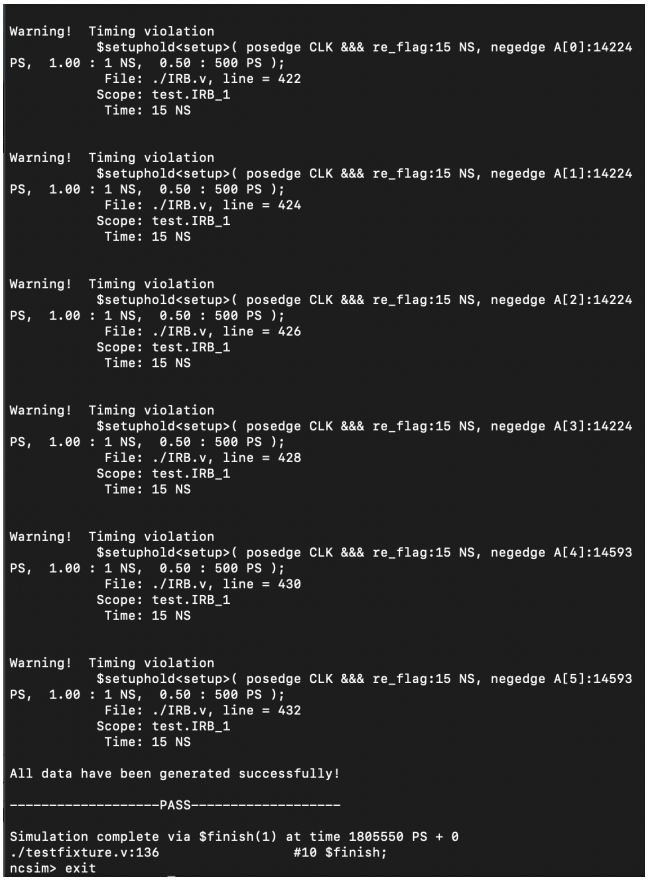
```
****************************************
Report : power
        -analysis_effort low
Design : LCD_CTRL
Version: N-2017.09-SP2
Date   : Tue May  7 11:05:44 2019
****************************************


Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
LCD_CTRL               tsmc13_wl10       slow


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   1.5605 mW   (78%)
  Net Switching Power  = 436.7635 uW   (22%)
                         ---------
Total Dynamic Power    =   1.9973 mW  (100%)

Cell Leakage Power     =  10.8840 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  At
trs
------------------------------------------------------------------------------------------------
---
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           1.5308        1.5743e-02        5.2061e+06            1.5518  (  77.27%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational  2.9676e-02            0.4210        5.6779e+06            0.4564  (  22.73%)
------------------------------------------------------------------------------------------------
---
Total              1.5605 mW         0.4368 mW     1.0884e+07 pW         2.0081 mW
1
```

III. Gate level 模擬通過截圖

- tb1 （左）
- tb2 （右）



```
Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[0]:14224
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 422
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[1]:14224
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 424
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[2]:14224
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 426
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[3]:14224
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 428
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[4]:14593
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 430
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[5]:14593
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 432
          Scope: test.IRB_1
           Time: 15 NS

All data have been generated successfully!

--------------------PASS--------------------

Simulation complete via $finish(1) at time 1435550 PS + 0
./testfixture.v:136               #10 $finish;
ncsim> exit
```



```
Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[0]:14224
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 422
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[1]:14224
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 424
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[2]:14224
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 426
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[3]:14224
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 428
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[4]:14593
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 430
          Scope: test.IRB_1
           Time: 15 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CLK &&& re_flag:15 NS, negedge A[5]:14593
PS,  1.00 : 1 NS,  0.50 : 500 PS );
           File: ./IRB.v, line = 432
          Scope: test.IRB_1
           Time: 15 NS

All data have been generated successfully!

--------------------PASS--------------------

Simulation complete via $finish(1) at time 1805550 PS + 0
./testfixture.v:136               #10 $finish;
ncsim> exit
```