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通過gate-level simulation之cell area report：**1077195.507237 nm²**

```
****************************************
Report : area
Design : CONV
Version: N-2017.09-SP2
Date   : Sun Jun 23 22:05:45 2019
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                          105
Number of nets:                         74579
Number of cells:                        53473
Number of combinational cells:          44812
Number of sequential cells:              8661
Number of macros/black boxes:               0
Number of buf/inv:                       4537
Number of references:                      60

Combinational area:             798221.037068
Buf/Inv area:                    18248.747163
Noncombinational area:          278974.470169
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:               1077195.507237
Total area:                 undefined
1
```

通過gate-level simulation之clock cycle time (ns): **8.0ns**

```
`timescale 1ns/10ps
`define CYCLE      8.0           // Modify your clock period here
`define SDFFILE    "./syn/CONV_syn_8_0.sdf"       // Modify your sdf file name
`define End_CYCLE  10000000           // Modify cycle times once your design need more cycle times!
```

通過post-layout simulation之clock cycle time (ns)：**8.35ns**

```
`timescale 1ns/10ps
`define CYCLE      8.35          // Modify your clock period here
`define SDFFILE    "./CONV_APR_last.sdf"          // Modify your sdf file name
`define End_CYCLE  10000000           // Modify cycle times once your design need more cycle times!
```