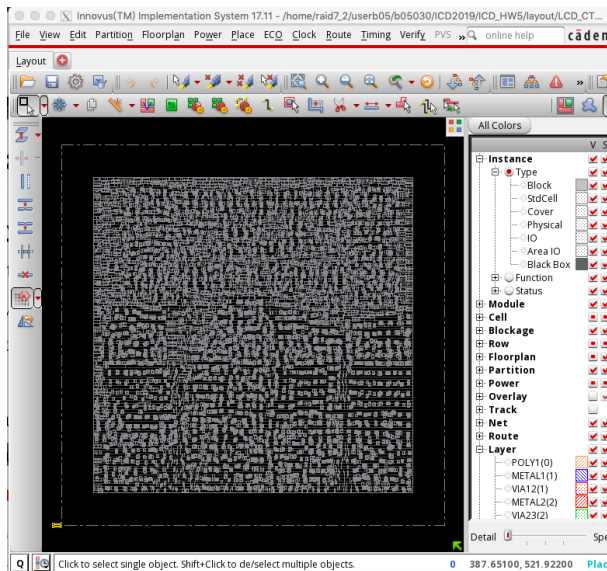


Report

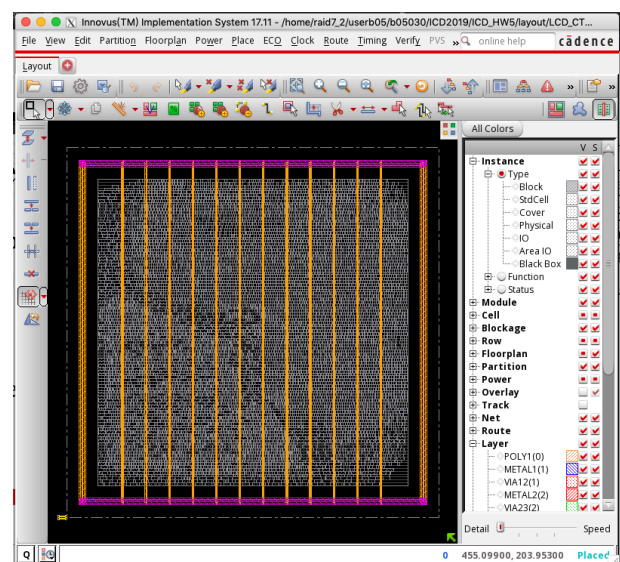
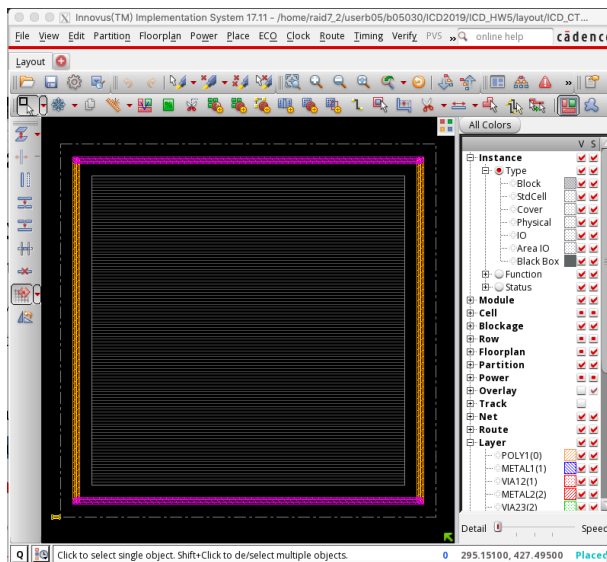
B05901030 電機三 陳欽安

I. Innovus 步驟截圖

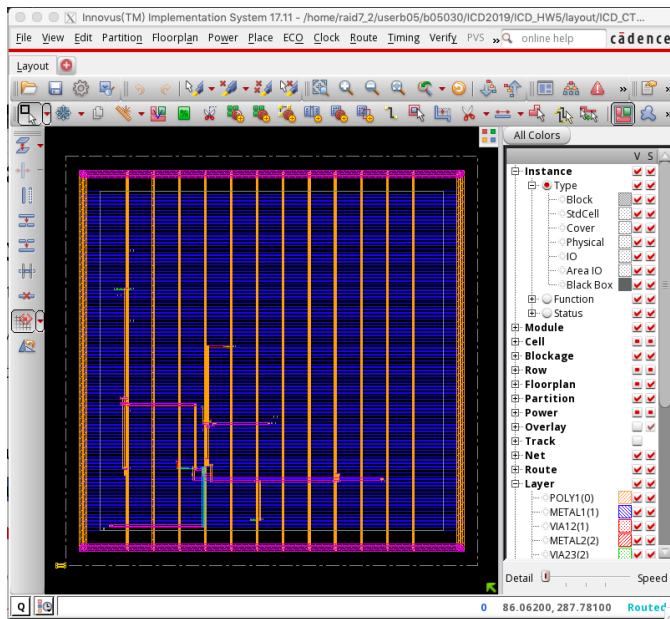
A. Floorplan



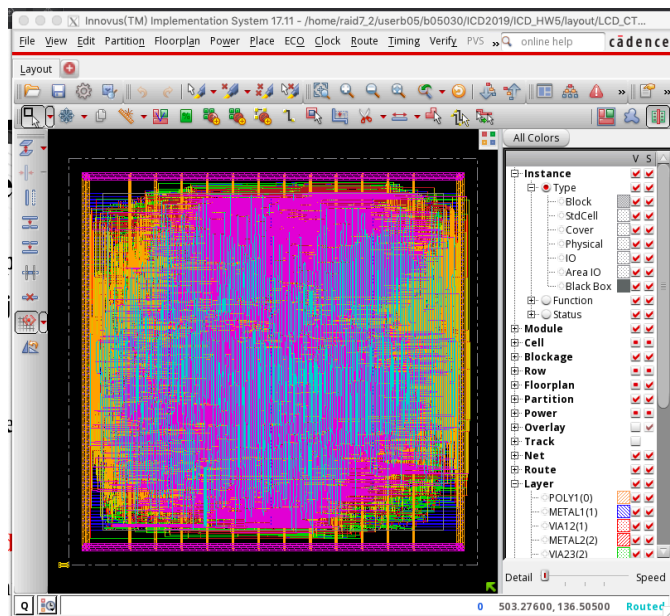
B. Power ring (left) & Power stripe (right)



C. Special Route



D. NanoRoute



II. Post-APR simulation 通過截圖

```
ICD_HW4 — b05030@cad17:ICD_HW5 — ssh -X b05030@140.112.20.60 — 80...
8)
*Verdi* WARNING: [NoReadAccess][FilterOut]Name:test.IROM_1.irom_1.LAST_NOT_A(48)
*Verdi* WARNING: [NoReadAccess][FilterOut]Name:test.IROM_1.irom_1.LAST_NOT_CLK_P
ER(48)
*Verdi* WARNING: [NoReadAccess][FilterOut]Name:test.IROM_1.irom_1.LAST_NOT_CLK_M
INH(48)
*Verdi* WARNING: [NoReadAccess][FilterOut]Name:test.IROM_1.irom_1.LAST_NOT_CLK_M
INL(48)
*Verdi* WARNING: The above messages are printed 50 times. No more similar messag
e will be printed out.
*Verdi* WARNING: [NoReadAccess][FilterOut]Name:test.IROM_1.irom_1.LATCHED_CEN(48
)
*Verdi* WARNING: [NoReadAccess][FilterOut]Name:test.IRB_1.mem(116)
*Verdi* : End of traversing.
All data have been generated successfully!

-----PASS-----

Simulation complete via $finish(1) at time 1436600 PS + 0
./testfixture.v:136          #10 $finish;
ncsim> exit
[b05030@cad17 ICD_HW5]$
```

III. 通過 Post-APR simulation 的 cycle time

Cycle time = 10.0 ns

testfixture.v

```
`timescale 1ns/10ps
`define CYCLE      10.0           // Modify your clock period here
```

lcd_ctrl_APR.v

```
# You can only modify clock period

set cycle 10
```