NAND3

VDD = 2.0 V

temperature = 25℃

NMOS: W/L = 2160n/360n

PMOS: W/L = 1440n/360n

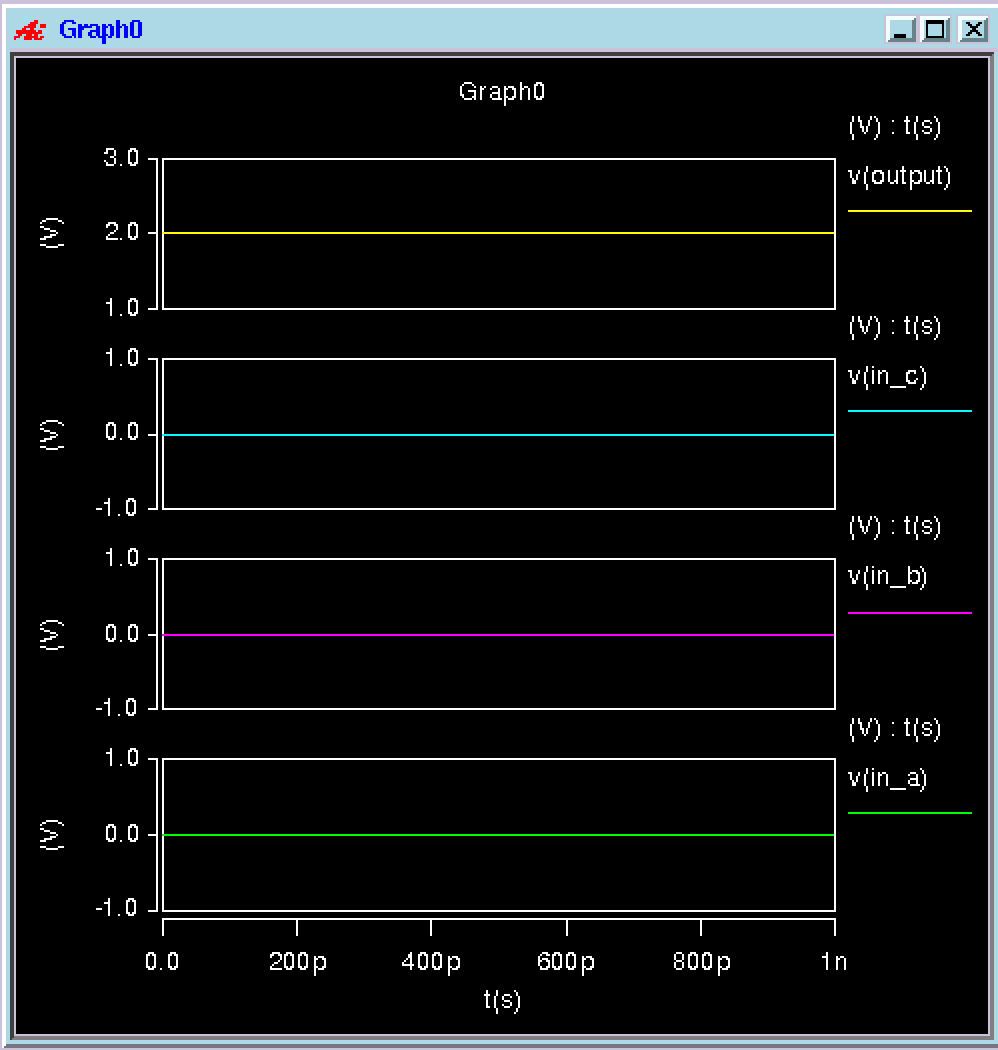
input nodes: in\_a, in\_b, in\_c

output node: output

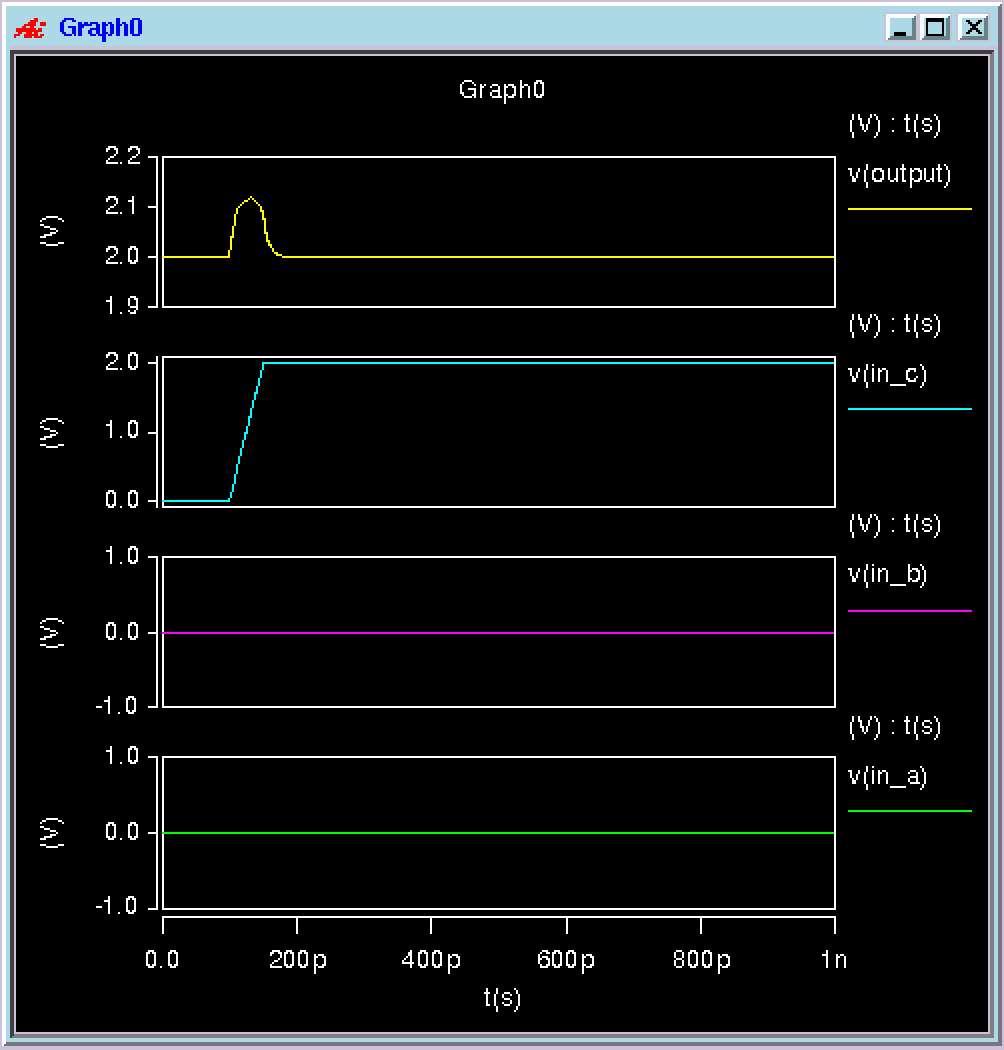
voltage source for input nodes: piecewise linear(pwl)

CASES: logic 0-> 0V; logic1->2.0V

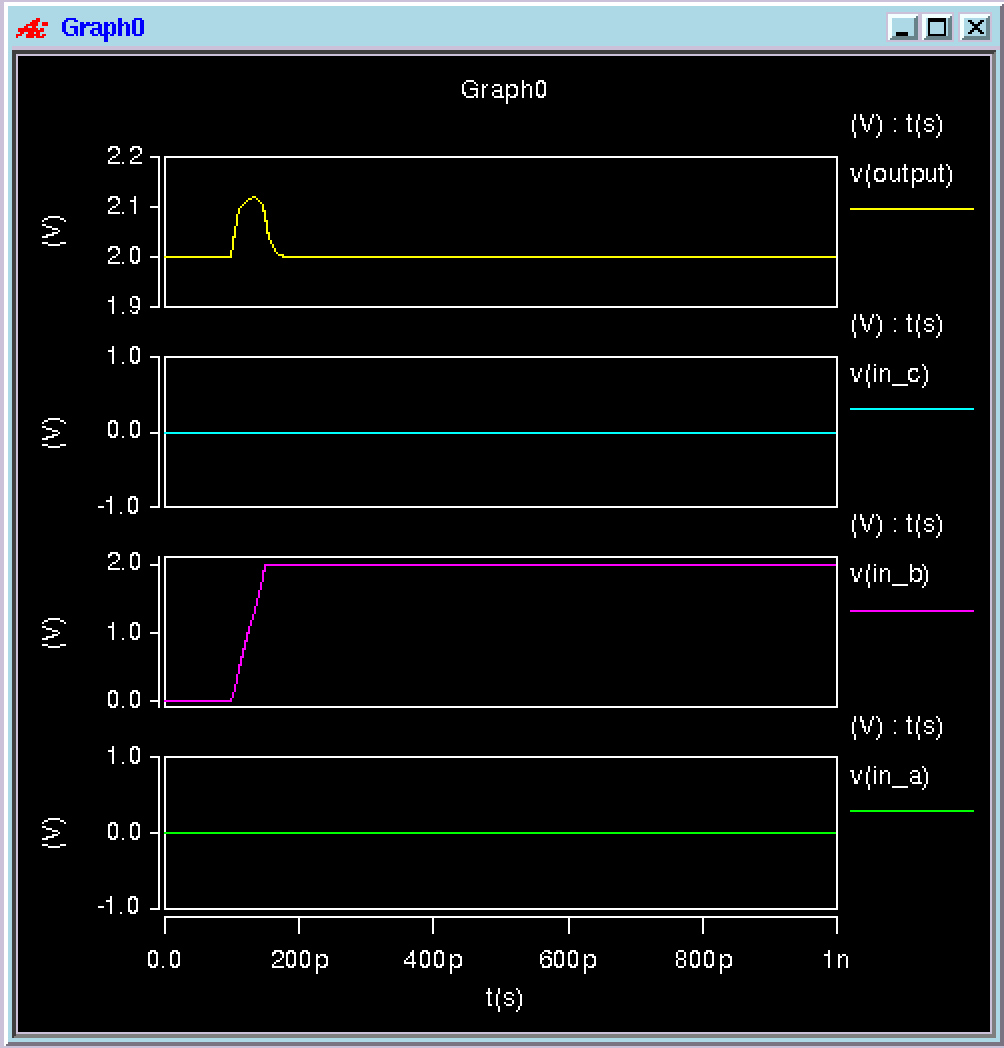
1. (a,b,c) = (0,0,0) -> (abc)’ = 1



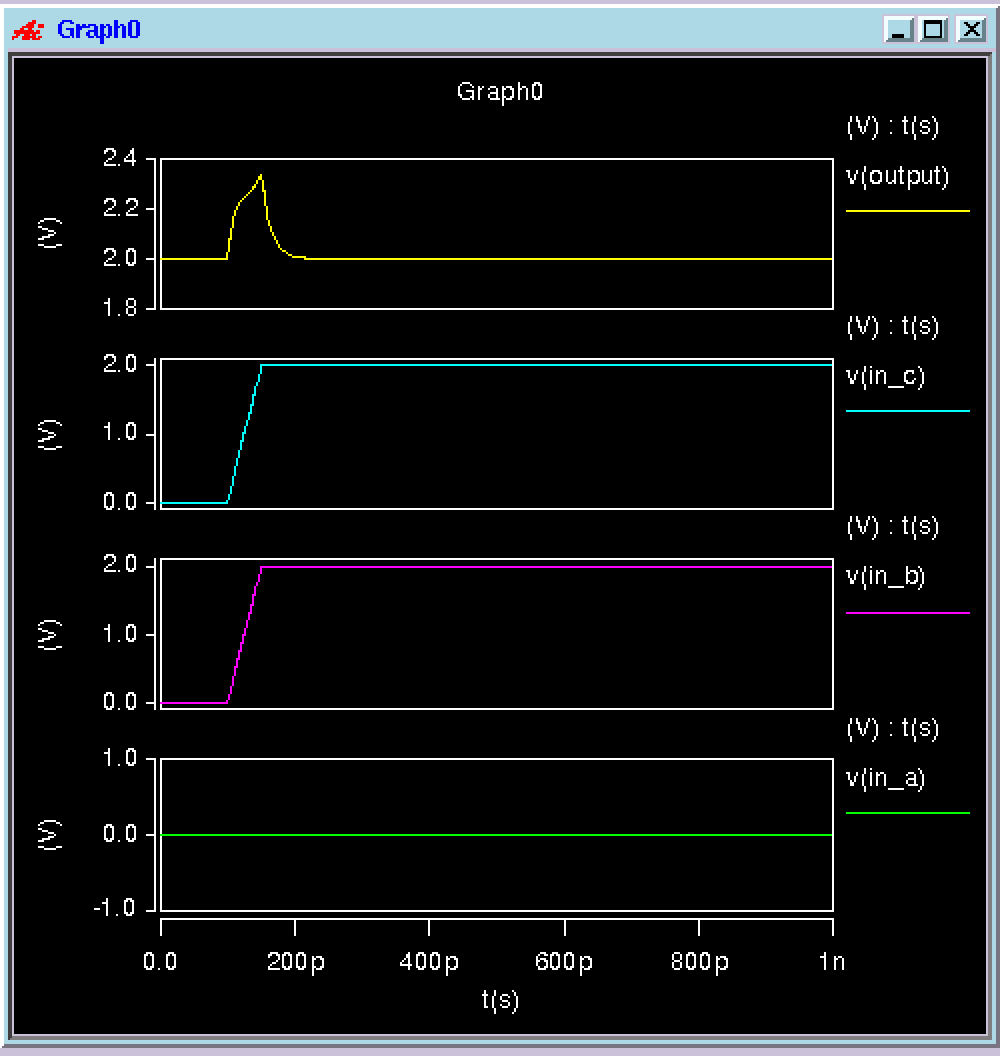
1. (a,b,c) = (0,0,1) -> (abc)’ = 1



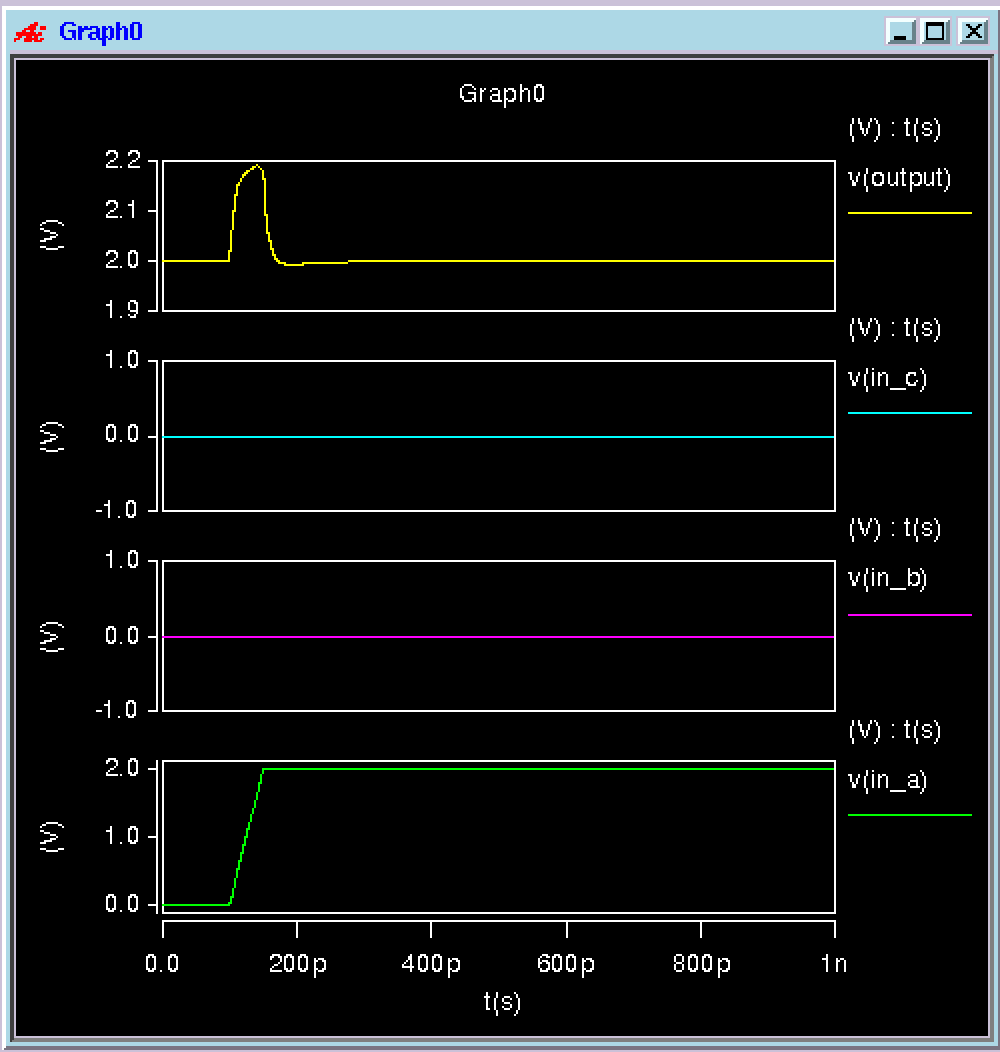
1. (a,b,c) = (0,1,0) -> (abc)’ = 1



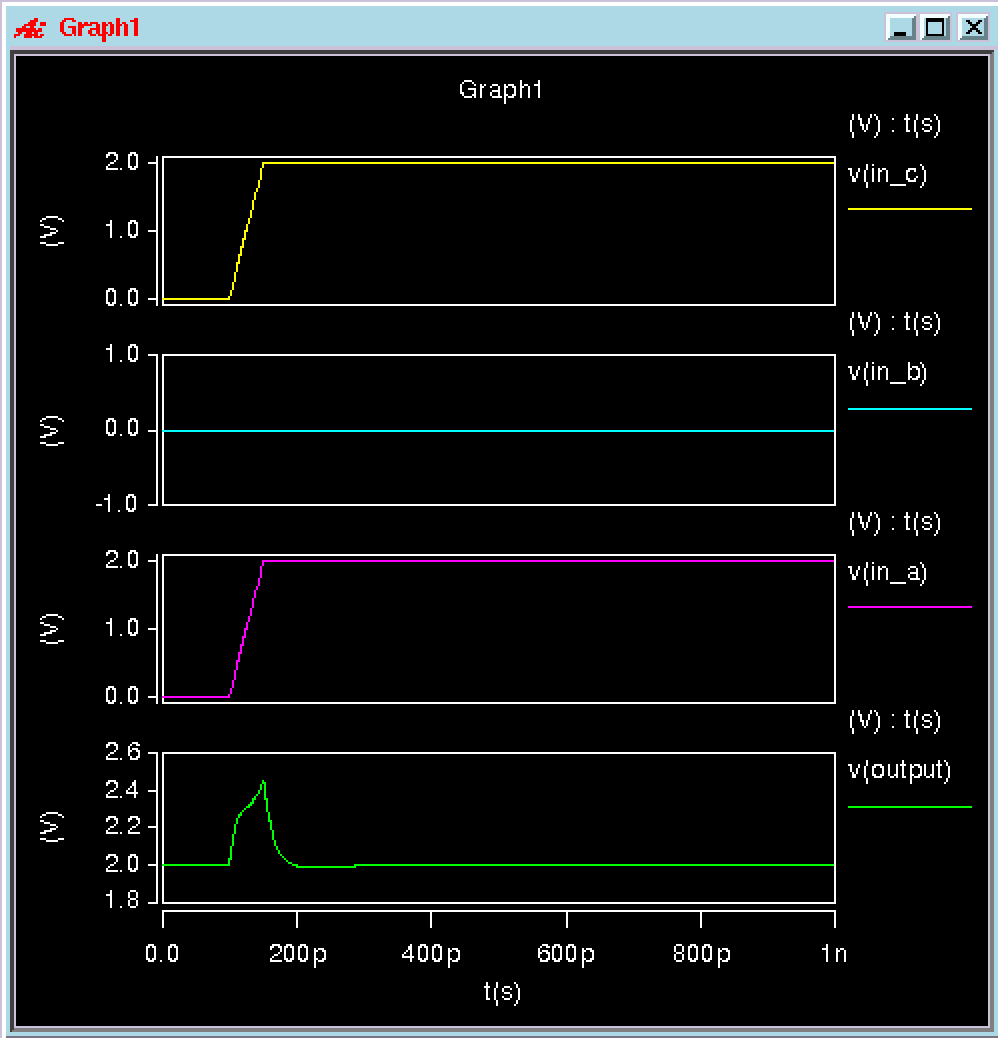
1. (a,b,c) = (0,1,1) -> (abc)’ = 1



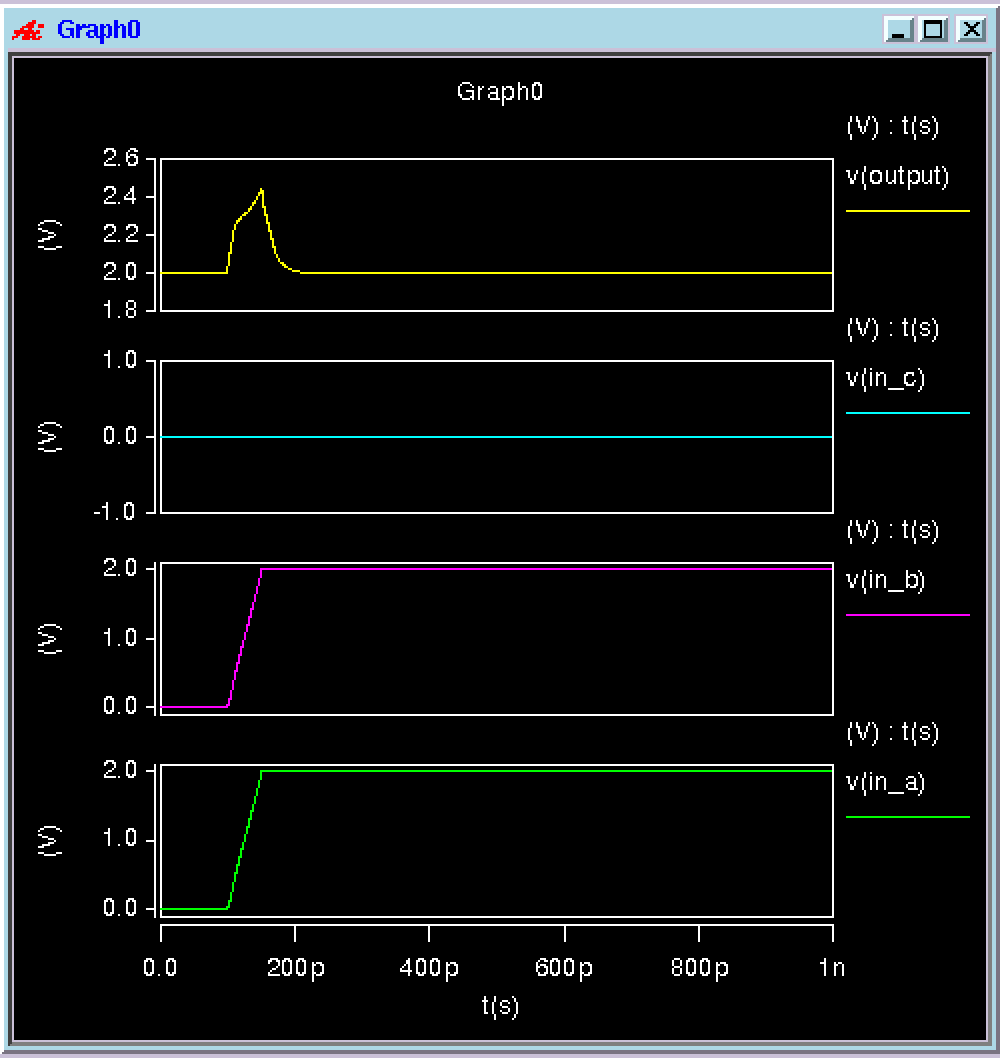
1. (a,b,c) = (1,0,0) -> (abc)’ = 1



1. (a,b,c) = (1,0,1) -> (abc)’ = 1



1. (a,b,c) = (1,1,0) -> (abc)’ = 1



1. (a,b,c) = (1,1,1) -> (abc)’ = 0

