

- Low $r_{DS(on)}$. . . 5 Ω Typical
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Devices Are Cascadable
- Low Power Consumption

description

The TPIC6B595 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

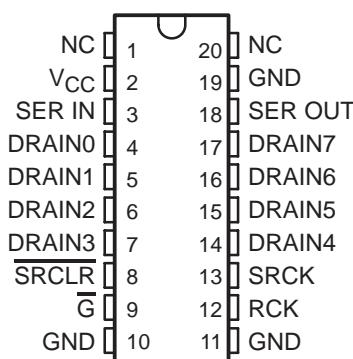
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear (\overline{SRCLR}) is high. When \overline{SRCLR} is low, the input shift register is cleared. When output enable (\overline{G}) is held high, all data in the output buffers is held low and all drain outputs are off. When \overline{G} is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_C = 25^\circ\text{C}$. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B595 is characterized for operation over the operating case temperature range of -40°C to 125°C .

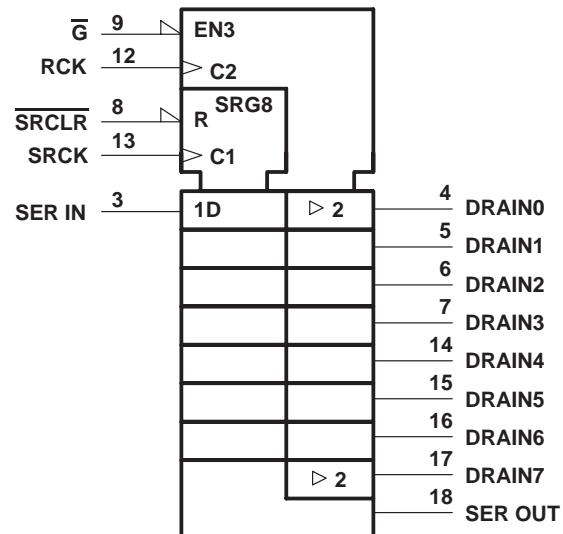
DW OR N PACKAGE

(TOP VIEW)



NC – No internal connection

logic symbol†

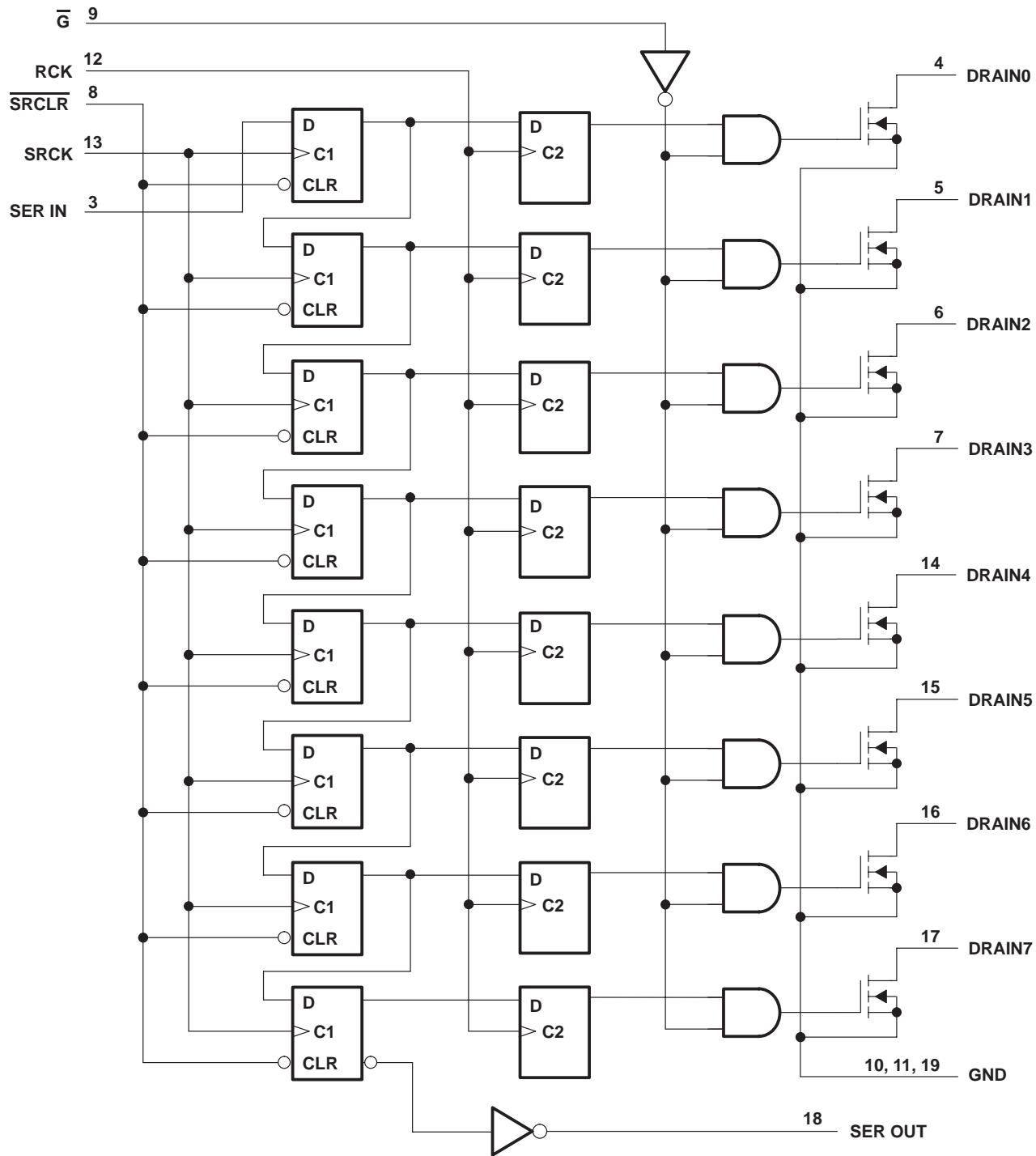


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

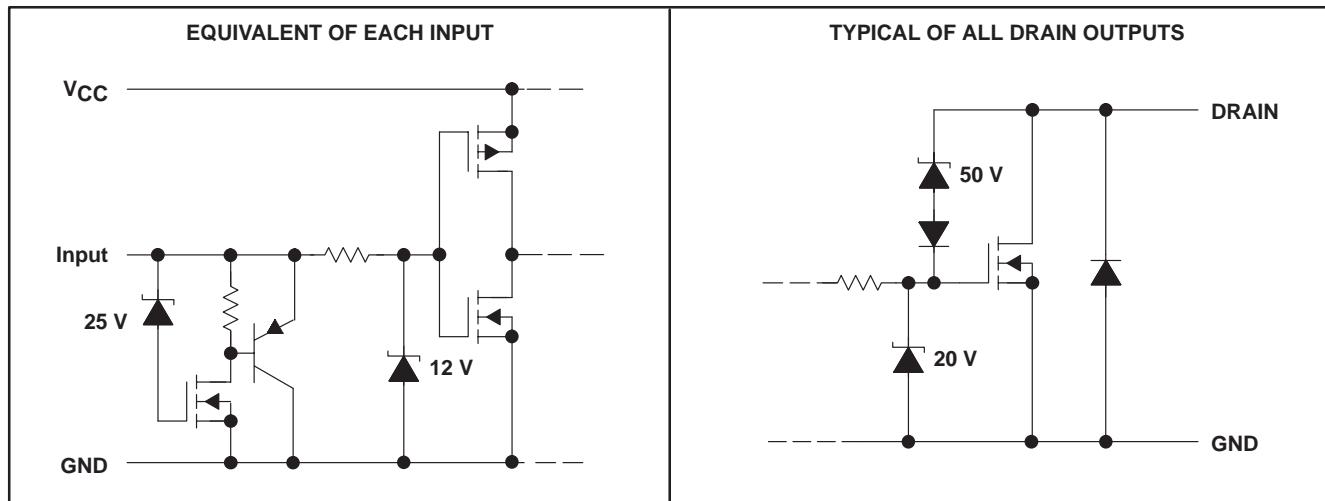
TPIC6B595 POWER LOGIC 8-BIT SHIFT REGISTER

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logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)[†]

Logic supply voltage, V _{CC} (see Note 1)	7 V
Logic input voltage range, V _I	-0.3 V to 7 V
Power DMOS drain-to-source voltage, V _{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I _D , T _C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I _D , T _C = 25°C	150 mA
Peak drain current single output, I _{DM} , T _C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E _{AS} (see Figure 4)	30 mJ
Avalanche current, I _{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T _J	-40°C to 150°C
Operating case temperature range, T _C	-40°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. Each power DMOS source is internally connected to GND.

3. Pulse duration $\leq 100 \mu\text{s}$ and duty cycle $\leq 2\%$.

4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	T _C ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _C = 25°C	T _C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

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recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}	0.15 V_{CC}		V
Pulsed drain output current, $T_C = 25^\circ C$, $V_{CC} = 5 V$ (see Notes 3 and 5)	-500	500	mA
Setup time, SER IN high before SRCK↑, t_{SU} (see Figure 2)	20		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	20		ns
Pulse duration, t_w (see Figure 2)	40		ns
Operating case temperature, T_C	-40	125	°C

electrical characteristics, $V_{CC} = 5 V$, $T_C = 25^\circ C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-to-source breakdown voltage	$I_D = 1 \text{ mA}$		50			V
V_{SD} Source-to-drain diode forward voltage	$I_F = 100 \text{ mA}$		0.85	1		V
V_{OH} High-level output voltage, SER OUT	$I_{OH} = -20 \mu\text{A}$, $V_{CC} = 4.5 \text{ V}$		4.4	4.49		V
	$I_{OH} = -4 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$		4	4.2		
V_{OL} Low-level output voltage, SER OUT	$I_{OL} = 20 \mu\text{A}$, $V_{CC} = 4.5 \text{ V}$		0.005	0.1		V
	$I_{OL} = 4 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$		0.3	0.5		
I_{IH} High-level input current	$V_{CC} = 5.5 \text{ V}$, $V_I = V_{CC}$			1		μA
I_{IL} Low-level input current	$V_{CC} = 5.5 \text{ V}$, $V_I = 0$			-1		μA
I_{CC} Logic supply current	$V_{CC} = 5.5 \text{ V}$	All outputs off	20	100		μA
		All outputs on	150	300		
$I_{CC(FRQ)}$ Logic supply current at frequency	$f_{SRCK} = 5 \text{ MHz}$, $C_L = 30 \text{ pF}$, All outputs off, See Figures 2 and 6		0.4	5		mA
I_N Nominal current	$V_{DS(on)} = 0.5 \text{ V}$, $I_N = I_D$, $T_C = 85^\circ C$	See Notes 5, 6, and 7		90		mA
I_{DSX} Off-state drain current	$V_{DS} = 40 \text{ V}$, $V_{CC} = 5.5 \text{ V}$		0.1	5		μA
	$V_{DS} = 40 \text{ V}$, $V_{CC} = 5.5 \text{ V}$, $T_C = 125^\circ C$		0.15	8		
$r_{DS(on)}$ Static drain-source on-state resistance	$I_D = 100 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$		4.2	5.7		Ω
	$I_D = 100 \text{ mA}$, $T_C = 125^\circ C$, $V_{CC} = 4.5 \text{ V}$		6.8	9.5		
	$I_D = 350 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$		5.5	8		

- NOTES:
- 3. Pulse duration $\leq 100 \mu\text{s}$ and duty cycle $\leq 2\%$.
 - 5. Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.
 - 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
 - 7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^\circ C$.



switching characteristics, $V_{CC} = 5 \text{ V}$, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from \bar{G}	$C_L = 30 \text{ pF}$, $I_D = 100 \text{ mA}$, See Figures 1, 2, and 9	150			ns
t_{PHL} Propagation delay time, high-to-low-level output from \bar{G}		90			ns
t_r Rise time, drain output		200			ns
t_f Fall time, drain output		200			ns
t_a Reverse-recovery-current rise time	$I_F = 100 \text{ mA}$, $dI/dt = 20 \text{ A}/\mu\text{s}$, See Notes 5 and 6 and Figure 3	100			ns
t_{rr} Reverse-recovery time		300			

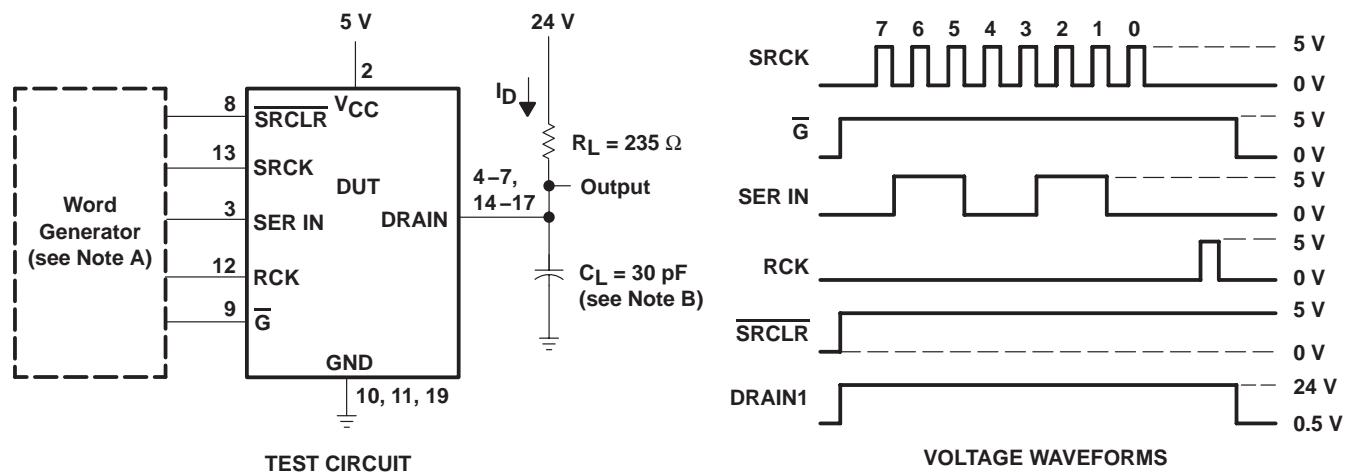
NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$ Thermal resistance, junction-to-ambient	DW package	90		°C/W
	N package	95		

PARAMETER MEASUREMENT INFORMATION



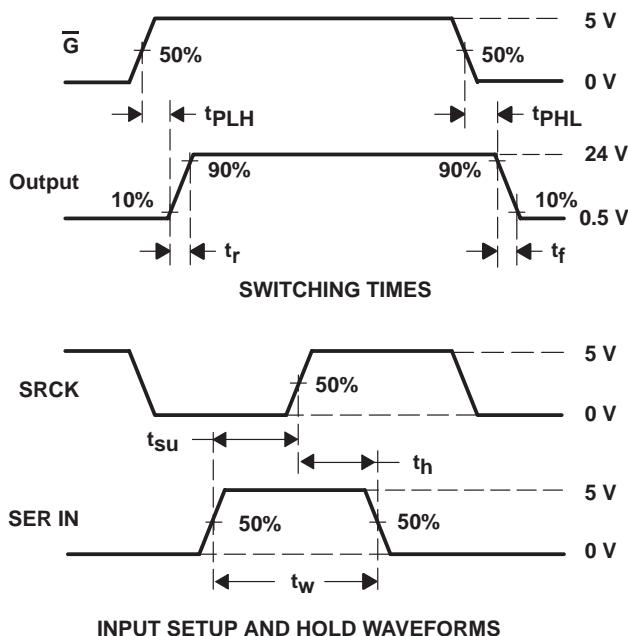
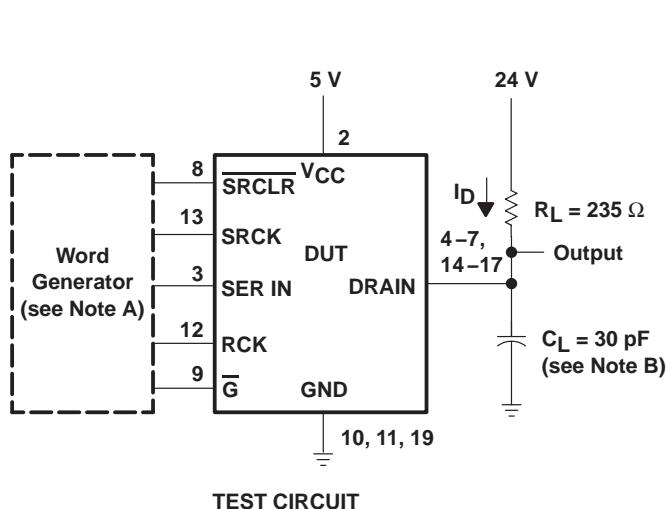
NOTES: A. The word generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_w = 300 \text{ ns}$, pulsed repetition rate (PRR) = 5 kHz, $Z_0 = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

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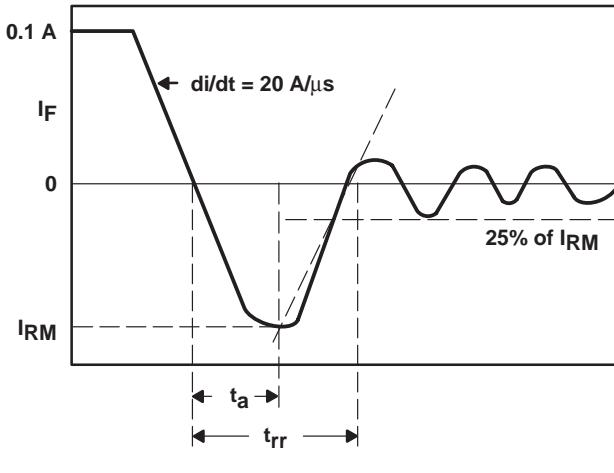
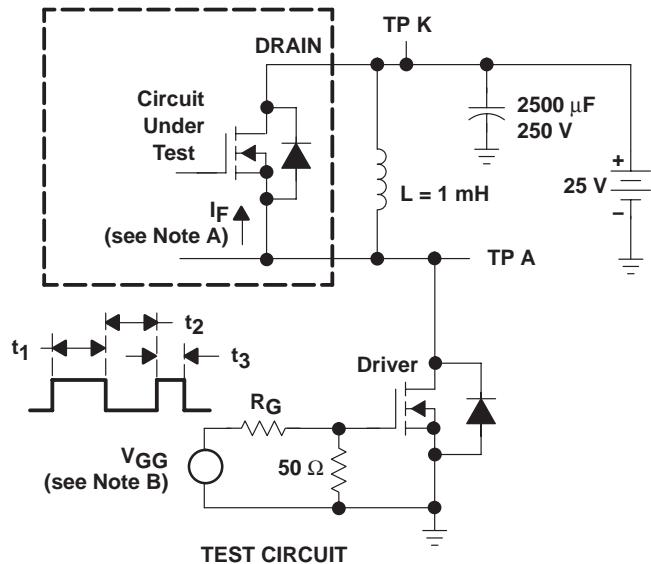
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

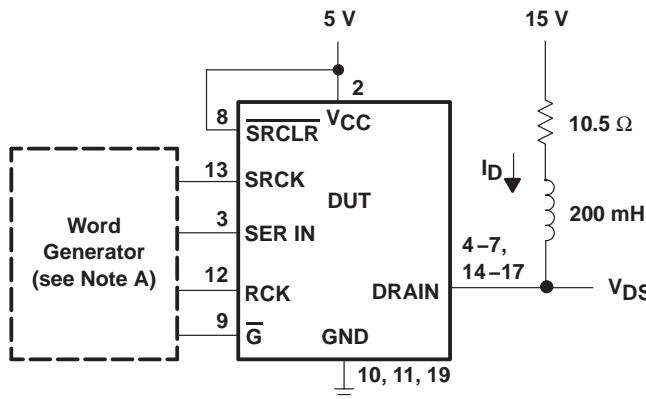
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms



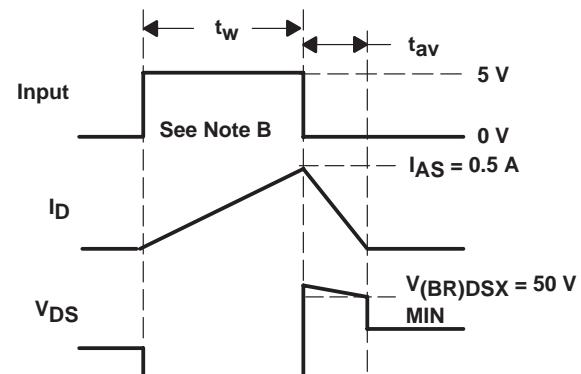
- NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
 B. The V_{GG} amplitude and R_G are adjusted for $di/dt = 20$ A/ μ s. A V_{GG} double-pulse train is used to set $I_F = 0.1$ A, where $t_1 = 10 \mu$ s, $t_2 = 7 \mu$ s, and $t_3 = 3 \mu$ s.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50$ Ω.
 B. Input pulse duration, t_W , is increased until peak current $I_{AS} = 0.5$ A.
 Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

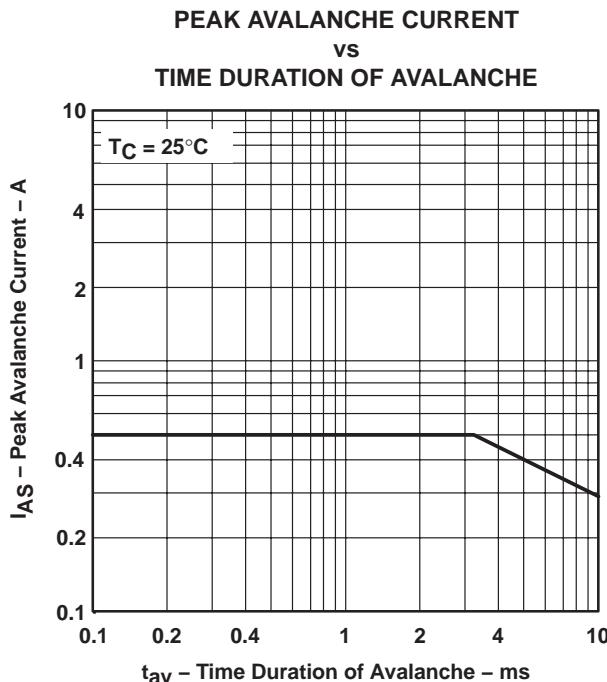


Figure 5

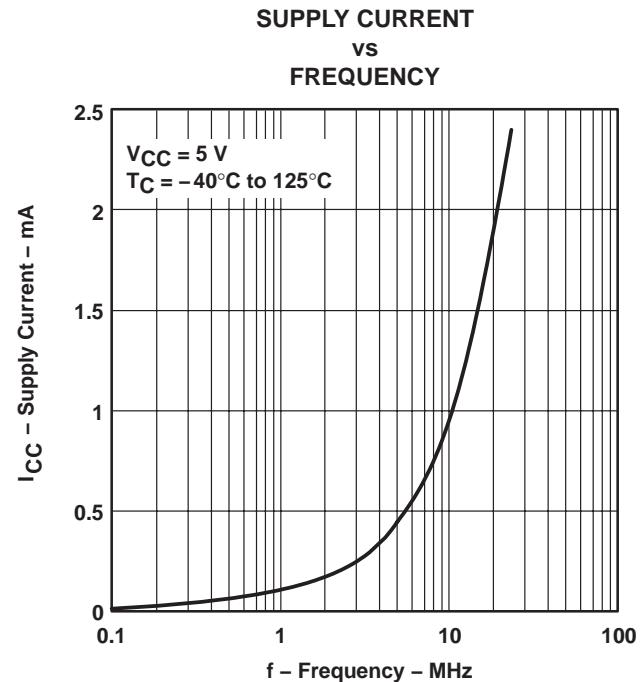


Figure 6

TPIC6B595

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TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

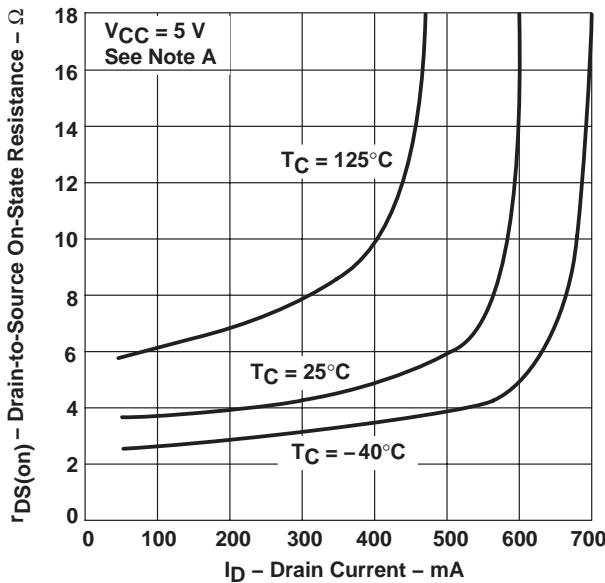


Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
LOGIC SUPPLY VOLTAGE

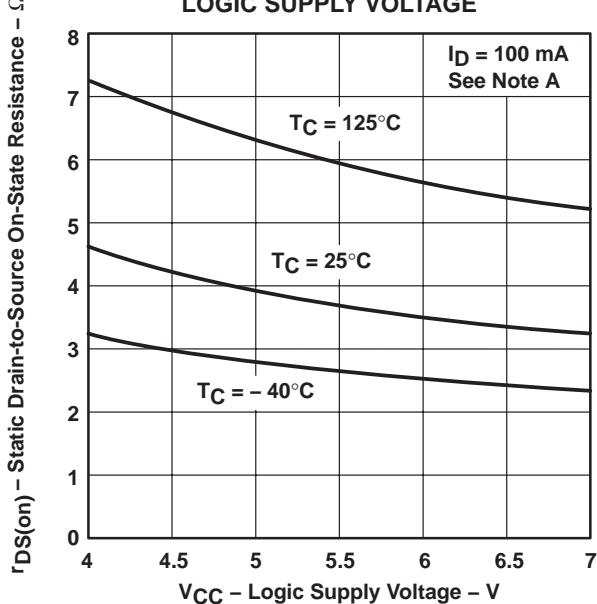


Figure 8

SWITCHING TIME
vs
CASE TEMPERATURE

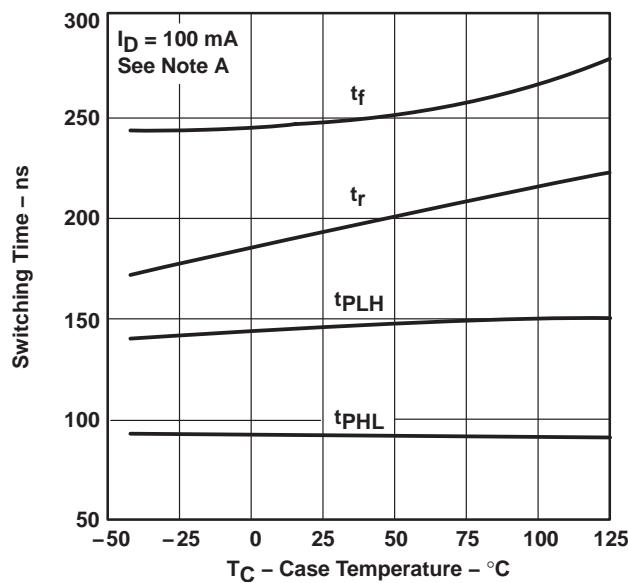


Figure 9

NOTE C: Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

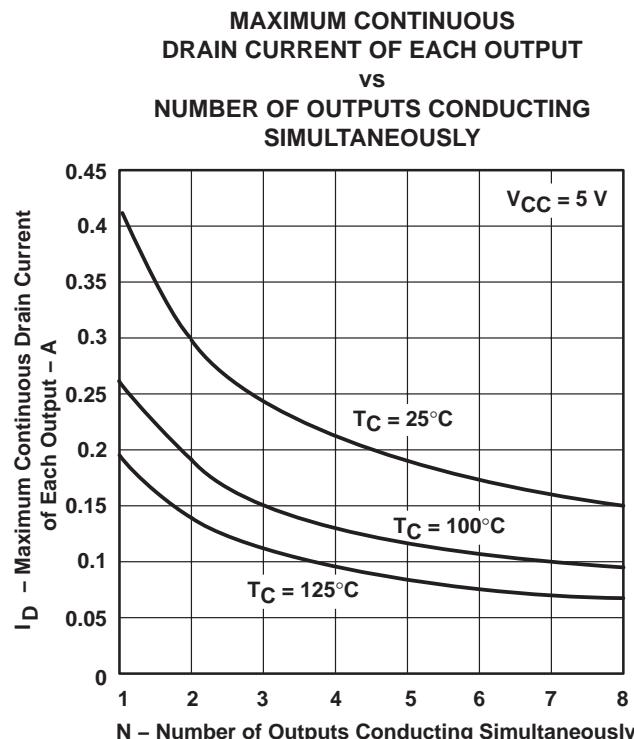


Figure 10

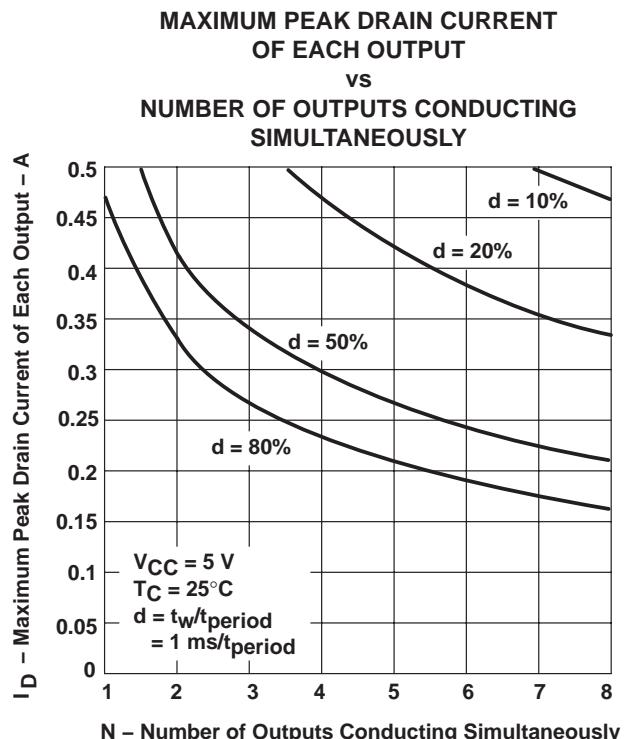


Figure 11

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
5/18/05	A	5	Figure 1	Changed SRCLR timing diagram
7/1995	*			Original reversion

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPIC6B595DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6B595DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6B595DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6B595DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPIC6B595N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

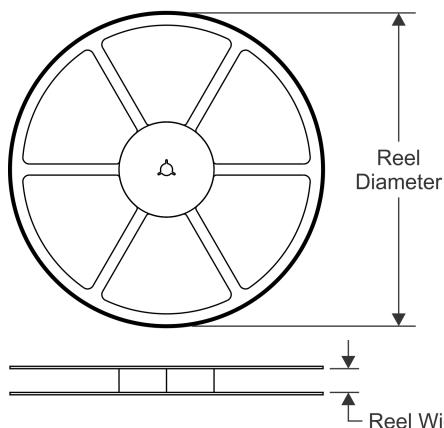
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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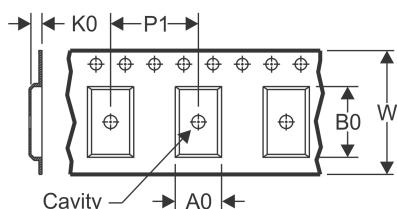
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

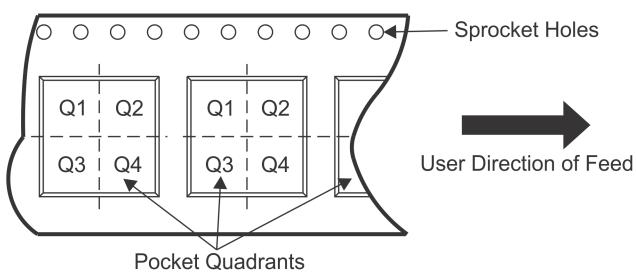


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

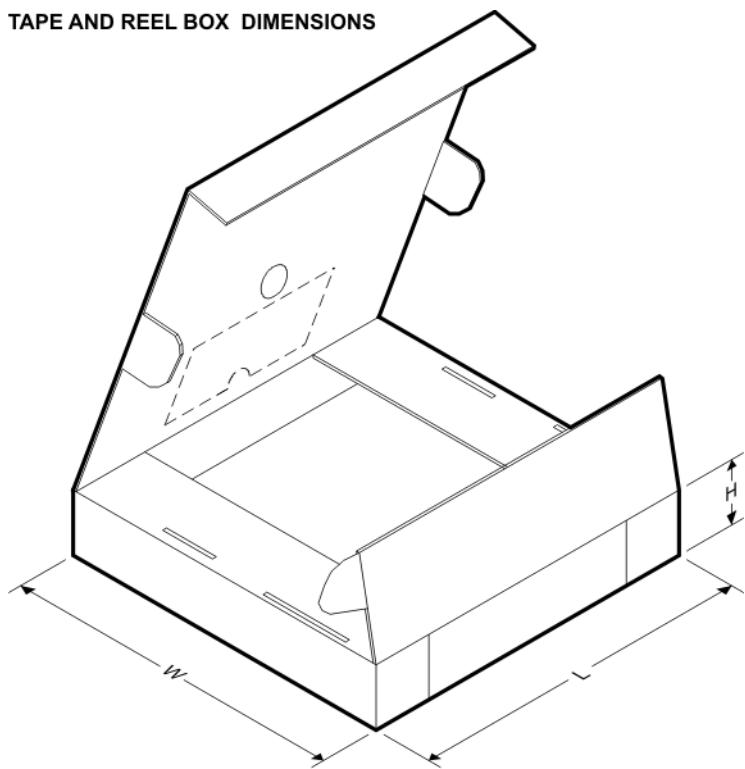
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6B595DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



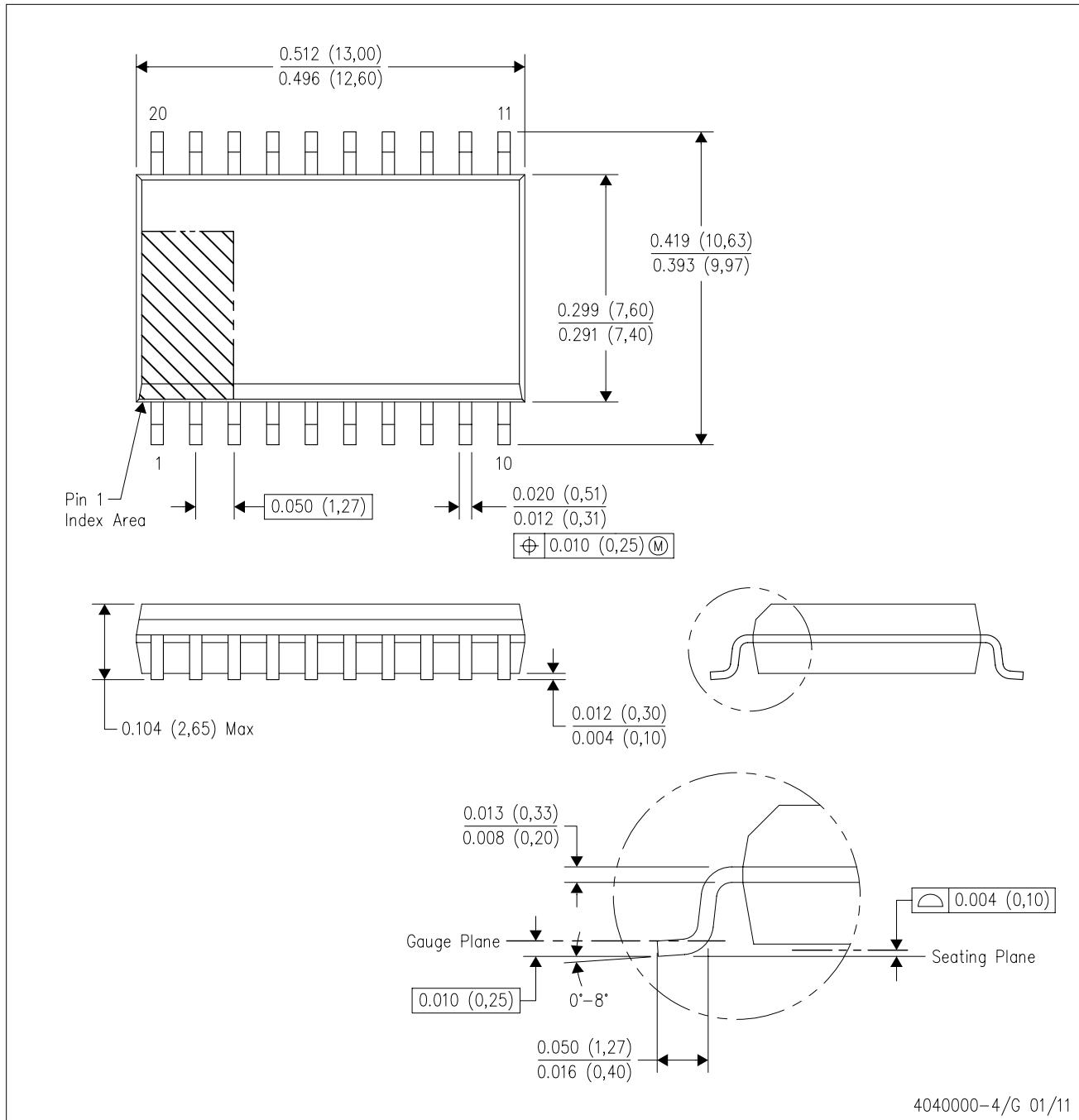
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6B595DWR	SOIC	DW	20	2000	367.0	367.0	45.0

MECHANICAL DATA

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



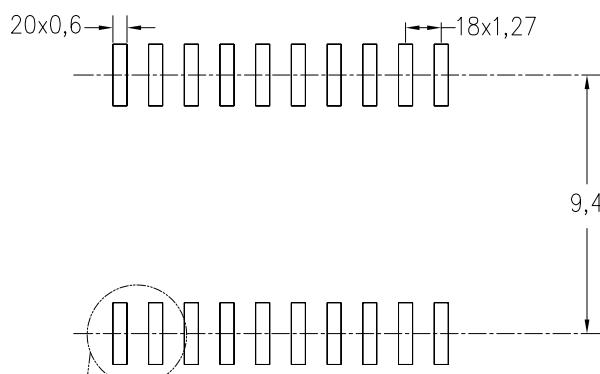
- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
 - D. Falls within JEDEC MS-013 variation AC.

LAND PATTERN DATA

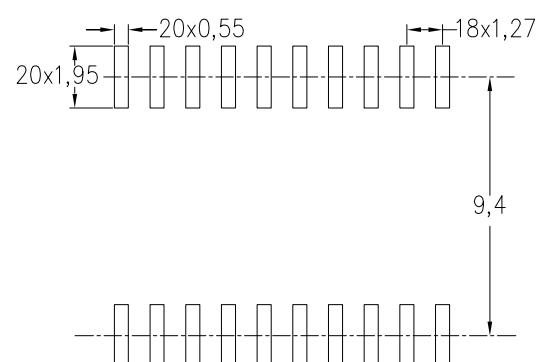
DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

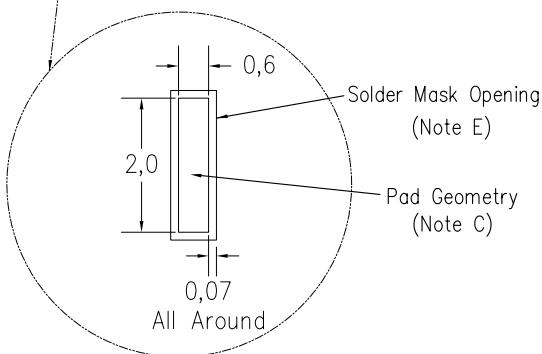
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Non Solder Mask Define Pad



4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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