Code	Domain	Title	Responsible	Duration	Deliverables	Prerequisites	Description	Required Resources/Facilities	Predecessor WPs:	Successor WPs	Completeness
SD.TTC.DES.01.00	TTC	**Creation and Testing of Downlink Communications System**	RF Specialist	1 Year 4 months	Downlink communications system design	STRATHcube mission documentation	Evaluation of requirements, implementation on engineering model, integration with PPL system and performance testing	Mission documentation, Target SDR documentation, MATLAB, Simulink, Vivado, Python, C++, Static analysis tools, FPGA Development board, transceiver development board	N/A	N/A	50%
SD.TTC.DES.01.01	TTC	**Assess STRATHcube Communication System Work to Date**	RF Specialist	2 weeks	Literature review of STRATHcube communication system	STRATHcube mission documentation	Evaluate current state of communication system to identify progress, gaps and requirements	Mission documentation	N/A	SD.TTC.DES.01.04	100%
SD.TTC.DES.01.02	TTC	**Review DVB-S2 Standard and Relevant Communication Standards**	RF Specialist	2 weeks	Literature review of relevant standards	None	Analyse DVB-S2 system, determine suitability to mission, identify suitable architecture	Standards Documents	N/A	SD.TTC.DES.01.06	100%
SD.TTC.DES.01.03	TTC	**Research DVB-S2 SDR Implementations**	RF Specialist	1 month	Literature review of previous implementations	None	Research previous implementations of DVB-S2 transmitters on SDR	Research Papers, Open Source Repositories	N/A	SD.TTC.DES.01.06	100%
SD.TTC.DES.01.04	TTC	**Functional Requirement Generation for Downlink Communication System**	RF Specialist, Systems Engineer	1 week	Functional Requirements	SD.TTC.DES.01.01, SD.TTC.DES.01.02, SD.TTC.DES.01.03	Collaborate with Systems Engineers to develop functional requirements for system development.	N/A	N/A	SD.TTC.DES.01.06	100%
SD.TTC.DES.01.05	TTC	**Review of Target SDR Hardware**	RF Specialist	1 week	FPGA resource requirements, identification of suitable development boards for engineering model	None	Investigate available documentation regarding the target SDR platform to evaluate FPGA resources and design requirements.	Target SDR Documentation	N/A	SD.TTC.DES.01.06	100%
SD.TTC.DES.01.06	TTC	**Downlink Communications Architecture Development**	RF Specialist	3 months	High level end to end system design document for downlink transmitter	SD.TTC.DES.01.02, SD.TTC.DES.01.03, SD.TTC.DES.01.04	Identification of all blocks required to implement downlink communication system. Identification of suitable resources to aid implementation.	N/A	SD.TTC.DES.01.02, SD.TTC.DES.01.03, SD.TTC.DES.01.04	SD.TTC.DES.01.07, SD.TTC.DES.01.09	100%
SD.TTC.DES.01.07	TTC	**Implement DVB-S2 Transmitter on Engineering Model (Programmable Logic)**	RF Specialist	3 months	DVB-S2 Transmitter FPGA Implementation	SD.TTC.DES.01.06	Creation of FPGA design to implement DVB-S2 Transmission System	MATLAB, Simulink, Vivado	SD.TTC.DES.01.06	SD.TTC.DES.01.8	50%
SD.TTC.DES.01.08	TTC	**Validation of DVB-S2 Transmitter on Engineering Model (Programmable Logic)**	RF Specialist	1 month	Validated DVB-S2 Transmitter Design	SD.TTC.DES.01.07	Validation of implemented DVB-S2 transmitter to ensure adherence to standard and suitability.	MATLAB, Simulink, Vivado	SD.TTC.DES.01.07	SD.TTC.DES.01.11	0%
SD.TTC.DES.01.09	TTC	**Implementation of Packet Handling on Engineering Model (Processing System)**	RF Specialist	1 month	Packet Handling System Software Implementation	SD.TTC.DES.01.06	Implementation of the packet handling system in software	Python, C++	SD.TTC.DES.01.06, SD.TTC.DES.01.08	SD.TTC.DES.01.10	0%
SD.TTC.DES.01.10	TTC	**Validation of Packet Handling on Engineering Model (Processing System)**	RF Specialist	1 month	Validated Packet Handling Software	SD.TTC.DES.01.09	Validation of packet handling system in software.	Python, C++, Static Analysis Tools	SD.TTC.DES.01.09	SD.TTC.DES.01.11	0%
SD.TTC.DES.01.11	TTC	**Downlink Engineering Model End to End Testing**	RF Specialist	1 month	Downlink Engineering Model Test Report	SD.TTC.DES.01.06, SD.TTC.DES.01.08	Validation of entire system in hardware.	Appropriate FPGA development board, Appropriate transceiver development board	SD.TTC.DES.01.06, SD.TTC.DES.01.08	SD.TTC.DES.01.12	0%
SD.TTC.DES.01.12	TTC	**Combination of PPL and Primary Downlink on Engineering Model**	RF Specialist, PBR Specialist	1 month	Engineering model of combined PPL and downlink communications system	SD.TTC.DES.01.11, SD.PPL.PRF.03.06	Combine PPL and Downlink FPGA design	Appropriate FPGA development board, Appropriate transceiver development board	SD.TTC.DES.01.11, SD.PPL.PRF.03.06	SD.TTC.DES.01.13	0%
SD.TTC.DES.01.13	TTC	**Analyse FPGA Resource Usage of PPL System and Downlink System on Engineering Model**	RF Specialist, PBR Specialist	2 weeks	Resource Usage Report of combined design	SD.TTC.DES.01.12	Ensure that both designs can fit on target FPGA. Optimising as necessary.	Appropriate FPGA development board, Appropriate transceiver development board	SD.TTC.DES.01.12	SD.TTC.DES.01.14	0%
SD.TTC.DES.01.14	TTC	**End to End Testing of Combined PPL and Downlink System on Engineering Model**	RF Specialist, PBR Specialist	1 month	Test report of combined design	SD.TTC.DES.01.13	Ensure both systems work as expected when combined	Appropriate FPGA development board, Appropriate transceiver development board	SD.TTC.DES.01.13	SD.TTC.DES.01.15	0%
SD.TTC.DES.01.15	TTC	**End to End Testing of Combined PPL and Downlink System on Target SDR**	RF Specialist, PBR Specialist	3 months	Downlink System Test Report	SD.TTC.DES.01.14	Ensure design works as expected on target SDR.	Target SDR	SD.TTC.DES.01.14	SD.TTC.DES.01.00	0%
SD.TTC.ANL.01.00	GS	**Receiver Analysis and Modelling**	RF Specialist	3 months	Receiver Analysis Results and requirements	Ground station site selection	Modelling of receive channel for satellite and subsequent receiver requirement	MATLAB, STK, Simulink	GD.GS.TRD.09.00	SD.TTC.DES.02.00	0%
SD.TTC.ANL.01.01	GS	**Channel Research**	RF Specialist	1 month	Interference	Ground station site selection	Identification of relevant literature and model parameters including interference	MATLAB, STK, Simulink	GD.GS.TRD.09.00	SD.TTC.ANL.01.02	0%
SD.TTC.ANL.01.02	GS	**Channel Model Creation**	RF Specialist	1 month	Channel Analysis Results, Link Budget	Ground station site selection	Modelling expected channel with interference for satellite receiver over course of mission. Creation of link budget	MATLAB, STK, Simulink	SD.TTC.ANL.01.01	SD.TTC.ANL.01.03	0%
SD.TTC.ANL.01.03	GS	**Receiver Requirement Generation**	RF Specialist	1 month	Receiver functional and performance requirements	SD.TTC.ANL.01.02			SD.TTC.ANL.01.02	SD.TTC.ANL.01.00	
SD.TTC.DES.02.00	GS	**Primary Uplink Receiver Design & Implementation**	RF Specialist	6 months	Primary uplink receiver system	Ground station site interference analysis, ground station hardware selection	Design and implement receiver system for primary uplink communications with appropriate filtering to improve SINR.	MATLAB, Simulink, GNU Radio, Vivado	SD.TTC.TRD.02.00	None	0%
SD.TTC.DES.02.01	GS	**Receiver Implementation Research**	RF Specialist	1 month	Primary uplimk receiver system architecture, identification of open source resources for development		Research into requirements for receiver, previous implementations	Research papers, STRATHcube documents	N/A	SD.TTC.DES.02.02	0%
SD.TTC.DES.02.02	GS	**Receiver Interference Filter Design**	RF Specialist	3 months	Interference Filter Design	SD.TTC.DES.02.01, SD.TTC.ANL.01.00	Design of anti interference filter based on literature and previous analysis	Interference Report, Research Paper	SD.TTC.DES.02.01, SD.TTC.ANL.01.00	SD.TTC.DES.02.03	0%
SD.TTC.DES.02.03	GS	**Receiver Implementation**	RF Specialist	1 month	Primary uplink receiver design	SD.TTC.DES.02.02	Implementation of primary uplink receiver	GNU Radio, MATLAB, Simulink, C++	SD.TTC.DES.02.02	SD.TTC.DES.02.04	0%

SD.TTC.DES.02.04	GS	**Receiver Testing on Engineering Model**	RF Specialist	1 month	Tested primary uplink receiver design	SD.TTC.DES.02.03, SD.TTC.DES.01.11	Testing of design with synthesised data	Tx capable SDR	SD.TTC.DES.02.03, SD.TTC.DES.01.11	SD.TTC.DES.02.00	0%
SD.TTC.DES.02.04	GS	**Receiver Testing on Target SDR**	RF Specialist	1 month	Tested primary uplink receiver design	SD.TTC.DES.02.03, SD.TTC.DES.01.11	Testing of design with synthesised data	Tx capable SDR	SD.TTC.DES.02.03, SD.TTC.DES.01.11	SD.TTC.DES.02.00	0%
SD.TTC.TRD.02.00	GS	**Uplink System Configuration**	RF Specialist	2 months	Decision for Uplink System Design	SD.TTC.ANL.01.00	Perform tradeoff of options for uplink system	MATLAB, Simulink	SD.TTC.ANL.01.00	SD.TTC.DES.02.00	0%
SD.TTC.TRD.02.01	GS	**Tradeoff of Modulation, Coding Methods and Rates**	RF Specialist	2 weeks	Tradeoff Analysis of uplink modulation, coding method and rates.	SD.TTC.ANL.01.00	Identification of suitable methods, tradeoff report outlining expected performance of each	Channel analysis results	SD.TTC.ANL.01.00	SD.TTC.TRD.02.02	0%
SD.TTC.TRD.02.02	GS	**Recommendation of Uplink System Configuration**	RF Specialist	2 weeks	Final report including methodology, results, and recommendations	SD.TTC.TRD.02.01	Compile all findings and select suitable option.	Tradeoff Analysis Result	SD.TTC.TRD.02.01	SD.TTC.TRD.02.00	0%