TOTEM

27 September 2024 15:12

Interfaces

PC104:
CAN, I2C
CAN: https://www.ti.com/lit/an/sloa101b/sloa101b.pdf?ts=1733044391620&ref_url=https%253A%252F%252Fwww.google.com%252F
1Mbps

I2C:
https://www.nxp.com/docs/en/user-guide/UM10204.pdf

AQWQWAQZWQAWQWQA	XAWX100kbps -> 5Mbps

Debug:
UART + Ethernet

Standard

27 September 2024 15:14

https://www.etsi.org/technologies/dvb-s-s2

ETSI is the standards body that defined DVB-S2

"
DVB-S2X targets the core application areas of DVB-S2 and new application areas requiring very-low carrier-to-noise and carrier-to-interference operation (VL-SNR), such as mobile applications. It also provides format to enable beam hopping operations.

From <https://www.etsi.org/technologies/dvb-s-s2>
"

https://www.etsi.org/deliver/etsi_en/302300_302399/30230701/01.04.01_60/en_30230701v010401p.pdf

ETSI EN 302 307-1 V1.4.1

DVB-S2 Standard

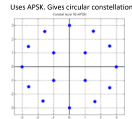
What is DVB-S2

"
• a flexible input stream adapter, suitable for operation with single and multiple input streams of various formats (packetized or continuous);
• a powerful FEC system based on LDPC (Low-Density Parity Check) codes concatenated with BCH codes, allowing Quasi-Error-Free operation at about 0,7 dB to 1 dB from the Shannon limit, depending on the transmission mode (AWGN channel, modulation constrained Shannon limit);
• a wide range of code rates (from 1/4 up to 9/10); 4 constellations, ranging in spectrum efficiency from 2 bit/s/Hz to 5 bit/s/Hz, optimized for operation over non-linear transponders;
• a set of three spectrum shapes with roll-off factors 0,35, 0,25 and 0,20; • Adaptive Coding and Modulation (ACM) functionality, optimizing channel coding and modulation on a frame-by-frame basis.
"

DVB-S2 Defines **FORWARD PATH**. Several Return path implementations:

- DVB-RCS
- DVB-RCP
- DVB-RCG
- DVB-RCC

Uses APSK. Gives circular constellation, QAM gives square.



Transmission System

15 ETSI EN 302 307-1 V1.4.1 (2014-11)

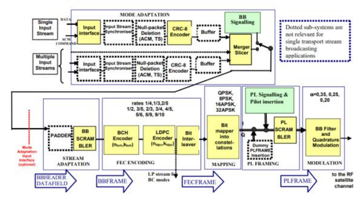


Figure 1: Functional block diagram of the DVB-S2 System

"The System is designed to support source coding as defined in ISO/IEC 13818 [1], TR 101 154 [i.3] and TS 102 005 [i.1]. Data services may be transported in Transport Stream format according to EN 301 192 [4] (e.g. using Multi-protocol Encapsulation), or Generic Stream format."

FEC: "Transport Stream Packet Error Ratio PER< 10-7 before de-multiplexer"

Coding

Bose–Chaudhuri–Hocquenghem (BCH) codes (outer)

From <https://www.google.com/search?q=bch+code&rlz=1C1GCEA_enGB1120GB1120&oq=bch+code&gs_lcrp=EgZjaHJvbWUyBggAEEUYOdIBBzgwMGowajeoAgCwAgA&sourceid=chrome&ie=

https://www.etsi.org/deliver/etsi_tr/102300_102399/10237601/01.02.01_60/tr_10237601v010201p.pdf

Implementation guidelines

UTF-8>

Concatenated with LDPC inner
"(rates 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10). "

In Adaptive coding is used, FEC and modulation modes are constant within frame, can change between frames.

CRC-8 (packetised only)

Mapping

QPSK, 8PSK, 16APSK, 32APSK constellations

Physical Layer Framing

- Synchronous with FEC frames
- Includes
  - Physical Layer Signalling
    - Start of frame
    - Transmission mode
  - (optional) pilot insertion
    - 36 pilot symbols / 16 slots of 90 symbols
    - Pilotless adds 2.4% useful capacity
  - Physical Layer scrambling
- Dummy PLFRAME sent when no useful data
- Slot = 90 modulated symbols

Base Band Filtering, Quadrature modulation

Rolloff factors: 0.35, 0.25 or 0.20

Configurations

16 ETSI EN 302 307-1 V1.4.1 (2014-11)

Table 1: System configurations and application areas

System configurations		Broadcast services	Interactive services	DSNG	Professional services
QPSK	1/4,1/3, 2/5	O	N	N	N
	1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10	N	N	N	N
8PSK	3/5, 2/3, 3/4, 5/6, 8/9, 9/10	N	N	N	N
16APSK	2/3, 3/4, 4/5, 5/6, 8/9, 9/10	O	N	N	N
32APSK	3/4, 4/5, 5/6, 8/9, 9/10	O	N	N	N
CCM		N	N (see note 1)	N	N
VCM		O	O	O	O
ACM		NA	N (see note 2)	O	O
FECFRAME (normal)	64 800 (bits)	N	N	N	N
FECFRAME (short)	16 200 (bits)	NA	N	O	N
Single Transport Stream		N	N (see note 1)	N	N
Multiple Transport Streams		O	O (see note 2)	O	O
Single Generic Stream		NA	O (see note 2)	NA	O
Multiple Generic Streams		NA	O (see note 2)	NA	O
Roll-off 0,35, 0,25 and 0,20		N	N	N	N
Input Stream Synchronizer		NA except (see note 3)	O (see note 3)	O (see note 3)	O (see note 3)
Null Packet Deletion		NA except (see note 3)	O (see note 3)	O (see note 3)	O (see note 3)
Dummy Frame insertion		NA except (see note 3)	N	N	N
Wide-band mode	(see annex M)	O	O	O	O
N = normative, O = optional, NA = not applicable.					
NOTE 1: Interactive service receivers shall implement CCM and Single Transport Stream. NOTE 2: Interactive Service Receivers shall implement ACM at least in one of the two options: Multiple Transport Streams or Generic Stream (single/multiple input). NOTE 3: Normative for single/multiple TS input stream(s) combined with ACM/VCM or for multiple TS input streams combined with CCM.					

Within the present document, a number of configurations and mechanisms are defined as "Optional". Configurations and mechanisms explicitly indicated as "optional" within the present document, for a given application area, need not be implemented in the equipment to comply with the present document. Nevertheless, when an "optional" mode or mechanism is implemented, it shall comply with the specification as given in the present document.

Subsystems

Mode Adaption

- Input Interfacing
- Input Stream Sync (optional)
- Null packet deletion (TS, ACM)
- CRC-8 (packetized)
- Stream merging (multi streams)
- Input stream slicing in DATA FIELD
- Base band signalling to indicate Mode Adaption Format

Input sequences:

- Single or multiple Transport Stream (TS)
- Single or multiple generic streams (packetised or continuous)

- Output
  - 80 bit BBHEADER
  - DATA FIELD

Table 2: System interfaces

Location	Interface	Interface type	Connection	Multiplicity
Transmit station	Input	MPEG [1, 4] Transport Stream (see note 1)	from MPEG multiplexer	Single or multiple
Transmit station	Input (see note 2)	Generic Stream	From data sources	Single or multiple
Transmit station	Input (see note 3)	ACM command	From rate control unit	Single
Transmit station	Output	70 MHz/140 MHz IF, L-band IF, RF (see note 4)	to RF devices	Single or multiple
Transmit station	Input	Mode Adaptation	from Mode Adaptation block	Single
NOTE 1: For interoperability reasons, the Asynchronous Serial Interface (ASI) with 188 bytes format, data burst mode (bytes regularly spread over time) is recommended. NOTE 2: For data services.				

https://www.sunshine2k.de/articles/coding/crc/understanding_crc.html

Understanding CRC / CRC-8

Table 2: System interfaces

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Transmit station	Input	MPEG [1, 4] Transport Stream (see note 1)	from MPEG multiplexer	Single or multiple
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Transmit station	Input	Mode Adaptation	from Mode Adaptation block	Single
NOTE 1: For interoperability reasons, the Asynchronous Serial Interface (ASI) with 188 bytes format, data burst mode (bytes regularly spread over time) is recommended. NOTE 2: For data services. NOTE 3: For ACM only. Allows external setting of the ACM transmission mode. NOTE 4: IF shall be higher than twice the symbol rate.				

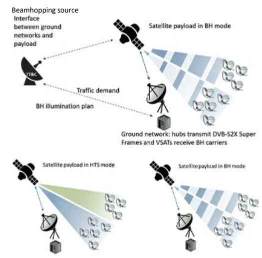
Transport Stream

- User Packets (UP)
- 188*8 bits
- First byte is sync byte, 0x47

- Generic Stream
  - Continuous bit stream
  - Or Stream of constant-length UP of length UPL
    - UPL Max is 64kb
    - UPL = 0 -> continuous stream
  - Variable length packet stream or UPL > 64kb -> cont stream

http://www.satmagazine.com/story.php?number=330838379

Beamhopping source



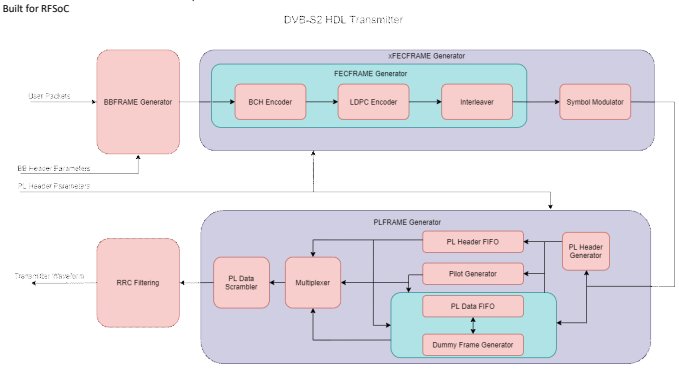
Mainly for high throughput

Implementation

27 September 2024 15:14

https://uk.mathworks.com/help/satcom/ug/dvbs2-hdl-transmitter.html

Mathworks DVB-S2 HDL Transmitter example
Built for RFSoC



Resources	Usage
CLB LUT	10701
CLB Registers	9024
RAMB36	99
RAMB18	6
DSP48	42

53k LUT on Zynq 7020
20% utilisation is too high?

https://www.design-reuse.com/

ASIC IP vendors

Zedboard Development

Tuesday, December 03, 2024 12:03 PM

Petalinux

https://github.com/sdonchez/petalinux-zedboard-test

Board Support / Reference

Only supports software versions up to like 2017
https://www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/zedboard/

Again, very out of date vivado support
https://github.com/jiafulow/zedboard-guide/tree/master?tab=readme-ov-file

GNU Radio

01 November 2024 15:06

https://github.com/drmpeg/gr-dvbs2
GNU Radio flow graph for DVB-S2 tx

https://igorauad.github.io/gr-dvbs2rx/
Receiver and transmitter

Open Source Toolchains

22 October 2024 12:07

https://github.com/kangyuzhe666/ZYNQ7010-7020_AD9363/blob/main/README.md
Looks like they're running pluto

https://github.com/hz12opensource/libresdr
Libre/zynq SDR
Pluto firmware clone

https://wiki.gnuradio.org/index.php?title=Zynq
Obsolete instructions for zynq development with gnuradio

https://strathprints.strath.ac.uk/86118/1/Siauciulis_etal_NEWCAS2023_100GBit_s_RF_sample_offload_for_RFSoC.pdf
StrathSDR paper on gnu radio

https://github.com/ryanvolz/radioconda
Installing gnuradio on windows

https://wiki.analog.com/resources/tools-software/linux-software/libiio
About libiio

https://www.adiuvoengineering.com/post/microzed-chronicles-industrial-input-output-petalinux
Libiio example

https://analogdevicesinc.github.io/hdl/library/axi_ad9361/index.html
Ad9361 IP core
https://ez.analog.com/fpga/f/q-a/51874/what-is-difference-between-ad9361-ad9364
Should be fine to use 61 for 64

https://ez.analog.com/linux-software-drivers/f/q-a/85538/crosscompiling-gnuradio-for-zedboard-fmcomms2
This guy compiling gnuradio for zedboard w. ad9361

Toolchain:
GNU Radio -> Libiio driver -> DVB accelerator IP -> AD IP -> DAC

ADC -> AD IP -> DVB rx accelerator IP -> Libiio driver -> GNURadio

https://github.com/analogdevicesinc/hdl/tree/main/library/axi_ad9361
https://github.com/analogdevicesinc/hdl/blob/main/docs/library/axi_ad9361/index.rst

https://wiki.analog.com/resources/tools-software/linux-software/gnuradio
Gnu radio on ad9361

17:25 28/10/2024

https://www.controlpaths.com/2021/04/05/managing-axi4-stream-from-matlab/
https://github.com/controlpaths/matlab_libiio
LIBIIO + axi interface from MATLAB w. HDL Coder

AD9364 eval board

22 October 2024 12:43

https://ez.analog.com/linux-software-drivers/f/q-a/85538/crosscompiling-gnuradio-for-zedboard-fmcomms2

https://wiki.analog.com/resources/eval/user-guides/ad-fmcomms4-ebz

ad-fmcomms4-ebz-...

Matlab HDL Coder Ex

20 October 2024 16:04

20/10/2024
https://uk.mathworks.com/help/satcom/ug/dvbs2-hdl-transmitter.html

Original example compiled for RFSoC, reran and compiled for 7020

7020 Utilisation

+----------------------------+-------+-------+------------+-----------+-------+
| Site Type | Used | Fixed | Prohibited | Available | Util% |
+----------------------------+-------+-------+------------+-----------+-------+
Slice LUTs*	11762	0	0	53200	22.11
LUT as Logic	7963	0	0	53200	14.97
LUT as Memory	3799	0	0	17400	21.83
LUT as Distributed RAM	3308	0			
LUT as Shift Register	491	0			
Slice Registers	9453	0	0	106400	8.88
Register as Flip Flop	9453	0	0	106400	8.88
Register as Latch	0	0	0	106400	0.00
F7 Muxes	1509	0	0	26600	5.67
F8 Muxes	20	0	0	13300	0.15
+----------------------------+-------+-------+------------+-----------+-------+

22% Slice LUTS
75% BRAM util!

+-------------------+------+-------+------------+-----------+-------+
| Site Type | Used | Fixed | Prohibited | Available | Util% |
+-------------------+------+-------+------------+-----------+-------+
Block RAM Tile	104	0	0	140	74.29
RAMB36/FIFO*	99	0	0	140	70.71
RAMB36E1 only	99				
RAMB18	10	0	0	280	3.57
RAMB18E1 only	10				
+-------------------+------+-------+------------+-----------+-------+

Verification

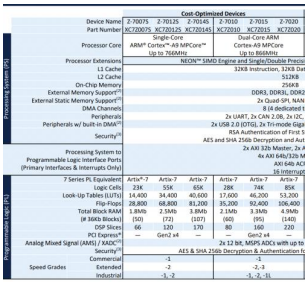
07 October 2024 15:44

https://uk.mathworks.com/help/satcom/ug/dvbs2_receiver_using_sdr.html
Receiver example

Resource Optimisation

17 October 2024 12:48

- Modulation
  - Only implement Q/BPSK
    - Probs not going to have the bandwidth to go higher
- Coding
  - Limited coding rate selection?



		Cost-Optimized Devices					
	Device Name	Z-70075	Z-70125	Z-70145	Z-7010	Z-7015	Z-7020
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz		
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precisi					
	L1 Cache	32KB Instruction, 32KB Da					
	L2 Cache	512KB					
	On-Chip Memory[1]	256KB					
	External Memory Support[2,3]	DDR3, DDR3L, DDR2					
	External Static Memory Support[2]	2x Quad-SPI, NAN					
	DMA Channels	8 (4 dedicated t					
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C,					
	Peripherals w/ built-in DMA[4]	2x USB 2.0 (OTG), 2x Tri-mode Giga					
	Security[5]	RSA Authentication of First S AES and SHA 256b Decryption and Aut					
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x A 4x AXI 64b/32b M AXI 64b ACI 16 Interrupt					
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7
	Logic Cells	23K	55K	65K	28K	74K	85K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400
	Total Block RAM	1.8Mb	2.5Mb	3.8Mb	2.1Mb	3.3Mb	4.9Mb
	(# 36Kb Blocks)	(50)	(72)	(107)	(60)	(95)	(140)
	DSP Slices	66	120	170	80	160	220
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—
	Analog Mixed Signal (AMS) / XADC[6]	2x 12 bit, MSPS ADCs with up to					
	Security[5]	AES & SHA 256b Decryption & Authentication f					
	Speed Grades Commercial	-1			-1		
	Speed Grades Extended	-2			-2, -3		
	Speed Grades Industrial	-1, -2			-1, -2, -1L		

Packets

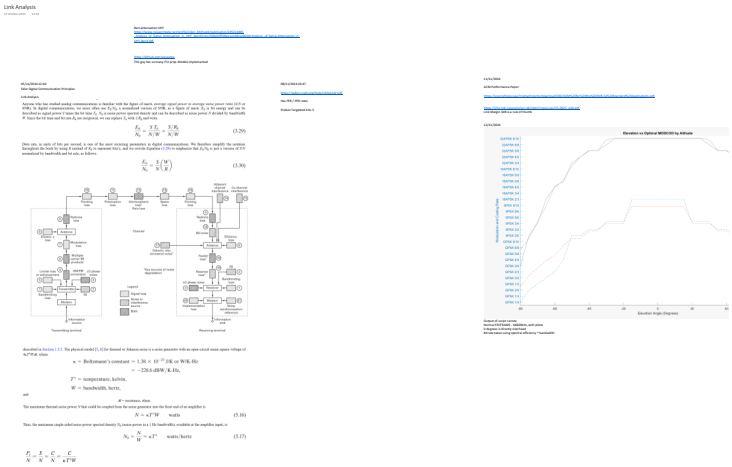
28 October 2024 17:27

https://public.ccsds.org/Pubs/660x2g2.pdf
https://www.omg.org/spec/XTCE/1.2/PDF

https://pypi.org/project/space-packet-parser/4.0.1/
XTCE parser
Could use in PS

NASA XTCE Tutorial
https://ntrs.nasa.gov/api/citations/20090017706/downloads/20090017706.pdf

https://github.com/nasa/CCDD/tree/CCDD-2



6/01 Setup

Monday, January 06, 2025 10:47 AM

Setting up MATLAB

- Reinstalled OS, have to reinstall all tools
- Setting up ADI toolbox for transceiver integration
- Resetting up HDL Coder example

Setting up C++ environment

- Installed req programs
- Setup vscode

Vivado + Vitis

- Some issues with generating device list.

12/01 Transmitter

Sunday, January 12, 2025 2:07 PM

MATLAB

Had to switch to 2024b to get the correct simulink block.
Existing Simulink model outputs fixed, need int16 vector
https://uk.mathworks.com/help/soc/ref/ad936xtransmitter.html

New issue:

MATLAB System block 'dvbs2hdlTransmitter/DVB-S2 HDL Transmitter/AD936x Transmitter/Sink Variant/To Connected IO/AD936x Transmitter' error occurred when invoking 'validateInputsImpl' method of 'comm.SDRTxAD936x'. The error was thrown from '/home/daniel/Documents/MATLAB/SupportPackages/R2024b/toolbox/shared/sdr/rfconverter_libiio/+comm/+libiio/+AD9361/tx.p' at line 0
'/usr/local/MATLAB/R2024b/toolbox/simulink/ui/studio/config/m/+SLStudio/ToolBars.p' at line 0
'/usr/local/MATLAB/R2024b/toolbox/simulink/ui/studio/config/m/+SLStudio/ToolBars.p' at line 0'.
Caused by:

- In single channel mode the number of samples per frame must be even.

Supervisor Meeting 3/12/24

Tuesday, December 03, 2024 10:48 AM

- Showed Louise progress on Interim Report
  - Flow of subsystem research -> overall design
  - Relaxation of filter coefficients
- Told her that I'm focusing on engineering model as TOTEM not ready
- She suggesed adding numbers to project plan
- Seemed satisfied with progress
- Louise will be away a lot of next week.
  - Can send draft of interim, leave time to spare!
- Meetings next semester
  - Around this time looks good
  - 471 has lecture scheduled at 10am, probs not real
  - 579 appearin gsomewhere
- Oral in consolidation week
  - Probs Monday, Tue / wed
  - Will try to schedule a meeting before then
  - Consider having some work done between interim report submission and oral!
    - Having nothing new might look bad

Statement of Intent

07 October 2024 14:01

19496_statement_of_intent_...

Department of Electronic & Electrical Engineering
MEng/BEng in EEE
19496 Individual Project

This document is organised in to six parts:

PART 1: STATEMENT OF INTENT
PART 2: PROJECT WORK PLAN
PART 3: RESOURCE REQUIREMENTS
PART 4: RISK ASSESSMENT
PART 5: SUSTAINIBILITY, ETHICS, INCLUSIVITY
PART 6: SAFETY DECLARATION & ETHICS APPROVAL

- All parts of the form must be completed jointly by the student and Project Supervisor, and lodged (by the student) on MyPlace by 14.00 on 16th October 2024.
- Copies of the completed form should be sent to the Project Supervisor.
- The student is advised to retain a copy of the completed form for future reference - ideally affixed inside their project logbook.
- Students will be asked to reflect upon parts 1, 2 and 4 at the interim stage and also in the final report.

Supervisor's Name:	**Student's Name:**
Project Title:	

PART 1: STATEMENT OF INTENT

The purpose of this section is: (i) to provide a concise description of the project, and (ii) to state a set of objectives that will provide the guide for assessing the project. Students should note the importance of item (ii), which should be discussed in detail with their project supervisors.

A. Project Description:

The student, in consultation with the Project Supervisor, is required to describe the project in THEIR OWN WORDS in the space provided below (in about 200 to 300 words). Note that simply copying descriptions in the project listing is unacceptable. THIS PART SHOULD NOT BE COMPLETED BY THE PROJECT SUPERVISOR other than ensuring the accuracy of the description. DO NOT ATTACH EXTRA PAGES.

Project Description:

Can be very similar to proposal?

Objectives:

1. Assess previous investigations into downlink.
2. Research DVB-S2 standard
3. Research existing implementations
4. Review of provided software and RTL from manufacturer.
5. Write RTL for transmitter.
6. Write verification testbenches and study robustness of design and processing pipelines.
7. Optimise resource requirements to ensure compatibility with target hardware, including all RTL required for mission.
8. Write and test software drivers for GNU Radio.
9. Analyse performance of solution to ensure compliance with mission requirements.
10. Collaborate with STRATHcube masters team.
11. (Stretch) Test implementation on development board.
12. (Stretch) Test implementation on TOTEM SDR.

From <https://strath-my.sharepoint.com/personal/daniel_stebbings_2021_uni_strath_ac_uk/Documents/EEE/Y4/Dissertation/Dissertation%20Project%20Proposal.docx>

B. Project Objectives:

Project objectives must be stated in such a way that they can be translated into achievable goals during the conduct of the project. For this reason, the stated objectives must be specific and realistic to be attained within the time provided. It will be very helpful if supervisors encourage their students to come up with initial objectives from students' perspective as this exercise could help students to better understand the aims of the project. It is important to note that the achievements of the project work will be measured against the objectives stated here. Copies of this section will be made available to persons involved with the assessment of this project.

1. *Under the "Importance" column below, enter one of the following as appropriate: "Major", "Minor", or "Optional".*
2. *If at a later stage, the project objectives change significantly, these changes must be communicated clearly in the interim and final report as appropriate.*

Project Objectives	**Importance**

PART 2: PROJECT WORK PLAN

Identify project milestones and summarise your work plans in the table below in the order you do them. (Example: preliminary design, prototyping, simulation modelling, results validation, write-up, etc.).

	Project Milestones/Work Phases	**Expected Week Time** *Enter start and end week Ex.: Week 6 to week 8*
1		
2		
3		
4		
5		
6		

PART 3: RESOURCE REQUIREMENTS

A. Software:

List the software required for the project. This includes programming languages, application packages, CAD tools, etc.

Software *(indicate version no. if applicable)*	Software Administrator *(EEE/MAE/CIS Dept, Comp. Centre)*	Installed Location (Dept/Central University/ Personal computer).	Expected Usage *(hours/week)*

B. Hardware:

List major hardware components such as circuit boards, microcontrollers, LSI/VLSI integrated circuits, and special purpose equipment and facilities.

C. Background Information & Required Reading

Describe sources of information (in library and elsewhere) required to undertake project

Provide details of the two most important sources of information already identified

D. Laboratory/Work Area:

Indicate the laboratory room(s) and/or project work area for the project.

With regards to practical work there is no expectation/requirement that practical work on the project is carried out anywhere other than on University campus. Any work that is carried out off-site must be fully agreed by supervisor and explicitly covered by the project's risk assessment – and listed in the space provided below.

D. Logbook:

Confirmation that student has A4, hardback, bound logbook that has been viewed by the supervisor and/or arrangements have been made for shared access for electronic logbook/progress records. (Teams/OneNote recommended) YES/NO (delete one)

PART 4: TECHNICAL RISK

Management of project work requires that technical risk be assessed in advance, during initial planning and as an ongoing process. As the first stage to this process, identify any aspects of risk associated with your project proposal. Risk in this context is taken to mean any event or action (or inaction) that would jeopardise any project outcomes or significantly impede project progress. Furthermore, having identified such potential risks, indicate what actions you would take to mitigate the effects of this risk. (Consult your supervisor for advice but examples of such risks include non-delivery of a key component, illness or absence from University, non-completion by student or other of key deliverable, equipment malfunction, extended learning curves-new techniques or software, etc.).

	Possible Risk:	**Mitigating Action:**
1		
2		
3		
4		
5		

PART 5: SUSTAINABILITY, ETHICS AND INCLUSIVITY

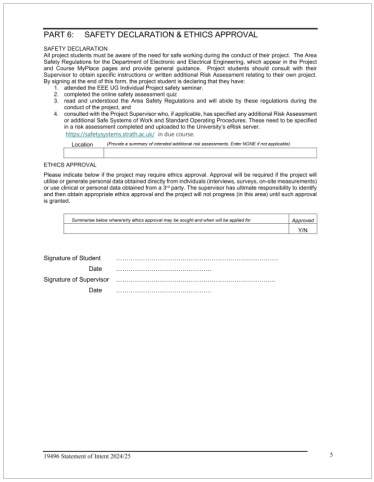
All project students will in the course of their work implement and develop technological advancements, either through the creation of prototypes, software tools and or generation of new know-how/ways of doing things. The focus of such development is typically aligned to a combination of technological, societal or financial drivers.

As major drivers of technology advancement, engineers have key role in stewardship of the planet's resources. Sustainability could be demonstrated by comparing the developments, techniques and ideas that encompass the project and making comparison to status quo, how resources can be saved/reserved etc. Furthermore, new developments to address current needs should not negatively impact the ability of future generations to meet and address their own needs. How would that be achieved/developed in the course of the project?

Ethics form an essential part of engineering practise and ensure that project teams and persons affected by project outcomes are all treated fairly, equally, openly and with integrity. These ethical standards can be considered and applied to the different phases of the project: planning; sourcing and utilisation of project inputs (data, raw materials, components etc.); milestones/decision points through the course of the project; implementation of the final deliverable(s); manufacturing; safety implications, both during the course of the project and in utilisation of any final deliverable.

Engineering and technology are for everyone and technological solutions to the many challenges we face as a society should encompass and benefit all members of society irrespective of age, gender, race, ability or socio-economic standing.

In considering your project, describe how aspects of sustainability, ethics and inclusivity have been considered and impacted the project and its outcomes. The SoI can be used to capture how such factors have influenced the initial planning of the project and subsequent reports, both interim and final, can be used to record how such factors have influenced the course of the project, deliverables, milestones, and outcomes.



PART 6: SAFETY DECLARATION & ETHICS APPROVAL

SAFETY DECLARATION

All project students must be aware of the need for safe working during the conduct of their project. The Area Safety Regulations for the Department of Electronic and Electrical Engineering, which appear in the Project and Course. MyPlace pages and provide general guidance. Project students should consult with their Supervisor to obtain specific instructions or written additional Risk Assessment relating to their own project. By signing at the end of this form, the project student is declaring that they have:

1. attended the EEE UG Individual Project safety seminar.
2. completed the online safety assessment quiz
3. read and understood the Area Safety Regulations and will abide by these regulations during the conduct of the project, and
4. consulted with the Project Supervisor who, if applicable, has specified any additional Risk Assessment or additional Safe Systems of Work and Standard Operating Procedures. Thses need to be specified in a risk assessment completed and uploaded to the University's eRisk server.
   https://safetysystems.strath.ac.uk/ In due course.

Location *(Provide a summary of interated additional risk assessments. Enter 'NONE if not applicable)*

ETHICS APPROVAL

Please indicate below if the project may require ethics approval. Approval will be required if the project will utilise or generate personal data obtained directly from individuals (interviews, surveys, on-site measurements) or use clinical or personal data obtained from a 3rd party. The supervisor has ultimate responsibility to identify and then obtain appropriate ethics approval and the project will not progress (in this area) until such approval is granted.

Summarise below where/why ethics approval may be sought and when will be applied for	*Approved* Y/N

Signature of Student .....

Date .....

Signature of Supervisor .....

Date .....

19496 Statement of Intent 2024/25 5

Interim Report Meeting

15 November 2024 12:09

Draft 12h00 06 Dec 2024

Final	12h00 13 Dec 24

"originality" subjective

Cover, project status report
2 pages context bckground
1 page project plan
1 page fully describe plan and tech risk
More pages for bib.
No additional allowed

Body 4 pages A4
What why - financial, societal

Possible to have no technical risk. Explain why!

Include changes made, and location of code / files in logbook

Links

Saturday, November 30, 2024 5:59 PM

Frequencies

Amsat band : https://rsgb.org/main/operating/band-plans/vhf-uhf/432mhz-band/
OFCOM FAT: https://www.ofcom.org.uk/siteassets/resources/documents/spectrum/spectrum-information/frequency-allocation-table/uk-fat-2017.pdf?v=322554
(Very unhelpful to read tbh)

SRD

Saturday, November 30, 2024 8:11 PM

Found a good ESA example
https://climate.esa.int/media/documents/Snow_cci_D3.2_SSD_v4.0.pdf