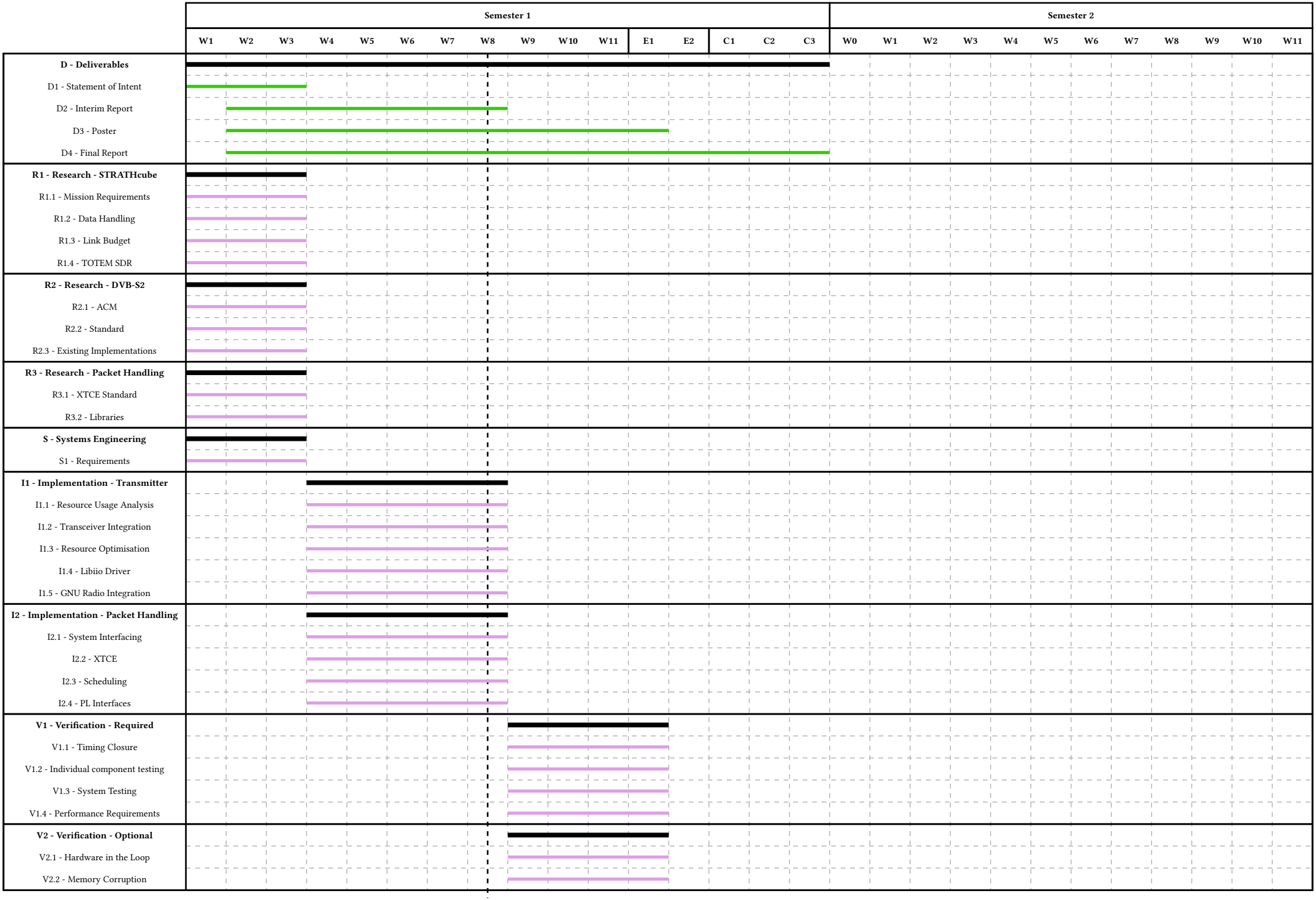
1. Hello

1.1.

This is a test of the timeliney preview.

2. Project Timeline


Semester 1
Semester 2
W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 E1 E2 C1 C2 C3
W0 W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11
D - Deliverables
D1 - Statement of Intent
D2 - Interim Report
D3 - Poster
D4 - Final Report
R1 - Research - STRATHcube
R1.1 - Mission Requirements
R1.2 - Data Handling
R1.3 - Link Budget
R1.4 - TOTEM SDR
R2 - Research - DVB-S2
R2.1 - ACM
R2.2 - Standard
R2.3 - Existing Implementations
R3 - Research - Packet Handling
R3.1 - XTCE Standard
R3.2 - Libraries
S - Systems Engineering
S1 - Requirements
I1 - Implementation - Transmitter
I1.1 - Resource Usage Analysis
I1.2 - Transceiver Integration
I1.3 - Resource Optimisation
I1.4 - Libiio Driver
I1.5 - GNU Radio Integration
I2 - Implementation - Packet Handling
I2.1 - System Interfacing
I2.2 - XTCE
I2.3 - Scheduling
I2.4 - PL Interfaces
V1 - Verification - Required
V1.1 - Timing Closure
V1.2 - Individual component testing
V1.3 - System Testing
V1.4 - Performance Requirements
V2 - Verification - Optional
V2.1 - Hardware in the Loop
V2.2 - Memory Corruption
proof of concept
4 channel n77 receiver