

# DVB-S2

Figures from ETSI EN 302 307-1 V1.4.1

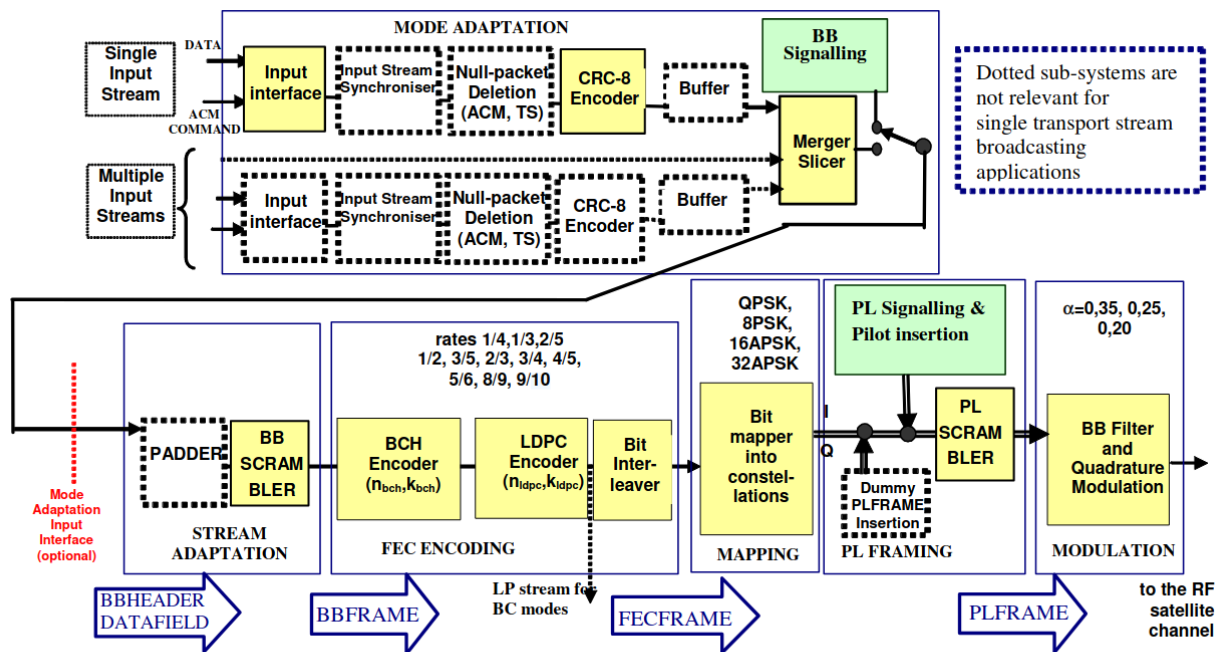


Figure 1: Functional block diagram of the DVB-S2 System

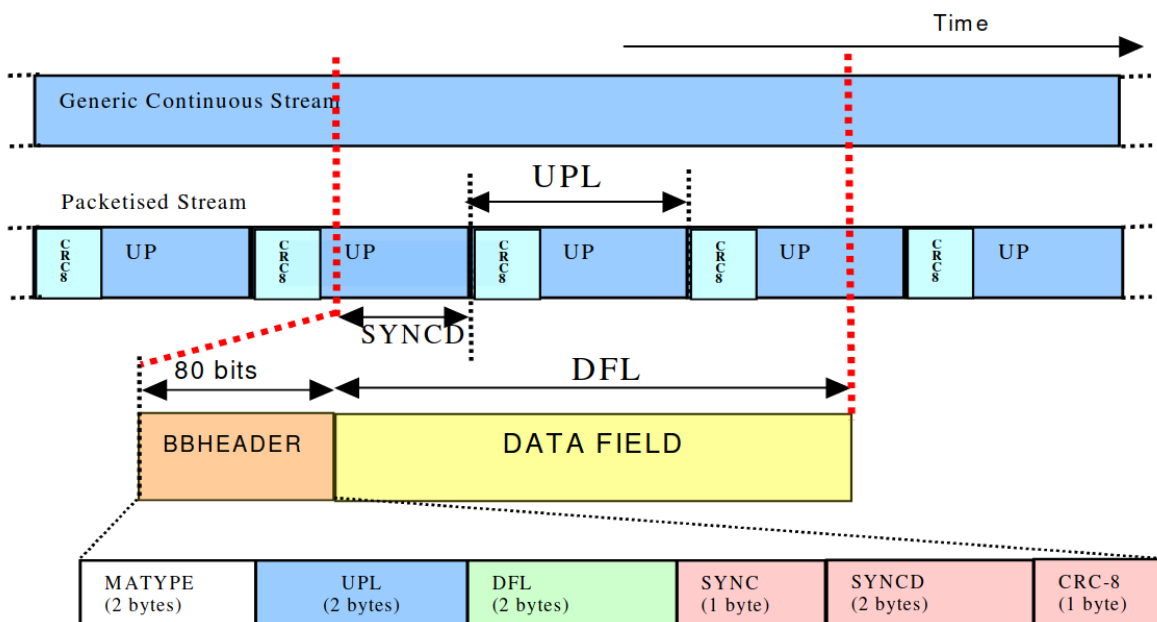


Figure 3: Stream format at the output of the MODE ADAPTER

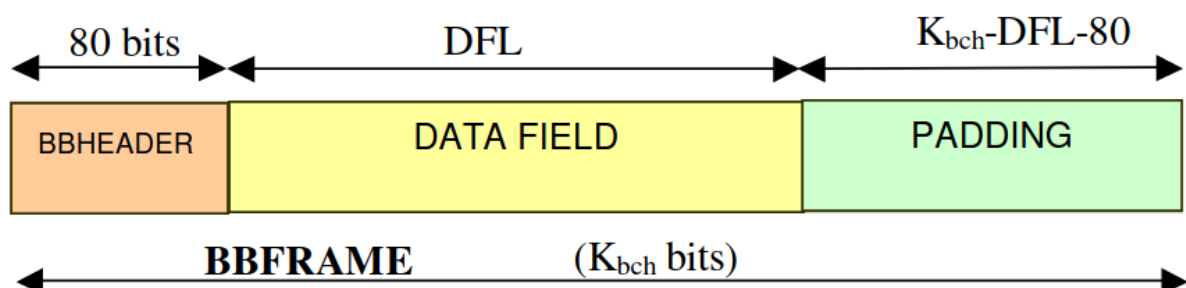


Figure 4: BBFRAME format at the output of the STREAM ADAPTER

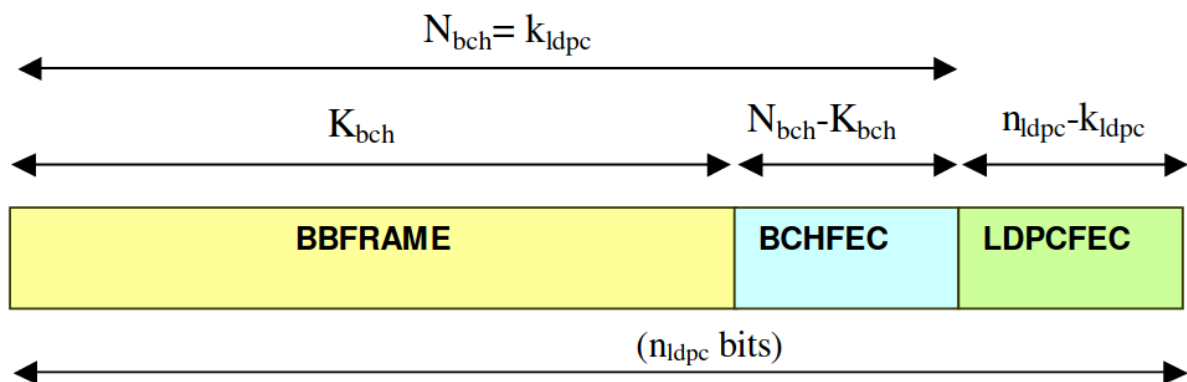


Table 5a: Coding parameters (for normal FECFRAME  $n_{ldpc} = 64\,800$ )

LDPC code	BCH Uncoded Block $K_{bch}$	BCH coded block $N_{bch}$ LDPC Uncoded Block $K_{ldpc}$	BCH t-error correction	LDPC Coded Block $n_{ldpc}$
1/4	16 008	16 200	12	64 800
1/3	21 408	21 600	12	64 800
2/5	25 728	25 920	12	64 800
1/2	32 208	32 400	12	64 800
3/5	38 688	38 880	12	64 800
2/3	43 040	43 200	10	64 800
3/4	48 408	48 600	12	64 800
4/5	51 648	51 840	12	64 800
5/6	53 840	54 000	10	64 800
8/9	57 472	57 600	8	64 800
9/10	58 192	58 320	8	64 800

Table 12: MODCOD coding

Mode	MOD COD	Mode	MOD COD	Mode	MOD COD	Mode	MOD COD
QPSK 1/4	1 <sub>D</sub>	QPSK 5/6	9 <sub>D</sub>	8PSK 9/10	17 <sub>D</sub>	32APSK 4/5	25 <sub>D</sub>
QPSK 1/3	2 <sub>D</sub>	QPSK 8/9	10 <sub>D</sub>	16APSK 2/3	18 <sub>D</sub>	32APSK 5/6	26 <sub>D</sub>
QPSK 2/5	3 <sub>D</sub>	QPSK 9/10	11 <sub>D</sub>	16APSK 3/4	19 <sub>D</sub>	32APSK 8/9	27 <sub>D</sub>
QPSK 1/2	4 <sub>D</sub>	8PSK 3/5	12 <sub>D</sub>	16APSK 4/5	20 <sub>D</sub>	32APSK 9/10	28 <sub>D</sub>
QPSK 3/5	5 <sub>D</sub>	8PSK 2/3	13 <sub>D</sub>	16APSK 5/6	21 <sub>D</sub>	Reserved	29 <sub>D</sub>
QPSK 2/3	6 <sub>D</sub>	8PSK 3/4	14 <sub>D</sub>	16APSK 8/9	22 <sub>D</sub>	Reserved	30 <sub>D</sub>
QPSK 3/4	7 <sub>D</sub>	8PSK 5/6	15 <sub>D</sub>	16APSK 9/10	23 <sub>D</sub>	Reserved	31 <sub>D</sub>
QPSK 4/5	8 <sub>D</sub>	8PSK 8/9	16 <sub>D</sub>	32APSK 3/4	24 <sub>D</sub>	DUMMY PLFRAME	0 <sub>D</sub>

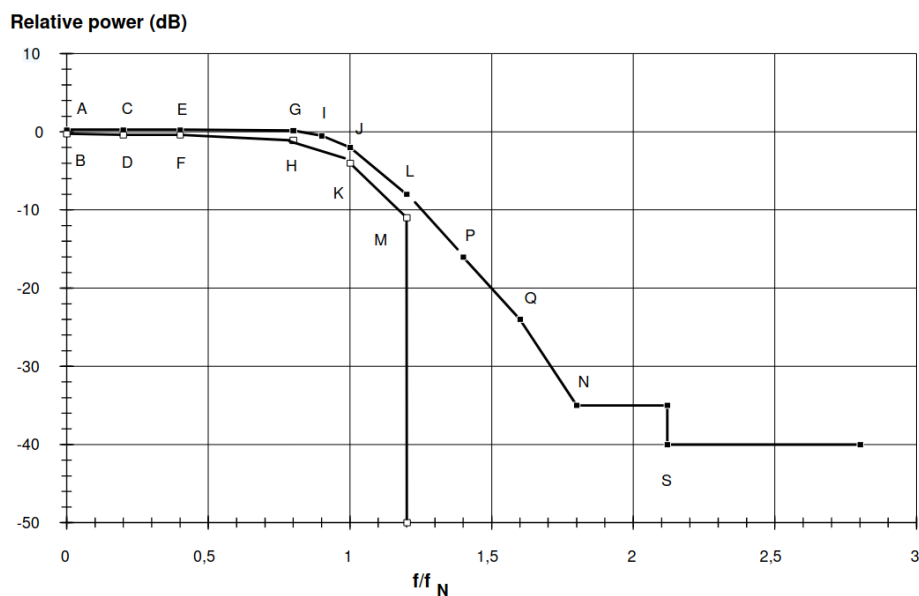


Figure A.1: Template for the signal spectrum mask at the modulator output represented in the baseband frequency domain, the frequency axis is calibrated for roll-off factor  $\alpha = 0,35$

# GSE

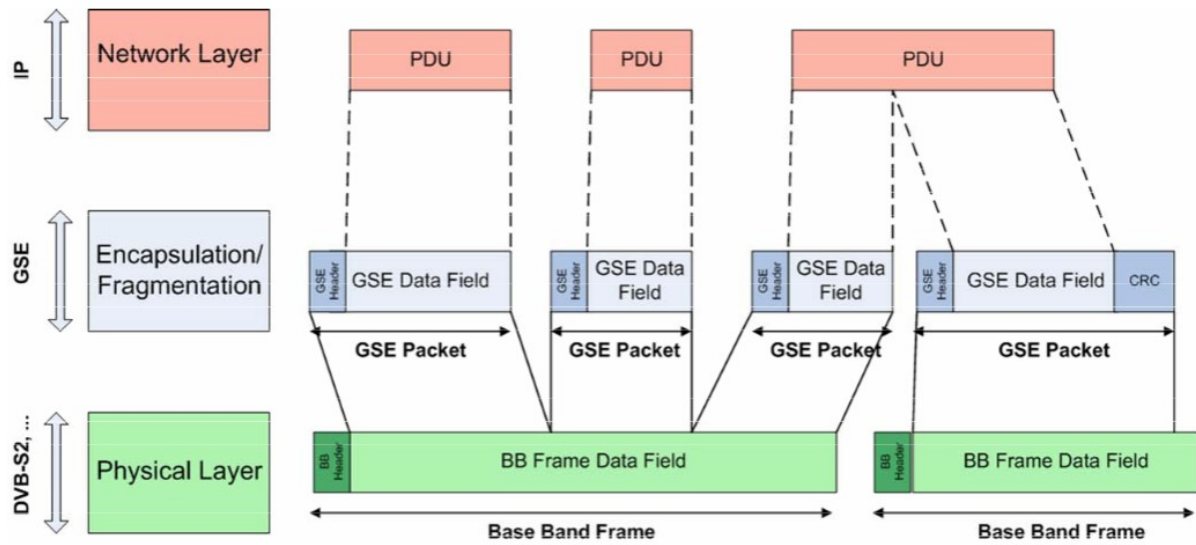


Figure 1: GSE encapsulation within DVB protocol stack

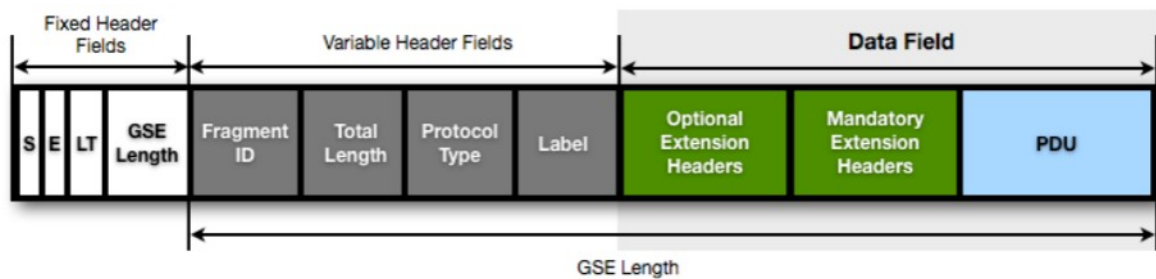


Figure 4: Data field structure

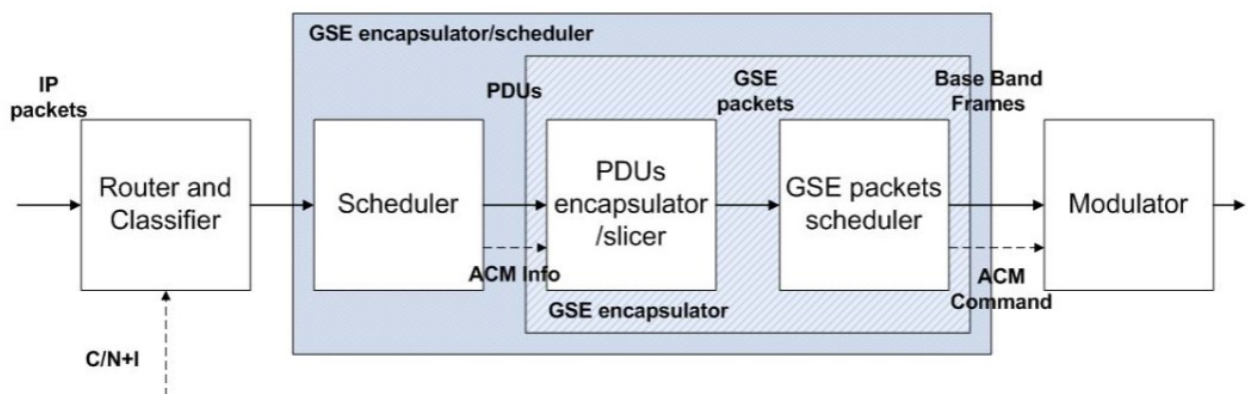
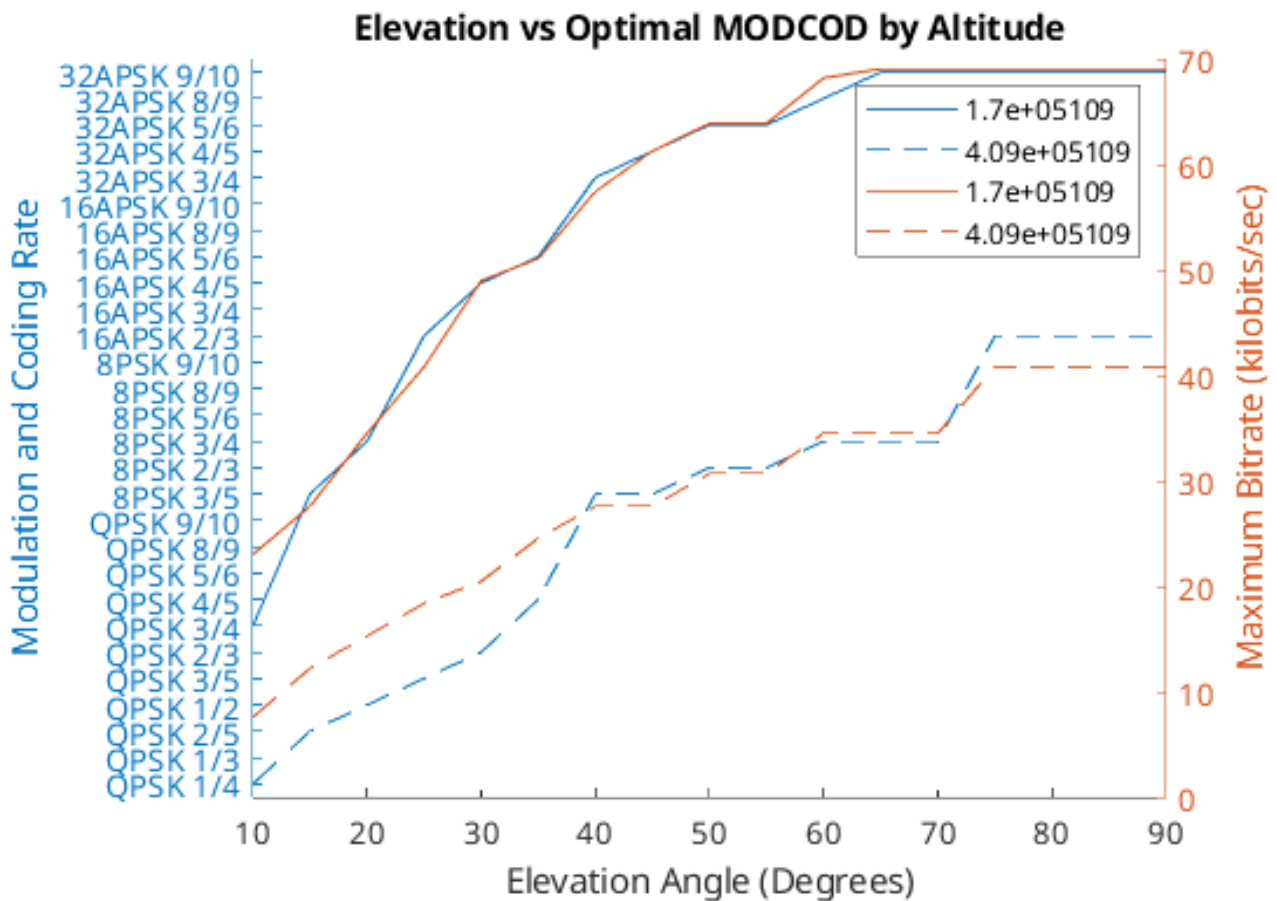
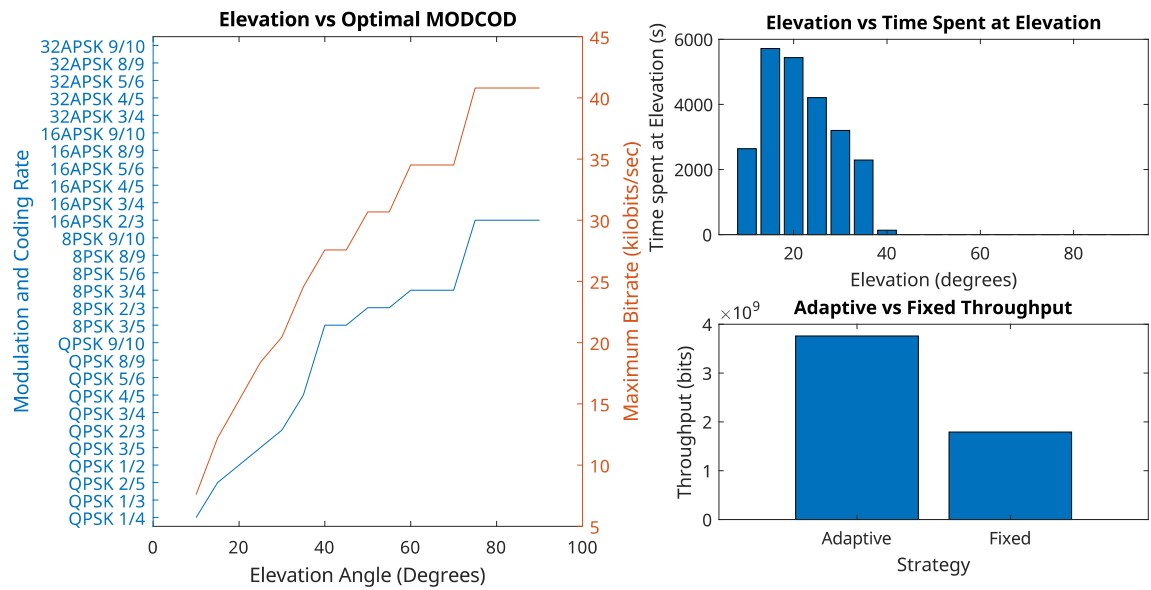


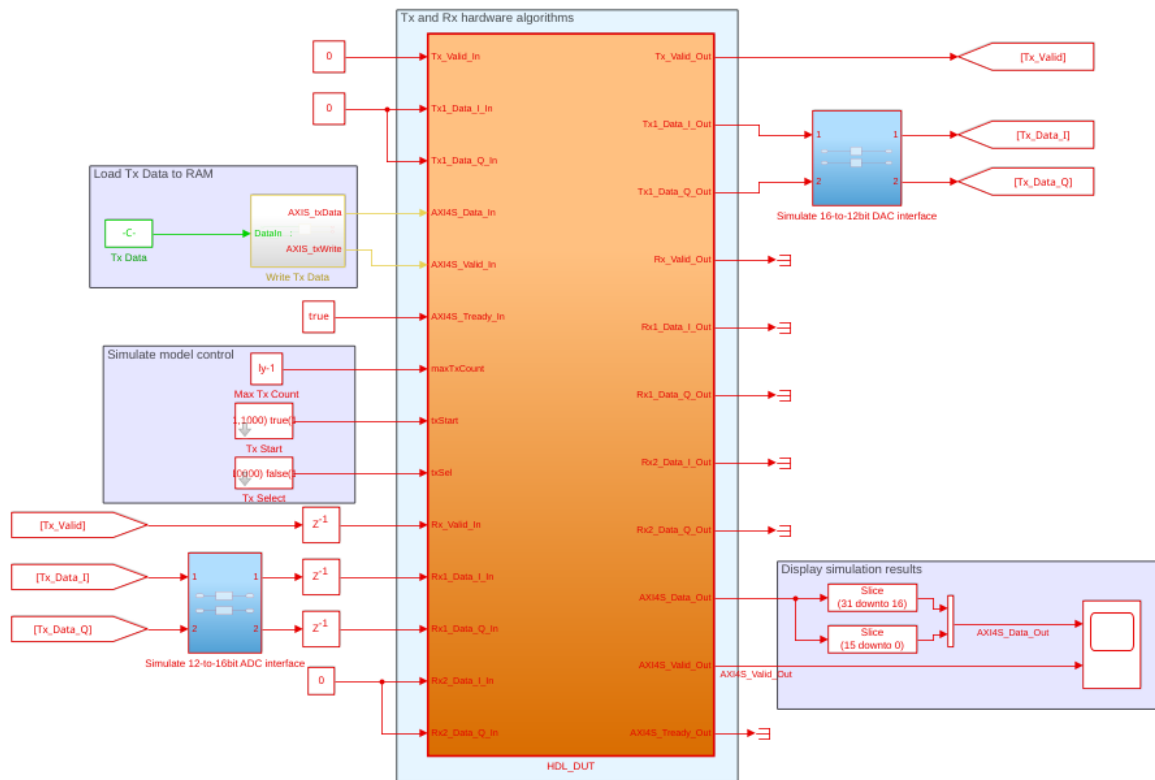
Figure B.1: Encapsulator/scheduler block diagram

# ACM Analysis



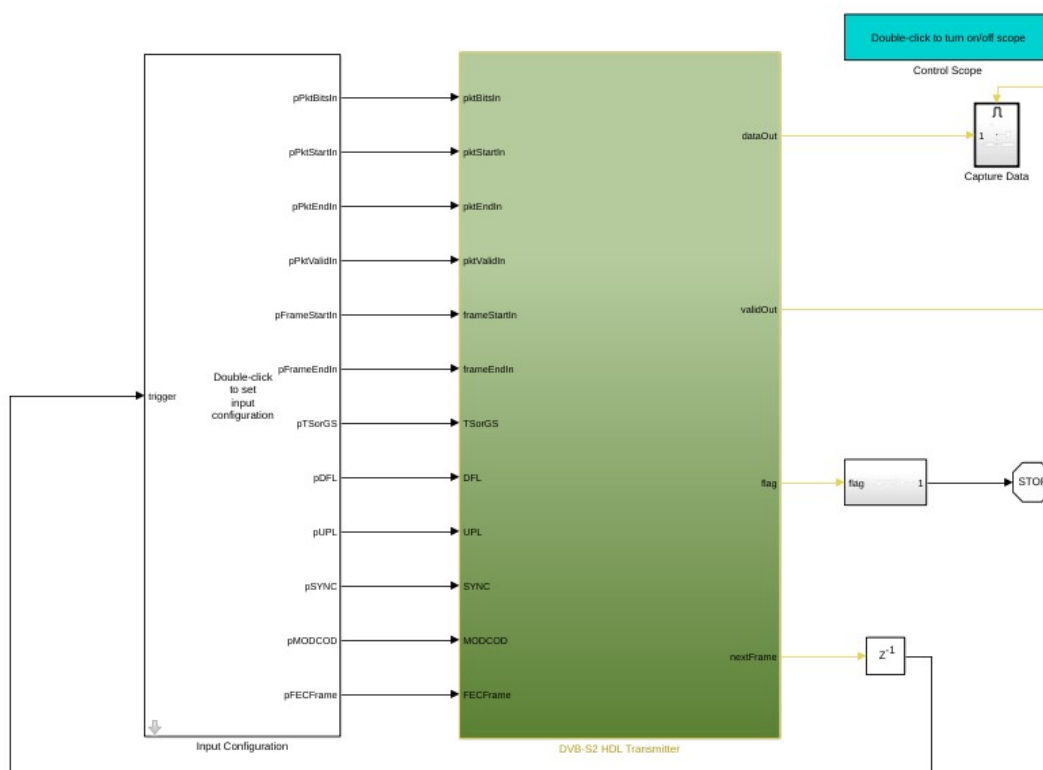
# MATLAB Implementation

## HW/SW Co-Design AXI4-Stream Hardware Generation Model



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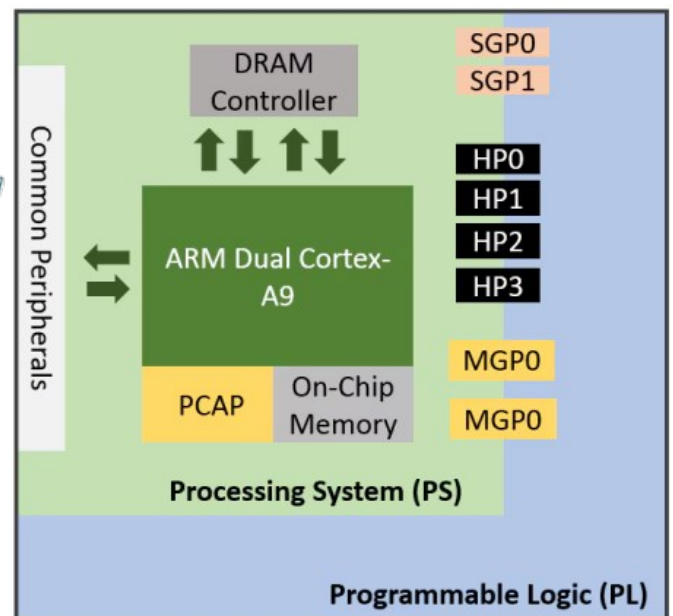
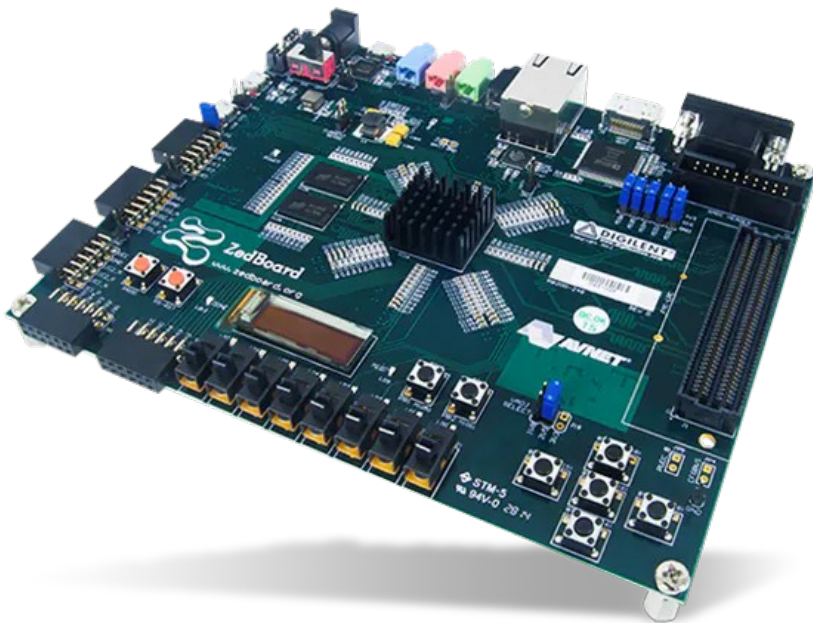
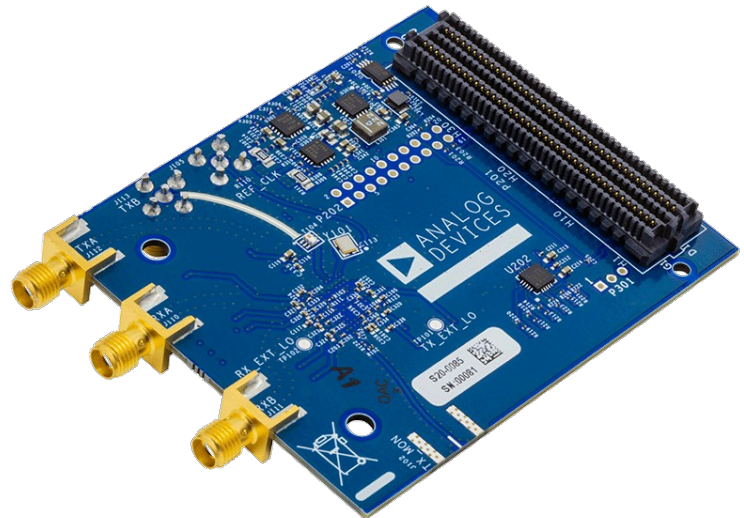
## DVB-S2 HDL Transmitter



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## Hardware



## STRATHcube

