a-Si:H TFTs MADE ON POLYIMIDE FOIL BY PE-CVD AT 150°C

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ABSTRACT

We have fabricated high-performance amorphous silicon thin-film transistors (a-Si:H TFTs) on 2 mil. (51 μm) thick polyimide foil substrates. The TFT structure was deposited by r.f.-excited plasma enhanced chemical vapor deposition (PECVD). All TFT layers, including the gate silicon nitride, the undoped, and the n^+ amorphous silicon were deposited at a substrate temperature of 150°C. The transistors have inverted-staggered back-channel etch structure. The TFT off-current is ~ 10^{-12} A, the on-off current ratio is > 10^7, the threshold voltage is 3.5 V, the sub-threshold slope is ~ 0.5V/decade, and the linear-regime mobility is ~ 0.5 $cm^2 V^{-1} s^{-1}$. We compare the mechanical behavior of a thin film on a stiff and on a compliant substrate. The thin film stress can be reduced to one half by changing from a stiff to a compliant substrate. A new equation is developed for the radius of curvature of thin films on compliant substrates.

INTRODUCTION

Large-area a-Si:H thin-film-based electronics is becoming part of our everyday life. Active matrix liquid crystal displays are a good example. Currently, large-area electronics typically is fabricated on glass substrates. However, there is a growing interest in replacing glass with plastic substrates to make large-area electronics flexible, light-weight and unbreakable.

The glass transition temperature of plastics (≤ 200°C) is much lower than those of the conventional substrates, Corning 7059 and 1737 glass (> 600°C). Therefore, the standard a-Si:H TFT processes cannot be used on plastics because they require temperatures of up to 350°C. Two attempts have been made to fabricate a-Si:H TFTs at temperatures ≤ 150°C on Corning 7059 glass substrates. Feng et al. [1] used r.f.-excited PECVD to grow a-Si:H TFTs at 150°C substrate temperature. These transistors had low on-off current ratio and low mobility. McCormick et al. [2] employed d.c. magnetron reactive sputtering to fabricate a-Si:H TFTs on glass at 125°C. This device was incomplete because no n^+ contact layer was used. Gates [3] reported the first attempt to fabricate a-Si:H TFTs on polycarbonate using the magnetron sputtering technique of [2]. However, no data on TFT performance were provided.

In this paper we report a-Si:H TFTs fabricated on 51 μm (2 mil) thick polyimide foil. We chose Kapton® E (DuPont) because among the commercially available polyimide grades it has the lowest coefficients of thermal ($12x10^{-6}$/°C) expansion. Its coefficient of humidity expansion is $9x10^{-6}$/% Relative Humidity.

The transfer of such low-temperature technology from glass to plastic substrates brings new processing and mechanical issues to the a-Si:H TFT fabrication. In the case of the comparatively thick glass substrate, the deposited thin-film layers must comply with the glass plate, because the product of Young's modulus Y and thickness d of the glass far exceeds that of the thin-film circuit. However, Y of a typical polymer is two orders of magnitude lower than that of glass. The contribution of a thin plastic foil to the mechanical behavior of the large-area circuit becomes comparable to that of the semiconductor structure. Therefore, with silicon on plastic foil technology we enter a new regime of mechanical behavior of semiconductor circuits. In the

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following section we analyze the mechanics of a single film on such a compliant substrate, after first describing the conventional situation of a film on a stiff substrate (which is identical to the mechanics of the thin films in a silicon integrated circuit).

STRESS, STRAIN AND CURVATURE OF A FILM / COMPLIANT SUBSTRATE COUPLE

The stress in a thin film deposited at elevated temperature typically has two components, the intrinsic stress and the thermal mismatch stress. At the deposition temperature, the film may develop an intrinsic stress. The intrinsic stress arises from a mismatch strain, which we denote as ε_0, taken to be positive when it induces a tensile stress in the film. Its origin varies widely and is poorly understood for many systems [4]. One type of intrinsic stress is caused by lattice parameter mismatch. If the film is perfectly epitaxial on the substrate, ε_0 simply relates to the lattice constants of the two materials. Most other mechanisms are difficult to model. In practice, ε_0 is determined experimentally as a function of deposition condition and materials system. The other component of the stress arises from thermal expansion mismatch. When the temperature drops by ΔT, the difference in the thermal expansion coefficients of the film and the substrate, α_f and α_s, causes an additional mismatch strain. The total mismatch strain is the sum of the two contributions:

$$\varepsilon_M = \varepsilon_0 + (\alpha_f - \alpha_s)\Delta T. \tag{1}$$

In our present discussion we assume that this strain is not relaxed by any inelastic process such as plastic deformation of the film or substrate. We now compare the mechanical behavior of a film on a stiff substrate to one on a compliant substrate.

Stiff substrate. First recall the basic relations for a film on a stiff substrate. Because the substrate is stiff, the film has to conform to it. A biaxial stress, σ_f, arises in the plane of the film, which relates to the mismatch strain as

$$\sigma_f = \varepsilon_M Y_f^*. \tag{2}$$

Here $Y_f^* = Y_f / (1 - \nu_f)$ is the biaxial elastic modulus of the film, with Y_f being Young's modulus and ν_f Poisson's ratio. The stress in the substrate is much smaller than the stress in the film. The mismatch causes the substrate to bend. The radius of curvature R is given by the well known Stoney formula [5]:

$$R = \frac{Y_s^* d_s^2}{6\sigma_f d_f}, \tag{3}$$

where d_f is the film thickness, d_s the substrate thickness, and Y_s^* the biaxial elastic modulus of the substrate. Because the substrate is stiff, the radius of curvature is very large. Determining the stress in the film by measuring this radius of curvature is an established practice.

Compliant substrate. When a film is deposited on a thin, compliant substrate, the substrate also deforms considerably. Consequently, *the stress in the film is reduced.* In addition, the radius of curvature R can become very small. During deposition, we hold the substrate in a rigid frame, so that the substrate is flat. Under this condition, the stress in the film is given by

$$\sigma_f = \frac{\varepsilon_M Y_f^*}{1+\left(Y_f^* d_f\right)/\left(Y_s^* d_s\right)}. \tag{4}$$

In our system of silicon-based and chromium films on polyimide foil, the films have much higher elastic moduli than the substrate. Therefore, the products $Y_f^* d_f$ and $Y_s^* d_s$ are comparable in magnitude. Consequently, the stress in the film deposited on the thin, compliant substrate is reduced by a factor of about 2 from a film on a stiff substrate. The formula also indicates that we must abandon the notion of an *intrinsic* stress for the film, because the stress in the film is no longer set by a rigid substrate, but now depends on the substrate thickness and elastic modulus. The stress in the substrate is given by

$$\sigma_s = -\sigma_f d_f / d_s. \tag{5}$$

This stress is still quite small compared to the stress in the film for a thickness ratio d_f / d_s = 1/50 (e. g., 1-μm thick film on 50-μm thick substrate).

One can also flatten the substrate by depositing films of the same thickness on both sides of the substrate. The above equations are still applicable, with d_f being the sum of the thicknesses of the two films. For multilayer films of dissimilar materials, corresponding equations can also be developed.

When a film is deposited on a compliant substrate which is held in a frame, and the structure then is released from the frame, the substrate bends substantially. Although the stresses in the film and the substrate are biaxial, the substrate bends into a roll. This is different from a stiff wafer, which bends into a spherical cap, with a biaxial curvature. The transition from a spherical cap to a roll as the substrate becomes thinner and more compliant has been studied extensively [6]. Our substrates are so compliant that they are on the "roll side" far from the transition point, so that we can model them simply with elementary beam theory. The problem is similar to a bimetallic strip. The radius of curvature is given by

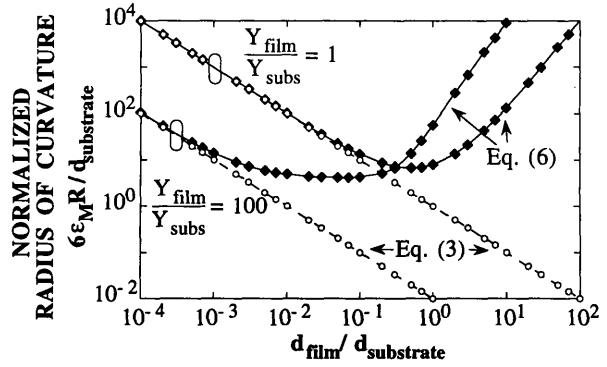


Figure 1. Normalized radius of curvature as a function of film/substrate thickness ratio. Two different substrates are illustrated: glass ($Y_{film} / Y_{substrate} \cong 1$) and polyimide ($Y_{film} / Y_{substrate} \cong 100$). We assume $\nu_{film} = \nu_{substrate}$. Full lines represent exact solution (Eq. (6)), dashed lines approximation for thick, stiff substrate (Eq. (3)).

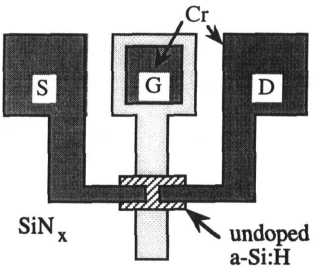
$$R = \frac{\left(\bar{Y}_s d_s^2 - \bar{Y}_f d_f^2\right)^2 + 4\bar{Y}_f \bar{Y}_s d_f d_s \left(d_f + d_s\right)^2}{6\varepsilon_M \bar{Y}_f \bar{Y}_s d_f d_s \left(d_f + d_s\right)}. \quad (6)$$

Here $\bar{Y} = Y/\left(1-\nu^2\right)$ is the plane strain elastic modulus [5]. For a compliant substrate, Eq. (6) must be used instead of the Stoney formula (Eq. (3)), for example, when calculating the mismatch strain from the experimentally determined radius of curvature. Figure 1 shows the normalized radius of curvature, calculated using Eq. (3) and Eq. (6), plotted as a function of the film-to-substrate thickness ratio. In the case of inorganic semiconductors and metals on a glass substrate, $Y_f / Y_s \cong 1$, and the Stoney formula is a good approximation if $d_f / d_s \leq 0.1$. In the case of an organic polymer substrate, $Y_f / Y_s \cong 100$, and the Stoney formula is useful only for $d_f / d_s \leq 0.001$. Because our substrate is only 50 μm thick, $d_f / d_s \cong 0.01$, and Eq. (6) must be used. Another important conclusion from Figure 1 is that even with a compliant substrate, theoretically there are two regimes when the film/substrate couple is flat, i.e., $R \to \infty$: (1) the film is much thinner than the substrate and therefore must comply with it, and (2) the film is much thicker than the substrate and therefore the substrate must comply with the film.

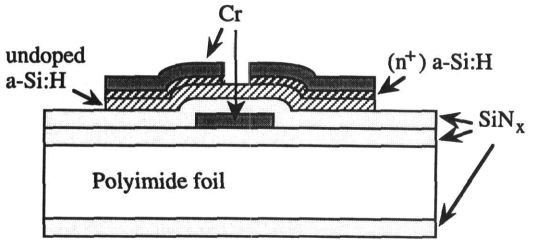
TRANSISTOR FABRICATION

Before proceeding with a-Si:H TFT fabrication, the deposition of all layers had to be re-optimized for 150°C to obtain electrical properties comparable to those obtained at higher temperature. The gate SiN_x was deposited from a mixture of SiH_4, NH_3 and H_2, the undoped a-Si:H from a mixture of SiH_4 and H_2, and the (n^+) a-Si:H from a mixture of SiH_4 and PH_3.

The TFTs have a bottom gate, back-channel etch structure. We began by passivating the polyimide substrate on both sides with a 0.5 μm thick layer of SiN_x. These layers serve as a barrier against the solvents, bases and acids used during photolitography. An ~ 100 nm thick Cr layer was thermally evaporated and wet etched to create the gate electrode. Then we deposited a sequence of the following layers in a three-chamber PECVD deposition system: ~ 400 nm of SiN_x, ~ 200 nm of undoped a-Si:H, and ~ 50 nm of (n^+) a-Si:H. An ~ 100 nm thick Cr layer was thermally evaporated. We wet etched the Cr source-drain pattern and dry etched the (n^+) a-Si:H in CF_4 gas. Then the undoped a-Si:H was dry etched to define the transistor island. In the last photolithographic step, we dry etched windows into the SiN_x to open access to the gate contact pad. Arrays of six TFTs were fabricated on 1.5 x 1.5 sq. in. substrates. Four substrates were processed simultaneously. Figure 2 shows the top and the cross-sectional views of one TFT.



a) Top view



b) Cross-sectional view through TFT and substrate.

Figure 2. Top and cross-sectional views of one TFT. (a) The areas marked S, G, D are the contact pads.

RESULTS AND DISCUSSION

The dependence of the source-drain current I_{ds} on the gate voltage V_{gs} for V_{ds} = 0.1 V and 10 V is shown in Figure 3 (a). The source-drain current I_{ds} as a function of the source-drain voltage V_{ds} for nine different V_{gs} voltages is shown in Figure 3 (b). The off-current is ~ 1 x 10^{-12} A (< 1 x 10^{-14} A/μm) and the on-off current ratio is > 10^7.

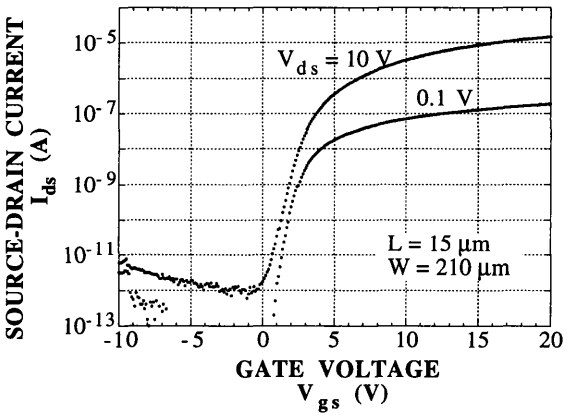


Figure 3 (a). Source-drain current as a function of gate voltage for V_{ds} = 0.1 V and 10 V. The source electrode is grounded.

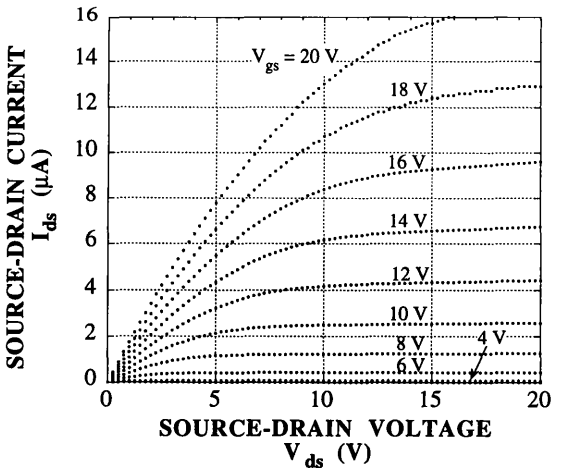


Figure 3 (b). Source-drain current as a function of source-drain voltage for V_{gs} = 4, 6, 8, 10, 12, 14, 16, 18, and 20 V. The source electrode is grounded.

In the linear approximation the source-drain current is given by:

$$I_{ds} = \frac{W}{L} C_{SiN} \mu_n \left[\left(V_{gs} - V_T \right) V_{ds} - \frac{V_{ds}^2}{2} \right], \tag{7}$$

where W is the channel width, L the channel length, C_{SiN} the capacitance of the gate insulator, μ_n the effective electron mobility, and V_T the threshold voltage. At $V_{ds} = 0.1$ V we obtain $V_T \sim$ 3.5 V and a value of 1.12 x 10^{-8} AV^{-1} for the $(C_{SiN} \mu_n V_{ds} W / L)$ product. The dielectric constant of our 150°C nitride measured at 1 MHz is 7.46. Using C_{SiN} = 1.65 x 10^{-8} F cm^{-2} we calculate a linear mobility of ~ 0.5 cm^2 V^{-1} s^{-1}. These values are comparable to those of a-Si:H TFTs fabricated on glass substrates at temperatures between 250°C and 350°C.

SUMMARY

We have fabricated high-performance a-Si:H TFTs on 2-mil. (51 μm) thick polyimide foil (Kapton® E) substrate at a temperature of 150°C. These transistors exhibit performance comparable to that of a-Si:H TFTs fabricated on glass substrate at temperatures between 250°C and 350°C. The off-current is ~ 10^{-12} A, the on-off current ratio is > 10^7, the threshold voltage is 3.5 V, the sub-threshold slope is ~ 0.5V/decade, and the linear-regime mobility is ~ 0.5 cm^2 V^{-1} s^{-1}. Mechanical analysis shows that the stress developed in the transistor structure on the compliant polyimide substrate is approximately one-half of the stress of the same structure when deposited on a glass substrate. A new expression for the radius of curvature of the film/substrate couple is developed for the case of such compliant substrates.

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REFERENCES

1. M.S. Feng, C.W. Liang, and D. Tseng, J. Electrochem. Soc. **141**, 1040 (1994).

2. C.S. McCormick, C.E. Weber, J.R. Abelson, and S.M. Gates, Appl. Phys. Lett. **70**, 226 (1997).

3. S.M. Gates, in Amorphous and Microcrystalline Silicon Technology - 1997, edited by S. Wagner, M. Hack, E.A. Schiff, R. Schropp and I. Shimizu (Mat. Res. Soc. Proc. **467**, Pittsburgh, PA, 1997), pp. 843-849.

4. A.G. Evans and J.W. Hutchinson, Acta Materialia **43**, 2507 (1995).

5. S. P. Timoshenko and J. N. Goodier, Theory of Elasticity (McGraw-Hill, New York, 1970).

6. M. Finot and S. Suresh, J. Mech. Phys. Solids **44**, 683 (1996).