

5 Novel Processing Technology for Macroelectronics

S. Wagner¹, H. Gleskova¹, J.C. Sturm¹, and Z. Suo²

¹ Department of Electrical Engineering and Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ 08544, USA
E-mail: wagner@princeton.edu

² Department of Mechanical and Aerospace Engineering, Princeton University, Princeton, NJ 08544, USA

Abstract. Large-area electronic circuits on thin foil substrates can be made with techniques adapted from conventional printing. Conventional printing can provide a resolution and an overlay registration of 10 µm and ±5 µm, respectively, which will allow making thin-film transistors (TFTs) at densities above 10 000 per square centimeter. An early example is the use of laser-printed toner etch masks for the fabrication of amorphous silicon TFTs. Patterned devices can be made by direct printing, as demonstrated by the jet printing of the active polymer for organic light-emitting diodes (OLEDs). Paper-thin foils of glass, steel, and polyimide can serve as substrates for making TFTs with characteristics comparable to those made on glass plates. Materials options for thin foil substrates are described. A study of the mechanics of films on stiff and compliant foil substrates shows that particularly rugged and flexible device structures can be made when the foils are very thin. Integrating OLEDs with thin-film transistors on steel foil substrates provides an early example of 3-D integrated components for macroelectronics.

5.1 Introduction

Following many years of experimentation, development and manufacturing, the active-matrix liquid crystal display (AM-LCD) has become a very successful product in laptop computers, workstations and personal computers (see Chap. 2). Its success seems assured in view of the favorable reaction of early users, who experience less eye fatigue when working with AM-LCD than with cathode ray tube (CRT) screens. For the wide-spread application of large-area electronics such as digital wallpaper, smart materials, and intelligent barcodes, its cost must be reduced to well below the present value of approximately \$5 per square inch (\$8 000/m²). This need for cost reduction has been recognized for some time. In the Giant Electronics program a group of Japanese laboratories sought to introduce printing techniques to the fabrication of AM-LCDs [5.1]. A group at the Philips Research Laboratories has been developing a technology for producing organic electronics by using a combination of photochemical and wet chemical reactions in spun-on layers on plastic substrates [5.2]. In this chapter we explore the application of printing techniques and thin foil substrates to large-area electronic, or macroelectronic, technology.

We begin with a brief discussion of the per-area cost of macroelectronics and make a case for the advantages of direct printing. The practicality of printing depends on the resolution and the overlay registration achievable by conventional printing techniques. These two parameters are discussed next. Then we describe the fabrication of amorphous silicon thin-film transistors with a process that uses laser printed toner masks instead of photoresist. This process illustrates the reduction in the number of steps achievable by printing. Our goal, the direct printing of patterned device materials, is illustrated by the jetting of polymer solutions to produce organic light-emitting diodes. Printing equipment often relies on the use of flexible substrates, which can be of particular advantage to macroelectronics because they are lightweight and can be very rugged. In this spirit we continue with a discussion of substrate materials, and of the mechanics of thin films on stiff and on compliant substrates. The practicality of a compliant substrate is illustrated with transistors on polyimide foil. Finally, we show that TFTs and OLEDs can be integrated to create a thin-film display on a foil substrate.

Macroelectronic products, for example display banners, digital wallpaper, or smart greeting cards in many cases must be large but need not necessarily have a high device density. Hence it is useful to gauge the cost of electronics per unit area rather than by cost of function.

We do this in Table 5.1. Inspection of the cost of integrated circuits (ICs) and displays shows that AM-LCDs cost an order of magnitude less than silicon ICs, but an order of magnitude more than present-day large-area photovoltaic (PV) modules. Thin-film PV modules are complex multilayer devices (Chap. 6). For example, the triple-junction module made by United Solar Systems Corporation contains 12 layers, some of which are only 10 nm thick [5.3]. These modules are integrated monolithically over large areas. In the Solarex module, a 0.80 m^2 large ten-layer device structure is interconnected using laser scribing [5.4]. Experience with PV modules shows that complex, multilayer, active electronics can be made at a cost well below \$ 1 000 per square meter. However, integrated PV modules need few patterning steps, and the individual diodes still measure many square centimeters. What will it take to fabricate inexpensive, large-area transistor electronics with a useful device density?

Table 5.1. The cost of integrated circuits and information displays

Technology	Cost ($\$ \cdot \text{m}^{-2}$)
Silicon integrated circuit (microprocessor – memory)	500 000–50 000
Active-matrix liquid crystal display	10 000–6 000
Cathode ray tube	3 000–1 000
Amorphous silicon solar module (present → target)	400 → 100
Mail-order catalog (four-color print)	0.1

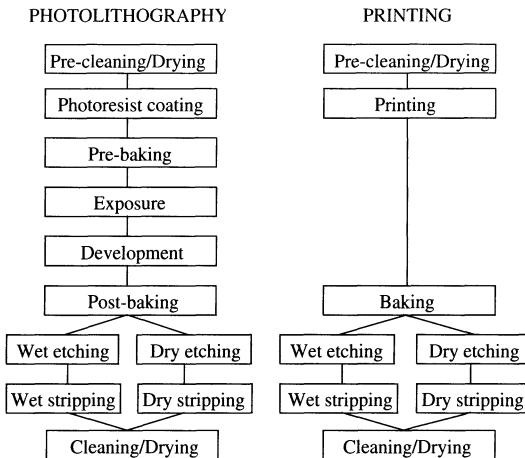


Fig. 5.1. *Left:* Steps in typical photolithography. *Right:* Steps in a process by which devices are patterned using printed etch masks. This figure illustrates the reduction in the number of process steps made possible by printing (from [5.5])

If we take the development of thin-film PV as a guide, we see that the introduction of large-area electronics relies on two coupled developments. One is the reduction of materials input, and the other is the reduction of the number of process steps. Using thin films, thin substrates and thin encapsulation reduces materials input. Reducing the number of process steps lowers the cost of equipment, and the consumption of the ancillary chemicals that are used in circuit processing. The number of process steps could be reduced greatly by the direct printing of the active materials as illustrated in Fig. 5.1 [5.5]. In drawing an analogy between the printing of books and the fabrication of integrated circuits this reduction becomes evident. If books were made like ICs, the paper would be first blackened with ink, and then the ink would be removed selectively to leave letters standing on a white background. Thus the use of laser printed masking layers, instead of photoresist, for etch or lift-off provides a good example for the transition from IC fabrication to book-printing techniques.

In IC fabrication the application or modification of the active material is separate from its patterning, because the material properties and the material pattern are optimized best when done in separate steps. If one wishes to print active circuits directly, one must devise materials that can be applied and patterned in a single step. The materials needed for the printing of active circuits include metallic conductors, insulators, semiconductors for transistors and light emitters, piezoelectric materials, etc. This approach to the printing of active circuits explores the territory that lies between ICs and printed-wire boards. In effect, large-area printed electronics will be active circuits monolithically integrated with their packaging.

Completed thin-film circuits are at most a few micrometers thick. Therefore the substrate and encapsulation constitute the bulk of the finished product. Reduction of their weight and thickness becomes important. When the substrate is reduced to a thickness where it becomes flexible, it also becomes usable in continuous, roll-to-roll paper-like production. The finished circuit then is a flexible foil, and using equally thin encapsulation will preserve this flexibility. We shall see that rugged thin-film circuits are a natural consequence of the mechanics of thin foil substrates.

Large-area transistor circuits may be integrated with light valves or emitters, light sensors, piezoelectric actuators, and many other opto-electronic or microelectromechanical devices. At the end of this chapter we illustrate the beginning of this integration with a TFT/organic light-emitting diode (OLED) pixel.

When large-area circuits are made by programmable printing, for example xerography or ink jetting, they can serve as vehicles for rapid prototyping [5.6]. It is conceivable that in an electronic printing shop single copies or short runs of circuits will be programmed and printed on short order. The laser printing of toner etch masks, which are designed on the computer that drives the laser printer, and the jet printing of polymers for organic light-emitting diodes illustrate this emerging capability.

5.2 Resolution and Registration: The Density of Functions Achievable by Printing

Programmable advertising banners may have square-centimeter size pixels and cover an area of many square meters. Intelligent barcodes, on the other hand, may cover only a few square centimeters but need high resolution. The development of microelectronics has shown that the search for high pattern density is one of the main drivers of IC technology. Therefore, it is instructive to estimate the density of active devices that could be produced by using conventional printing techniques.

Let us look at the density of amorphous-silicon thin-film transistors achievable by printing. The smallest size of a TFT will be set by two parameters. One is the smallest size of a pattern that can be defined by additive printing, which in IC technology is specified as the design rule. We give it the symbol λ . The second parameter is the accuracy of overlay, or registration, of subsequent patterns, which is quantified as the overlay alignment error $\pm\delta$. We illustrate the effect of these two parameters on the achievable density of thin-film transistors with the layout illustrated in Fig. 5.2, of a conventional inverted-staggered a-Si TFT without back channel passivation. Here we assume that any subsequent layer can be registered to any preceding layer with an accuracy of $\pm\delta$. Figure 5.2 shows that the overall length of the TFT is $(\lambda + 8\delta)$, its overall width $(W + 6\delta)$. We assume an inactive fringe of width δ . Thus the area occupied by the device is $(\lambda + 8\delta)(W + 6\delta)$.

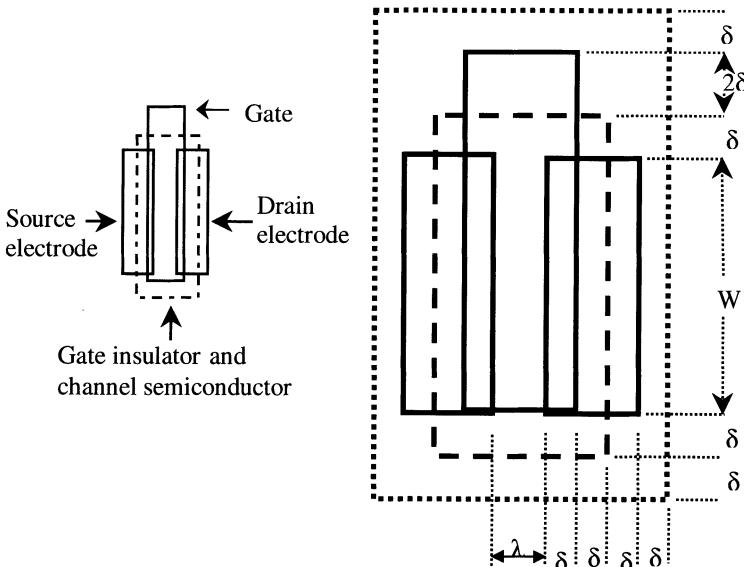


Fig. 5.2. *Left:* Layout of a thin-film transistor in the inverted staggered configuration. *Right:* The effects of resolution λ and overlay registration δ on the size of the TFT. λ sets the channel length L . The effect of the channel width W is discussed in the text

The printing industry defines resolution differently from the semiconductor industry, because it gauges by visual impact rather than device geometry and electrical function. However, the term resolution in spots per inch (spi) employed in digital imaging by the printing industry [5.7] is coming close to its use in microelectronics. For our first-order estimate we will assume that to both industries “resolution” means the number of resolvable, unbroken, line pairs per unit length. Resolution of present-day high-quality, large volume color printing is exemplified by the offset printing for the National Geographic Magazine, which is ≈ 2500 spi. Experts agree that current printing technology can achieve a resolvable line separation of $\lambda = 10\mu\text{m}$. This value will be our TFT gate length L . The accuracy of overlay registration δ achievable with present-day printing technology is $\pm 5\mu\text{m}$. This value will be our alignment tolerance [5.8].

The value of the W/L ratio will depend on the TFT application. It will be small in switches, and large in power transistors for driving OLEDs. Let us assume that we are building a logic circuit made of switches that need an ON current of $I_{\text{ON}} = 5\mu\text{A}$. The drain current in saturation is given by,

$$I_{\text{D}}(\text{sat}) = (W/L)\mu_{\text{e}} (\varepsilon_{\text{ins}}\varepsilon_0/d_{\text{ins}}) (V_g - V_{\text{th}})^2/2 . \quad (5.1)$$

For the typical values of the electron mobility μ_{e} of $1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, insulator dielectric constant ε_{ins} of 7.5, insulator thickness d_{ins} of 320 nm, and $(V_g - V_{\text{th}}) = V_{\text{S/D}} = 10\text{ V}$, $I_{\text{D}}(\text{sat})$ becomes $(W/L) \mu\text{A}$. The equivalent source-

drain resistance is $R_{SD} = 10(L/W) \text{ M}\Omega$. A TFT that delivers $I_{ON} = 5 \mu\text{A}$ will need $W/\lambda = 5$. The area of each TFT will be $4000 \mu\text{m}^2$ (Fig. 5.2), and the packing density will be 25 000 transistors per cm^2 .

Note that this packing density of a-Si TFTs is less than 1/1 000 that of IC MOSFETs, and that the speed of a printed a-Si:H TFT will be 1/10 000 the MOSFET speed. Obviously, printed TFTs will not make sense as competitors of IC MOSFETs. But at a packing density of 25000 cm^{-2} , printed TFTs will be acceptable for many applications that need large area, or integrated packaging. Building-sized displays may require only a few TFTs per square centimeter, and a printed-TFT smart card with a surface of $\approx 50 \text{ cm}^2$ will hold as many as 10^6 printed TFTs on one level.

The physical limits of the resolution λ and the overlay registration $\pm\delta$ depend on the tools and materials that are used for printing. First, the ink must have sufficiently fine grain. This condition is easy to meet in principle by using molecule-based inks (solutions) or inks containing fine particles like polystyrene latex, which is available commercially in sizes down to $\approx 10 \text{ nm}$. Second, the tools for printing and alignment must have sufficient resolution. When light is used for both printing (as in electrophotography) and alignment, the physical limits for both λ and $\pm\delta$ are $\leq 1 \mu\text{m}$. Thus, in principle, both ink and tools can easily meet our requirements of 10 and $\pm 5 \mu\text{m}$, respectively.

Commercial printing is carried out in two steps. In the pre-press step, text or image is transferred to a printing plate. In a second step this plate is used to do the printing [5.7]. The resolution of plate-making and printing techniques can be as high as 2 000–4 000 spi (12.7 – $6.4 \mu\text{m}$). By using either three-point mechanical or optical alignment the overlay registration can be brought to $\pm 5 \mu\text{m}$ [5.9]. Thus the know-how and the components for the printing of active electronics at useful resolution and registration do exist.

The ratio of resolution to registration accuracy appears to be the same at all scales ranging from microelectronics to large-scale printing [5.10]. The IC resolution is $\approx 0.25 \mu\text{m}$ and the overlay tolerance $\leq 0.1 \mu\text{m}$. High-speed gravure presses print a linewidth of $\approx 150 \mu\text{m}$ with a registration of $\approx 50 \mu\text{m}$. The printing speeds are very different, though. While a modern IC plant produces approximately 10000 m^2 of ICs per year, a modern gravure press prints on this surface in about 5 min. Indeed the speed of today's printing presses is so high that large-area electronics may first be printed on plate-making equipment rather than printing presses. Note that a ratio of $\lambda/\delta = 3$ is easily compatible with the assumptions we used in calculating the packing density of printed TFTs.

The physical limits of several printing techniques are considerably finer than the resolution and registration of conventional printing equipment. Laser writing can produce a resolution of the order of $1 \mu\text{m}$. Nanoimprinting has demonstrated a resolution in the tens of nanometer range [5.11]. Therefore, the density of directly printed devices can be raised orders of magnitude above

$\approx 10\,000$ per square centimeter. We can anticipate continuous improvements of resolution and registration once a direct-printing industry for electronics has come into existence.

5.3 Printed Toner Masks for Etching and Liftoff

The fabrication of integrated circuits alternates between deposition or modification of a layer of material and the patterning of this layer. The established patterning process is photolithography, which typically consists of the nine steps shown in Fig. 5.1. The patterned photoresist serves as the etch mask for the active material that it covers. This step is shown as wet etching or dry etching in Fig. 5.1. Patterned photoresist also can serve for patterning overlying active material in a process called Liftoff. Both processes can be shortened by three steps if the etch or liftoff masks are printed directly. A typical patterning sequence using a printed mask is shown on the right-hand side of Fig. 5.1. We now describe two practical processes that use laser-printed toner as masks for etch and liftoff. The first process relies on a combination of mask printing and of toner transfer via an auxiliary paper substrate. The second exclusively uses masks that are printed directly on the substrate. The mask material is xerographic toner, which is applied with a 600 dpi laser printer. The two processes represent chronological developments and are not necessarily tied to either glass or steel substrates.

5.3.1 Toner Masks via Paper Transfer: TFTs on Glass Foil

TFTs from a-Si:H have been fabricated on $50\,\mu\text{m}$ thick alkali-free glass foil (Schott AF45), with the glass foil providing the flexibility required by an office-type laser printer. The bottom-gate, back-channel-etch TFTs need four mask levels, or patterning steps. These steps include direct laser printing of the first mask [5.6] and toner transfer for the higher levels. The channel length L and width W of the TFTs are $100\,\mu\text{m}$ and $500\,\mu\text{m}$, respectively. The gate electrode is $300\,\mu\text{m}$ long. The complete TFT process is shown in Fig. 5.3 [5.5]. The first step is to run the glass foil through the laser printer to print a negative toner gate mask. Then an $\approx 100\,\text{nm}$ thick Cr layer is thermally evaporated and the Cr-on-toner is lifted off in toluene. The silicon stack is deposited in a three-chamber plasma-enhanced chemical vapor deposition system: $\approx 410\,\text{nm}$ of SiN_x , $\approx 160\,\text{nm}$ of undoped a-Si:H and $\approx 50\,\text{nm}$ of (n^+) a-Si:H. An $\approx 100\,\text{nm}$ thick Cr layer for source/drain contacts is thermally evaporated. Then a positive source/drain pattern is printed using transfer paper [5.12, 14]. The Cr layer is wet etched, the (n^+) a-Si:H layer dry etched in CF_4 , and the toner is removed. Next, a positive toner mask is printed to define the TFT island, again using transfer paper. The undoped a-Si:H layer is dry etched in CF_4 . Without stripping the island mask, the final toner mask for opening the gate electrode pad is printed, again using transfer paper. The

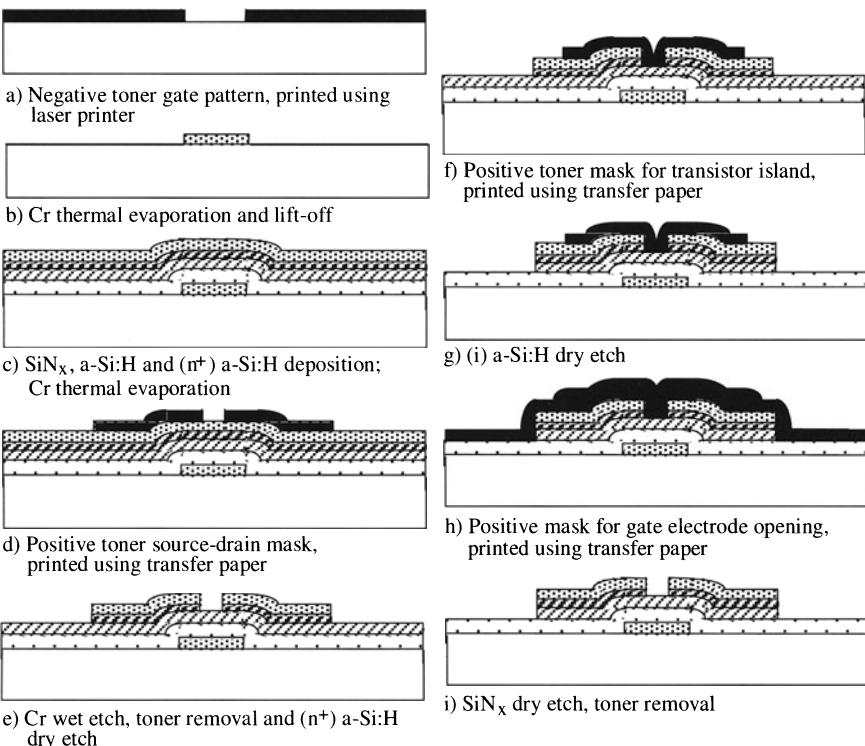
Cross-section through the transistor island

Fig. 5.3a–i. Process for making TFTs using toner masks. Steps (a) and (b) show lift-off. The other toner steps are etch masks applied by using transfer paper. Function and composition of the layers is evident from the captions (from [5.5])

SiN_x is dry etched in CF₄ and the toner is removed. Finally the TFTs are annealed in forming gas at 200°C to anneal out the radiation damage caused by the plasma during dry etching.

The photograph of a TFT made by this process, and the transfer characteristics of this transistor are shown in Fig. 5.4 [5.5]. These characteristics are identical to those of TFTs made on glass plate substrates by conventional photolithography. The channel of this transistor lies at the bottom center of the photograph, which is dominated by the contact pads, which were made large to ease the probing of curved substrates.

The size distribution of toner particles for commercial laser printers is centered at 7–10 µm [5.15]. This large particle size produces irregular edges, as can be seen in Fig. 5.5a [5.16]. The toner particles also spread into open areas, and they do not coat the printed areas perfectly. This irregularity is a consequence of the mutual repulsion of toner particles, of variations in the surface charge density of the toner particles, and of the attenuation by the glass substrate of the electric field gradient that directs the toner particles.

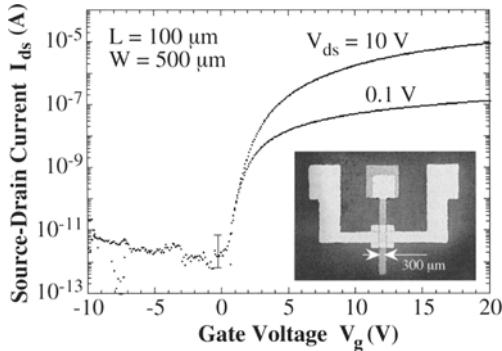


Fig. 5.4. Transfer characteristics of an a-Si:H TFT made by the process of Fig. 5.3 on glass foil. The inset is a photograph of the TFT structure. Source, gate, and drain contact pads lie near the upper edge of the photograph. The 100 μm long channel lies in the center of the TFT island, which is close to the lower edge. The gate electrode is 300 μm wide (from [5.5])

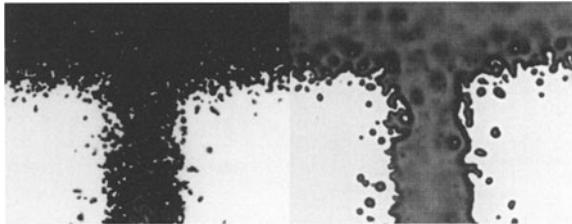


Fig. 5.5. An as-printed toner pattern before (*left*) and after (*right*) post-printer fusing. The vertical line is $\approx 100 \mu\text{m}$ wide ([5.16])

The laser printer has a fusing stage in which the toner particles are sintered to the substrate and to each other. The bulk of a typical toner particle is a polystyrene-based copolymer with a glass temperature near 100°C. During the fusing step in the printer the temperature may reach 170°C for a fraction of a second, but this treatment does not suffice to melt the toner particles completely. Printed areas therefore remain porous to etchants. A post-printer anneal for 1 h at 120°C melts the toner to the extent that it forms a contiguous, impermeable layer, and that small holes in the printed layer close. The pattern of Fig. 5.5b was fused at 160°C for 30 min. Figure 5.6 [5.17] shows surface profiler traces of a toner layer out of the laser printer, and after the post-printer anneal, respectively.

5.3.2 All Masks Printed Directly: TFTs on Steel Foil

If provisions are made for reproducible alignment of the substrate in the laser printer, all toner masks can be printed directly onto the substrate [5.18]. To do so, the substrate is aligned mechanically for each patterning step by

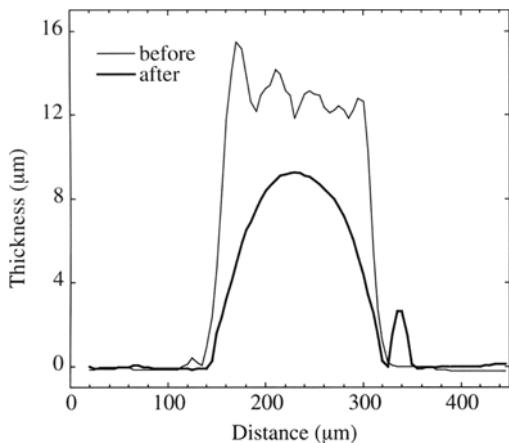


Fig. 5.6. Surface profiler traces across a toner line as produced by the printer, and after the post-print anneal. Note the reduction in cross section caused by compaction of the toner (from [5.17])

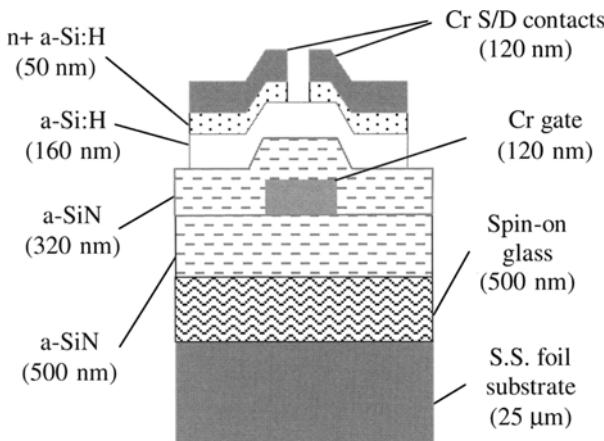


Fig. 5.7. Cross-section of a TFT on steel foil, showing materials and typical layer thicknesses (from [5.18])

matching registration marks between the substrate and a rigid carrier. The carrier is fed into the laser printer and is aligned in the printer just like a sheet of paper. The schematic cross section of a TFT on steel foil is shown in Fig. 5.7 [5.18]. The performance of TFTs made by printing all toner masks directly is comparable to that of TFTs made on similar steel foil but using photolithography, as is evident from Fig. 5.8 [5.18].

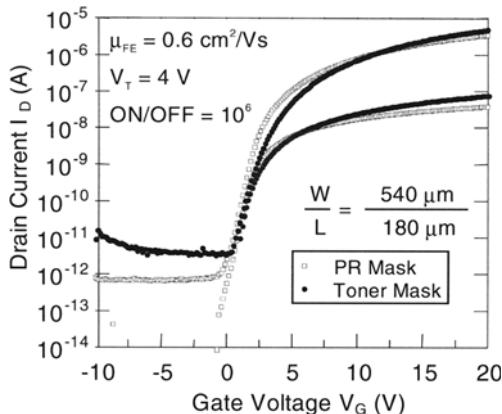


Fig. 5.8. Transfer characteristics of two TFTs made on 25 μm thick steel foil. One TFT was made using conventional photolithography, the other by printing all mask layers directly in a laser printer (from [5.18])

5.4 Printing Active Materials: Jetting Doped Polymers for Organic Light Emitting Devices

Direct printing of active materials is expected to produce large-area electronics at very low cost. An early example of direct printing is the printing of the active polymers for organic light-emitting diodes [5.19]. One group of organic materials for OLEDs consists of polymer hosts that permit charge transport and are doped with color centers. The color centers are organic dyes that emit light upon electron–hole recombination. The choice of dopant dye determines the color of emitted light. In the case of organic device materials the direct printing provides a particular advantage: It is the first simple process for the patterning of monolithically integrated three-color OLEDs.

An ink-jet printer was used with a resolution of 640 dots per inch. The piezoelectric printhead squirts ink droplets from a nozzle with a 65 μm opening. Four ink cartridges and four nozzles enable the printer to print four different colors simultaneously. As the printer head scans the page and the piezoelectric materials are pulsed, ink is squirted from the nozzles onto the page. The only modification to the ink-jet printer for printing OLEDs was to replace the original inks in the cartridges with polymer solutions.

The hole-transport polymer poly(N-vinylcarbazole) (PVK), and one of the fluorescent dyes coumarin 6 (C6) for green, coumarin 47 (C47) for blue, and nile red were dissolved into chloroform solution, which was then deposited by jetting, or by spin coating for comparison. No electron transport material was used in this initial work. After deposition the chloroform evaporates leaving a doped polymer material. Typical concentrations of PVK dissolved in chloroform were 10 g/l, and dye dissolved in chloroform were 0.1 g/l, yielding on the order of 1% dye in the PVK. Chloroform solutions containing varying

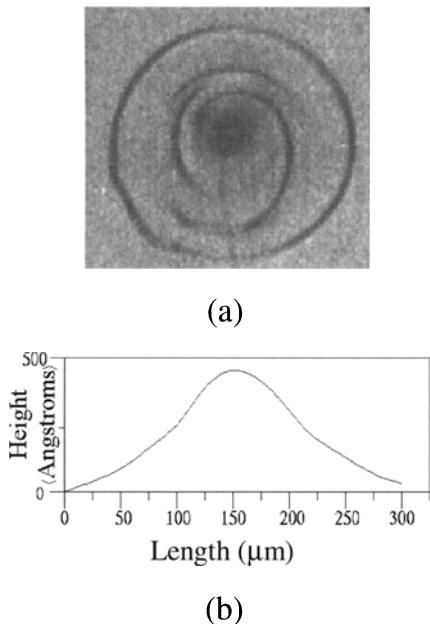


Fig. 5.9. (a) Photograph of a jet-printed dot; (b) surface profile of a jet-printed dot 300 μm wide (from [5.19])

amounts of PVK and luminescent materials were prepared by stirring and were passed through 0.45 μm filters. Thin films were jettet onto 175 μm thick flexible polyester coated with indium tin oxide (ITO). Before deposition, the ITO was treated with an oxygen plasma to modify its surface properties for making ohmic contact to the OLEDs.

The optical micrograph of a jet-printed dot and a surface profile of the shape of a typical dot are shown in Fig. 5.9 [5.19]. The thickness of the dots ranged from 40 to 70 nm and the dot widths ranged from 150 to 300 μm . The larger-diameter dots tended to be thicker, indicating that the thickness variation is due to the total amount of deposited solution. One can see some structure within the dot, which may be evidence of mass transport due to segregation as the solvent evaporated. To demonstrate the ability of the jet-printing technique to deposit patterns, PVK doped with C6 or nile red was deposited in a jet-printed test pattern. This sample was then illuminated using ultraviolet light, which excited green (or red) emission from the patterned polymer.

Figure 5.10 shows the photoluminescence spectra of three individual jet-printed thin films and of spin-coated films made from the same solution, each with a different dye [5.19]. The photoluminescence was measured with an excitation wavelength of 380 nm for the C47 doped film and 440 and 520 nm for C6 and nile red doped films, respectively. No significant difference in shape or magnitude is seen between the films prepared by jet-printing vs.

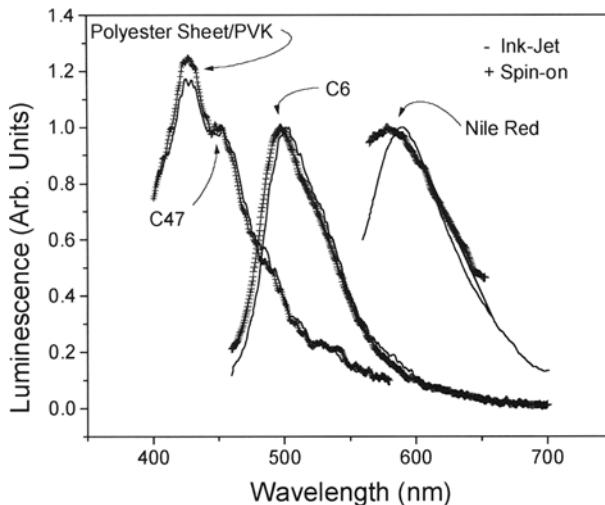


Fig. 5.10. Photoluminescence spectra of PVK doped with coumarin 47, coumarin 6, or nile red. The spectra of jet-printed and spin-coated films are shown for each band. The luminescence spectra are identical for the two techniques of application (from [5.19])

spin coating. It should be noted that the peak of 420 nm in the C47 spectra is due to a combination of the polyester substrate and the PVK host, not the deposited film. The dye luminescence appears as a peak at 450 nm on the shoulder of the 420 nm peak.

It is difficult to fabricate devices directly on top of the polymer dots made by jet-printing because of the difficulty in aligning a shadow mask for metal cathode formation directly over a polymer dot. Therefore, to fabricate test devices the ink-jet printer was operated in a mode to create a continuous film of polymer rather than discrete dots. After jet-printing, the samples were loaded into a vacuum chamber with a base pressure of $< 10^{-7}$ torr for the metallization step of device fabrication. Typically, at least ≈ 90 min were allowed between loading of samples and metal evaporation, and no further heating of samples was done. Top metal cathodes were deposited through a shadow mask to form an array of 250 μm diameter devices on the polymer film. Metal alloys such as Mg:Ag (10:1) were deposited by co-evaporation from two separate sources, followed by the deposition of Ag as a protective layer. The ITO on the polyester sheet served as the anode. The devices were then measured in air without any protective coating.

Figure 5.11 shows the I - V curves of typical devices made by this procedure and a control device fabricated on a film spin-coated from the same polymer solution [5.19]. The organic film thickness of the control device was about 50 nm. Current densities of $\approx 2 \text{ mA cm}^{-2}$ are achieved at a voltage of $\approx 7 \text{ V}$ for the control device, and $\approx 7\text{--}11 \text{ V}$ for the jet printed devices. The

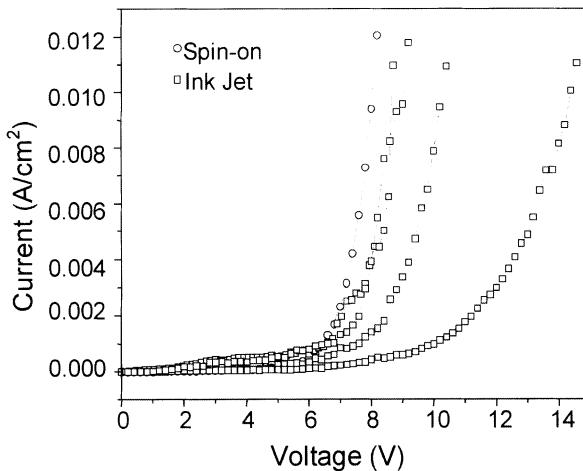


Fig. 5.11. Current-voltage characteristics for one spin-coated and four jetted OLEDs. The turn-on voltage of diodes made by jetting can come close to that of the spin-coated diode (from [5.19])

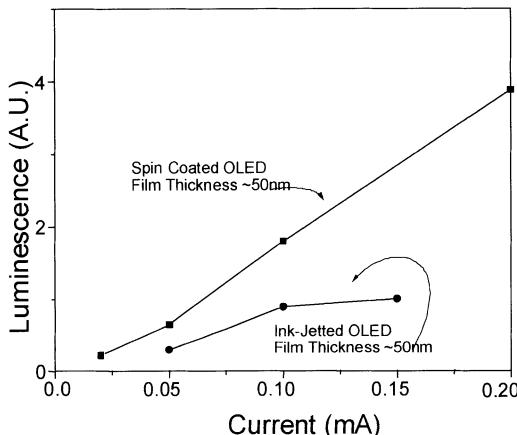


Fig. 5.12. Luminescence versus current characteristics of a spin-coated and a jetted OLED. The efficiency of the jetted OLED is lower than that of the more-developed spin-coated OLED (from [5.19])

luminescence versus current characteristics of the two OLEDs show that the efficiency of this early jet-printed device is about a factor of two lower than that of the spin coated device (Fig. 5.12 [5.19]).

A very promising modification of the approach described above is the local modification of a large-area spin-coated layer of host material by the jetting of solutions of the fluorescent-dye light-emitting dopants [5.20]. The jetted dye diffuses into the host (PVK) and forms the OLED material. This approach allows easy tuning of the UV fluorescence spectra of the film and

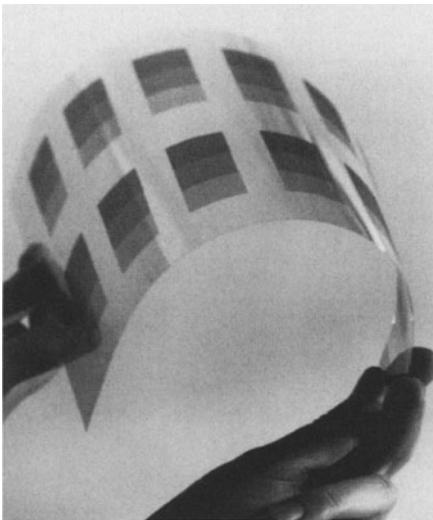


Fig. 5.13. Photograph of a page-size glass foil of 80 µm thickness printed with a transistor pattern of toner (from [5.6])

the spectra of the OLEDs made from the film, while retaining the planarity and film thickness advantages of spin-coating.

5.5 Substrates and Encapsulation for Macroelectronic Circuits

Substrates and encapsulation function as the mechanical support and protection of the thin film circuits. For use in AM-LCDs both must be transparent, while in an OLED display only the encapsulation may need to be transparent. The choice of substrate materials broadens considerably when the process temperature is reduced to below 200°C, and then ranges from the conventional silicate glasses over metals to organic polymers. A concurrent trend to thinner substrates and encapsulation seeks to reduce weight, and for very thin substrates, to increase flexibility and ruggedness. Tables 5.2 and 5.3 list properties of twelve materials that may be used as substrates or encapsulants. Note that the melting, strain or glass temperature, the thermal conductivity, and the coefficient of thermal expansion do vary widely between the materials of the table.

Glass substrates for active TFT circuits are best known and characterized [5.21]. One of the main advantages of borosilicate glasses is that their coefficients of thermal expansion are similar to those of the silicon TFT materials. Glass foil substrates that can be fed through printers with curved paper paths are available with thickness down to 50 µm from DESAG, a Schott subsidiary. The DESAG glass foil is made of borosilicate. This glass needs no

Table 5.2. Optical and electrical properties of materials for substrates and encapsulation^a

Material	Brand name	Density (g cm ⁻³)	Appearance and range of optical transparency (μm)	Refract. index at 0.55–0.6 μm	Dielectric constant at 0.1–1 MHz
Cryst. silicon		2.33	Opaque	3.4	11.8
Soda lime glass	Corning 0211	2.53	Clear 0.4–2.2	1.52	6.7
Borosilicate glass	Corning 7059 Schott AF 45	2.76	Clear 0.35–> 2.5	1.53	5.9
Borosilicate glass	Corning 1737	2.54			
Invar		8.0	Opaque		
Stainless steel	AISI 304	7.93	Opaque		
Aluminum		2.70	Opaque		
Perfluorocyclo- butane aromatic ether polymer	DowXU- 35033.00		Milky white <0.4–>0.6	1.50	2.45
Polyimide	DuPont Kapton E	1.46	Amber		3.4 50% RH
Polyethersulfone		1.37	Pale amber	1.65	3.7
Polyarylate	Kaneka F-1100	1.20	Clear	1.60	2.7
Polycarbonate	Lexan	1.2	Clear	1.58	2.9

^a For references and comments see footnotes to Table 5.3

further passivation prior to a standard a-Si:H TFT process. Foils of soda lime glass with thickness down to 50 μm are available from Corning, or down to 30 μm from DESAG. Soda lime glass must be passivated with a deposited SiO₂ or SiN_x barrier to prevent Na diffusion. Fusing or HF-etching the edges reduces breakage, because cracks propagate easily from the saw-damaged edges. When supported uniformly, glass foil is surprisingly resistant against impact by blunt objects, but it does shatter upon impact of sharp objects. The Corning glass foils tend to have a wavy surface that gives it anisotropic flexibility but does not affect the a-Si:H fabrication and laser printing. The flexibility of an 80 μm thick page-size glass foil is demonstrated in Fig. 5.13, which shows a laser-printed toner pattern [5.6]. A transistor made on 50 μm

Table 5.3. Mechanical and thermal properties of materials for substrates and encapsulation

Material (same brands as in Table 5.2)	Young's modulus Y (GPa)	$T_{\text{melt}},$ T_{strain} , or T_{glass} ($^{\circ}\text{C}$)	Coefficient of thermal expansion at 20°C (10^{-6} K^{-1})	Thermal conductivity ($\text{W m}^{-1} \text{ K}^{-1}$)	(Primary lit. references) Comments Chemical composition
Cryst. Silicon	190	$1415 T_{\text{m}}$	2.4	165	^(a,b) For comparison.
Soda lime glass	74	$508 T_{\text{s}}$	7.4 at 300°C	0.12	^(c) KNaZn borosilicate T_{strain} at 10^{14} Poise
Borosilicate glass	68	$593 T_{\text{s}}$	4.7	≈ 1	^(d,e) BaAl borosilicate T_{strain} at $10^{14.6}$ P Shrinks 10^{-4} at 450°C 8 h
Borosilicate glass		$670 T_{\text{s}}$	3.7	≈ 1	^(f) Shrinks 3×10^{-4} at 450°C 8 h
Invar	140	$1430 T_{\text{m}}$	1.2	13	^(g) 64 Fe, 36 Ni (wt.%)
Stainless steel	190	$\approx 1400 T_{\text{m}}$	18	16	^(g) 18 Cr, 10 Ni (wt.%)
Aluminum	70	$660 T_{\text{m}}$	24	237	^(g) Y for hard Al
Perfluorocyclo- butane aromatic ether polymer	2.3	$400 T_{\text{g}}$	90		^(h) Experimental grade. Contains 0.021 wt.% water. Wt. loss 0.4%/h air 350°C
Polyimide	5.2	$\geq 250 T_{\text{g}}$ (est.)	12	≥ 0.1	^(i,g) CHE $9.10^{-6}/\%$ RH. Shrinks 0.3×10^{-3} at 200°C
Polyether-sulfone	2.4	$200 T_{\text{g}}$	55	0.15	^(g)
Polyarylate	≥ 2 (est.)	$215 T_{\text{g}}$	51		^(j) Shrinks 2×10^{-3} at 180°C 3 h
Polycarbonate	2.3	$160 T_{\text{g}}$	70	0.2	^(g,k) Degasses $> 160^{\circ}\text{C}$

^a Bell Labs Quick Reference Manual (May 1975).^b AIP Handbook, McGraw Hill, New York (1972).^c Corning Product Information PI-0211-87.^d N.P. Bansal, R.H. Doremus, Handbook of Glass Properties. Academic (1986).^e Schott/DESAG spec. sheet AF 45 and D 263.^f D.M. Moffatt, Mat. Res. Soc. Symp. Proc. **377** (1995).^g Goodfellow Catalog (1996/97).^h D. Perettie, L. Bratton, J. Bremmer, D. Babb, Liq. Cryst. Mater., Devices and Applications II, SPIE **1911** 15 (1993).ⁱ J.A. Kreuz, S.N. Milligan, R.F. Sutton: DuPont Films Technical Paper 3/94, Reorder No. H-54504 Properties, Academic (1986).^j Kaneka spec. sheet.^k S.M. Gates: Mat. Res. Symp. Proc. **467**, 843 (1997)

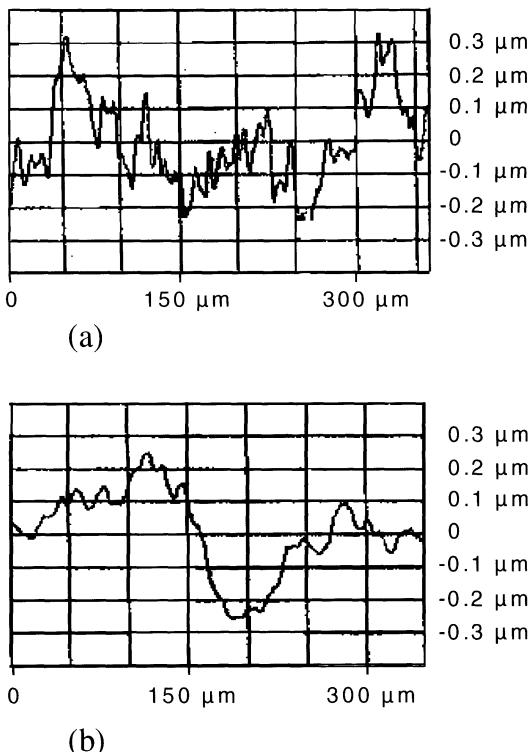


Fig. 5.14a,b. Surface profiles of a steel foil (a) as received and (b) after planarization with spin-on-glass. SOG removes the short-wavelength roughness that reduces transistor yield. The full vertical scales measures $0.8 \mu\text{m}$, and the traces are $400 \mu\text{m}$ wide (from [5.24])

thick Schott AF45 glass foil and its transfer characteristics are shown in Fig. 5.4 [5.5].

Stainless steel foil with thickness between nominally 125 and $200 \mu\text{m}$ (5 and 8 mils) has been used for many years as the substrate for amorphous silicon solar cells made in a roll-to-roll process [5.3]. It is also possible to make TFTs on steel foil [5.22], even with less than $10 \mu\text{m}$ thickness [5.23]. At low thickness the handling of the foil – if processed in free-standing form – dominates TFT fabrication. Steel foil must be coated with an insulator prior to TFT fabrication. A convenient insulator is the silicon nitride that is used as the a-Si:H TFT gate dielectric. Steel foils are made with a wide variation of surface finish, which depends on the state of the rolling equipment. Some surface finish will give high transistor yield with just the SiN_x barrier layer alone. Other surfaces have short-wavelength roughness that needs planarization, which can be done by using the sol-technique of spin-on glass (SOG) [5.24]. The most viscous spin-on-glass precursor results in $\approx 500 \text{ nm}$ thick oxide layers. A surface profile of an as-received $75 \mu\text{m}$ thick AISI 304 stain-

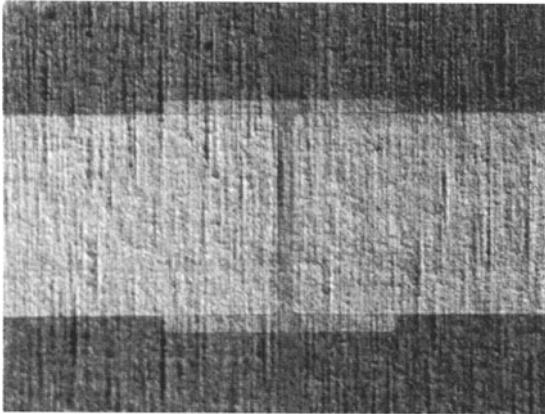


Fig. 5.15. Photograph of a working TFT made on non-planarized $15\text{ }\mu\text{m}$ thick steel foil. The surface finish of the as-received foil was adequate for high TFT yield. Source and drain contacts lie to the left and right of the channel at the center of the TFT island. The channel is $48\text{ }\mu\text{m}$ long (from [5.23])

less steel foil is shown in Fig. 5.14a [5.24]. The TFT yield on this substrate was $\approx 50\%$. Figure 5.14b illustrates the effect of SOG planarization, which suppresses the short-wavelength asperities [5.24]. The TFT yield on this substrate approaches 100%. Figure 5.15, which is a photograph of a functioning TFT on a $15\text{ }\mu\text{m}$ stainless steel foil, illustrates the ruggedness of a-Si:H TFT technology [5.23]. The gap L between the source/drain electrodes on this photograph is $48\text{ }\mu\text{m}$. Despite its rough appearance, the surface of this foil was sufficiently smooth on a microscale that it needed no SOG planarizing layer.

Foil substrates lend themselves to roll-to-roll fabrication and curved process paths. They also provide flexibility and ruggedness during use. Figure 5.16 illustrates the flexibility of TFTs fabricated on a $25\text{ }\mu\text{m}$ thick stainless steel foil [5.25]. The transistors were tested after successive bending to decreasing radii of curvature. They failed by delamination of the spin-on glass from the steel under concave (facing in) bending to 2.5 mm radius, and under convex (facing out) bending to 1.5 mm radius.

This result can be understood using a first-order analysis of the strain of a continuous thin film of TFT material deposited on a steel foil. Film and substrate have nearly identical Young's moduli of $\approx 200\text{ GPa}$ (Table 5.3). The bending is dominated by the substrate, which is much thicker than the $\approx 1\text{ }\mu\text{m}$ thick transistor film. Bending the film/foil couple, if free of strain when flat, to a cylinder as shown in Fig. 5.17 induces a strain ε in the surface [5.18].

For a film thickness d_{film} much smaller than the substrate thickness $d_{\text{substrate}}$, the strain-free neutral plane lies in the center of the foil,

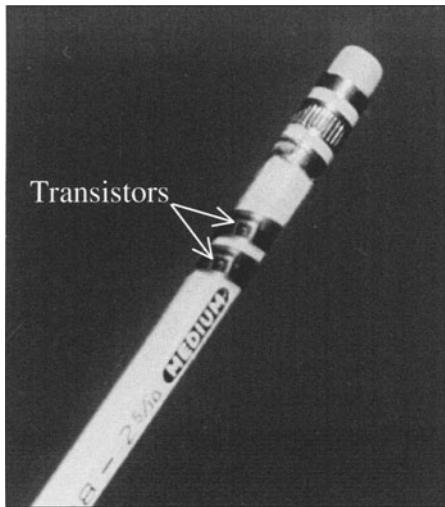


Fig. 5.16. The TFT characteristics are not affected by wrapping the TFT-on-foil around a pencil. The steel foil substrate is $25\text{ }\mu\text{m}$ thick. Note the TFT islands (from [5.25])

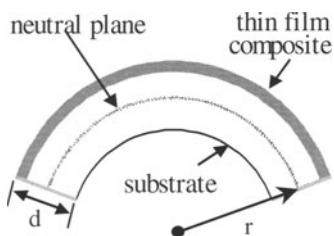


Fig. 5.17. The principal parameters of a film/substrate couple bent into cylindrical shape. The neutral plane is free of strain (from [5.18])

$\approx d_{\text{substrate}}/2$ away from the film [5.18]. The strain ε in the film induced at the bending radius r is given by:

$$\varepsilon \cong d_{\text{substrate}}/2r . \quad (5.2)$$

Assuming that the transistors fail when a certain level of strain ε_{\max} is reached, it can be seen that the minimum allowable radius of bending r_{\min} scales linearly with foil thickness $d_{\text{substrate}}$

$$r_{\min} = d_{\text{substrate}}/2\varepsilon_{\max} . \quad (5.3)$$

When the sample is held flat during film growth, it usually is under strain after fabrication, before intentional bending. Transistors grown on steel (Figs. 5.7, 5.15, 5.16) are under compressive strain as a result of differential thermal contraction between the steel ($\alpha_{\text{substrate}} = 18 \times 10^{-6}\text{ K}^{-1}$) and the silicon lay-

ers grown at $\approx 300^\circ\text{C}$ (α_{film} of a-Si:H $\cong 4 \times 10^{-6} \text{ K}^{-1}$ [5.26]). This contraction produces a mismatch strain ε_M , which is given by,

$$\varepsilon_M = (\alpha_{\text{film}} - \alpha_{\text{substrate}}) \Delta T , \quad (5.4)$$

where ΔT is the difference between the temperature of growth and room temperature. The stress in the film σ_{film} produced by the mismatch strain ε_M is given by,

$$\sigma_{\text{film}} = \varepsilon_M Y_{\text{film}}^* . \quad (5.5)$$

Here $Y_{\text{film}}^* = Y_{\text{film}}/(1 - \nu_{\text{film}})$ is the biaxial elastic modulus of the film, with Y_{film} being Young's modulus of the film and ν_{film} its Poisson ratio. This stress causes the substrate to bend to a radius of curvature R , which is given by the Stoney formula [5.27]

$$R = Y_{\text{substrate}}^* d_{\text{substrate}}^2 / 6\sigma_{\text{film}} d_{\text{film}} . \quad (5.6)$$

When the in-plane stiffness of film and substrate becomes comparable, $Y_{\text{film}} d_{\text{film}} \approx Y_{\text{substrate}} d_{\text{substrate}}$, the substrate may deform considerably, which in turn reduces the stress in the film. Thus a substrate becomes compliant in two circumstances. In one, a high-modulus substrate material is made very thin (e.g., steel foils a few μm thick). In the other a low-modulus substrate material is chosen (typical plastic substrates have Young's moduli of $\approx 2 \text{ GPa}$, which is 1% of those of the TFT materials). When the film/substrate couple is held flat in a frame, the stress in the film is given by,

$$\sigma_{\text{film}} = \varepsilon_M Y_{\text{film}}^* / (1 + Y_{\text{film}}^* d_{\text{film}} / Y_{\text{substrate}}^* d_{\text{substrate}}) . \quad (5.7)$$

It can be seen that for $Y_{\text{film}} d_{\text{film}} = Y_{\text{substrate}} d_{\text{substrate}}$ the stress produced in a device film deposited on a compliant substrate is reduced by a factor of 2 below that on a stiff substrate.

When a film is deposited on a compliant substrate that is held flat in a frame, and the structure then is released from the frame, the structure bends. A mismatch strain ε_M , which may include thermal and intrinsic components, produces a radius of curvature R that is given by [5.31],

$$R = \frac{(Y_{\text{substrate}}^* d_{\text{substrate}}^2 - Y_{\text{film}}^* d_{\text{film}}^2)^2}{6\varepsilon_M(1 + \nu) Y_{\text{film}} Y_{\text{substrate}}^* d_{\text{film}} d_{\text{substrate}} (d_{\text{film}} + d_{\text{substrate}})} + 4(d_{\text{film}} + d_{\text{substrate}})/6\varepsilon_M(1 + \nu) . \quad (5.8)$$

Here we assume that $\nu = \nu_{\text{film}} = \nu_{\text{substrate}}$. The normalized radius of curvature as a function of the film/substrate thickness ratio $d_{\text{film}}/d_{\text{substrate}}$ is plotted in Fig. 5.18 for two different ratios of Young's moduli, $Y_{\text{film}}/Y_{\text{substrate}}$ [5.31]. A ratio of $Y_{\text{film}}/Y_{\text{substrate}} = 1$ corresponds to steel or glass substrates, and a ratio of 100 to plastic substrates. Note that for very small and very large $d_{\text{film}}/d_{\text{substrate}}$ ratios the substrate or the film dominate, and the radius of curvature R assumed by the structure after processing is large, reflecting

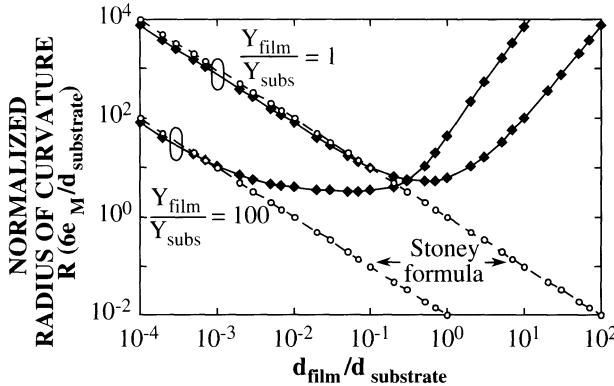


Fig. 5.18. When a film/substrate couple is released after deposition, it will assume a radius of curvature R that depends on the mismatch strain ε_M and on the elastic moduli of film and substrate. The Stoney equation is seen to be valid for $d_{\text{substrate}} \gg d_{\text{film}}$. Results of the complete theory are shown by diamonds (from [5.31])

a flat sample. The radius of curvature becomes smallest for thickness ratios near unity. Figure 5.18 also shows the results of the Stoney equation, which is seen to be a good approximation only if $d_{\text{substrate}} \gg d_{\text{film}}$.

We have seen that the stress induced in a film deposited on a compliant substrate can be reduced by a factor of 2 below that on a stiff substrate. Returning to our initial discussion of the bending of TFTs on steel foil, we now proceed to analyze the forced bending of a compliant substrate after a device film has been deposited on it. We shall see that this bending may induce much less strain in the film than on a stiff substrate. This consequence becomes qualitatively obvious from a re-inspection of Fig. 5.17. When the sheet is bent, the outside surface is in tension, and the inside surface is in compression. If the film/substrate foil has uniform elastic constants, the neutral plane coincides with the mid-plane of the sheet, as in Fig. 5.17. But if the structure consists of a stiff layer on top on a compliant substrate, the neutral plane is shifted from mid-plane toward the stiff layer. Consequently, for a given curvature R , the strain in the outside (film) surface is reduced, and is given by,

$$\varepsilon_{\text{top}} = \left(\frac{d_f + d_s}{2R} \right) \frac{(1 + 2\eta + \gamma\eta^2)}{(1 + \eta)(1 + \gamma\eta)} . \quad (5.9)$$

Here R is the radius of curvature, $\eta = d_f/d_s$ and $\gamma = Y_f/Y_s$. This situation is illustrated by Fig. 5.19, where the normalized strain in the film is plotted vs. film/substrate thickness ratio for the two ratios of Young's moduli of 1 (stiff substrate) and 100 (compliant substrate). Note that a compliant substrate can reduce the normalized strain by as much as a factor of five. In this way thin-film circuits on compliant substrates become particularly insensitive to bending. When favorable combinations of Y and d are used, the structure

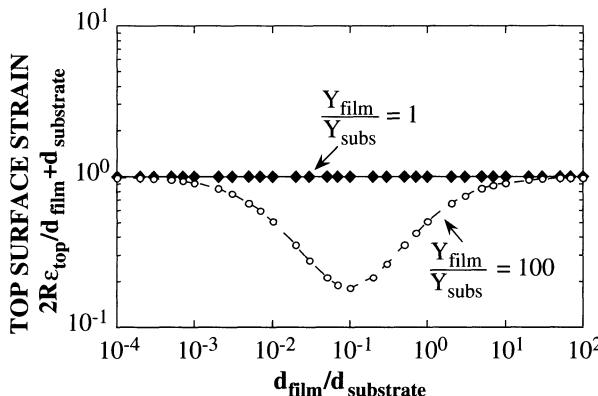


Fig. 5.19. In-plane strain ϵ_{top} induced in the top surface by bending an initially flat and strain-free film/substrate couple. The strain ϵ_{top} is reciprocal to the radius of curvature R . For a given value of R , choosing a compliant substrate and the appropriate film/substrate thickness ratio can reduce the strain by a factor of up to five

may allow extremely small radii of curvature. It even might be folded like a map.

It is noted above that TFTs made on steel foil peel off at a radius of curvature that is smaller for convex than for concave bending. This behavior is a consequence of the way the thermal strain ϵ_M and the strain induced by bending ϵ_{top} add [5.18]. For our sample this strain ϵ_M is $\approx 4.5 \times 10^{-3}$. (We assume that the sample is free of any intrinsic strain that often is established during growth.) Bending to a 1.5 mm radius adds a strain of $\pm 8.5 \times 10^{-3}$. The sum of bending and thermal strain in the convex (facing out) surface is $+4.5 \times 10^{-3}$, and on the concave (facing in) surface -13×10^{-3} . (We define tensile strain as positive, and compressive strain as negative). It is easy to see why the film peels off the concave surface at a larger radius than from the convex surface. Note that the peeling occurs at the large strain of close to 0.5%.

5.6 Plastic Substrate Foil: TFT on Polyimide

Thin film transistors made on thin foils of plastic serve as a good illustration of the compliant-substrate situation discussed in the preceding section. The glass transition temperatures of most organic polymers lie below 200°C, much lower than those of inorganic glass substrates (Tables 5.2 and 5.3). Therefore, the standard a-Si:H TFT processes cannot be used on plastics because they require temperatures of up to 350°C. We have fabricated a-Si:H TFTs on 51 µm (2 mil) thick polyimide foil after re-optimizing the TFT process for a maximum temperature of 150°C [5.28]. The commercially available polyimide grade Kapton® E was selected because it has a low coefficient of thermal

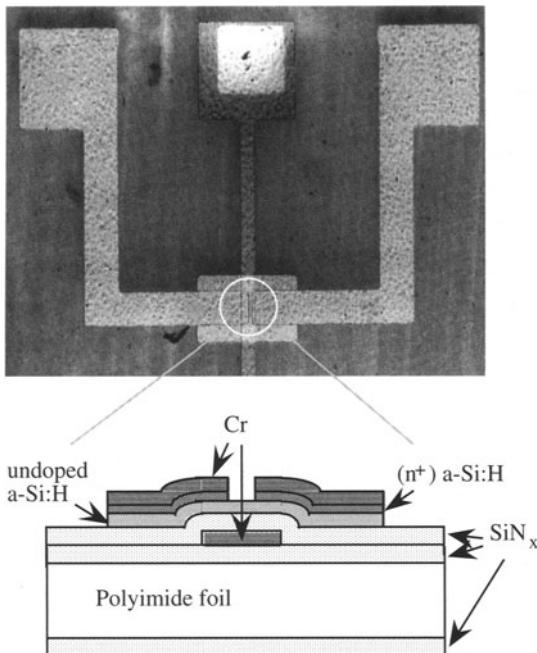


Fig. 5.20. Top: Top view of a TFT on a polyimide substrate. The channel is $15\text{ }\mu\text{m}$ long. Bottom: Cross sectional view (from [5.28])

expansion of $12 \times 10^{-6}/^\circ\text{C}$, and its coefficient of humidity expansion is $9 \times 10^{-6}/\%$ Relative Humidity.

The transfer of such low-temperature technology from glass to plastic substrates brings new processing and mechanical issues to a-Si:H TFT fabrication. A widely usable low-temperature TFT needs to be compatible with a number of other polymers whose T_g is lower than that of Kapton. When a silicon thin film is grown on plastic foil, the contribution of the semiconductor to the mechanical behavior of the film/substrate couple becomes comparable to that of the plastic foil. This is very noticeable during processing, when the structure is observed to bend inward or outward with varying radii of curvature after each process step. We are entering a regime in which the film controls the mechanical properties of the structure as much as the substrate.

Before proceeding with a-Si:H TFT fabrication, the deposition of all layers was re-optimized for 150°C to obtain TFT electrical properties comparable to those obtained at higher temperature. The gate SiN_x was deposited from a mixture of Si:H_4 , NH_3 and H_2 , the undoped a-Si:H from a mixture of Si:H_4 and H_2 , and the (n^+) a-Si:H from a mixture of Si:H_4 , PH_3 and H_2 . The TFTs have a bottom gate, back-channel etch structure. We began by passivating the polyimide substrate on both sides with a $0.5\text{ }\mu\text{m}$ thick layer of SiN_x . These layers serve as a barrier against the solvents, bases and acids used during

photolithography. An ≈ 100 nm thick Cr layer was thermally evaporated and wet etched to create the gate electrode. Then we deposited a sequence of: ≈ 400 nm of SiN_x , ≈ 200 nm of undoped a-Si:H, and ≈ 50 nm of (n^+) a-Si:H. An ≈ 100 nm thick Cr layer was thermally evaporated. The Cr source-drain pattern was wet etched and the (n^+) a-Si:H was dry etched in CF_4 gas. Then the undoped a-Si:H was dry etched to define the transistor island. In the last photolithographic step, dry etched windows into the SiN_x were opened to access the gate contact pad. Arrays of six TFTs were fabricated on 1.5×1.5 in.² substrates. Four substrates were processed simultaneously. Figure 5.20 shows the cross section of one TFT [5.28].

The dependence of the source-drain current I_{ds} on the gate voltage V_{gs} for $V_{ds} = 0.1$ V and 10 V is shown in Fig. 5.21 [5.28]. The off-current is $\approx 1 \times 10^{-12}$ A ($< 1 \times 10^{-14}$ A/ μm gate width at $V_{DS} = 10$ V) and the on-off current ratio is 10^7 . At $V_{ds} = 0.1$ V we obtain $V_T \approx 3.5$ V. The dielectric constant of our 150°C nitride measured at 1 MHz is 7.46. The electron mobility in the linear regime is $\approx 0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These characteristics are comparable to those of a-Si:H TFTs fabricated on glass substrates at temperatures between 250 and 350°C. They suggest that a low-temperature a-Si:H technology can be developed that is fit for a large variety of plastic substrates.

5.7 3-D Integration on a Foil Substrate: OLED/TFT Pixel Elements on Steel

An active-matrix thin-film emissive display requires the integration of a light-emitting device with a switch. Organic light-emitting diodes can be integrated with amorphous silicon thin film transistors on steel foil, in a circuit that demonstrates the monolithic 3-D integration of very different thin-film devices on a foil substrate [5.24, 25, 29, 30]. While the devices were fabricated by conventional, non-printing techniques, the nature of the thin-film structure and the foil substrate suggests that large-area circuits based on such devices can be made by printing. A schematic cross-section of the integrated TFT/OLED structure on the steel foil is shown in Fig. 5.22a, and its equivalent circuit is shown in Fig. 5.22b [5.29]. The as-rolled stainless steel foil is planarized with 0.5 μm thick spin-on glass to remove the short-wavelength roughness of 0.3 μm rms. This planarization functions as primary insulation. Further insulation is provided by a 0.5 μm thick plasma-enhanced CVD SiN_x layer. The TFTs are made in the inverted-staggered, back-channel etch configuration with 120 nm thick Cr gates, 400 nm PECVD gate SiN_x dielectric, 150 nm a-Si:H channel layer, and 50 nm (n^+) a-Si contacts, followed by 120 nm Cr source/drain contacts. The channel length and width are 42 μm and 776 μm , respectively. The TFTs and contact pads are made large, to ease probing and diagnosis on bent or rolled substrates.

Following the fabrication of TFTs, OLEDs were made on the surface of the 2×2 mm² Cr source/drain contact pads. Conventional OLEDs are built

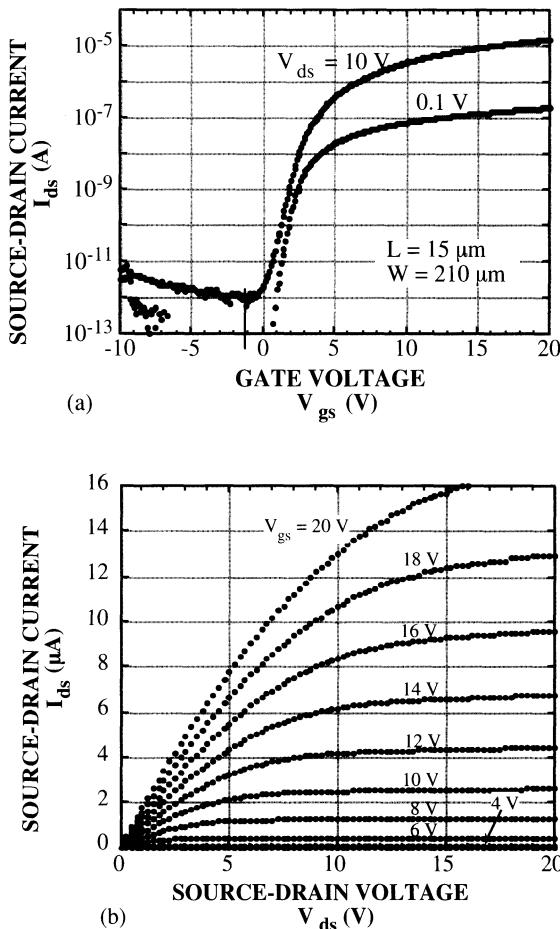


Fig. 5.21. (a) Transfer characteristics and (b) current-voltage characteristics of a TFT made at 150°C on a polyimide substrate (from [5.28])

on transparent substrates coated with a transparent hole-injecting anode contact such as indium tin oxide (ITO), so that light can be emitted through the substrate, because the top contact is an opaque electron-injecting metal cathode. Because of the opacity of the steel substrate, we developed the top-emitting structure in which the high work function metal Pt functions as the reflective bottom anode and a semi-transparent cathode is applied on top. OLEDs were fabricated by sequential electron-beam deposition and patterning of 40 nm Pt anode contacts, spin-coating of a continuous layer of 170 nm active luminescent molecularly doped polymer (MDP), followed by the electron beam evaporation of a 14 nm semi-transparent Ag top cathode. The overlap of the anode and cathode contact areas determines the active OLED device area, a $250 \mu\text{m}$ diameter dot, without the need to separately

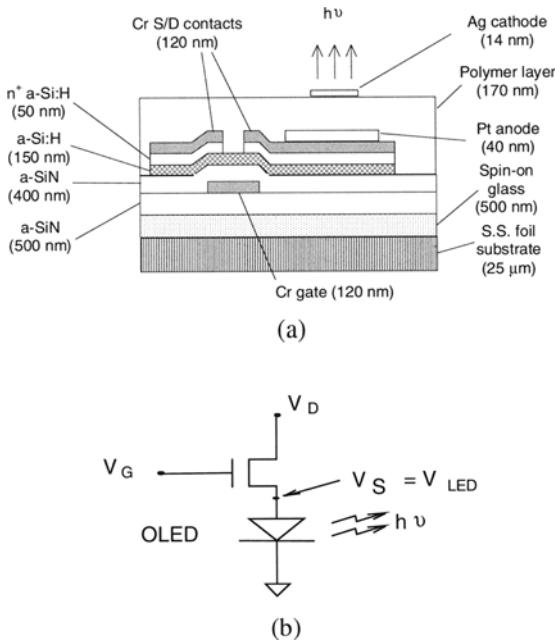


Fig. 5.22. (a) Cross section of the integrated OLED/TFT structure made on steel foil. (b) Equivalent circuit of the OLED/TFT (from [5.29])

isolate the organic layers. All OLED fabrication steps were performed at room temperature and are compatible with finished TFTs.

The active organic material used is a single-layer thin film. The hole-transport matrix polymer poly(N-vinylcarbazole) (PVK) contains dispersed electron-transport molecules of 2(-4-biphenyl)-5-(4-tert-butyl-phenyl)-1,3,4-oxadiazole and a small amount of the green fluorescent dye, coumarin 6 (C6), which provides efficient emission centers. The OLED luminescence depends linearly on device current as already shown for the spin-coated OLED of Fig. 5.12 [5.19]. The factor limiting the luminance in this device is not the polymer material itself, but rather the poor transparency of the top contact and its work function mismatch with the organic material. Here, we obtain 50 cd/m² at 40 mA/cm² (20 μA/device) with $V_G = V_D = 40$ V. Figure 5.23a shows the I - V characteristics of the integrated TFT/OLED device on a linear current scale [5.25]. Figures 5.23b,c illustrate how the voltage is applied to obtain the OLED and TFT/OLED curves, respectively. The shift in turn-on voltage results from the additional 3.5 V required to turn on the TFT. This functional OLED/TFT pixel circuit illustrates the ease of integrating very different materials into a 3-D thin-film configuration that could be fabricated by printing.

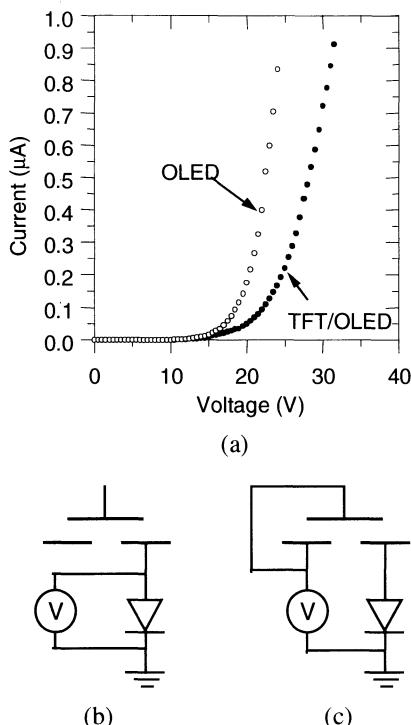


Fig. 5.23. (a) Current-voltage characteristics of the OLED and of the OLED/TFT; (b) and (c) show the circuits used for these measurements (from [5.25])

5.8 Outlook

We saw in this chapter that laser and jet printing techniques can be used to pattern thin-film transistors and organic light-emitting diodes. The resolution and registration achievable by conventional printing techniques will provide a packing density of more than 10 000 transistors per square centimeter. These transistors can be made on glass, steel, and plastic foils. The OLED/TFT structure suggests that they can be integrated into three-dimensional thin-film circuits. Direct printing will enable the manufacture of such circuits with very large-area. We also saw that these circuits are very rugged by virtue of the mechanics of thin structures.

The direct printing of macroelectronic circuits is receiving growing and worldwide attention. This newly found focus will facilitate the marriage of electronics and printing that is needed to develop the manufacturing technology for macroelectronics. An important ingredient is the development of printable materials for active circuits, which will draw on chemistry, materials science, and surface physics.

Early applications can be expected to make use of existing printing technology to make large-area circuits for displays, sensor arrays, and large-area

micro-electromechanical circuits. The pattern of increased resolution and enhanced performance that is well known from the development of silicon integrated circuits will be repeated in large-area electronics as more and more macroelectronic products are introduced.

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References

- 5.1 E. Kaneko, Displays 14 (1993) 125–130. E. Kaneko, in Thin Film Transistor Technologies III, Electrochemical Society PV96-23, p. 8 (1997).
- 5.2 D.M. de Leeuw, P.W.M. Blom, C.M. Hart, C.M.J. Mutsaers, C.J. Drury, M. Matters and H. Termeer, Tech. Digest IEDM 1997, p 331. IEEE, New York 1997. C.J. Drury, C.M.J. Mutsaers, C.M. Hart, M. Matters, D.M. de Leeuw, Appl. Phys. Lett. **73**, 108 (1998).
- 5.3 J. Yang, A. Banerjee, T. Glatfelter, S. Sugiyama, and S. Guha, Conf. Record 26th IEEE PVSC, IEEE, New York (1997), p 563.
- 5.4 D.E. Carlson, R.R. Arya, M. Bennett, L.-F. Chen, K. Jansen, Y.-M. Li, J. Newton, K. Rajan, R. Romero, D. Talenti, E. Tweseme, F. Willing and L. Yang, Conf. Record 25th IEEE PVSC, IEEE, New York (1996), p 1023.
- 5.5 H. Gleskova, S. Wagner, and D.S. Shen, J. Non-Cryst. Solids **227–230**, 1217 (1998).
- 5.6 H. Gleskova, S. Wagner, and D.S. Shen, IEEE Electron Devices Letters **16**, 418 (1995).
- 5.7 Pocket Pal, 16th ed., International Paper Company, Memphis, Tennessee (1995).
- 5.8 The values for λ and δ are a consensus on the capability of high-quality printing equipment. Agreement on the feasibility of $\lambda = 10 \mu\text{m}$ is better than on $\delta = \pm 5 \mu\text{m}$. The value for δ is considered less certain, because the two alternatives for obtaining registration, mechanical or by optical alignment, are so different. The consensus values were reached in discussions with experts in three laboratories of the printing industry: Mr. Shinichi Hikosaka and colleagues of the Central Research Institute of Dainippon Printing Co., Ltd., Dr. Kaneki Yoshida and colleagues of the Technical Research Institute of Toppan Printing Co., Ltd., and of Mr. Russell Fling and colleagues of the Technical Center of R.R. Donnelley Printing Co.
- 5.9 We thank the researchers of Dai-Nippon and Toppan for discussions of alignment techniques.
- 5.10 A point made by Mr. Russell Fling of R.R. Donnelley.
- 5.11 S.Y. Chou, P.R. Krauss, and P.J. Renstrom, Science **272**, 85 (1996).
- 5.12 H. Gleskova, R. Könenkamp, S. Wagner, and D.S. Shen, IEEE Electron Devices Lett. **17**, 264 (1996).
- 5.13 H. Gleskova, S. Wagner, and D.S. Shen, MRS Symp. Proc. **467**, 869 (1997).
- 5.14 B. Green, “A New Way to Make PC Boards,” Electronics Now (November 1997), p. 52.

- 5.15 For introductions to xerography and laser printing, see L.B. Schein, "Electrophotography and Development Physics", Springer, New York (1992), and R.M. Schaffert, "Electrophotography," Halstead Press, New York (1975).
- 5.16 H. Gleskova and S. Wagner, unpublished results.
- 5.17 H. Gleskova, S. Wagner, and D.S. Shen, Proc. AMLCDs '95, Lehigh University, 25–26 (Sep. 1995), p 16.
- 5.18 E.Y. Ma and S. Wagner, MRS Symp. Proc. **508**, 18 (1998).
- 5.19 T. R. Hebner, C. C. Wu, D. Marcy, M. H. Lu, and J. C. Sturm, Applied Physics Letters **72**, 519 (1998).
- 5.20 T.R. Hebner and J.C. Sturm, Applied Physics Letters **73**, 1775 (1998).
- 5.21 D.M. Moffat, MRS Symp. Proc. **377**, 871 (1995).
- 5.22 S.D. Theiss and S. Wagner, MRS Symp. Proc. **424**, 65 (1996).
- 5.23 E.Y. Ma, Ph.D. thesis, Princeton University (1998).
- 5.24 S.D. Theiss, C.C. Wu, M. Lu, J.C. Sturm and S. Wagner, MRS Symp. Proc. **471**, 26 (1997).
- 5.25 E.Y. Ma, S.D. Theiss, M.H. Lu, C.C. Wu, J.C. Sturm and S. Wagner, IEEE (1997) Internat. Electron Devices Meeting Tech Digest p 535.
- 5.26 T. Dragone, S. Wagner and T.D. Moustakas, Tech Digest PVSEC-1, Kobe, Japan (Nov 13–16, 1984); p 711.
- 5.27 S.P. Timoshenko and J.N. Goodier, Theory of Elasticity, McGraw-Hill, New York (1970).
- 5.28 H. Gleskova, S. Wagner, and Z. Suo, MRS Symp Proc. **508**, 73 (1998).
- 5.29 C.C. Wu, S.D. Theiss, G. Gu, M.H. Lu, J.C. Sturm, S. Wagner and S.R. Forrest, Society for Information Display, Intern. Symp. Digest, Vol. XXVIII, SID, Santa Ana, CA (1997), 67.
- 5.30 C.C. Wu, S.D. Theiss, G. Gu, M.H. Lu, J.C. Sturm, S. Wagner and S.R. Forrest, IEEE Electron Devices Lett. **18**, 609 (1997).
- 5.31 Z. Suo, E.Y. Ma, H. Gleskova and S. Wagner, Appl. Phys. Lett. **74**, 1177 (1999).