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Compliant substrates for thin-film transistor backplanes

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ABSTRACT

The emergence of wearable electronics is leading away from glass substrates for the display backplane, to plastic and metal. At the same time the substrate thickness is reduced to make displays lighter. These two trends cooperate toward the development of compliant substrates, which are designed to offload mechanical stress from the active circuit onto the substrate (and encapsulation). Compliant substrates make the circuit particularly rugged against rolling and bending. Design principles for compliant substrates include: (a) Moving the circuit plane as close as possible to the neutral plane of the structure, and (b) Using substrate and encapsulation materials with low stiffness. Design principle (a) is demonstrated on thin-film transistors made on thin steel foil. Such transistors function well after the foils are rolled to small radii of curvature. Principle (b) of compliant substrates is demonstrated with bending experiments of a-Si:H TFTs made on thin substrates of polyimide foil. TFTs on 25-μm thick polyimide foil may be bent to radii of curvature as low as 0.5 mm without failing. The reduction in bending radius, from $R \sim 2$ mm on same-thickness steel foil, agrees with the theoretical prediction that changing from a stiff to a compliant substrate reduces the bending strain in the device plane by a factor of up to 5.

Keywords: thin-film transistor, steel substrate, plastic substrate, mechanical stress, hydrogenated amorphous silicon, plasma enhanced chemical vapor deposition

1. INTRODUCTION

The advent of active-matrix liquid crystal displays has opened the era of large-area electronics. Many anticipated macroelectronic products, including X-ray sensors and digital wallpaper, will be far bigger than today's integrated circuits. Their widespread use will depend on a low cost per circuit area rather than per circuit function. Part of this reduction will come from low material consumption and new manufacturing technologies. For example, when thin-film transistors (TFTs) are made on thin foil substrates,[1,2] they use less material per unit area and also lend themselves to roll-to-roll fabrication. Here we show theoretically and experimentally that such devices can be made particularly rugged. Large-area electronics (LAE) that is rugged, rollable and non-breakable is attracting considerable interest for products that are subjected to frequent stress and mechanical shock. These products include displays for portable electronics, X-ray sensor arrays for ambulant use, and electronic maps. Plastic[2-7] and steel[1,8] are being investigated as alternatives to the conventional, fragile, glass substrates for such rugged electronics. Working with metal or plastic substrates introduces a number of novel aspects to LAE technology, such as the need for electrical insulation of steel and for low-temperature fabrication processes on plastic. The transition to new substrate materials also has important mechanical consequences, which form the primary subject of this paper, which is divided in two parts. In the first part we develop the mechanical theory of film-on-foil structures, and illustrate the theoretical results with mechanical bending experiments of thin-film transistors. Two cases serve as illustrations. One is TFTs on 25-μm thick steel foil, which demonstrates the bendability of TFTs on thin substrates. The other case, of TFTs on 25-μm thick polyimide foils, demonstrates the additional flexibility provided by a compliant substrate. In the second part of this paper we provide an account of the fabrication and overall electrical performance of the amorphous silicon thin-film transistors.

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2. FILM-ON-FOIL MECHANICS

2.1 Transistors on a stiff substrate

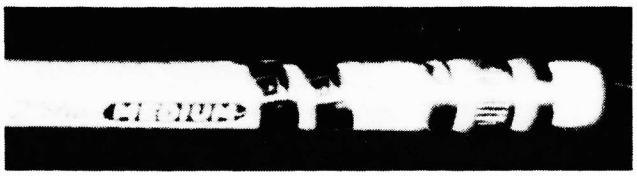

Figure 1. A 25-μm thick steel foil showing two transistor islands wrapped around a pencil.

Figure 1 shows two islands with amorphous silicon transistors on a 25-μm thick steel foil wrapped around a pencil. As Table 1 shows, our devices are affected very little by bending down to 2.5 mm radius of curvature. The OFF current increases slightly due to an increase in gate leakage, but parameters such as threshold voltage, mobility, sub-threshold slope and ON current remain relatively unchanged. At smaller radius of curvature, however, the devices begin to experience mechanical breakdown, with the deposited films peeling off of the underlying substrate. The electrical performance of the TFTs was not much affected by the rolling until the TFTs peeled off.

Radius of Curvature	*Device Orientation*	ΔV_T	ΔI_{OFF}	ΔI_{ON}
2.5 mm	facing out	+0.1 V	none	none
1.5 mm	facing out	-0.1 V	x 200	none
2.5 mm	facing in	-1.0 V	none	none
1.5 mm	facing in	n/a	n/a	n/a

Table 1. Electrical characteristics of the TFTs on 25-μm steel foil after bending.

Data could not be obtained for concave bending (devices facing in) at 1.5 mm radius of curvature because all devices peeled off the substrate. In all cases, separation occurs between the spin-on glass and barrier SiN layers. Under convex bending (devices facing out), 4 of 8 devices failed due to peeling. The other four devices continued to operate, though with higher leakage currents. Qualitatively, the damage from peeling was far more severe under concave bending than under convex. In other words, when the sheet was rolled around drill bits of successively smaller radii of curvature, the transistors functioned well until some critical radii were reached: 2.5 mm if the transistors faced in, or 1.5 mm if the transistors faced out. To appreciate these results, let us analyze the strain in a blanket film deposited on a foil substrate. Both fabrication process and externally applied bending moment cause strain in the film. We first consider the external bending moment. Figure 2 illustrates a sheet bent to a cylinder of radius R. The film and the substrate have thicknesses d_f and d_s and Young's moduli Y_f and Y_s. When the sheet is bent, the top surface is in tension, and the bottom surface is in compression. One surface inside the sheet, known as the neutral surface, has no strain. The strain in the top surface ε_{top}, in the bending direction shown in Fig. 2, equals the distance from the neutral surface divided by R. Typical silicon TFT materials and steel have about the same Young's modulus. Consequently, the neutral surface is the mid-surface of the sheet, and the strain in the top surface is given by

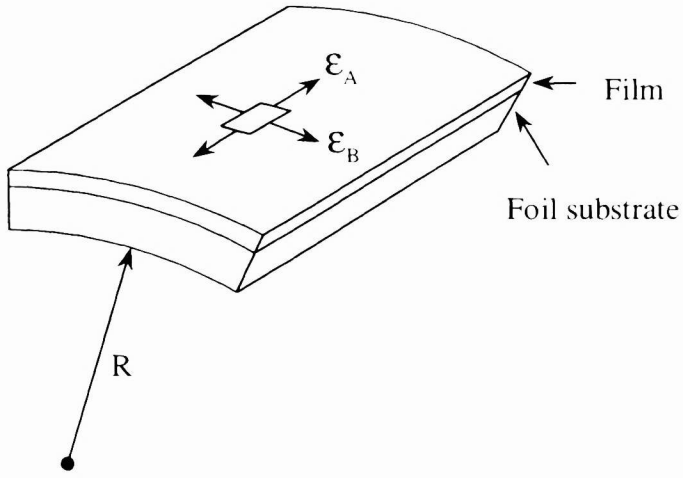

Figure 2. A film-on-foil structure bent to a cylindrical roll.

$$\varepsilon_{top} = (d_f + d_s) / 2R \,. \qquad (1)$$

The minimum allowable radius of curvature scales linearly with the total thickness, assuming that the transistors fail upon reaching a critical value of strain. The transistors peel off the steel substrate at a smaller radius of curvature when the transistors face out than when the transistors face in. This behavior

arises from the way the misfit strain e_M and the strain ε_{top} induced by forced bending add. For our sample, differential thermal expansion put the transistor material in compression, $e_M \cong 4.5\times10^{-3}$. (We neglect any intrinsic strain that may build up during film growth.) Bending to a 1.5 mm radius adds a strain $\varepsilon_{top} \cong 8.5\times10^{-3}$, tensile when the transistors face out, and compressive when the transistors face in. Consequently, the net strain is 4×10^{-3} *tensile* when the transistors face out, and 13×10^{-3} *compressive* when the transistors face in. For a given radius of curvature, then, the transistor films are under much higher stress when they face in. Therefore, the structure peels off at larger radii under concave bending.

2.2. Transistors on a compliant substrate

The bending of TFTs on the 25-μm steel foil serves as a good illustration of a thin-film device on a *stiff* substrate. In a thin-film circuit / substrate couple, the substrate becomes *compliant* when its stiffness is comparable to, or less than, the stiffness of the circuit films. This condition is given by $Y_s d_s \leq Y_f d_f$, where Y is Young's modulus of in-plane elasticity, d is thickness, and the subscripts stand for substrate and film. Because Y_f of the a-Si:H TFT materials is ~ 200 GPa, Y_s of the polyimide Kapton E is ~ 5 GPa, and d_f typically is ~ 1 μm, the compliant condition for TFTs on Kapton E is established for $d_s \leq 40$ μm.

Let us look more closely at the TFT film on a compliant substrate[9]. Because the film has a higher elastic modulus than the substrate ($Y_f > Y_s$), the neutral surface shifts from the mid-surface and toward the film. Consequently, the strain on the top surface is reduced, as given by

$$\varepsilon_{top} = [(d_f + d_s) / 2R][(1 + 2\eta + \chi\eta^2)/(1 + \eta)(1 + \chi\eta)] \quad (2)$$

where $\eta = d_f / d_s$ and $\chi = Y_f / Y_s$. Figure 3 plots the normalized strain in the film *vs.* $\eta = d_f / d_s$. Two kinds of substrates are compared: steel ($Y_f / Y_s \cong 1$) and plastic ($Y_f / Y_s \cong 100$). For given R and $\eta = d_f / d_s$, the compliant substrate can reduce the strain by as much as a factor of five.

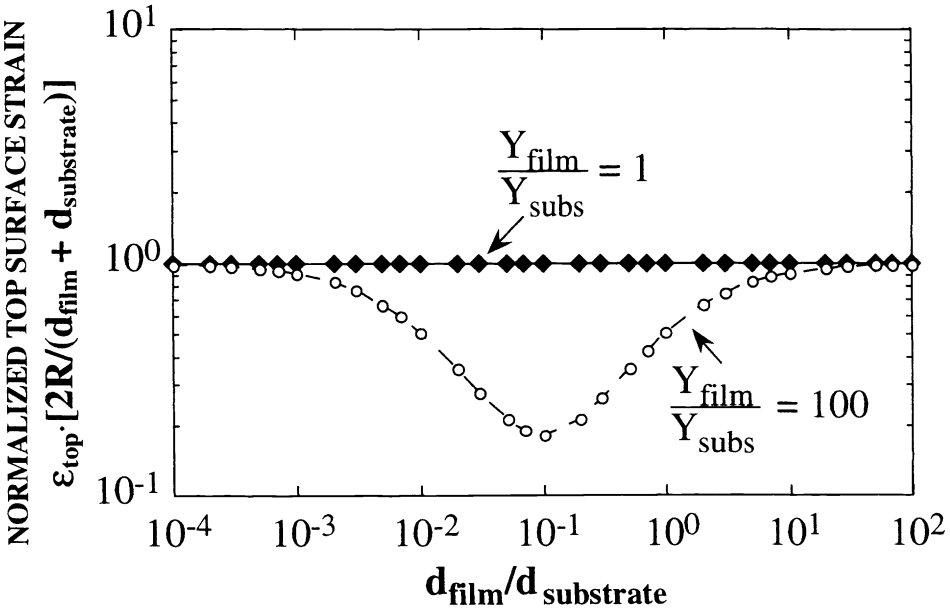

Figure 3. Normalized strain in the device film as a function of film/substrate thickness ratio. The ratio $Y_{film}/Y_{substrate} \cong 1$ is for steel, the ratio of 100 for plastic substrates.

The strain in a circuit is further reduced if it is placed in the neutral surface itself, sandwiched between the substrate and an encapsulation layer of suitable Young's modulus and thickness, Y_e and d_e. When the stiffness of the circuit proper is negligible, the circuit comes to lie in the neutral surface if

$$Y_s d_s^2 = Y_e d_e^2. \quad (3)$$

In this case bending does not add any strain to the circuit. Consequently, the bending curvature is no longer limited by the failure strains of the transistor materials, but by those of the substrate and the encapsulation. When low modulus, small thickness substrate and encapsulation are used, the whole structure can be bent to extremely small radii. It can even be folded like a map.

Next we consider bending caused by the fabrication process. During TFT fabrication, the substrate foil may be held in a frame, at elevated temperatures. Upon cooling and release from the frame, the structure often bends due to film growth strain

and differential thermal expansion. Several recent papers have adapted the classical theory of bimetallic strips to integrated circuits on crystalline substrates.[10-12] Film-on-foil structures exhibit some specific features. The stress field due to misfit strains is biaxial in the surface of the film and the substrate. A small, stiff wafer bends into a spherical cap with an equal and biaxial curvature. However, a film-on-foil structure bends into a cylindrical roll. The cap-to-roll transition as the substrate becomes thinner and larger has been studied extensively.[11] Our substrates are so compliant that they are on the "roll side", far from the transition point. Consequently, they are taken to bend into cylindrical shape, as shown in Fig. 2.

The strain in the axial direction, ε_A, is independent of the position throughout the sheet, a condition known as generalized plane strain. Let z be the through-thickness coordinate, whose origin is arbitrarily placed in the bottom surface. Although the deflection is much larger than the sheet thickness, the strain typically is small. The geometry dictates that the strain in the bending direction, ε_B, be linear in z, namely,

$$\varepsilon_B = \varepsilon_0 + z / R \tag{4}$$

where ε_0 is the strain at $z = 0$.

If the film and the substrate were separate, they would strain by different amounts, but develop no stress. Let e be the strain developed in a stress-free material. For example, thermal expansion produces $e = \alpha \cdot \Delta T$, where α is the thermal expansion coefficient, and ΔT the temperature change. One may also include in e the strain developed during film growth. Because the film and the substrate are bonded and do not slide relative to each other, a stress field arises. The two stress components in the axial and the bending directions, σ_A and σ_B, are both functions of z. Each layer of material is taken to be an isotropic elastic solid with Young's modulus Y and Poisson's ratio ν. The film and the substrate are dissimilar materials, so that e, Y and ν are the known functions of z. Hooke's law relates the stresses to the strains as

$$\sigma_A = [Y/(1-\nu)][(\varepsilon_A + \varepsilon_B)/2 - e] + [Y/(1+\nu)][(\varepsilon_A - \varepsilon_B)/2] \tag{5a}$$

$$\sigma_B = [Y/(1-\nu)][(\varepsilon_A + \varepsilon_B)/2 - e] - [Y/(1+\nu)][(\varepsilon_A - \varepsilon_B)/2] \tag{5b}$$

Assume that no external forces are applied. The force balance requires that

$$\int \sigma_A dz = 0 , \quad \int \sigma_B dz = 0 , \quad \int \sigma_B z dz = 0 . \tag{6}$$

Inserting (4) and (5) into (6) and integrating, we obtain three linear algebraic equations for the three constants ε_A, ε_B and $1/R$. The procedure outlined here is applicable to any number of layers, and arbitrary functions $e(z)$, $Y(z)$ and $\nu(z)$. A general solution can be developed. We consider two important special cases, assuming that Poisson's ratio ν is identical for the film and the substrate.

Suppose that a film-substrate couple is bent by differential thermal expansion. The difference in the thermal strain is $e_M = (\alpha_f - \alpha_s) \cdot \Delta T$. For a stiff wafer, an equal and biaxial stress arises in the plane of the film, which causes bending. The radius of curvature R is given by the Stoney formula:[10-12]

$$R = d_s / 6 \, e_M \, \chi\eta \tag{7}$$

When the substrate is thin and compliant, the film-substrate couple bends into a cylindrical roll instead of a spherical cap. Choose the origin of the z-axis such that $\int Y(z) z dz = 0$. Substituting equation (5) into the last of Equations (6), we can solve for the radius of curvature. The result is

$$R = [d_s / 6 \, (1+\nu) e_M \, \chi\eta] \, \{[(1 - \chi\eta^2)^2 + 4\chi\eta(1 + 2\eta)^2]/[1 + \eta]\} . \tag{8}$$

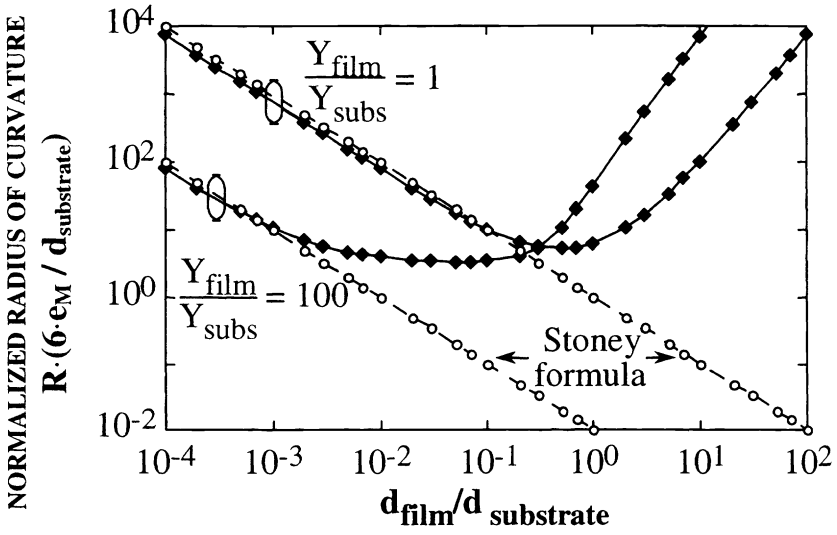

Figure 4. Normalized radius of curvature as a function of film/substrate thickness ratio. The full lines rare the solutions for a cylindrical roll, assuming $\nu = 0.3$ for all materials. The dashed lines represent the Stoney formula for the spherical cap that is formed on a thick, stiff wafer.

The term in the first bracket is the Stoney formula divided by $(1+\nu)$, a factor arising from the generalized plane strain condition. The term in the second bracket accounts for the effect of the compliant substrate. The radius of curvature, calculated from Eqs. (7) and (8), is plotted as a function of $\eta = d_f / d_s$ in Fig. 4. For typical TFT materials on a steel substrate, $\chi = Y_f / Y_s \cong 1$, and the Stoney formula is a good approximation if $d_f / d_s \leq 0.1$ and the $(1+\nu)$ factor is included. For an organic substrate, $Y_f / Y_s \cong 100$, and the Stoney formula is useful only for $d_f / d_s \leq 0.001$. In the specific case of a 50 μm thick polyimide substrate, $d_f / d_s \cong 0.01$, and Eq. (8) must be used.

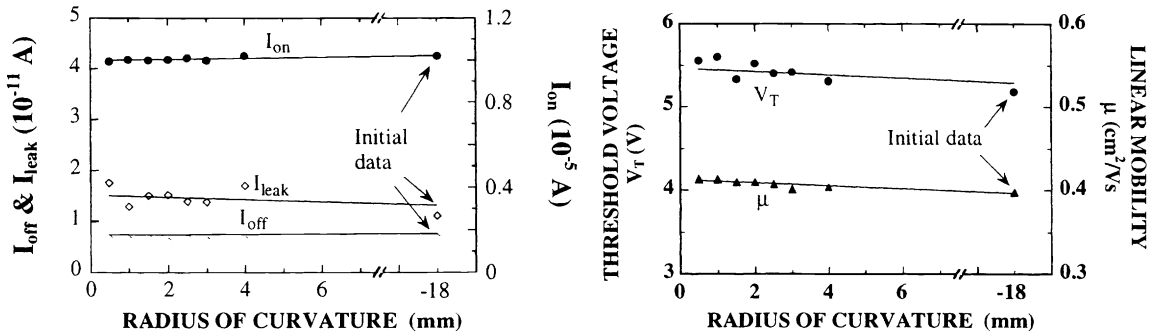

Figure 5. Summary of inward bending tests of TFTs on 25-μm Kapton foil, as a function of bending radius. (a) ON, OFF and gate leakage currents; (b) Threshold voltage and electron mobility in the linear regime. The initial built-in radius of -18 mm with the transistors facing out is defined negative. During the forced bending the transistors were made to face inward.

We performed a series of bending tests of TFTs on 25-μm thick Kapton substrates. The as-fabricated TFT/substrate structure had a built-in radius of curvature R of 18 mm, with the TFTs on the outside. Individual transistors were stressed mechanically by bending either outward (the devices facing out, bending stress subtracting from the built-in stress[13]) or inward (the devices facing in, bending stress adding to the built-in stress). Single TFTs were bent to decreasing R, beginning with R = 4 mm down to R = 0.5 mm. For each bending radius, the TFT was stressed for one minute, then released and remeasured.

Figure 5 summarizes the results of the inward bending test performed on TFTs fabricated on 25-μm thick Kapton foil. Figure 5(a) shows the off-current I_{off}, the on-current I_{on}, and the gate-leakage current I_{leak} as a function of the radius of curvature. The definition of these currents is as follows: the off-current is the smallest source-drain current at V_{ds} = 10V, the on-current is the source-drain current for V_{ds} = 10 V and V_{gs} = 20 V, and the leakage current is the source-gate current for V_{ds} = 10 V and V_{gs} = 20 V. No substantial change in these parameters for bending down to R = 0.5 mm was observed. Figure 5(b) shows the threshold voltage V_T and the linear electron mobility μ_n, calculated using Eq. (1), as a function of the bending radius. Both the threshold voltage and the mobility increase slightly with the decreasing radius of curvature, but again the changes are not

substantial. No catastrophic failure occurs. Similar results were obtained for the TFTs bent inward. The radius of 0.5 mm was the smallest controlled value we could set.

The experiments described in Section 2.1 on the bending TFTs on 25-μm thick steel foil (a stiff substrate) have shown that a-Si:H TFTs can be strained by at least 0.5 % before failing mechanically at a radius of curvature R of ~ 2 mm. Our present observation that TFTs made on the same thickness of Kapton foil function down to R = 0.5 mm provides direct evidence for the strain-reducing effect of a compliant substrate. The results agree with the theoretical prediction of a reduction of the strain in the plane of the circuit by a factor of up to 5 (Equation (2) and Figure 3). Thus both experiment and theory suggest that nearly-foldable thin-film circuits are a realistic prospect.

3. TRANSISTOR FABRICATION AND CHARACTERISTICS

3.1. Steel foil substrates

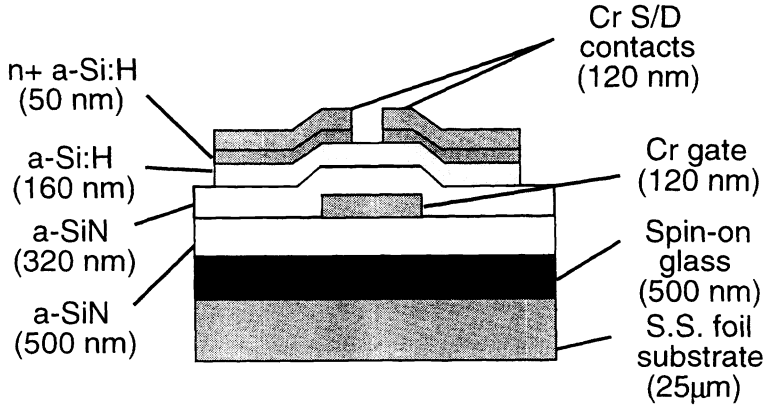

Figure 6. Schematic cross section of a TFT on steel foil.

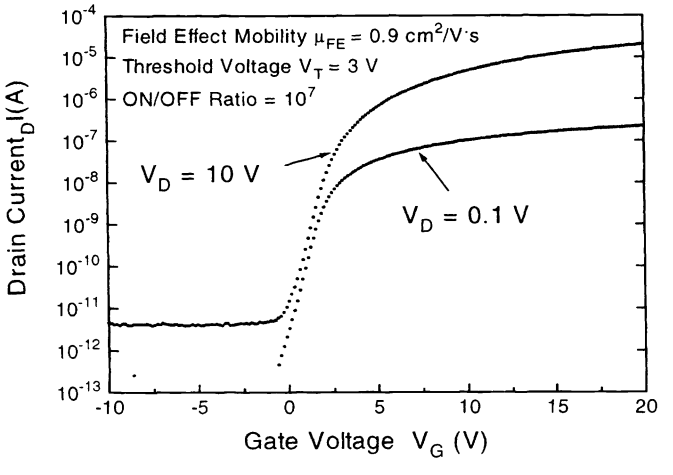

Figure 7. Trnsfer characteristics of a TFT made on 25-μm thick steel foil. The channel of length 42 μm and width 772 μm was made large to facilitate inspection while bent.

a-Si:H TFTs with the inverted-staggered back-channel etch structure shown in Figure 6 were fabricated on top of 25-μm AISI Grade 304 (Fe/Ni/Cr) foil substrates. The foils were cleaned first with soap solution and then de-ionized water in an ultrasonic bath. The foils were planarized with spin-on glass to reduce surface roughness[14]. Then the substrate was coated with 500 nm of a SiN_x passivation layer deposited by plasma-enhanced chemical vapor deposition (PE-CVD) under the same conditions as the TFT gate dielectric. a-Si:H TFTs in the inverted-staggered, back-channel etch configuration were made with 120 nm thick gate electrodes of thermally or electron beam evaporated Cr, a 350-nm SiN_x / 160-nm a-Si:H / 50-nm n^+ a-Si:H TFT stack deposited in a three-chamber PE-CVD system[15], and 120 nm evaporated Cr source/drain electrodes. The highest process temperature was 350°C for the SiN_x gate dielectric.

The as-processed TFTs had threshold voltages V_T = 3.5 V, field effect mobilities μ_{FE} = 0.9 cm²/V·s, OFF currents $I_{OFF} \approx 10^{-15}$ A/μm, and ON currents $I_{ON} \approx 10^{-8}$ A/μm, as shown in Figure 7. These strips were later rolled along their length and held for one minute under both convex (TFTs facing outward) and concave (TFTs facing inward) bending, and tested for topological integrity and electrical performance.

3.2. Polyimide substrates

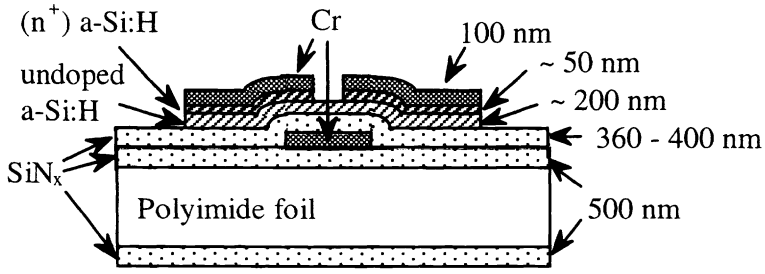

Figure 8. Schematic cross section of a TFT on Kapton. Note the SiN_x passivation on both faces of the substrate.

We fabricated TFTs on 25-μm and 51-μm thick polyimide foils. The TFTs have the bottom gate, back-channel etch structure shown in Fig. 8. First the substrate foil was coated on both sides with a 0.5 μm thick SiN_x layer. This layer serves as a barrier against the solvents, bases and acids used during photolitography. An ~ 100 nm thick Cr layer was evaporated and etched to create the gate electrode. Then the TFT stack of 360 to 400 nm of SiN_x, ~ 200 nm undoped a-Si:H, and ~ 50 nm of (n^+) a-Si:H were grown. An ~ 100 nm thick Cr layer was evaporated and etched to form the source-drain pattern. Finally, the back channel into the (n^+) a-Si:H, the transistor island, and the gate contact pads were defined by plasma etching. Arrays of TFTs with gate length L = 15 μm and width W = 210 μm were fabricated on 1.5 x 1.5 sq. in. substrates. Four substrates were processed simultaneously.

Because the glass transition temperature of plastics (≤ 200°C) is much lower than that of the conventional substrates, Corning 7059 and 1737 glass (> 600°C), the deposition of all a-Si:H TFT layers had to be re-optimized for 150°C to achieve electrical properties comparable to those obtained at the conventional process temperature of ≤ 350°C. All silicon layers were deposited using a three-chamber rf-excited plasma enhanced chemical vapor deposition system. The gate SiN_x was deposited from a mixture of SiH_4, NH_3 and H_2, the undoped a-Si:H from a mixture of SiH_4 and H_2, and the (n^+) a-Si:H from a mixture of SiH_4, PH_3 and H_2.

The TFT transfer characteristics I_{ds} vs. V_{gs}, for V_{ds} = 0.1 V and 10 V, are shown in Figure 9 (a). The source-drain current I_{ds} as a function of the source-drain voltage V_{ds} for nine different gate voltages V_{gs} is shown in Figure 9 (b). The off-current is ~ 1 x 10^{-12} A (< 1 x 10^{-14} A/μm) and the on-off current ratio is > 10^7. At V_{ds} = 0.1 V we obtain V_T ~ 3.5 V and a value of 1.12 x 10^{-8} AV^{-1} for the $(C_{SiN}\mu_n V_{ds} W / L)$ product. The dielectric constant of our 150°C nitride measured at 1 MHz is 7.46. For C_{SiN} = 1.65 x 10^{-8} F cm^{-2} we calculate a linear mobility of ~ 0.5 $cm^2V^{-1}s^{-1}$. These values are comparable to those of a-Si:H TFTs fabricated on glass substrates at temperatures between 250°C and 350°C.

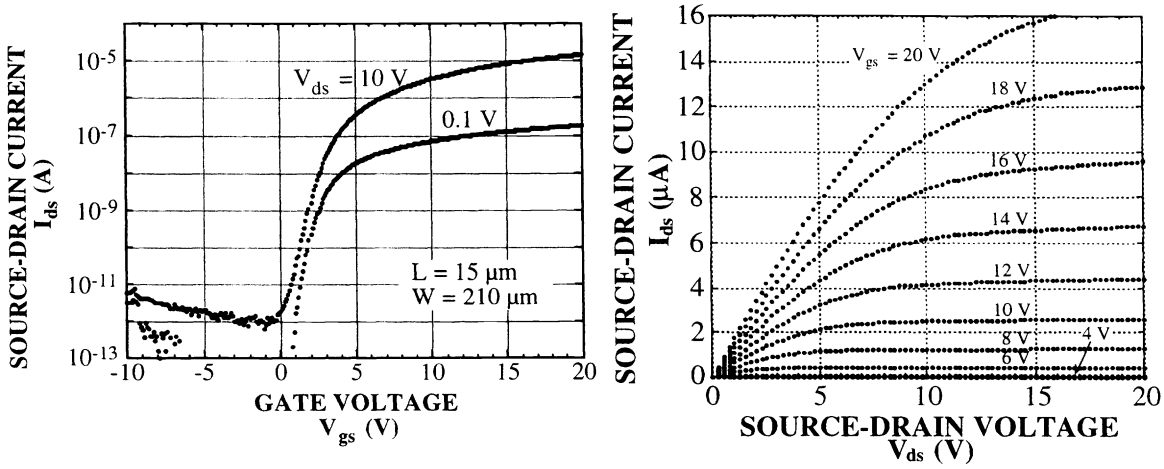

Figure 9. Characteristics of a TFT made on Kapton foil substrate. (a) Transfer characteristics. (b) Output characteristics.

4. SUMMARY

This paper presented the basic mechanics relations for externally forced and thermally induced bending of the film-on-foil devices. When TFTs are placed on the surface of a foil substrate, the smallest bending radius is set by the failure strain of the TFT materials. When the TFTs are placed on a low elastic modulus substrate, the smallest bending radius can be reduced. Furthermore, when the TFTs are placed in the neutral surface by sandwiching between the substrate and the encapsulation, the smallest bending radius is set by the failure strains of the substrate and the encapsulation materials. Consequently, extremely small radii of curvature can be achieved, which may open new applications of large-area electronics.

5. ACKNOWLEDGMENTS

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