

Saturated voids in interconnect lines due to thermal strains and electromigration

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(Received 10 June 2005; accepted 16 August 2005; published online 3 October 2005)

Thermal strains and electromigration can cause voids to grow in conductor lines on semiconductor chips. This long-standing failure mode is exacerbated by the recent introduction of low-permittivity dielectrics. We describe a method to calculate the volume of a saturated void (VSV), attained in a steady state when each point in a conductor line is in a state of hydrostatic pressure, and the gradient of the pressure along the conductor line balances the electron wind. We show that the VSV will either increase or decrease when the coefficient of thermal expansion of the dielectric increases and will increase when the elastic modulus of the dielectric decreases. The VSV will also increase when porous dielectrics and ultrathin liners are used. At operation conditions, both thermal strains and electromigration make significant contributions to the VSV. We discuss these results in the context of interconnect design. © 2005 American Institute of Physics. [DOI: 10.1063/1.2061896]

I. INTRODUCTION

Silicon dioxide has long been used on semiconductor chips as an interlevel dielectric. To enhance the performance of the chips, the industry has been introducing dielectrics with low permittivities.^{1–4} The rapid introduction of materials calls for effective methods to select materials and ensure reliability. This paper focuses on the impact of the dielectrics on a long-standing failure mode: the formation of voids in the conductor lines caused by thermal strains and electromigration.

Figure 1 sketches a representative life of a Cu line, encapsulated by a TaN liner, a SiN cap, and an interlevel dielectric, fabricated on a silicon substrate. These materials have dissimilar coefficients of thermal expansion (CTEs). When the structure is cooled from the processing temperature, a stress field arises in the conductor line, motivating Cu atoms to diffuse and voids to form.^{5–9} When an electric current is applied in the conductor, the electron wind also motivates Cu atoms to diffuse.^{10–12} The combined action of thermal strains and electromigration leads to a complex dynamics of the voids: they nucleate, disappear, drift, change shape, break up, and coalesce.^{13–15}

The complex dynamics of the voids is lively to watch, but difficult to translate into an engineering decision. The conductor line, however, may reach a *steady state*, a well-defined state that can be used in interconnect design. As Cu atoms diffuse in the direction of electron flow, the voids grow upstream and pressure rises downstream. During this process, the encapsulation prevents Cu atoms from diffusing out of the conductor line. Eventually, when the steady state is reached, a single void remains near the upstream via and the pressure gradient in the conductor line balances the electron wind: the net drift of Cu atoms stops and the void saturates.

If the volume of the saturated void (VSV) is too small to block the electric current, the conductor line is immortal.^{16–21} Consequently, the VSV can be used to rank materials and geometries of interconnect structures. A reliable method to determine the VSV will help to ensure the reliability of interconnect structures today, and to design those in the future.

Up to now the VSV due to thermal strains has only been considered in rudimentary terms. When a structure is cooled

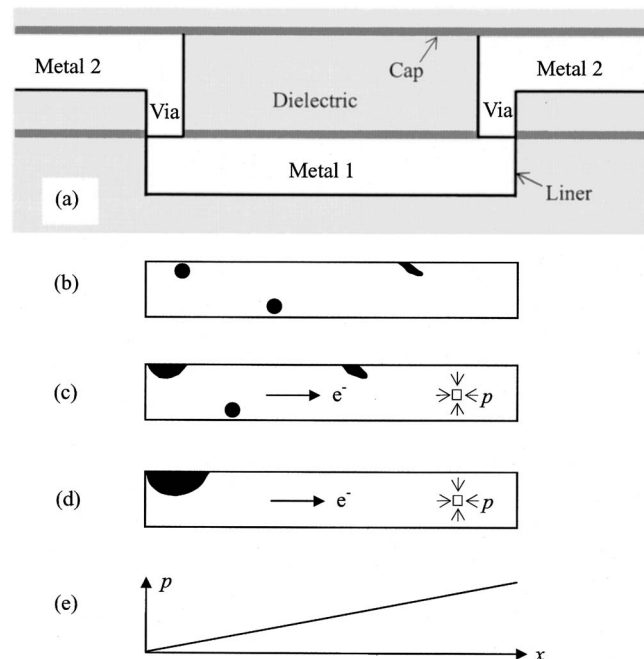


FIG. 1. (a) Schematic of a M1-V1-M2 structure. (b) Stresses arise upon cooling from the processing temperature and are relaxed by the formation of the voids. (c) Subject to an electric current, atoms diffuse in the direction of electron flow. Voids grow upstream and pressure builds up downstream. (d) When the pressure gradient balances the electron wind force, a single void is left near the upstream via and net atomic diffusion stops. (e) In the steady state, the pressure distributes linearly in the conductor line.

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TABLE I. Materials' properties used in calculation.

Materials	Young's modulus E (GPa)	Poisson's ratio ν	Coefficient of thermal expansion α (10^{-6} K $^{-1}$)
Cu	138	0.33	17
TaN	200	0.3	6
SiN	275	0.24	4
Si	165	0.22	3
SiO ₂	71	0.17	3
CDO	10	0.3 ^a	12
SiLK	3	0.3 ^a	50

^aPoisson's ratios of the CDO and the SiLK are unavailable to us and are assigned to be 0.3 in our calculations.

from a reference temperature T_0 to a temperature T , the VSV is proportional to the temperature drop and the conductor volume:

$$V_{sv}^{TH} = 3\alpha(T_0 - T)AL \quad (1)$$

where A is the cross-sectional area and L the length of the conductor line. The coefficient α , which we will call the effective mismatch in the CTEs, depends not only on the CTEs of the materials in the structure but also on their elastic moduli, as well as the aspect ratio of the conductor line and other geometric parameters. Table I gives representative properties of the materials, including three choices of interlevel dielectrics: SiO₂, carbon-doped oxide (CDO), and SiLK. (Although the use of the SiLK is limited,^{22,23} this material is included here to illustrate the effects of a dielectric with a large CTE.) When SiO₂ is used, all the materials surrounding the conductor have similar CTEs as silicon, so that the VSV scales with the difference in the CTE of copper and silicon: $\alpha = \alpha_{Cu} - \alpha_{Si} = 14$ ppm/K.¹⁷ When a dielectric with a large CTE is used, however, will the VSV increase or decrease, and by how much? Such question cannot be answered by the rudimentary consideration. Section II will describe a general method to calculate the VSV due to thermal strains.

By comparison, the VSV due to electromigration has been examined closely. When the conductor line is subject to an electric current, the VSV due to electromigration takes the form¹⁶

$$V_{sv}^{EM} = \frac{Z^* e \rho j L^2 A}{2 \Omega B}, \quad (2)$$

where Z^* is the effective valence, e the elementary charge, ρ the resistivity, j the current density, and Ω the volume per atom in the conductor line. The factor B is an effective modulus of the structure. In an analytical estimate of B , a conductor line is modeled as a cylinder of a circular cross section, embedded in an infinite homogenous matrix.¹¹ This model gives $B^{-1} = B_{Cu}^{-1} + G^{-1}$, where B_{Cu} is the bulk modulus of copper and G is the shear modulus of the matrix.²¹ As shown in Table I, the low-permittivity dielectrics have lower elastic moduli than SiO₂. The more compliant a dielectric is, the more Cu atoms need to move downstream to build up the pressure gradient to balance the electron wind, and the larger the VSV will be. In a realistic interconnect structure, the materials surrounding the conductor have dissimilar elastic

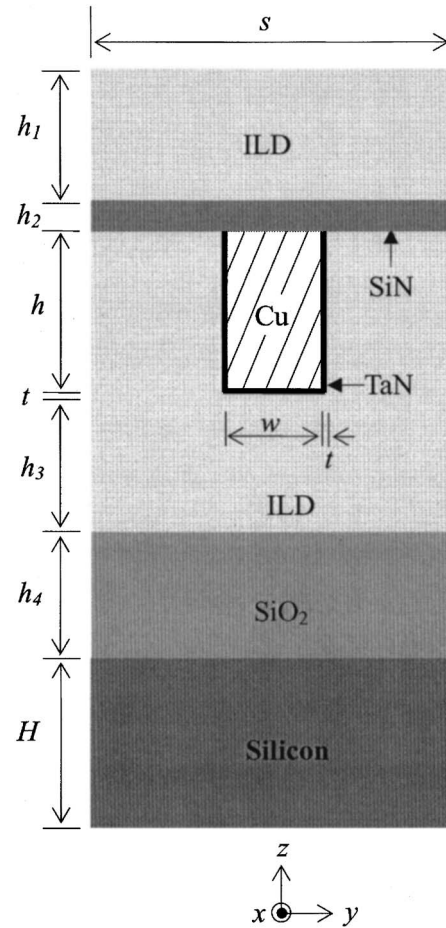


FIG. 2. The cross section of a Cu line, surrounded by a TaN liner, a SiN cap, and an interlevel dielectric (ILD).

moduli. This effect is accounted for in a finite element model, assuming that the interconnect structure is an elastic composite and the conductor line undergoes a transformation strain.¹⁸

It is difficult to justify the assumption that the conductor remains elastic when metal atoms can diffuse over the entire length of the conductor line. Recent experimental data have shown that the diffusivity of Cu atoms on grain boundaries in the conductor is larger than that on the interface between the conductor and the cap.²⁴ The grain boundaries and the interface will allow Cu atoms to redistribute by diffusion, a process that will stop only when deviatoric stresses in the conductor vanish. Consequently, when the void saturates, the stresses at every point in the conductor reach a state of hydrostatic pressure. On the basis of this picture, Sec. III will describe a method to calculate the VSV due to electromigration.

We study the impact of the dielectrics, as well as the effects of the width of the Cu lines, the thickness of the liners, and the spacing between the neighboring Cu lines. Section IV will study the impact on the VSV due to the use of porous dielectrics and ultrathin liners. Section V will place the results into the context of interconnect design.

II. SATURATED VOID DUE TO THERMAL STRAINS

As a computational model, Fig. 2 illustrates a cross sec-

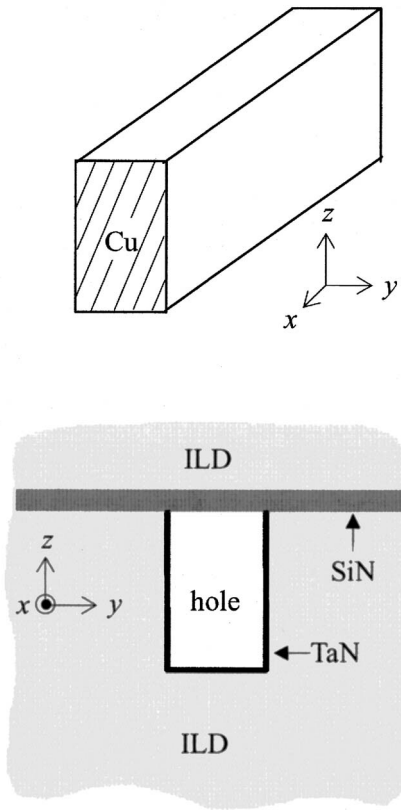


FIG. 3. The copper line is taken out of the surrounding structure, leaving a hole in the latter.

tion of a conductor line of Metal 1 surrounded by other materials. The structure is replicated periodically in the horizontal direction to represent an array of parallel conductor lines. The coordinate x is along the conductor line and z is normal to the substrate surface. In the current technology, the typical thickness of a conductor line is $h=150\text{--}250$ nm. Above the structure in Fig. 2 are several other levels of conductor lines. The actual thickness of the dielectric between levels, h_1 , is about h , but we set $h_1=2h$ to account for the constraint due to materials above the conductor. Similarly, to account for the constraint due to the silicon substrate, we set its thickness to be $50h$. Also fixed are the thicknesses of the SiN cap ($h_2=0.25h$), the dielectric beneath the conductor ($h_3=h$), and the SiO₂ buffer layer ($h_4=h$). We will vary the width of the conductor line w , the pitch between the neighboring conductor lines s , and the thickness of the liner t .

We at first consider the VSV due to thermal strains, in the absence of electric current. In this case, when the voids saturate, the stress in the copper line vanishes. Consequently, we take the Cu line out of its surrounding structure, leaving the latter with a hole (Fig. 3). On cooling the stress-free Cu line changes its volume by

$$\Delta V_{\text{Cu}}^{\text{TH}} = -3\alpha_{\text{Cu}}(T_0 - T)AL. \quad (3)$$

If all the surrounding materials had the same CTE as silicon, the volume of the hole would change by $-3\alpha_{\text{Si}}(T_0 - T)AL$. In reality, however, these materials have different CTEs, giving rise to an extra change in the volume of the hole. We write this extra change in the volume of the hole as $-3\beta(T_0$

$-T)AL$, an equation that defines the quantity β . The net change in the volume of the hole is

$$\Delta V_{\text{hole}}^{\text{TH}} = -3(\alpha_{\text{Si}} + \beta)(T_0 - T)AL. \quad (4)$$

The difference between the two changes, Eqs. (3) and (4), gives the VSV due to thermal strains: $V_{\text{sv}}^{\text{TH}} = \Delta V_{\text{hole}}^{\text{TH}} - \Delta V_{\text{Cu}}^{\text{TH}} = 3\alpha(T_0 - T)AL$, with

$$\alpha = \alpha_{\text{Cu}} - \alpha_{\text{Si}} - \beta = 14 \text{ ppm/K} - \beta. \quad (5)$$

The effective mismatch in the CTEs, α , scales the VSV due to thermal strains. In our sign convention, when the hole *shrinks* by an extra volume, $\beta > 0$, which decreases the VSV.

To calculate β , we focus on the structure surrounding the hole (Fig. 3). Upon cooling this structure develops a stress field in itself, which is governed by a three-dimensional thermoelastic boundary-value problem. This problem is reduced to a two-dimensional one on the basis of the following considerations. The extra change in the volume of the hole is calculated by replacing the CTE α_i of each material in the structure with $\alpha_i - \alpha_{\text{Si}}$. With this replacement, the silicon substrate undergoes no thermal strain and constrains the structure, and the strain in the x direction in the structure vanishes. Also vanishing are the displacements in the y direction at the lines of symmetry. The top surface is traction free. These considerations define a plane strain thermoelastic problem, which we solve using the commercial finite element code ABAQUS. We then calculate the extra change in the volume of the hole using an integral along the boundary of the hole, $L \int u_n ds$, where u_n is the displacement normal to the surface of the hole, positive when pointing outwards of the hole. By definition, β is calculated from

$$-3\beta(T_0 - T)AL = L \int u_n ds. \quad (6)$$

Since u_n is linear in the temperature drop $T_0 - T$, the calculated β is independent of the temperature drop.

Figure 4(a) shows the calculated α as a function of the aspect ratio h/w of the conductor line for the three choices of interlevel dielectrics. When the SiO₂ is used as the interlevel dielectric, the extra change in the volume of the hole is negligible: $\beta \approx 0$ and $\alpha \approx 14$ ppm/K. When the CDO is used, its CTE is large but its elastic modulus is much lower than that of silicon so that α only deviates slightly from 14 ppm/K. When the SiLK is used, however, its CTE is so large that α varies significantly: $\alpha > 14$ ppm/K for narrow lines and $\alpha < 14$ ppm/K for wide lines. For all cases calculated, α is positive; that is, on cooling the copper line shrinks more than the hole, even though the SiLK has a much larger CTE than copper.

These surprising results for the SiLK are understood as follows. Figure 5 shows an undeformed mesh at the reference temperature and a deformed mesh at the lower temperature. In the calculation, the CTE of the silicon substrate is set to be zero. The substrate constrains the structure so that the horizontal displacements vanish at the two lines of symmetry. When the structure is cooled, the dielectric on the side of the hole contracts in both vertical and horizontal directions. The vertical contraction moves the top and the bottom surface of the hole toward each other, decreasing the volume of

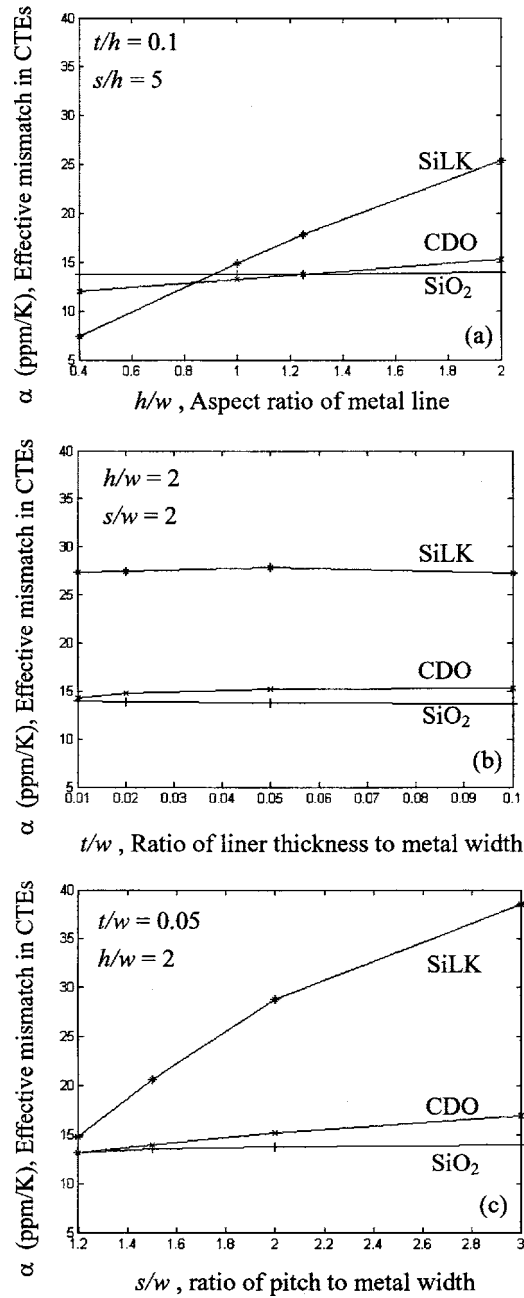


FIG. 4. The effective mismatch in CTE as a function of the aspect ratio of the copper line (a), of the thickness of the liner (b), and of the pitch between the neighboring copper lines (c).

the hole. By contrast, the horizontal contraction draws the side surface of the hole outward, increasing the volume of the hole. For a wide conductor line, the vertical contraction prevails and the saturated void decreases, $\alpha < 14$ ppm/K. For a narrow conductor line, the horizontal contraction prevails and the saturated void increases, $\alpha > 14$ ppm/K.

When the conductor line is very wide, or when the TaN liner and the dielectric between the neighboring conductor lines are thin, the side surface of the hole moves negligibly, and the top and bottom surfaces move to shrink the hole so that $\beta = (\alpha_{ILD} - \alpha_{Si})/3$, where α_{ILD} is the CTE of the inter-level dielectric. This maximum value of β is 3 ppm/K for the CDO and is 15.7 ppm/K for the SiLK. Regardless of the geometry of the structure, the effective mismatch α will be

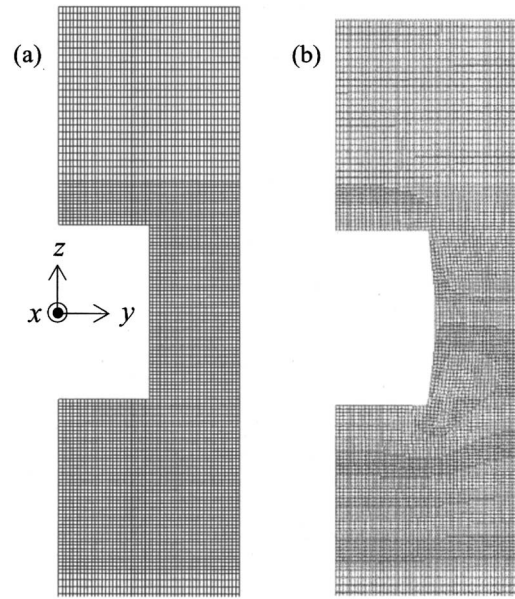


FIG. 5. (a) Undeformed mesh at the reference temperature. (b) Deformed mesh at a lower temperature. The displacement field is amplified by a factor of 10 for visual clarity.

positive if the maximum value $\beta = (\alpha_{ILD} - \alpha_{Si})/3$ is less than $\alpha_{Cu} - \alpha_{Si} = 14$ ppm/K, namely, if $\alpha_{ILD} < 45$ ppm/K.

Figure 4(b) shows that α weakly depends on the liner thickness. Figure 4(c) shows that α increases with the pitch between the neighboring conductor lines, a trend that can also be understood in a similar way as above.

III. SATURATED VOID DUE TO ELECTROMIGRATION

We next calculate the VSV due to electromigration, in the absence of thermal strains. When a Cu line is subject to an electric current, the momentum exchange between conduction electrons and Cu atoms results in an electron wind force, $F = Ze^*epj$, motivating Cu atoms to diffuse in the direction of the electron flow. As a void grows upstream, pressure rises downstream. When the gradient of the pressure balances the electron wind force, net atomic drift stops and the void saturates. In this steady state, the pressure in the conductor line vanishes at the upstream via ($x=0$), where the void forms, and builds up linearly toward the downstream via, $p = Fx/\Omega$.¹⁰

Once again, we take the Cu line out of its surrounding structure, leaving the latter with a hole. In the steady state, the Cu line is subject to the linear distribution of pressure and changes its volume by $\Delta V_{Cu}^{EM} = -A \int_0^L (p/B_{Cu}) dx$, or

$$\Delta V_{Cu}^{EM} = -\frac{FL^2A}{2\Omega B_{Cu}}. \quad (7)$$

Subject to the linear distribution of pressure, the hole enlarges its volume, which we write in a similar form:

$$\Delta V_{hole}^{EM} = \frac{FL^2A}{2\Omega\mu}. \quad (8)$$

This equation defines an effective modulus of the surrounding structure, μ . The difference between the two changes, Eqs. (7) and (8), gives the VSV due to electromigration:

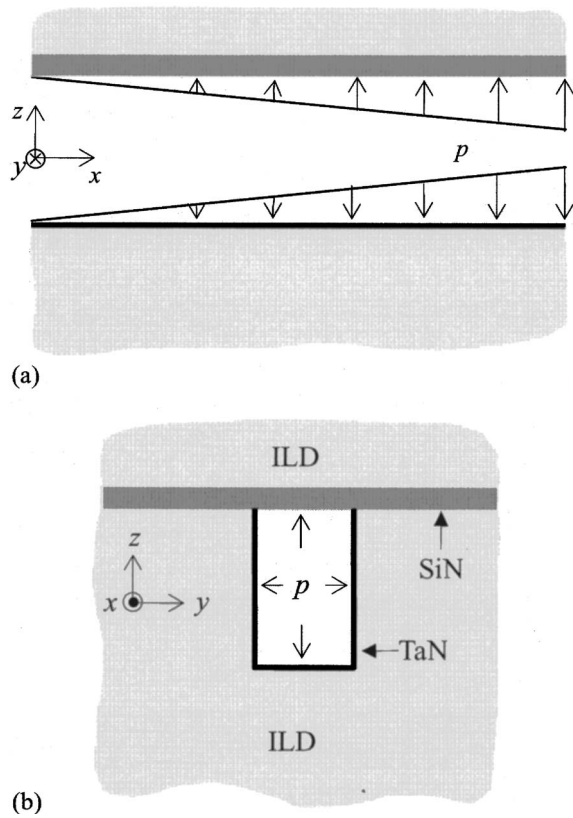


FIG. 6. (a) Pressure distribution along the hole. (b) A cross section of the structure surrounding the hole.

$$V_{sv}^{EM} = \Delta V_{hole} - \Delta V_{Cu} = (Z^* e p j L^2 A) / (2 \Omega B), \text{ with}$$

$$\frac{1}{B} = \frac{1}{B_{Cu}} + \frac{1}{\mu}. \quad (9)$$

The quantity $1/B$ is an effective compliance of the interconnect structure and scales the VSV due to electromigration.

Single crystalline copper has a cubic crystal structure, with elastic moduli $C_{11}=168$ GPa, $C_{12}=121$ GPa, and $C_{44}=75$ GPa. When a polycrystalline copper line is subject to a hydrostatic stress, the strains are identical in all directions and all grains. Consequently, the bulk modulus B_{Cu} of the polycrystal is the same as that of the single crystal, given by $B_{Cu} = (C_{11} + 2C_{12})/3 = 136$ GPa.

To calculate the effective modulus of the surrounding structure μ we prescribe on the surface of the hole the linear pressure distribution $p = Fx/\Omega$. As illustrated in Fig. 6(a), this is a three-dimensional elastic boundary-value problem. When the length of the conductor line is much larger than its height and width, the pressure varies slowly along the length of the hole. Consequently, the three-dimensional structure can be approximated by many slices, each is subject to a uniform pressure on the surface of the hole, deforming under the plane strain conditions [Fig. 6(b)]. We solve the plane strain elastic boundary-value problem using the finite element code ABAQUS. By definition, μ is calculated from

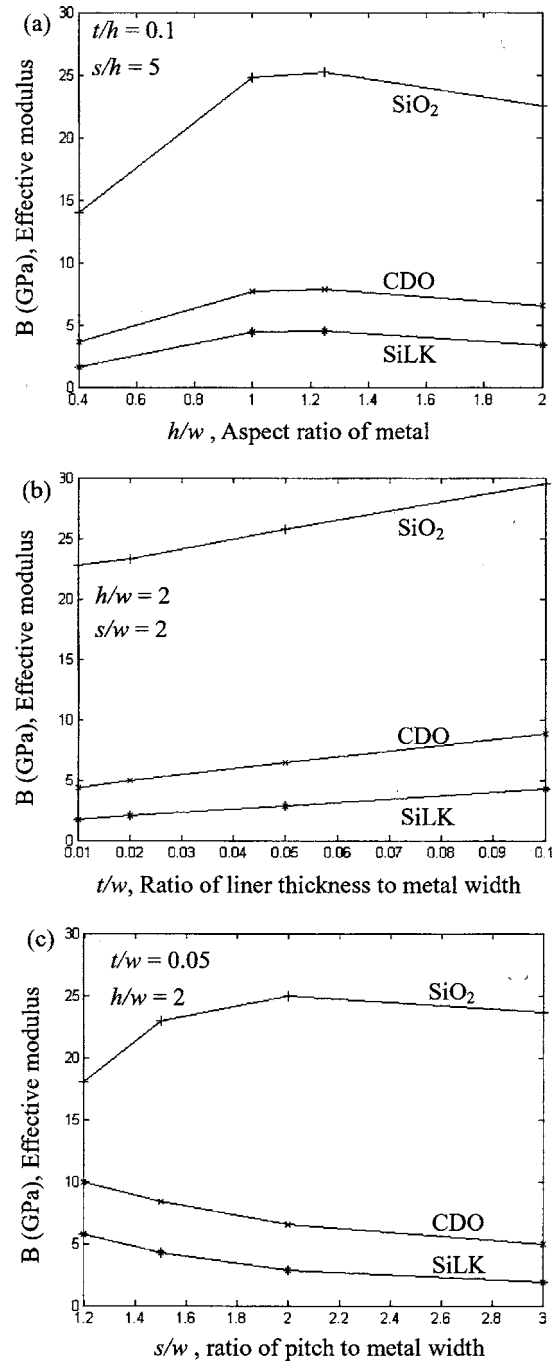


FIG. 7. The effective modulus B of the aspect ratio of the copper line (a), of the thickness of the liner (b), and of the pitch between the neighboring copper lines (c).

$$Ap/\mu = \int u_n ds. \quad (10)$$

Since the displacement u_n in this case is linear in the pressure, the calculated μ is independent of the pressure.

Figure 7(a) shows the calculated B as a function of the aspect ratio of the copper line for the three choices of interlayer dielectrics. The results are similar to those calculated using the models of transformation strains.¹⁸ In all cases, B is much below the bulk modulus of copper (136 GPa), suggesting that $\mu \ll B_{Cu}$ and $B \approx \mu$. It is mainly the surrounding materials, rather than the copper line itself, that accommodate

the Cu atoms relocated to the downstream. Of the three interlevel dielectrics, the SiO₂ is the least compliant, the CDO the intermediately compliant, and the SiLK the most compliant. For each dielectric, B reaches maximum at $h/w \approx 1.25$. This trend is understood as follows. In the analytical model of a conductor line of elliptic cross section embedded in an infinite homogeneous matrix, the effective modulus maximizes when the cross section of the conductor is circular.¹¹ However, in a realistic interconnect structure, a somewhat larger h/w makes the structure stiffest because the silicon substrate is stiffer than the dielectric and constrains the lateral deformation.

Figure 7(b) shows B as a function of the liner thickness. As shown in Table I, the TaN liner is a stiff material, so that B increases with the liner thickness. As remarked above, $\mu \ll B_{\text{Cu}}$ and $B \approx \mu$. An estimate is given by²¹

$$B \approx G_{\text{ILD}} + G_{\text{liner}} \cdot t/w, \quad (11)$$

where G_{ILD} and G_{liner} are the shear moduli of the two materials. This analytical solution is obtained for a conductor line of a circular cross section, which is a good approximation when the cross section is a square. For the results shown in Fig. 7(b), where $h/w=2$, the slopes are somewhat different from G_{liner} .

Figure 7(c) shows B as a function of the pitch between the neighboring conductor lines. For the SiLK and the CDO, the smaller the pitch, the stiffer the structure. For the SiO₂, however, B is not a monotonic function of the pitch. These trends can also be explained by the moves of various surfaces of the hole. Recall that the horizontal displacement vanishes at the vertical line of symmetry. The effect of this constraint is more pronounced when the neighboring lines are closer. On the other hand, the top surface is traction free. When the hole is subject to the pressure, the less the material on the side of the hole, the more readily the top and the bottom surface move apart. These two effects compete to determine B and give rise to the various trends in Fig. 7(c). When the pitch becomes very large, the effective modulus approaches an asymptote.

IV. EFFECTS OF POROUS DIELECTRICS AND ULTRATHIN LINERS

Two trends are anticipated for the interconnect structures of the coming generations. First, to increase the speed of the chips, the industry will introduce lower-permittivity dielectrics, mostly likely porous dielectrics. Second, to further miniaturize, the thickness of the liners, as well as all other features, will reduce. This section examines the effects of porous dielectrics and ultrathin liners on the VSV. We will use CDOs with an increasing amount of porosity as an example. When the porosity of the CDO increases, the elastic modulus decreases, but the CTE is nearly a constant.²⁵ In our calculations, we vary the modulus from 1 to 16 GPa and keep the CTE to be 12 ppm/K.

Figure 8 shows the calculated α and B as functions of the modulus of the dielectric for several values of the liner thickness. The effective mismatch in the CTEs, α , deviates slightly from $\alpha_{\text{Cu}} - \alpha_{\text{Si}} = 14$ ppm/K, as expected from the discussion in Sec. II. Consequently, the use of the porous CDOs

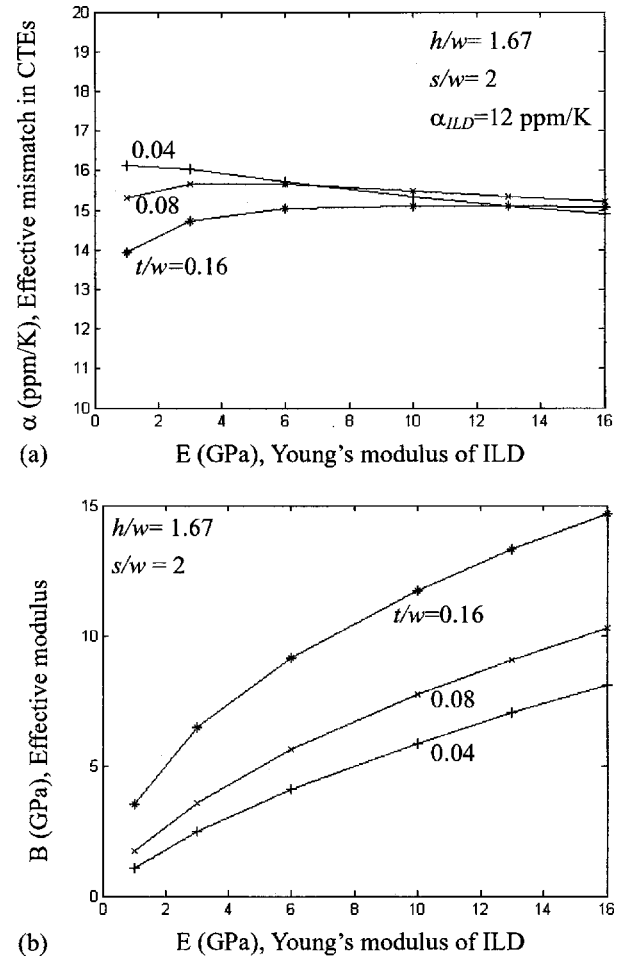


FIG. 8. The effect of elastic modulus of the dielectric and the thickness of the liner on the effective mismatch in the CTEs (a), and on the effective modulus (b).

and the ultrathin liners has little effect on the VSV due to thermal strains. By contrast, the porous CDOs and the ultrathin liners have a significant impact on the effective modulus B . For example, for representative values $t/w=0.08$ and $E=10$ GPa in the current technology, $B=7.7$ GPa. For a thinner liner and more compliant dielectric, $t/w=0.04$ and $E=3$ GPa, the effective modulus reduces to $B=2.5$ GPa, leading to a VSV three times larger.

V. DISCUSSIONS

In this section, we place the above results into the context of interconnect design. Unless otherwise stated, we will use the following values in numerical estimates: $Z^* = 1$, $\rho = 4 \times 10^{-8} \Omega \text{ m}$, $\Omega = 1.18 \times 10^{-29} \text{ m}^3$, $j = 10^{10} \text{ A/m}^2$, $w = 10^{-7} \text{ m}$, $h = 2 \times 10^{-7} \text{ m}$, $L = 10^{-5} \text{ m}$, $T_0 - T = 200^\circ \text{C}$, $\alpha = 15$ ppm/K, and $B = 7.7$ GPa.

Thus far we have focused on one kind of the steady state, in which a single void forms near the upstream via, and the electron wind is balanced by the pressure gradient $\partial p / \partial x = Z^* e j L / \Omega$. An alternative steady state is that no void forms, and the electron wind is balanced by the same pressure gradient. In this void-free steady state, the stress at the upstream via no longer vanishes. The pressure gradient induces a tensile stress $Z^* e j L / 2 \Omega$ near the upstream via and a

compressive stress of the same magnitude near the downstream via. In addition, the temperature change causes a uniform hydrostatic tensile stress $3B\alpha(T_0 - T)$ in the conductor. The sum of the two effects gives the net stress at the upstream via:

$$\sigma = 3B\alpha(T_0 - T) + \frac{Z^* e \rho j L}{2\Omega}. \quad (12)$$

Thermal stresses in encapsulated narrow Cu lines have been measured using x-ray diffraction, and calculated using the finite element method assuming the conductor line is elastic (e.g., Ref. 26). The mean of the stresses so obtained agrees well with thermal stress in Eq. (12).

Using the values listed in the beginning of this section, we find from Eq. (12) that the stress due to thermal strains is 69 MPa and that due to electromigration is 27 MPa. Let γ be the surface energy; for copper its value is on the order of 1 J/m². A void-like flaw in the conductor will grow if its initial size exceeds about γ/σ , which is on the order of 10 nm. Flaws of this size are likely to be present in the conductor lines. Also, right after the cooling, the stresses in the conductor can be very high at grain junctions. These high stresses are not described by the steady-state formula (12), but can motivate voids to nucleate in the conductor. Consequently, the void-free steady state is unlikely to be stable in practice, and will not be discussed any further in this paper.

The net VSV in a conductor line is the sum of the contributions from thermal strains, electromigration, and any other origins:

$$V_{sv} = V_0 + 3\alpha(T_0 - T)AL + \frac{Z^* e \rho j L^2 A}{2\Omega B}, \quad (13)$$

where V_0 is the contribution from all other origins. It is sometimes assumed that the conductor line is stress-free and void-free at the encapsulation temperature. Under this assumption, $V_0 = 0$ if the encapsulation temperature is set to be the reference temperature T_0 . In practice, however, this assumption is unreliable. As-deposited copper lines contain a large number of defects such as grain boundaries. During annealing and even after encapsulation, the defects are gradually removed, a process that generates stresses in the conductor line. Furthermore, encapsulation may introduce other defects that add to the void volume. On the basis of these considerations, a prudent approach is to set the reference temperature T_0 at an arbitrary level and determine V_0 by an independent measurement. Alternatively, the temperature at which a conductor line is stress-free and void-free should be determined independently.

Voids induced by thermal strains and electromigration are usually tested separately, under different conditions. This practice may lead to misleading predictions. For example, a representative stress-free, void-free temperature is 300 °C. At this temperature, when an electric current is applied, the VSV is solely due to electromigration, and is estimated to be 0.7×10^{-21} m³, using the numbers listed at the beginning of this section. However, at an operation temperature, say 100 °C, the VSV due to the temperature drop is 1.8×10^{-21} m³. Here the thermal strains contribute significantly

to the VSV. Consequently, subject to the same electric current, a conductor line found immortal at an elevated temperature can be mortal at the operation temperature.

A void in a conductor line becomes critical when it blocks the electric current. The volume of the critical void is a random variable depending on, among other factors, the exact location where the void forms. The smallest current-blocking void usually forms right at the upstream via. The volume of this critical void can be estimated as follows. Copper atoms are mobile on the void surface. The void shape depends on the relative magnitude of the electron flux and the surface energy, measured by the dimensionless number²⁷

$$\eta = \frac{Z^* e \rho j a^2}{\gamma \Omega}, \quad (14)$$

where a is a representative size scale of the void. For representative void size $a = 100$ nm, the dimensionless number is on the order $\eta = 10^{-1}$. Consequently, the void shape is largely determined by the surface energy. Furthermore, we will neglect the anisotropy in the surface energy, and assume that the surface diffusion is fast compared to the transport along the line. The critical void takes the equilibrium shape of a spherical cap, its base diameter coinciding with the via size d , giving the volume

$$V_{crit} = \frac{\pi d^3}{12} \left(\frac{1}{1 - \cos \Psi} + \frac{\cos \Psi}{2} \right) \sin \Psi, \quad (15)$$

where Ψ is the wetting angle of copper on the liner. The critical volume scales with the via diameter as $V_{crit} \sim d^3$, and increases as the wetting angle decreases. Taking $\Psi = 90^\circ$ and $d = 10^{-7}$ m, we find that $V_{crit} = 0.26 \times 10^{-21}$ m³.

When the volume of the saturated void is smaller than the volume of the critical void, $V_{sv} < V_{crit}$, the conductor line is immortal.¹⁶⁻²¹ The above numerical estimates, however, show that the VSV exceeds the V_{crit} , indicating that the conductor line is mortal. This prediction is consistent with the reported experimental data (e.g., Refs. 28 and 29). One remedy to immortalize a conductor line is to increase V_{crit} by introducing, for example, multiple vias, a large via, or an effective shunt. It is also possible to reduce the VSV by changing geometry. As evident in Eq. (13), the VSV due to electromigration is quadratic in the line length, and the VSV due to temperature change is linear in the line length. If the length of the line is reduced to $L = 0.5 \times 10^{-5}$ m, for example, the VSV due to electromigration is 0.18×10^{-21} m³, and the VSV due to a temperature drop of 200 °C is 0.9×10^{-21} m³. To further reduce the latter, one may explore processing conditions that lower the stress-free and void-free temperature of the conductor line. In a given interconnect structure, conductor lines may have different geometric parameters. Their effects on the VSV are contained in the numerical results presented in this paper. For example, for compliant dielectrics, the more closely spaced the neighboring conductor lines, the larger the effective modulus B and the smaller the VSV [Fig. 7(c)]. As another example, upper-level conductor lines in an interconnect structure are typically wide. Such wide lines have small effective modulus B [Fig. 7(a)].

When the volume of the saturated void exceeds the volume of the critical void, $V_{sv} > V_{crit}$ the conductor line is mortal. A design rule for mortal lines must ensure that the lifetime is long enough. Time-dependent models, invoking void nucleation and growth, have been discussed in Refs. 28–30. Further discussions of such models are beyond the scope of this paper.

VI. CONCLUSIONS

Voids caused by thermal strains and electromigration are a major concern in the semiconductor industry. In a conductor line a void may saturate to a deterministic volume, the VSV, a well-defined quantity that can be used to rank materials and geometries of the interconnect structures. We describe a general method to calculate the VSV, assuming that the steady state is reached when each point in a conductor line is in a hydrostatic state. The method circumvents the complexity caused by the transient processes of atomic migration and void dynamics. Numerical results show that the VSV can either increase or decrease when the coefficient of thermal expansion of the dielectric increases, and will increase when the elastic modulus of the dielectric decreases. The use of porous dielectrics and ultrathin liners will significantly increase the VSV. Thermal strains contribute significantly to the VSV, and must be taken into account in interpreting electromigration test. Subject to a given electric current, a conductor line found immortal at an elevated temperature can be mortal at the operation temperature. The method to determine the VSV provides a tool to assess options in interconnect design.

ACKNOWLEDGMENTS

This work was supported by the National Science Foundation through the MRSEC and by the Division of Engineering and Applied Sciences at Harvard University.

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