RNA logic gates

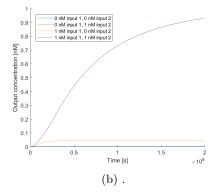
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0.1 Results

To test the perceptron compiling and training, 5 different truth tables were used, ranging from 2 to 3 inputs. The correct output was reached after 16-23 iterations of the learning algorithm. Input sizes greater than 3 was not tested, as the training time increases exponentially in time with the input size.

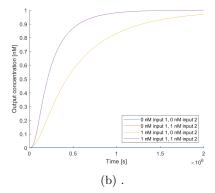
Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1



(a) Truth table for the 2-input AND gate.

Figure 1: Simulation results of the trained 2-input AND gate. The network is trained to activate when both of the inputs are active. The correct output was obtained after 21 iterations of the training algorithm, with a weight of 1.9 for all inputs, and a threshold of 10.

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1



(a) Truth table for the 2-input OR gate.

Figure 2: Simulation results of the trained 2-input OR gate. The network is trained to activate when one of the inputs is active. The correct output was obtained after 22 iterations of the training algorithm, with a weight of 2.1 for all inputs, and a threshold of 10.

Input 1	Input 2	Input 3	Out	0.9
0	0	0	0	0.8 \(\varphi\) 0.7
0	0	1	0	W_U 0.7
0	1	0	0	0.5 -
0	1	1	0	0.4 - 0 nM input 1, 0 nM input 2, 0 nM input 3
1	0	0	0	0 nM input 1, 0 nM input 2, 1 nM input 3 0 nM input 1, 1 nM input 2, 0 nM input 3 0 nM input 1, 1 nM input 2, 1 nM input 3
1	0	1	0	0.2 1 nM input 1, 0 nM input 2, 0 nM input 3 - 1 nM input 1, 0 nM input 2, 1 nM input 3
1	1	0	0	0.1 1 nM input 1, 1 nM input 2, 0 nM input 3 1 nM input 1, 1 nM input 2, 1 nM input 3
1	1	1	1	0 0.5 1 1.5 2 Time [s] ×10 ⁶
(a) Truth ta	ble for the 3	-input AND	gate.	(b) .

Figure 3: Simulation results of the trained 3-input AND gate. The network is trained to activate when all of the inputs are active. The correct output was obtained after 14 iterations of the training algorithm, with a weight of 1.2 for all inputs, and a threshold of 10.

Input 1	Input 2	Input 3	Out	0.9
0	0	0	0	0.8 ¥ 0.7
0	0	1	1	ug 0.6
0	1	0	1	0.5
0	1	1	1	We 0.7 100
1	0	0	1	0 nM input 1, 1 nM input 2, 1 nM input 3 0 nM input 1, 1 nM input 3 0 nM input 1, 1 nM input 2, 1 nM input 3
1	0	1	1	0.2 - 1 nM input 1, 0 nM input 2, 0 nM input 3 1 nM input 1, 0 nM input 2, 1 nM input 3
1	1	0	1	0.1
1	1	1	1	0 0.5 1 1.5 2 Time [s] ×10 ⁶
(a) Truth ta	ble for the 3-	-input 1-OR	gate.	(b) .

Figure 4: Simulation results of the trained 3-input 1-OR gate. The network is trained to activate when at least 1 of the inputs is active. The correct output was obtained after 16 iterations of the training algorithm, with a weight of 1.3 for all inputs, and a threshold of 10.

Input 1	Input 2	Input 3	Out	0.9
0	0	0	0	0.8 ₹ 0.7
0	0	1	0	uig 0.6
0	1	0	0	0.6 - 0.6 - 0.6 - 0.7 - 0 nM input 1, 0 nM input 2, 0 nM input 3 - 0 nM input 1, 1 n MM input 2, 0 nM input 3 - 0 nM input 1, 1 n MM input 2, 1 nM input 3 - 0 nM input 1, 1 nM input 3 - 0 nM input 3 - 0 nM input 4, 1 nM input 3 - 0 nM input 5 - 0 nM
0	1	1	1	0 nM input 1, 0 nM input 2, 0 nM input 3
1	0	0	0	0.3 - 0 nM input 1, 0 nM input 2, 1 nM input 3 0 nM input 1, 1 nM input 3 - 0 nM input 1, 1 nM input 2, 1 nM input 3
1	0	1	1	0.2 - 1 nM input 1, 0 nM input 2, 0 nM input 3 1 nM input 1, 0 nM input 2, 1 nM input 3
1	1	0	1	0.1 1 nM input 1, 1 nM input 2, 0 nM input 3 1 nM input 1, 1 nM input 2, 1 nM input 3
1	1	1	1	0 0.5 1 1.5 2 Time [s] ×10 ⁶
(a) Truth ta	ble for the 3-	-input 2-OR	gate.	(b) .

Figure 5: Simulation results of the trained 3-input 2-OR gate. The network is trained to activate when at least 2 of the inputs is active. The correct output was obtained after 15 iterations of the training algorithm, with a weight of 1.3 for all inputs, and a threshold of 10.