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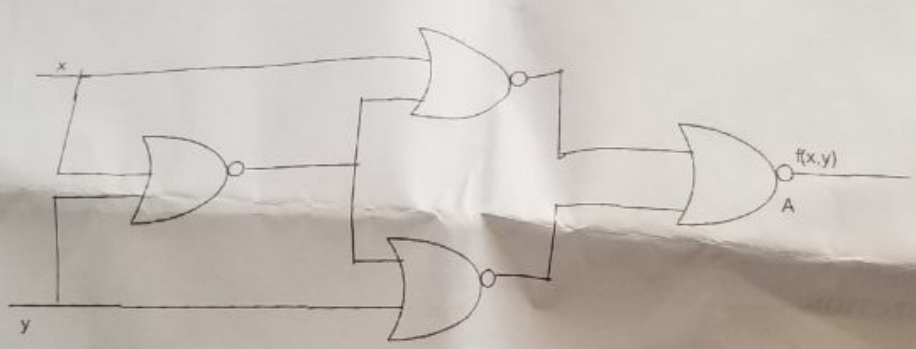
PART I: Multiple Choice Questions (2 pt. Each)

Choose the best answer among the choices provided and place your choice letter on the space provided

1. In which of the following gates, the output is 1, if and only if at least one input is 1?

   a) NOR b) AND
   c) OR d) NAND

2. Identify the logic function performed by the circuit shown in the given figure



   a) Exclusive OR b) Exclusive NOR
   c) NAND d) NOR

3. The number of full and half-adders required to add 16-bit numbers is

   a) 8 half-adders, 8 full-adders b) 1 half-adder, 15 full-adders
   c) 16 half-adders, 0 full-adders d) 4 half-adders, 12 full-adders

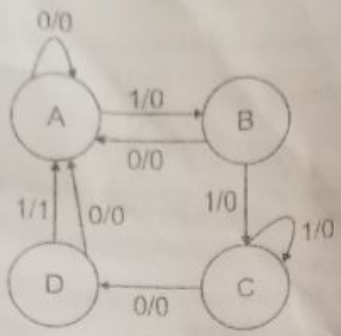
4. Which of the following expressions is not equivalent to X ' ?

   a) X NAND X b) X NOR X
   c) X NAND 1 d) X NOR 1

5. Which table shows the logical state of a digital circuit output for every possible combination of logical states in the inputs ?

   a) Function table b) Truth table
   c) Routing table d) ASCII table

6. The sequence detected by the state diagram shown below is



a)1110 sequence detector without overlap b)1110 sequence detector with overlap
c)1101 sequence detector without overlap d)1101 sequence detector with overlap

7. The characteristic equation of D flip-flop is:

a) Q = 1 b) Q = 0
c) Q = D d) Q= D

8. Flip-flop outputs are always

a) Complimentary b) The same
c)Independent of each other d) same as previous input

9. The output of a sequential circuit depends on

a) Present inputs only b) Past outputs only
c)Both present and past inputs d) Present outputs only

10. Diagram which is used to show logic elements and their interconnections is said to be

a) circuit diagram b) system diagram
c)logic diagram d) gate diagram

11. What function do the following Verilog module implement?

```
module example (x,s,y,f);
        input x,s,y;
        output f;
        wire t1,t2,t3;
                not(t1,s);
              and(t2,t1,x);
      and(t3,s,y);
            or(f,t2,t3);
endmodule
```

a) f= x.s + y.s'b) f= x.s + y.s c) f= x.s' + y.s d)None of these

12. Which of these sets of logic gates are known as universal gates?

a)XOR, NAND, OR b)OR, NOT, XOR c)NOR, NAND, XNOR d)NOR, NAND

13. A finite state machine in which

1. the output is a function of the current state and inputs
2. the output is a function of only the current state

Which of the following machines is respectively correct for these styles?

a)Mealy machine and Moore machine b)Moore machine and Mealy machine

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c)State machine and Mealy machine d) State machine and State Machine

14. The major difference between Mealy and Moore machine is about:

a) Output Variations b) Input Variations
c) Both d) None of the mentioned

15. Choose the correct option:

Statement 1: Mealy machine reacts faster to inputs.
Statement 2: Moore machine has more circuit delays.
a) Statement 1 is true and Statement 2 is true b) Statement 1 is true but Statement 2 is false
c) Statement 1 is false and Statement 2 is true d) None of the mentioned is true

16. In the toggle mode, a JK flip-flop has

a)J = 0, K = 1 b)J = 1, K = 1 c)J = 0, K = 0 d)J = 1, K = 0

17. Consider the following Verilog module

```
module ALU (data1, data2, cond, result);
    input[7:0]data1,data2;
    input[2:0] cond;
    output reg [7:0] result;
    always @(data1 or data2 or cond)
        begin
            if(cond==3'b000) result=data1;
            elseif(cond==3'b001) result=data2;
            elseif(cond==3'b010) result=data1+data2;
            elseif(cond==3'b011) result= data1-data2;
            elseif(cond==3'b101) result= data1&data2;
            elseif(cond==3'b110) result= data1|data2;
            elseif(cond==3'b111) result=0;
        end
endmodule
```

What will happen when the module is synthesized?

a. A combinational circuit will be generated

b. A sequential circuit with storage element will be generated

c. If the synthesizer supports adder and subtractor block , a combinational circuit will be generated.

d. None of these

18. Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

a) Simulation b) Optimization

c)Synthesis d) Verification

19. For the Verilog code segment below, circle correct answers:

```
1 always@ (posedge clk)
2 begin
3 z = y; y = x;
4 y1= x1; z1 = y1;
5 z2<= y2; y2 <= x2;
6 y3<= x3; z3 <= y3;
```

a) Line 3 implements a shift register b) Line 4 implements a shift register

c) Line 5 implements a parallel flip-flop. d) Line 6 implements a shift register.

20. If a variable is not assigned in all possible executions of an always statement then:

a) A don't care is inferred b) A latch is inferred

c) The variable is set to 0 d) The synthesis process will fail

PART II: True/False Questions (1 pt. each)

On the space provided write **True** if the statement is true and write **False** if the statement is false

1. A D flip-flop can be implemented with a JK flip-flop and one NOT gate
2. Verilog is case sensitive
$$a \oplus c = \overline{a} \cdot c + a \cdot \overline{c}$$
3. A T flip-flop can be implemented with only 6 NAND gates.
4. $1 \oplus 1 \oplus 0 = 1$
5. I forgot to write down my name and student ID number
6. Moore machine has fewer states than a mealy machine.
7. An "if" statement must always be inside of an "always" block.
8. An inverter output is the complement of its input.
9. Use of Blocking Assignments is preferable to Non-Blocking Assignments because race
10. A NOR gate output is LOW if any of its inputs is LOW.

conditions are less likely to occur.