Assignment 2

DIGITAL IC DESIGN I

EE4610

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Contents

1 Schematic

This chapter will show the schematics of the full adder we designed. For the simulation we use default processing speed.
Design details:
PMOS: width=$2\,\mu$m; length=180 nm ; NMOS: width=$1\,\mu$m; length=180 nm

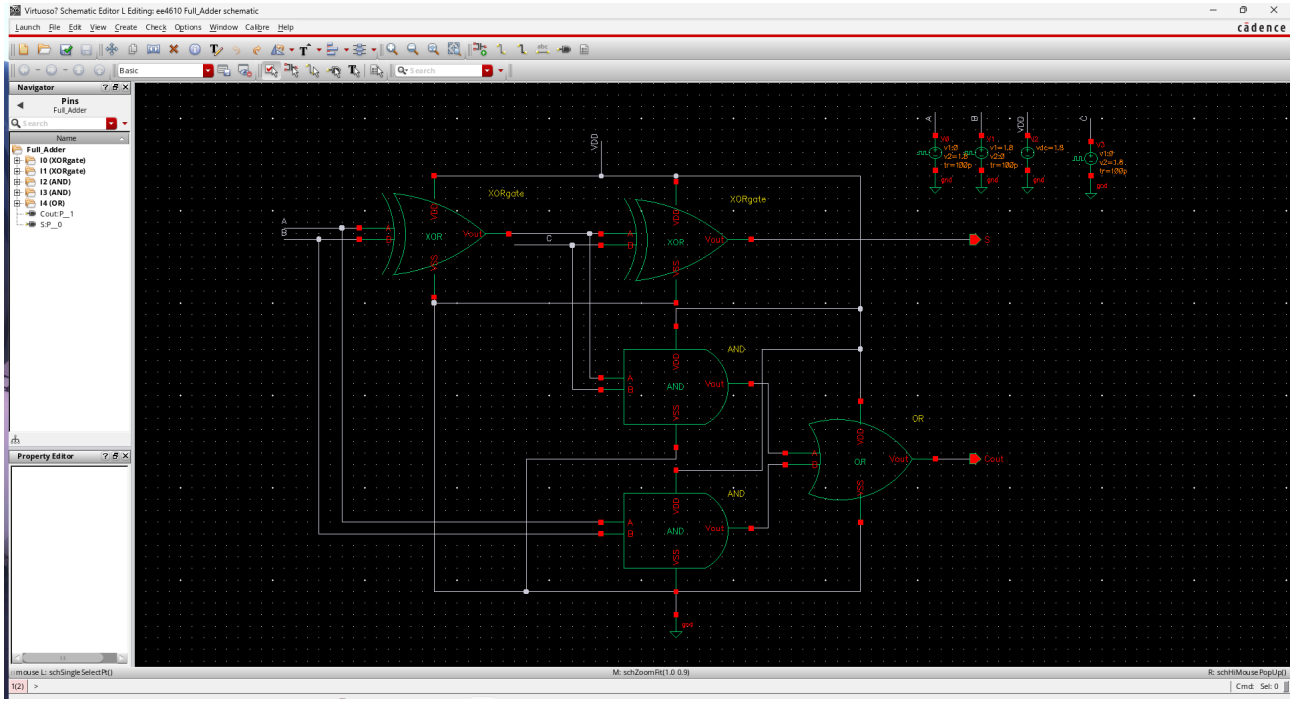


Figure 1: Full adder schematic.

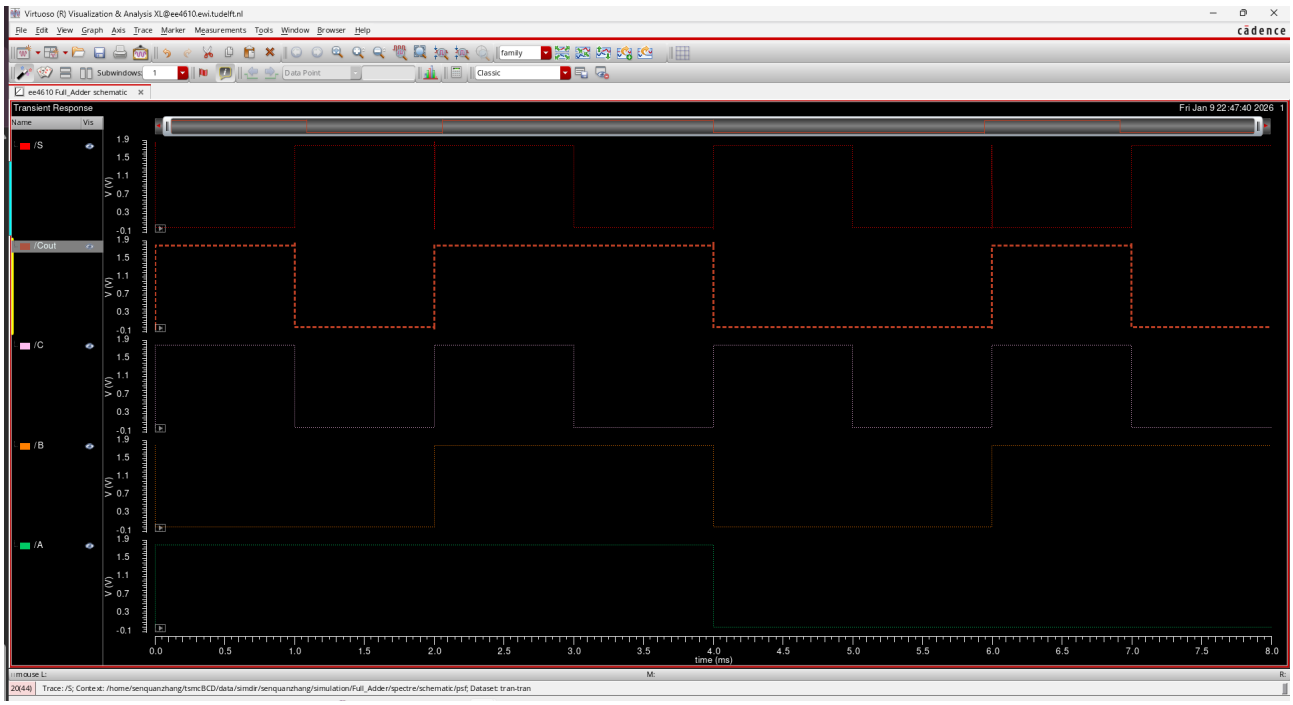


Figure 2: Full adder functional verification (inputs: A, B, C; outputs: S, Cout).

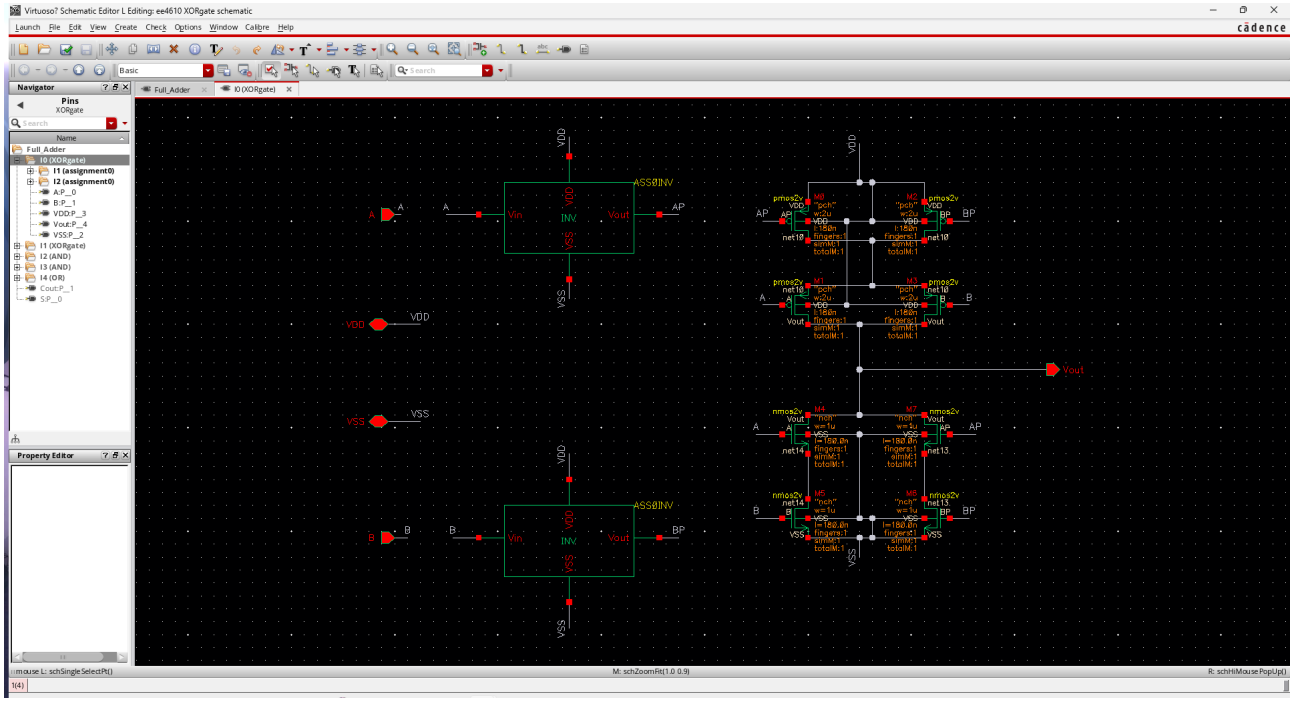


Figure 3: XOR gate schematic.

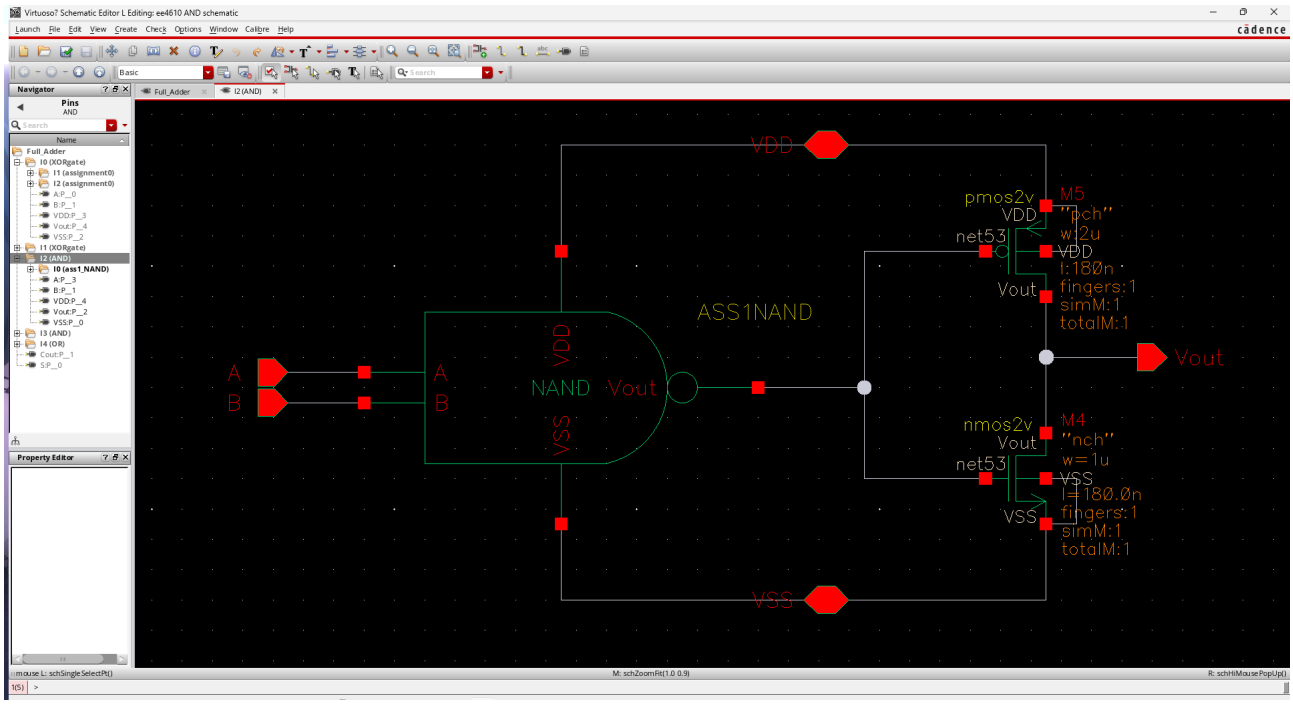


Figure 4: AND gate schematic.

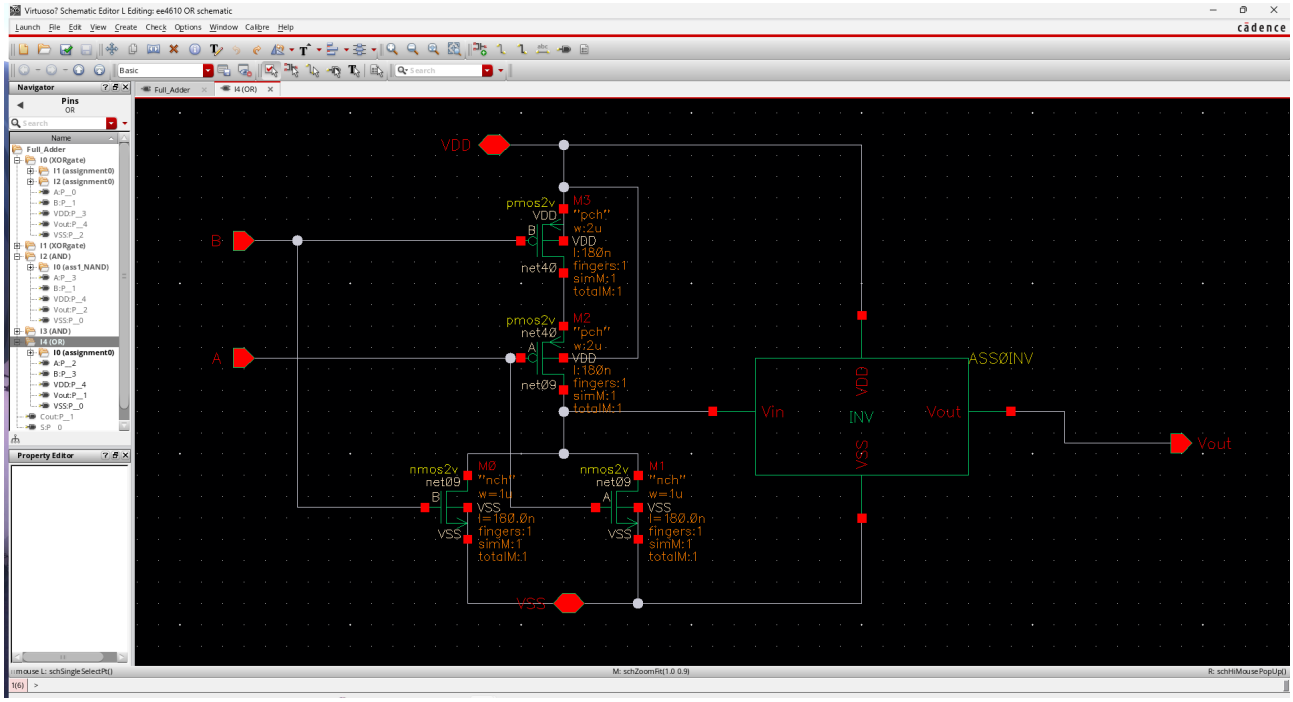


Figure 5: OR gate schematic.

2 Results

2.1 Propagation delay

We used the ADE L *Calculator* to automatically measure propagation delay and transition times from the transient waveforms. For example, to analyze the A-S route delay we applied these formulas:

```
delay(?wf1 VT("/A") ?value1 0.9 ?edge1 "rising" ?nth1 1 ?td1 0.0 ?tol1 nil ?wf2 VT("/S") ?value2 0.9 ?edge2 "rising" ?nth2 1 ?tol2 nil ?td2 nil ?stop nil ?multiple nil)
```

Figure 6: A–S t_{pLH} measurement expression.

```
delay(?wf1 VT("/A") ?value1 0.9 ?edge1 "falling" ?nth1 1 ?td1 0.0 ?tol1 nil ?wf2 VT("/S") ?value2 0.9 ?edge2 "falling" ?nth2 1 ?tol2 nil ?td2 nil ?stop nil ?multiple nil)
```

Figure 7: A-S tphl formula.

```
delay(?wf1 VT("/S"), ?value1 0.18, ?edge1 "rising", ?nth1 1, ?td1 0.0, ?tol1 nil, ?wf2 VT("/S"), ?value2 1.62, ?edge2 "rising", ?nth2 1, ?tol2 nil, ?td2 nil , ?stop nil, ?multiple nil)
```

Figure 8: A-S rising formula.

```
delay(?wf1 VT("/S"), ?value1 1.62, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?tol1 nil, ?wf2 VT("/S"), ?value2 0.18, ?edge2 "falling", ?nth2 1, ?tol2 nil, ?td2 nil , ?stop nil, ?multiple nil)
```

Figure 9: A-S falling formula.

The same measurement expressions were reused for each path, changing only the input and output node names. And each delay analysis are using the signal with 2ms as period duty cycle.

2.1.1 A-S route

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	☐	allv
2	B		☑	☐	allv
3	C		☑	☐	allv
4	S		☑	☐	allv
5	Cout		☑	☐	allv
6	A-S_tplh	249.2p	☑	☐	
7	A-S_tpHl	222.898p	☑	☐	
8	A-S_rising	83.2516p	☑	☐	
9	A-S_falling	78.1663p	☑	☐	

Figure 10: A-S propagation delay

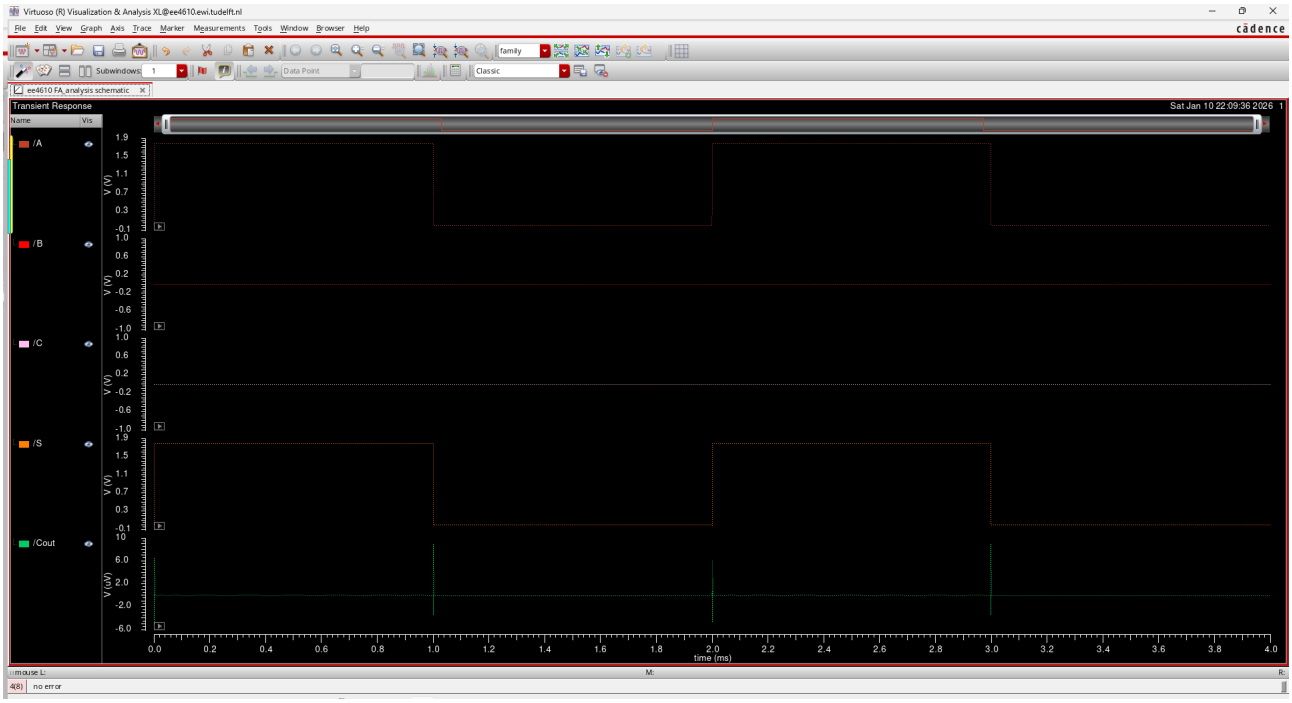


Figure 11: A-S propagation delay curve

The propagation delay of A-S route is:

$$t_{p(A-S)} = \frac{t_{pLH} + t_{pHL}}{2} = 236.049ps$$

2.1.2 B-S route

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	☐	allv
2	B		☑	☐	allv
3	C		☑	☐	allv
4	S		☑	☐	allv
5	Cout		☑	☐	allv
6	B-S_tplh	252.986p	☑	☐	
7	B-S_tphl	230.043p	☑	☐	
8	B-S_rising	83.2271p	☑	☐	
9	B-S_falling	78.0292p	☑	☐	

Figure 12: B-S propagation delay

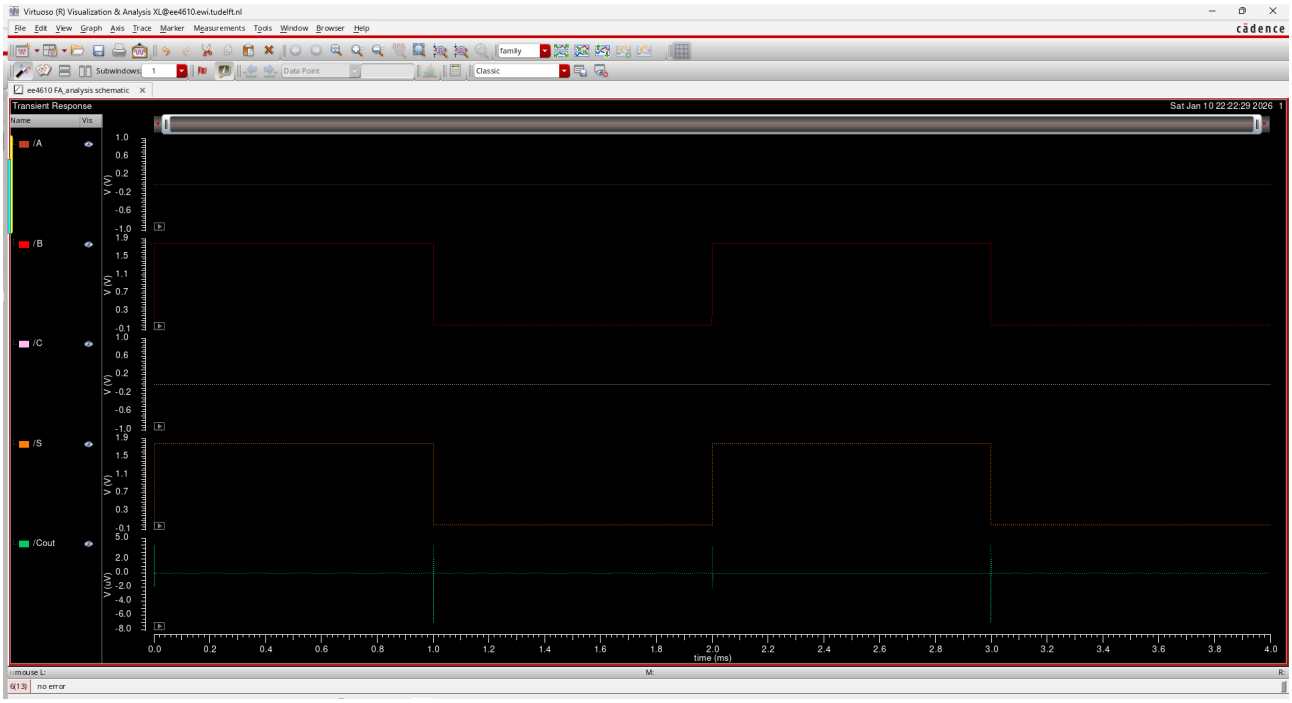


Figure 13: B-S propagation delay curve

The propagation delay of B-S route is:

$$t_{p(B-S)} = \frac{t_{pLH} + t_{pHL}}{2} = 241.708ps$$

2.1.3 C-S route

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	☐	allv
2	B		☑	☐	allv
3	C		☑	☐	allv
4	S		☑	☐	allv
5	Cout		☑	☐	allv
6	C-S_tplh	103.549p	☑	☐	
7	C-S_tphl	99.6081p	☑	☐	
8	C-S_rising	87.0622p	☑	☐	
9	C-S_falling	79.2009p	☑	☐	

Figure 14: C-S propagation delay

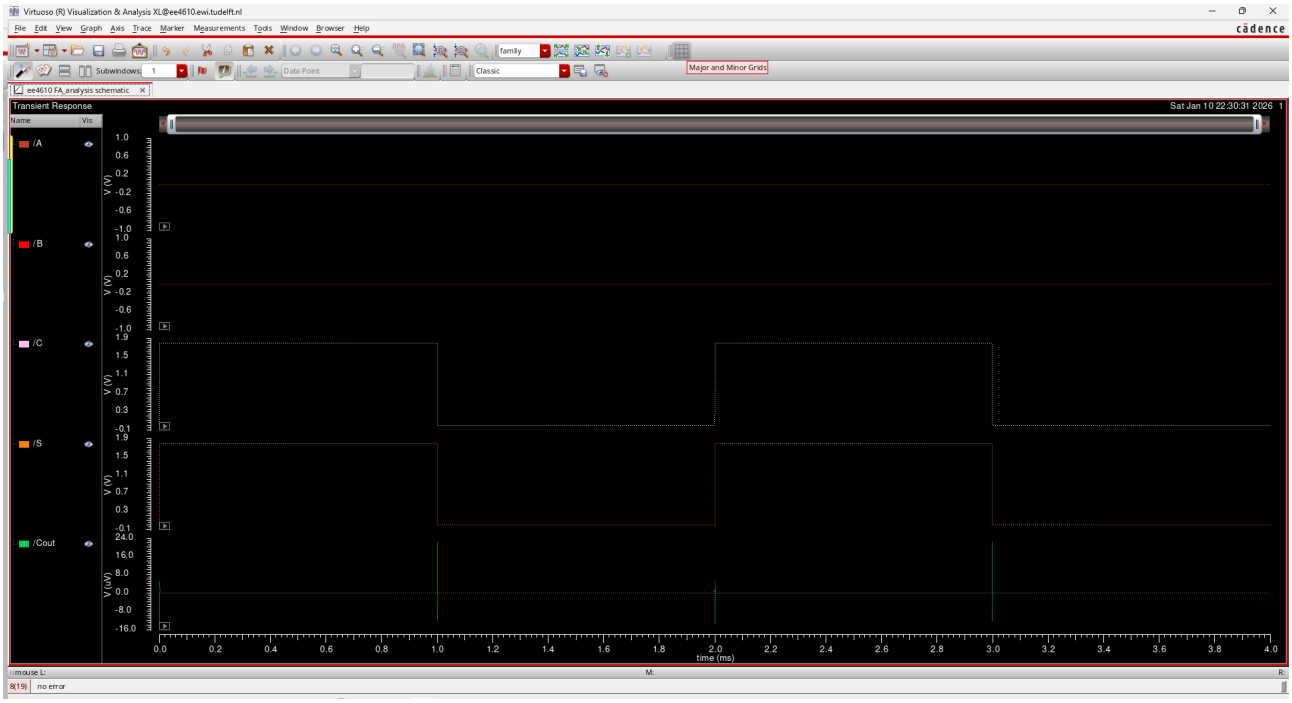


Figure 15: C-S propagation delay curve

The propagation delay of C-S route is:

$$t_{p(C-S)} = \frac{t_{pLH} + t_{pHL}}{2} = 101.579ps$$

2.1.4 A-Cout short route

Signal ’A’ and signal ’B’ will go through gate ’AND’ and gate ’OR’ to output.

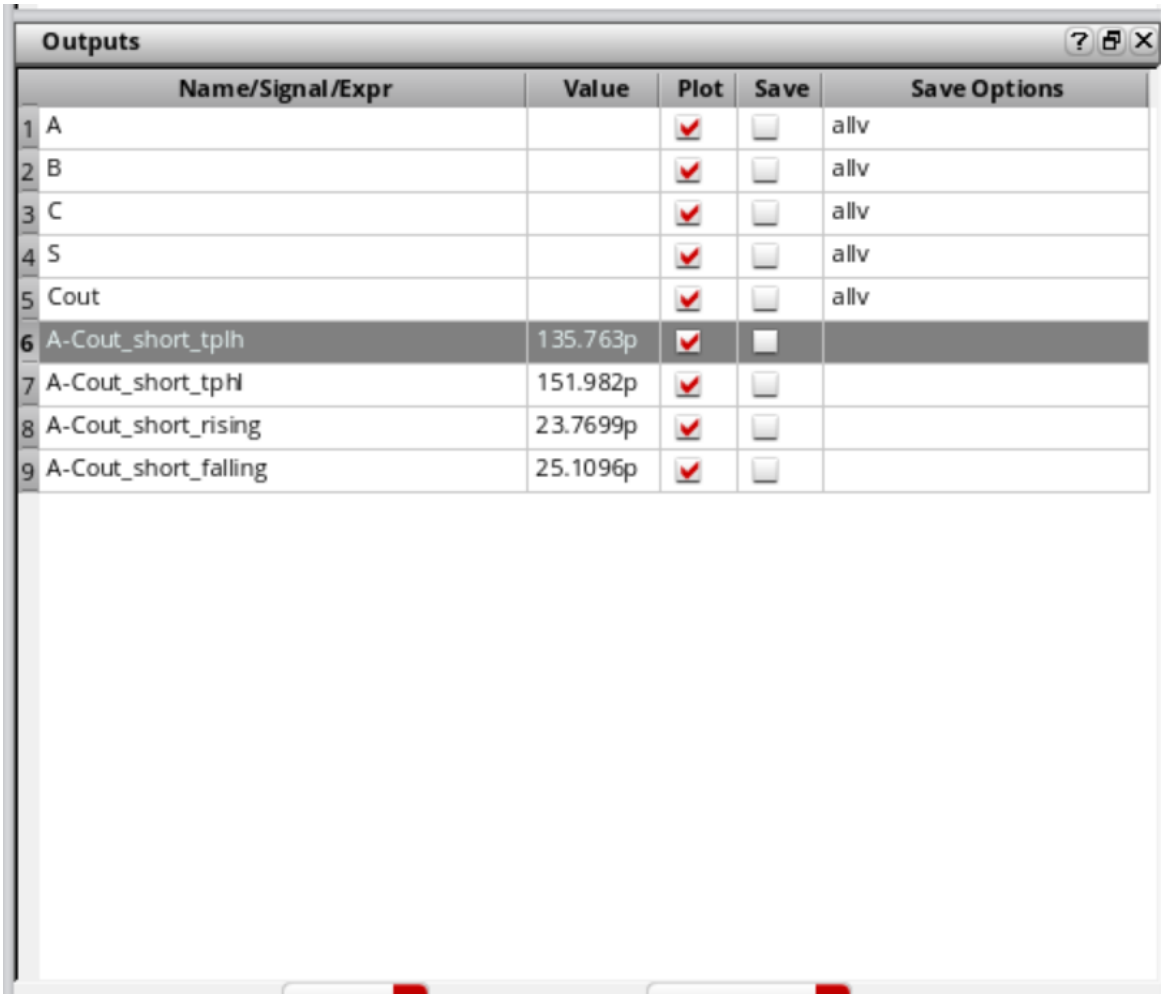


Figure 16: A-Cout short route propagation delay

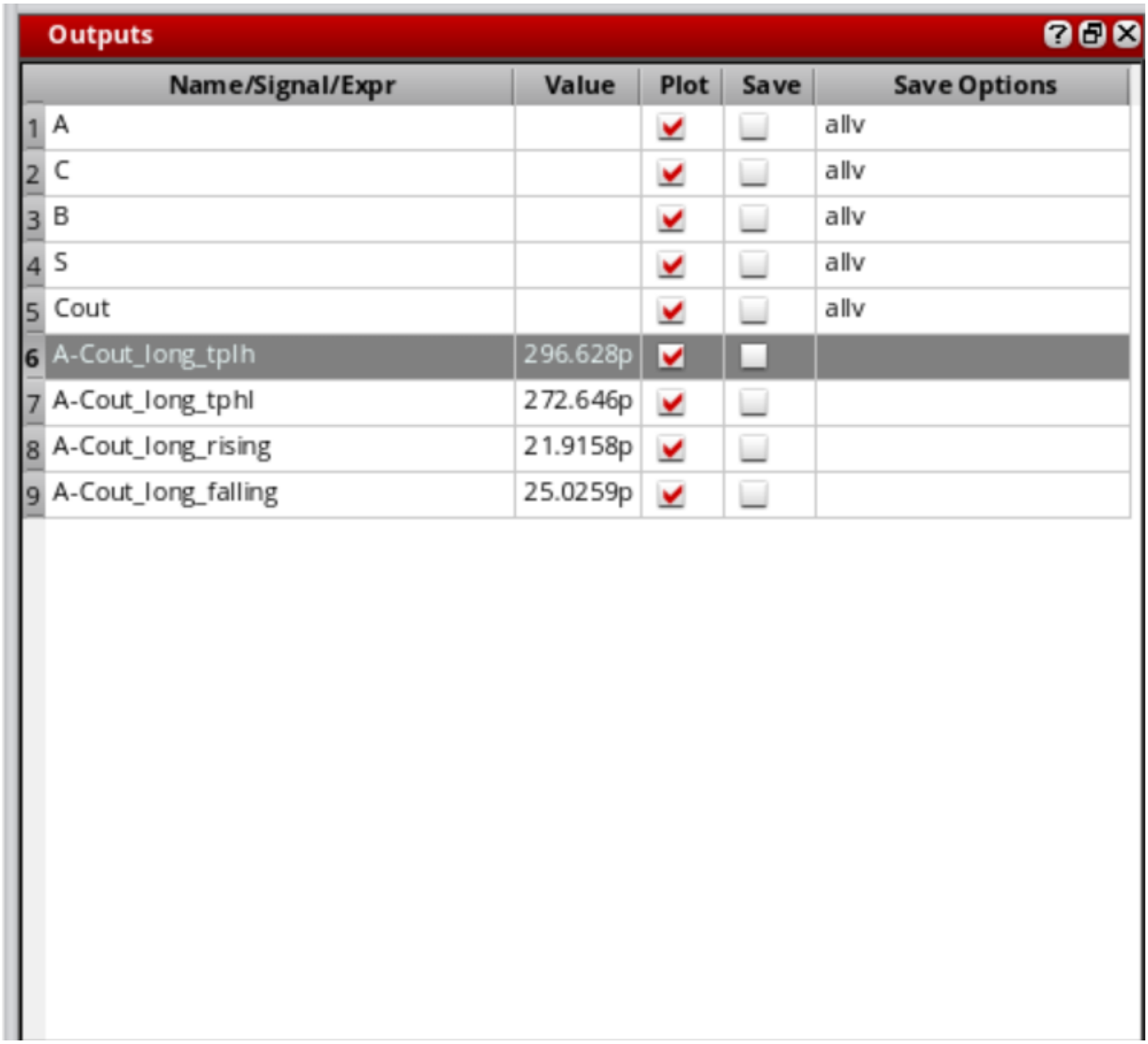
Figure 17: A-Cout short route propagation delay curve

The propagation delay of A-Cout short route is:

$$t_{p(A-Couts)} = \frac{t_{pLH} + t_{pHL}}{2} = 143.873ps$$

2.1.5 A-Cout long route

Signals ‘A‘ and ‘B‘ propagate through the XOR gate, then through the AND gate together with signal ‘C‘, and finally through the OR gate to produce *Cout*.



	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	☐	allv
2	C		☑	☐	allv
3	B		☑	☐	allv
4	S		☑	☐	allv
5	Cout		☑	☐	allv
6	A-Cout_long_tplh	296.628p	☑	☐	
7	A-Cout_long_tphl	272.646p	☑	☐	
8	A-Cout_long_rising	21.9158p	☑	☐	
9	A-Cout_long_falling	25.0259p	☑	☐	

Figure 18: A-Cout long route propagation delay

Figure 19: A-Cout long route propagation delay curve

The propagation delay of A-Cout long route is:

$$t_{p(A-Coutl)} = \frac{t_{pLH} + t_{pHL}}{2} = 284.637ps$$

2.1.6 C-Cout route

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	☐	allv
2	B		☑	☐	allv
3	C		☑	☐	allv
4	S		☑	☐	allv
5	Cout		☑	☐	allv
6	C-Cout_tplh	130.816p	☑	☐	
7	C-Cout_tphl	141.866p	☑	☐	
8	C-Cout_rising	21.8998p	☑	☐	
9	C-Cout_falling	24.9064p	☑	☐	

Figure 20: C-Cout propagation delay

Figure 21: C-Cout propagation delay curve

The propagation delay of C-Cout route is:

$$t_{p(C-Cout)} = \frac{t_{pLH} + t_{pHL}}{2} = 136.341ps$$

2.1.7 Data analysis

To conclude the delay analysis result is:

Table 1: Propagation delay

Item	Value
$t_{pd(A-S)}$	236.049 ps
$t_{pd(B-S)}$	241.708 ps
$t_{pd(C-S)}$	101.579 ps
$t_{pd(A-Couts)}$	143.873 ps
$t_{pd(A-Coutl)}$	284.637 ps
$t_{pd(C-Cout)}$	136.341 ps
$t_{pd(max)}$	284.637 ps

Table 2: Rising time

Item	Value
$t_{r(A-S)}$	83.252 ps
$t_{r(B-S)}$	83.227 ps
$t_{r(C-S)}$	87.062 ps
$t_{r(A-Couts)}$	23.770 ps
$t_{r(A-Coutl)}$	21.916 ps
$t_{r(C-Cout)}$	21.899 ps
$t_{r,S(max)}$	87.062 ps
$t_{r,Cout(max)}$	23.770 ps

Table 3: Falling time

Item	Value
$t_{f(A-S)}$	78.166 ps
$t_{f(B-S)}$	78.029 ps
$t_{f(C-S)}$	79.201 ps
$t_{f(A-Couts)}$	25.196 ps
$t_{f(A-Coutl)}$	25.026 ps
$t_{f(C-Cout)}$	24.906 ps
$t_{f,S(max)}$	79.201 ps
$t_{f,Cout(max)}$	25.196 ps

2.2 Quiescent power

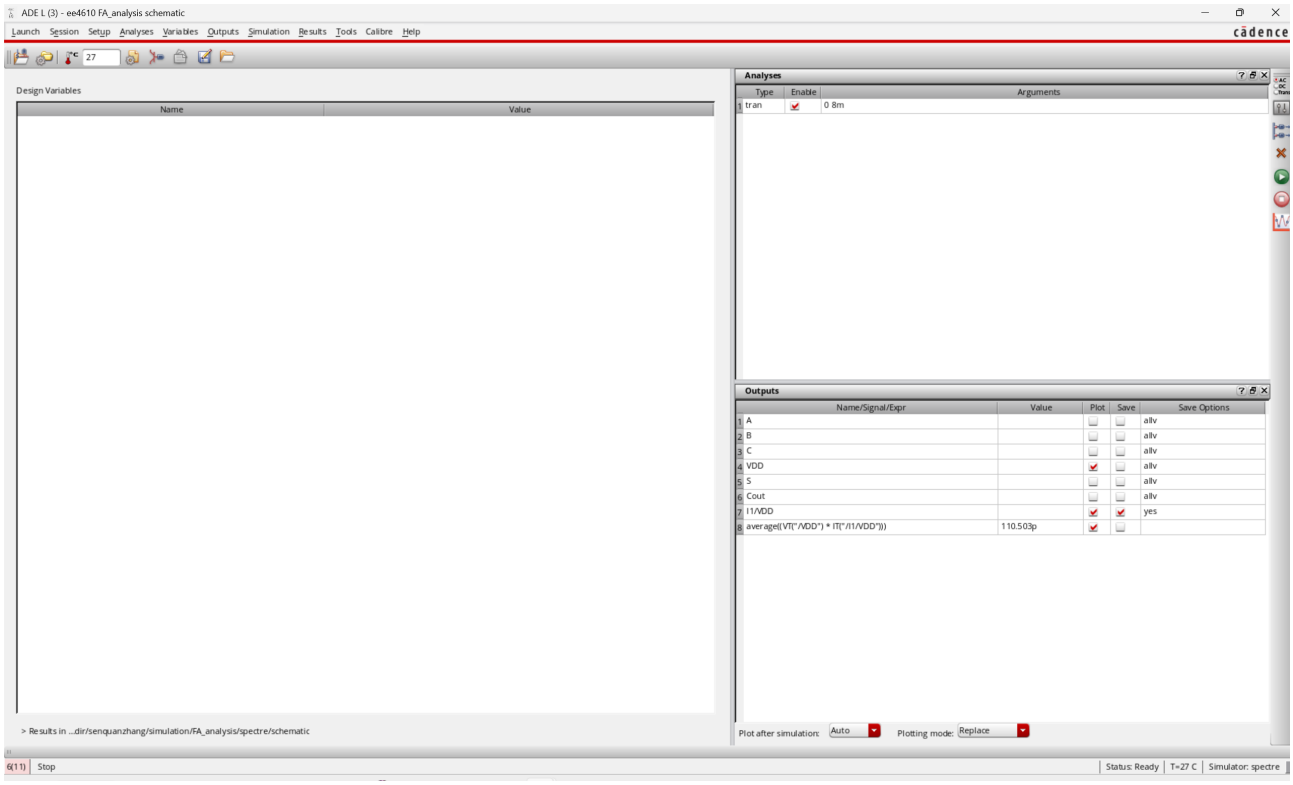


Figure 22: Quiescent power result

$$P_q = average(p(t)) = average(V \times I) = 110.503pW$$

2.3 Dynamic power

$$P_{\text{dyn}} = V_{\text{DD}}(I_{\text{avg,switch}} - I_{\text{avg,static}})$$

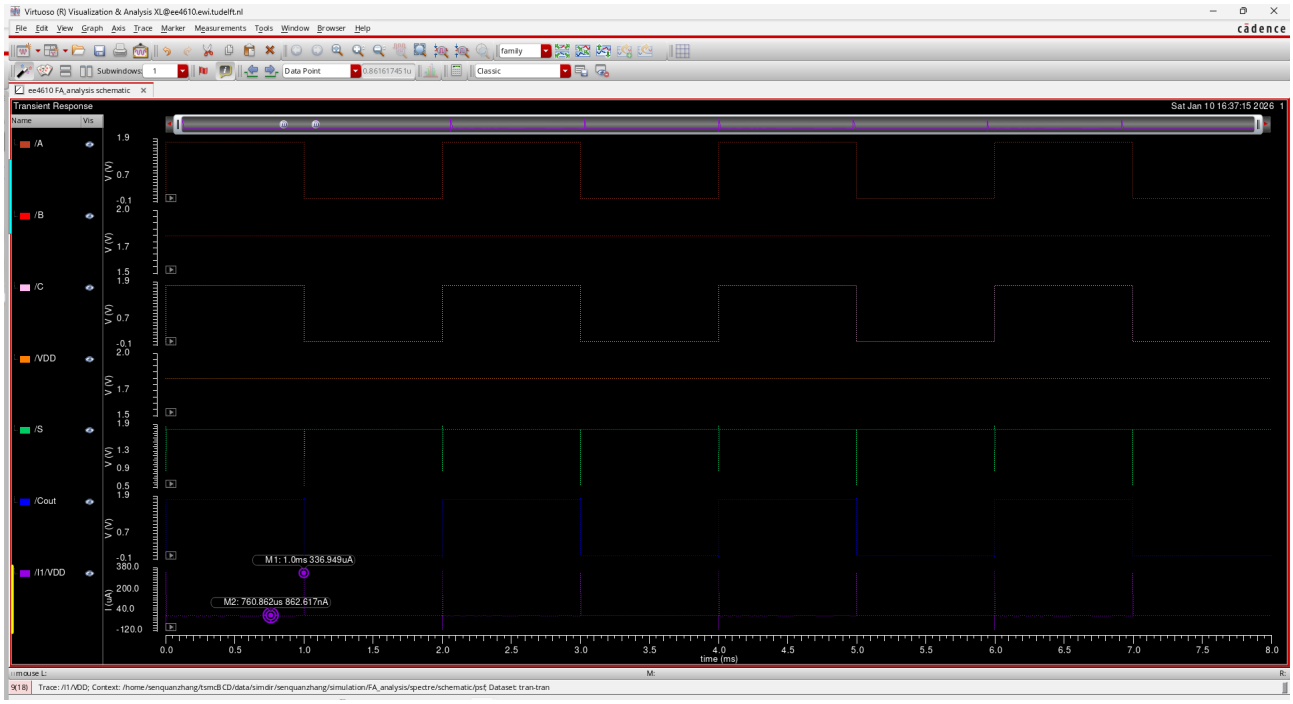


Figure 23: Dynamic power output curve

$$I_{\text{avg,switch}} = 336.949\mu A$$

$$I_{\text{avg,static}} = 862.617nA$$

$$P_{\text{dyn}} = V_{\text{DD}}(I_{\text{avg,switch}} - I_{\text{avg,static}}) = 604.955\mu W$$