

Assignments

EE4610 : DIGITAL IC DESIGN-I

Teaching Assistants:
Yunzhe Yang
y.yang-16@tudelft.nl

Introduction

Yunzhe Yang

email: y.yang-16@tudelft.nl

PhD Candidate at EI
Research interests:
Capacitive DC-DC
converters;
Thermoelectric energy
harvesting.



TA Task: assignments

For course-related questions:

Post on Brightspace → Collaboration → Discussions → Course Materials Q&A Forum

For assignment questions:

Post on Brightspace → Collaboration → Discussions → Cadence Assignments Q&A Forum

Haoyu Cai

email: H.Cai-2@tudelft.nl

PhD Candidate at ECTM
Research interests:
Isolated DC-DC converters;
Different types of power
management integrated
circuits



TA Task: assignments

Shunmin Jiang

email: s.jiang-12@student.tudelft.nl

Research interests:
Piezoelectric
Resonator-Based DC-
DC Converters;
Piezoelectric Energy
Harvesting Circuit.



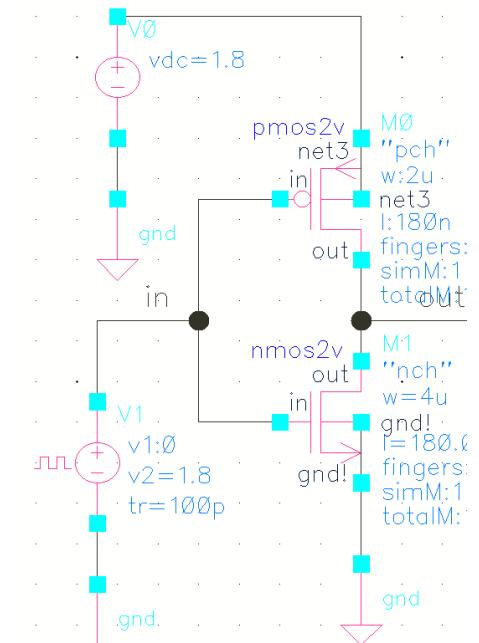
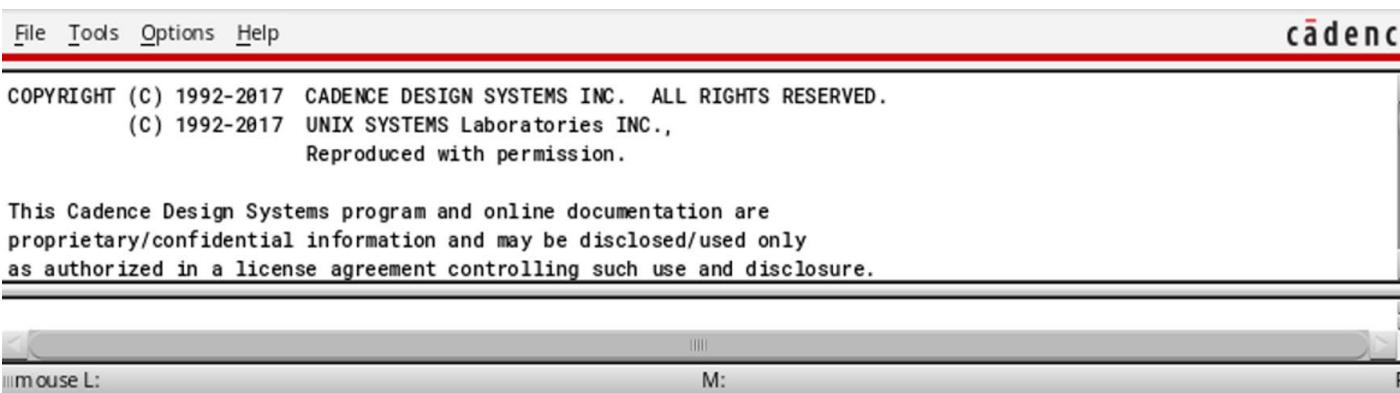
TA Task: course-related Q&A

General Description

- Be familiar with Cadence design & simulation flow
 - With the help of the tool: Virtuoso
 - Schematic design & simulation
 - Layout
 - Design rule check (DRC)

Pre-exercise

- Help you to get familiar with *Virtuoso*
- Get familiar with *TSMC 0.18μm Technology*
- Play & Exercise (*Don't need to submit*)
*Design an inverter (Example)



Assignments-Schematic & Layout design

- **Three people → Group**
- **Assignment 1 (Schematic & Layout Design)**
- **Assignment 2 (Schematic Design)**

Design flow referred to: EE4610_Assignment_Guide_2025

Assignment 1 – Schematic & Layout design

- **Design a NAND gate (Schematic & Layout)**
- **Do some analysis based on the schematic simulation:** propagation delay, rising time & falling time, quiescent power and dynamic power of the NAND
- **Finish the Layout of the NAND Gate (clean DRC errors as possible)**
- **More detailed technical requirements referred to EE4610_Assignment_Guide_2025 (Section 2.1 & 3.1)**

Assignment 1 – Schematic & Layout design

- **1-1: Schematic:**

*Width: $W_P = [(a+b+c) \bmod 3] + 1 (\mu\text{m})$, $W_N = 0.5 * W_P (\mu\text{m})$

(where a, b, c are the last digits of your group members' student ID)

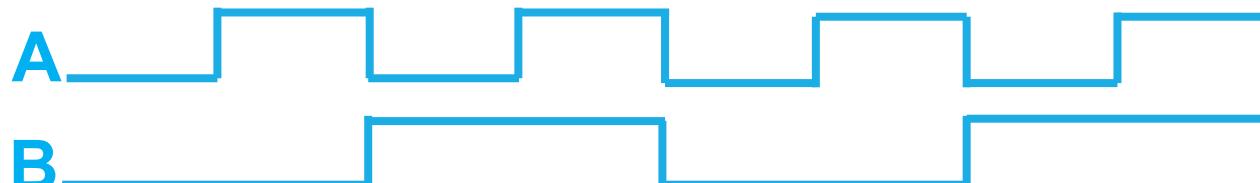
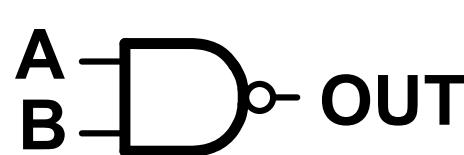
*Length: minimum length $0.18 \mu\text{m}$

Step (1): Verify the function

Build a testbench to prove the circuit works as a NAND gate correctly.

Here's an example of input signals. And you check the output.

Include a screenshot of the input/output signals' waveform in the report.



Assignment 1 – Schematic & Layout design

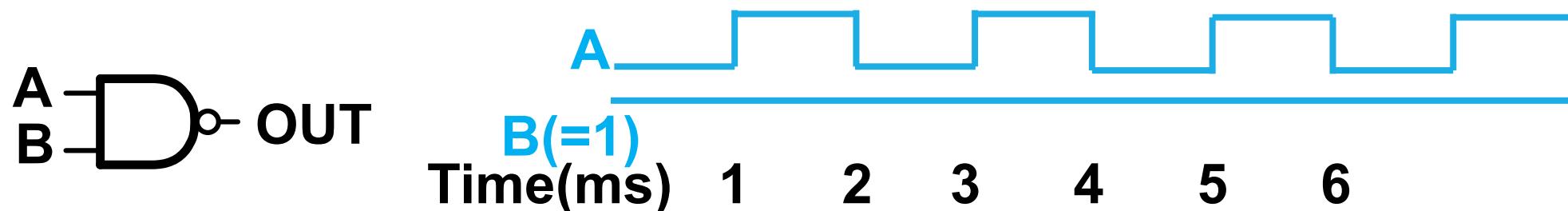
- **1-1: Schematic:**

Step (2): Simulate some performance parameters

*Input: A=101010..., B=111111... (rising/falling edge 100ps, period 2ms, pulse width 1ms)

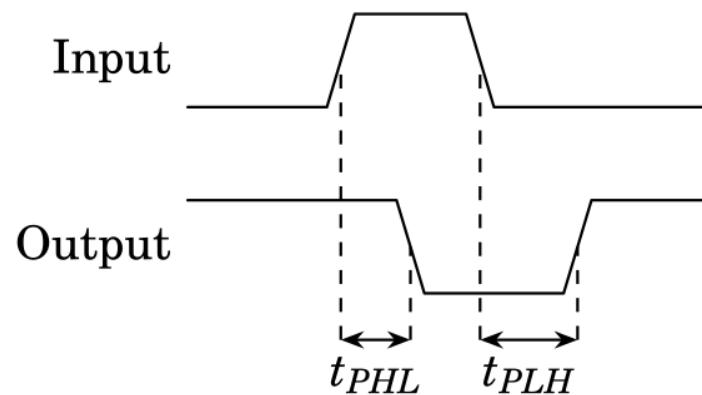
*Analysis: propagation delay, rising time & falling time, quiescent power and dynamic power of the NAND

Build another testbench. Input waveform as below.



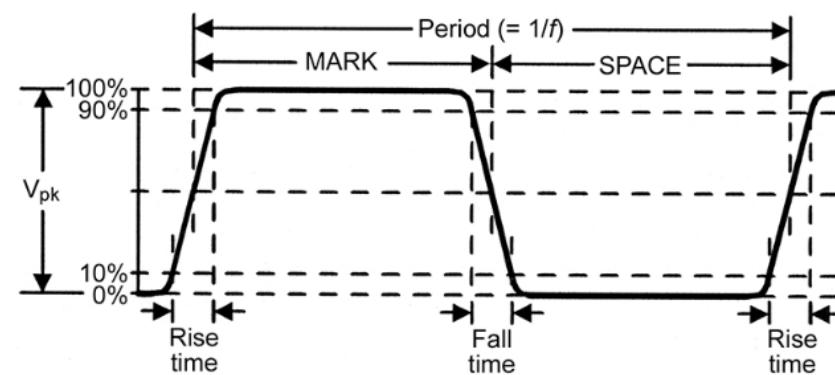
Assignment 1 – Schematic & Layout design

Analysis: propagation delay, rising time & falling time of the NAND



propagation delay

https://en.wikipedia.org/wiki/Signal_propagation_delay



rising time & falling time

https://www.nutsvolts.com/magazine/article/understanding_digital_logic_ics_part_1

Assignment 1 – Schematic & Layout design

- **1-2: Layout**

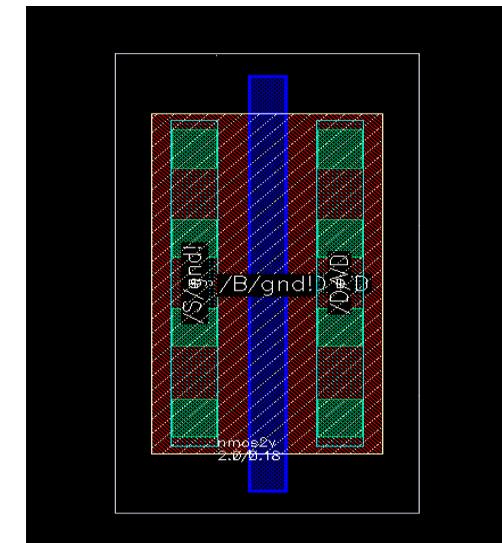
- *Finish the layout of your NAND

- Calibre Setup
 - Import your components
 - Draw with metal layers

- *Refer to layout rules at the end of the guide

- Metal width
 - Spacing, etc

- *Verify with DRC tool



Full descriptions on Brightspace: (Assignments>EE4610_Assignments_Guide_2025.pdf)

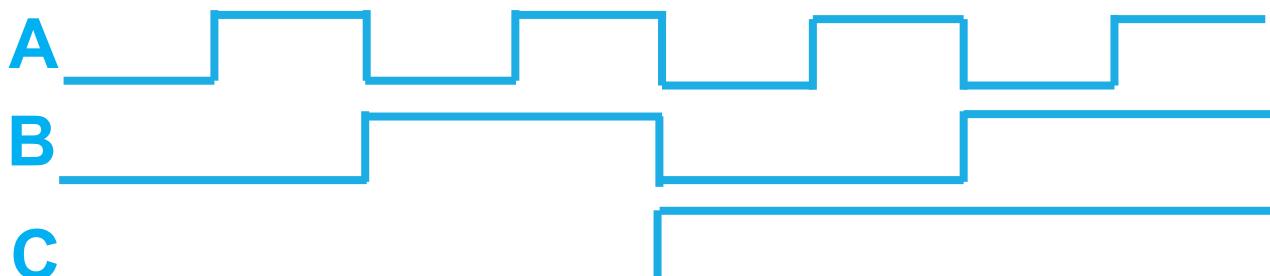
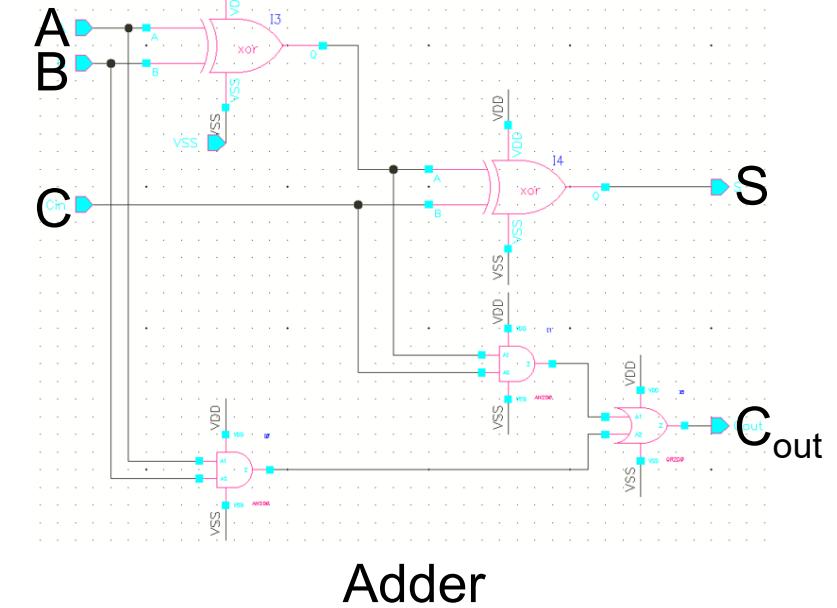
Assignment 2 – Schematic Design

- Design a full Adder
- On the right is an example. You can use another topology to build a full adder.
- Design from the transistor level and build your own gates as symbols (e.g. AND, OR, XOR)
- More detailed technical requirements referred to EE4610_Assignment_Guide_2025 (Section 2.1)
- **Step (1): Verify the function of the adder.**

Build a testbench to prove the circuit works as a full adder correctly.

Here's an example of input signals. And you check the output S & C_{OUT} .

Put screenshot of input/output signals' waveform on your report.



Assignment 2 – Schematic Design

- Step (2) Simulate some parameters**

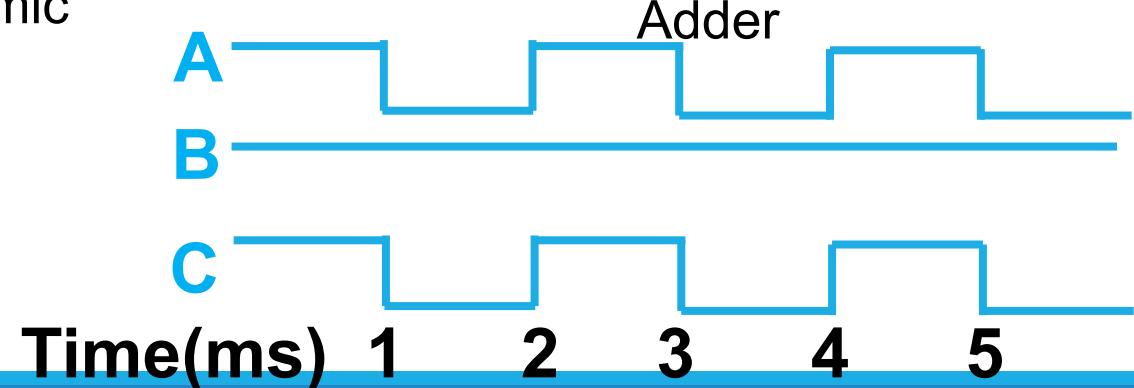
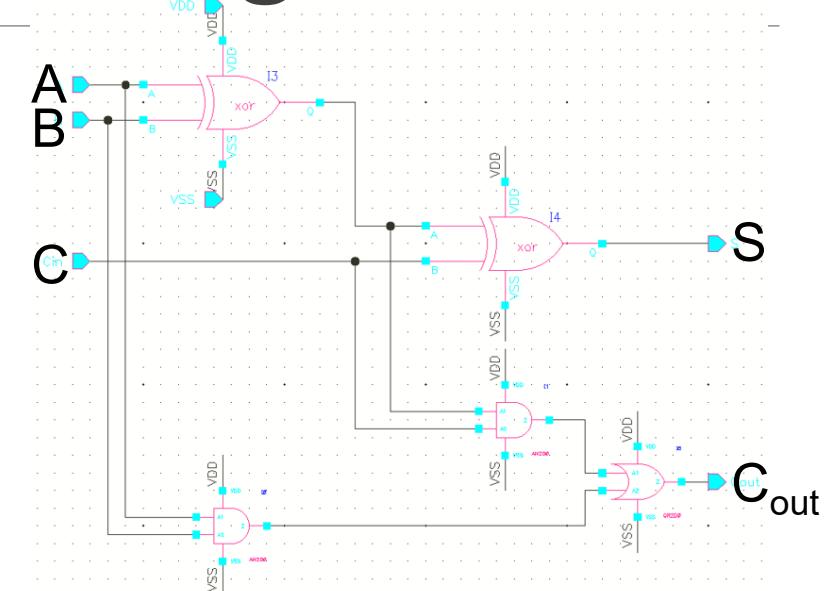
Build another testbench with the input waveform on the right side:

*inputs: A=101010..., B=111111..., C=101010...

(rising/falling edge 100ps, period 2ms, pulse width 1ms)

*Analysis: propagation delay, rising time

& falling time, quiescent power and dynamic power of the adder



Assignment Submission

- Needs to be completed
- Work in teams of **3** (Collaboration-> Groups-> Categories-> Select Cadence Assignment -> Choose Group)
- Submit the report to Brightspace when you are done

(Examples: *Report_Example_Schematic.pdf*; *Report_Example_Layout.pdf*)

- Ask TAs on Brightspace when you are stuck
- Submission date
 - Assignment 1 (report 1)– **Dec 19th**
 - Assignment 2 (report 2)– **Jan 12th**

Access to the server

- **Enroll** in Brightspace (if not done) to get access to the design environment + to make groups.
Deadline 19th, Nov, Wednesday 13:00 PM.
- Accessing the server: refer to ***EE4610_Instruction_Manual_2025*** on Brightspace
- From Linux:
 - Use this command in the terminal : 'ssh -X <netid>@ee4610.ewi.tudelft.nl'
 - The '-X' parameter is optional, but mandatory if you want to use graphical interfaces
 - The password should be the same as the one you use for e.g. Brightspace (NetID)
- From Windows:
 - Download MobaXterm (<https://mobaxterm.mobatek.net/>)
 - Perform the same steps listed for Linux

Please note that you have to use the TU Delft VPN if you are not on the TU network to access the server. (<https://www.tudelft.nl/en/student/ict/help/vpn-openvpn/>) Cadence might feel slow due to a slow internet connection.

Document References-Assignment Session

- Accessing the server: EE4610_Instruction_Manual_2025
 - Assignments Instruction: EE4610_Assignment_Guide_2025
 - Assignments Instruction Slides: EE4610_Assignment_Slides_2025
 - Submission Report Example: Report_Example_Schematic; Report_Example_Layout
 - Login Cadence Short Video: LoginYourServer
- ❖ TA Session 1 (onsite): Dec 10th, 11:30-12:30am
- ❖ TA Session 2 (onsite): Jan 7th , 11:30-12:30am

Thanks!

Any questions?