Assignment 1

DIGITAL IC DESIGN I

EE4610

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Contents

Introduction

The last three digits of the student numbers are 6, 7, and 9. Hence, the widths of the PMOS and the NMOS should be as follows:

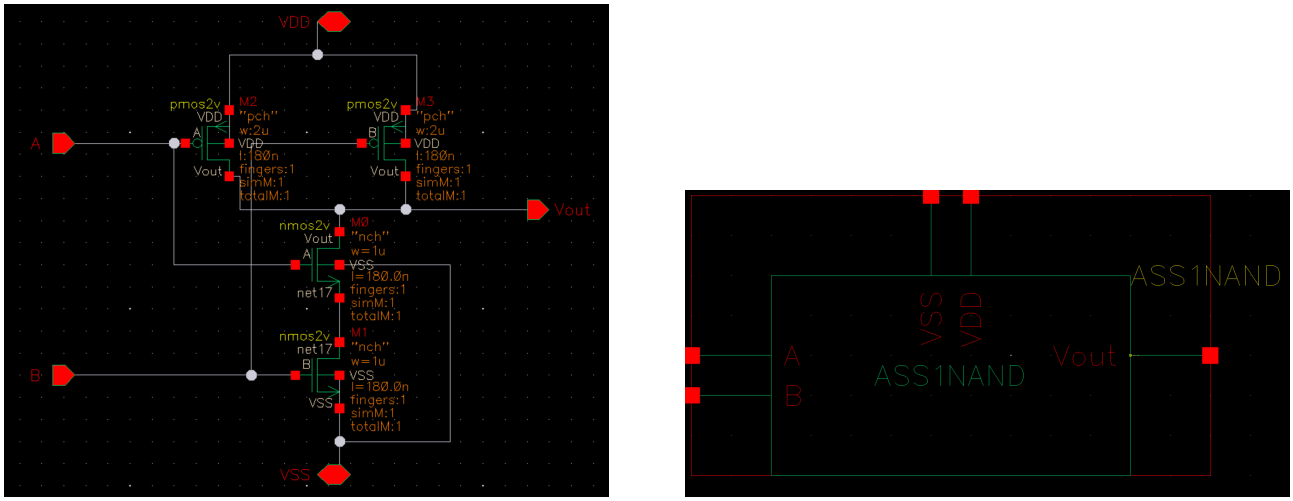
$$W_p = (9 + 6 + 7) \bmod 3 + 1 = 2\,[\mu m]\,, W_n = 0.5W_p = 1\,[\mu m] \tag{1}$$

1 Schematic

1.1 Details of the NAND:

PMOS: width=$2\,\mu$m; length=180 nm ; NMOS: width=$1\,\mu$m; length=180 nm

1.2 Schematic design about our NAND and symbol:



(a) Schematic of NAND

(b) Symbol of NAND

Figure 1: Propagation delay calculation settings

1.3 Test-bench design:

We add a capacitor after the 'Vout' to suppressing high-frequency spikes.

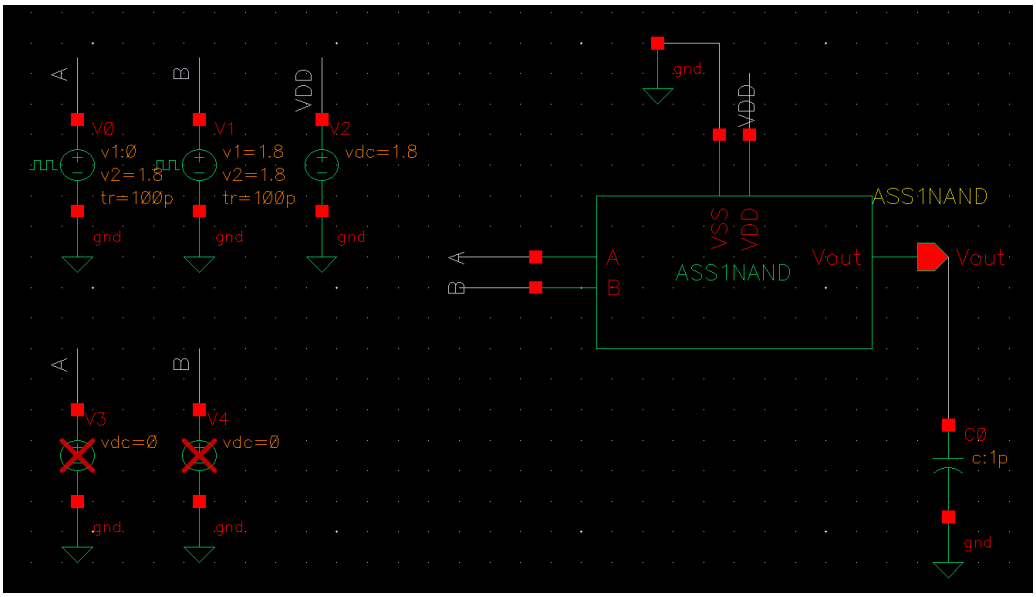


Figure 2: Test-bench design

1.4 Input signals and power supply:

(a) Input signal A (b) Input signal B (c) Power supply:VDD

Figure 3: Input signals and power supply settings

1.5 NAND circuit function validation:

To validate the function of our NAND logic circuit.We use ’1010’ as input signal A and ’1100’ as input signal B.The expected output is ’0111’.

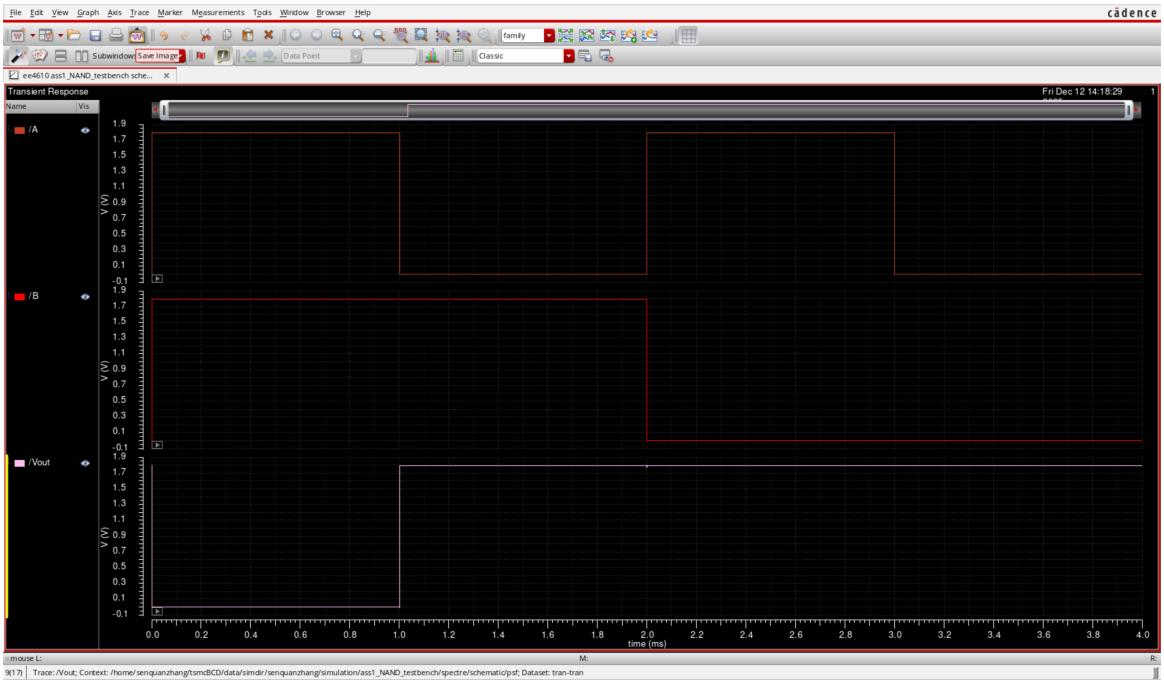


Figure 4: Test-bench design

From the simulation result, we can say that the function of our NAND logic circuit is validated.

1.6 Propagation delay and rising time & falling time analysis:

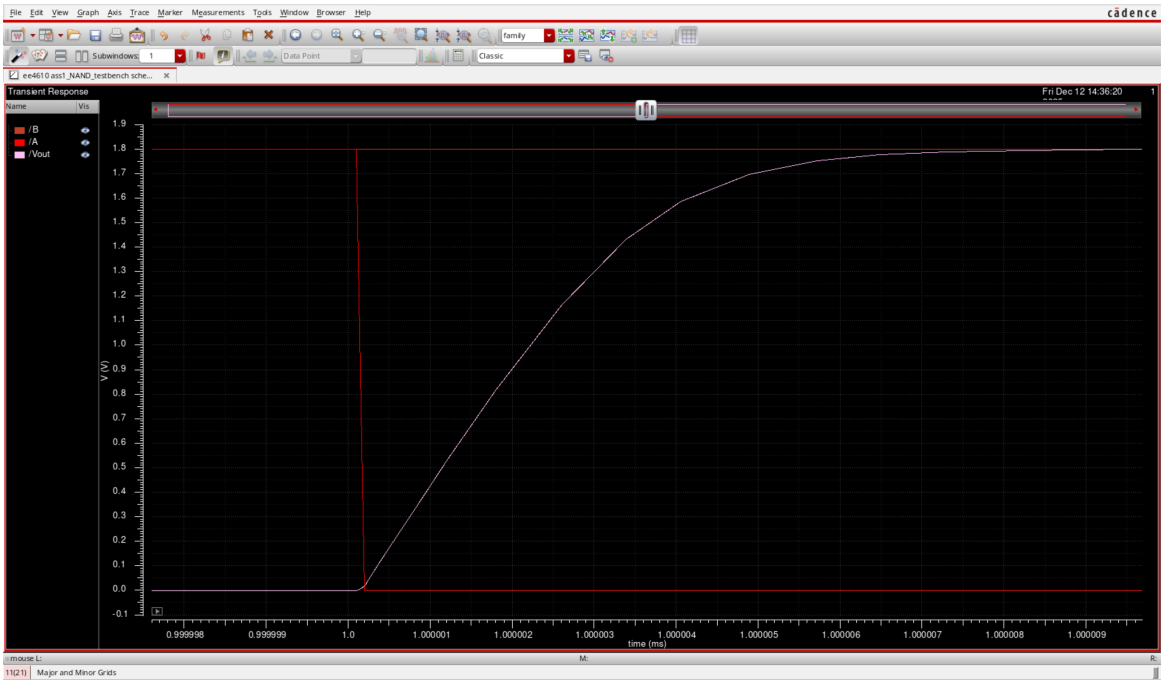
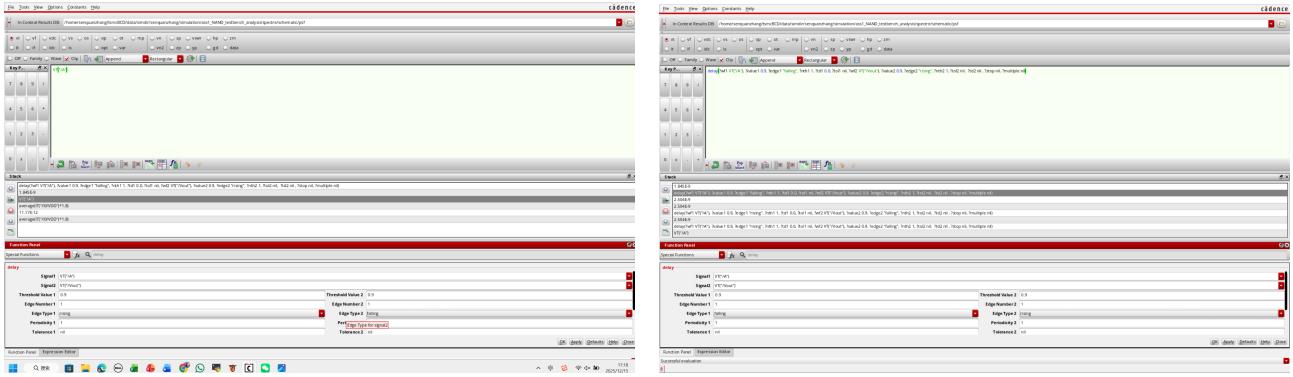


Figure 5: Delay analysis output

From definition, we use $50\%V_{DD} = 0.9V$ as threshold voltage.

$$t_{pHL} = t(V_{out} = 0.5\,V_{DD}) - t(V_{in} = 0.5\,V_{DD})$$
$$t_{pLH} = t(V_{out} = 0.5\,V_{DD}) - t(V_{in} = 0.5\,V_{DD})$$

To analysis 't_{pHL}' and 't_{pLH}',we used the 'calculator' tool in the 'ADE L' simulation.We set the 'function' with 'delay' as showed in following figures.



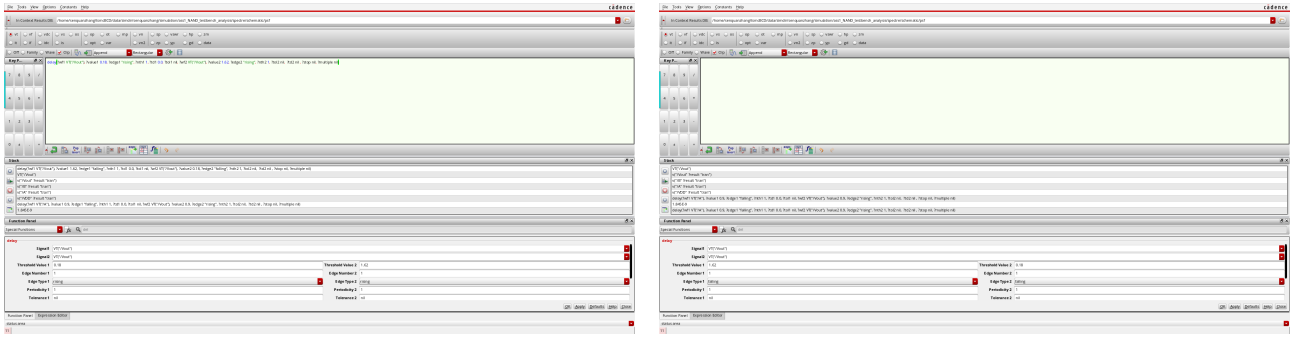
(a) t_{pHL} calculation setting

(b) t_{pLH} calculation setting

Figure 6: Propagation delay calculation settings

We also used the same way to analysis the rising time & falling time. But in rising time & falling time analysis, the threshold voltages are $10\%V_{DD} = 0.18V$ and $90\%V_{DD} = 1.62V$.

$$t_r = t(V_{out} = 0.9\,V_{DD}) - t(V_{out} = 0.1\,V_{DD})$$
$$t_f = t(V_{out} = 0.1\,V_{DD}) - t(V_{out} = 0.9\,V_{DD})$$



(a) Rising time calculation setting

(b) Falling time calculation setting

Figure 7: Propagation delay calculation settings

The result of the simulation is:

Analyses

	Type	Enable	Arguments
1	tran	☑	0 3m moderate

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	☐	allv
2	B		☑	☐	allv
3	Vout		☑	☐	allv
4	tplh	1.84479n	☑	☐	
5	tphl	2.50449n	☑	☐	
6	rising_time	3.80295n	☑	☐	
7	falling_time	4.83167n	☑	☐	

Figure 8: Propagation time and rising time & falling time simulation result)

Then the propagation delay is:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} = 2.17464ns$$

To conclude the delay analysis result is:

Item	Value
t_p	2.17464 ns
t_r	3.80295 ns
t_f	4.83167 ns

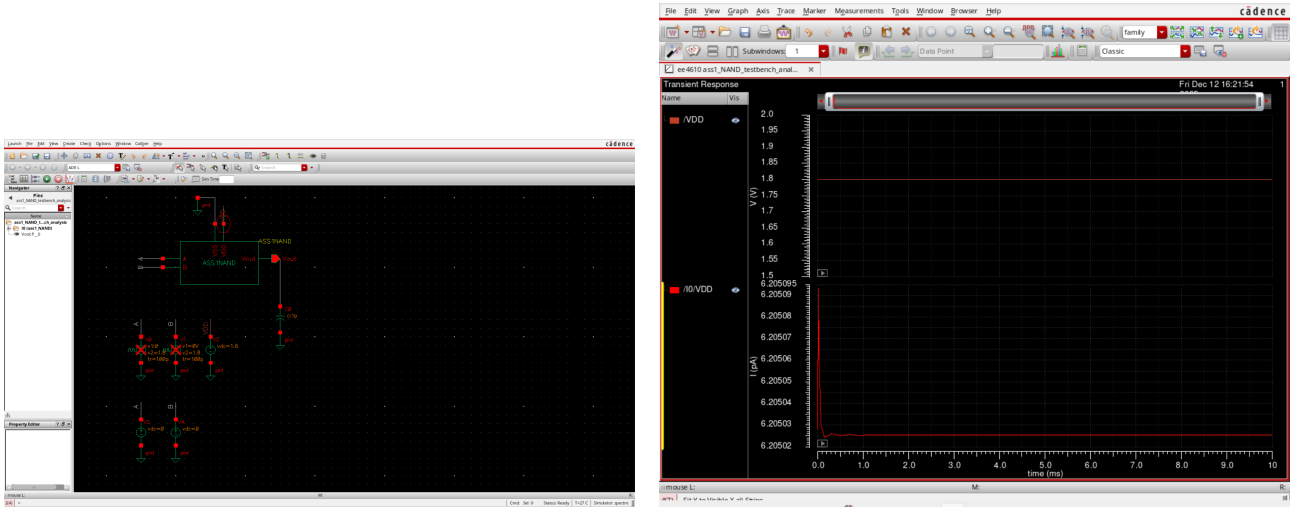
Table 1: Delay analysis results.

1.7 Power analysis:

1.7.1 Quiescent power:

$$P_q = average(p(t)) = average(V \times I)$$

Quiescent power of our circuit is 11.169 pW:



(a) Quiescent power schematic

(b) Quiescent power output curve

Figure 9: Input signals and power supply settings

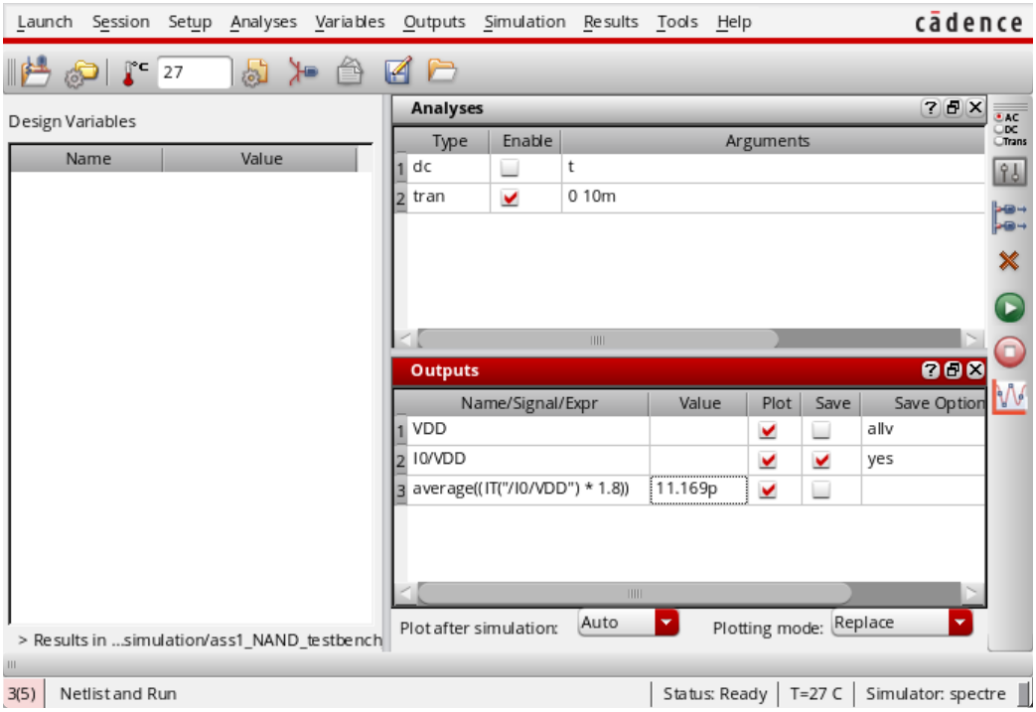


Figure 10: Quiescent power simulation result

1.7.2 Dynamic power:

$$P_{\text{dyn}} = V_{\text{DD}}(I_{\text{avg,switch}} - I_{\text{avg,static}})$$

In dynamic power analysis the test-bench is changed back to Figure 2

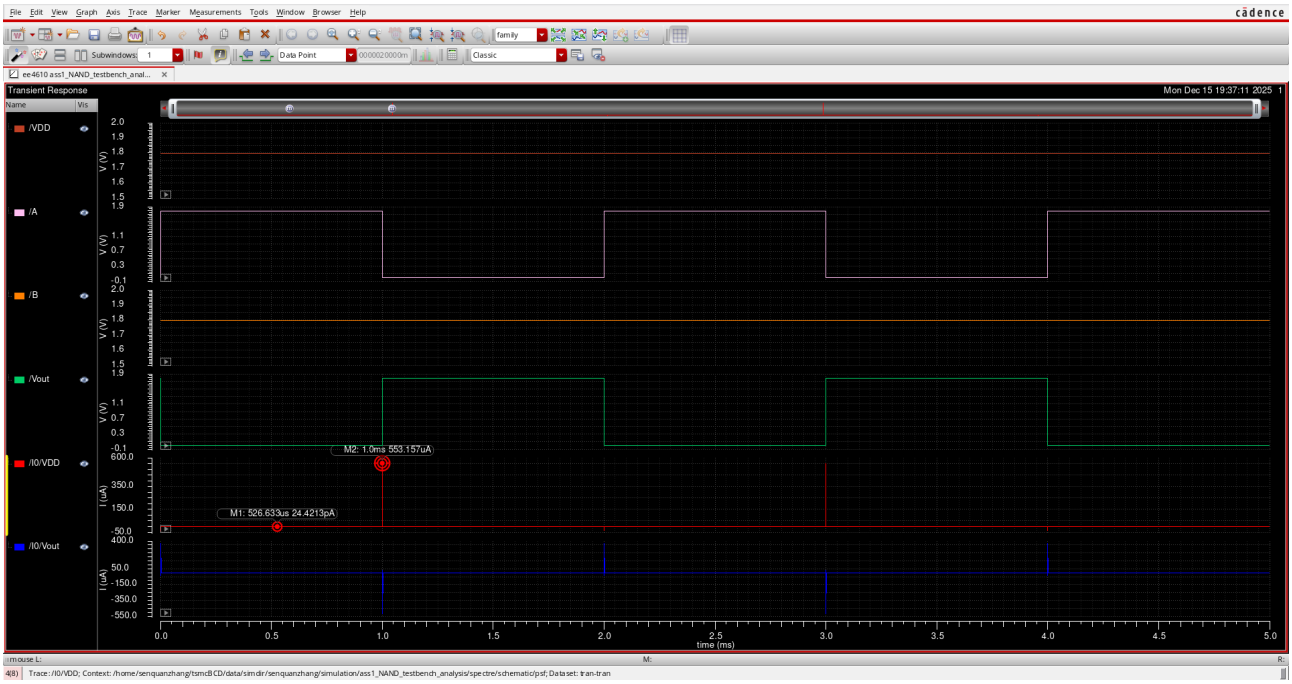


Figure 11: Dynamic power output curve

$$I_{\text{avg,switch}} = 553.157\mu A$$

$$I_{\text{avg,static}} = 24.4213pA$$

$$P_{\text{dyn}} = V_{\text{DD}}(I_{\text{avg,switch}} - I_{\text{avg,static}}) = 0.996 \times 10^{-4}W$$

2 Layout

2.1 Details of the POMS and NMOs

PMOS: width: 2 um, length 0.18 um.
NMOS: width: 1 um, length 0.18 um.
The value of width was calculated by the given formula in the assignment guide. Moreover, the length is the minimum length (0.18 um) given by the assignment slides.

2.2 Schematic

The schematic is labeled differently but the architecture of the NAND gate and bias voltage are the the same as the first section. The schematic can be found in Fig.12.

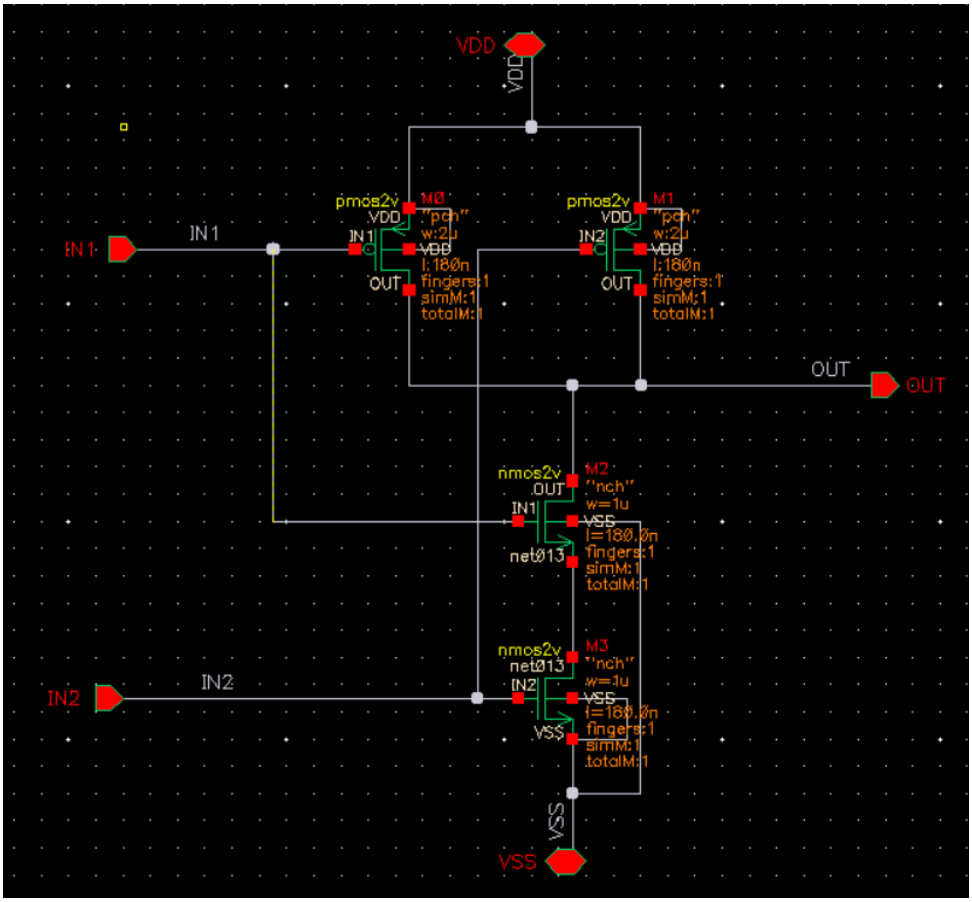


Figure 12: Schematic of NAND used by the layout

3 Layout

The layout with highlighted size can be found in Fig.13.

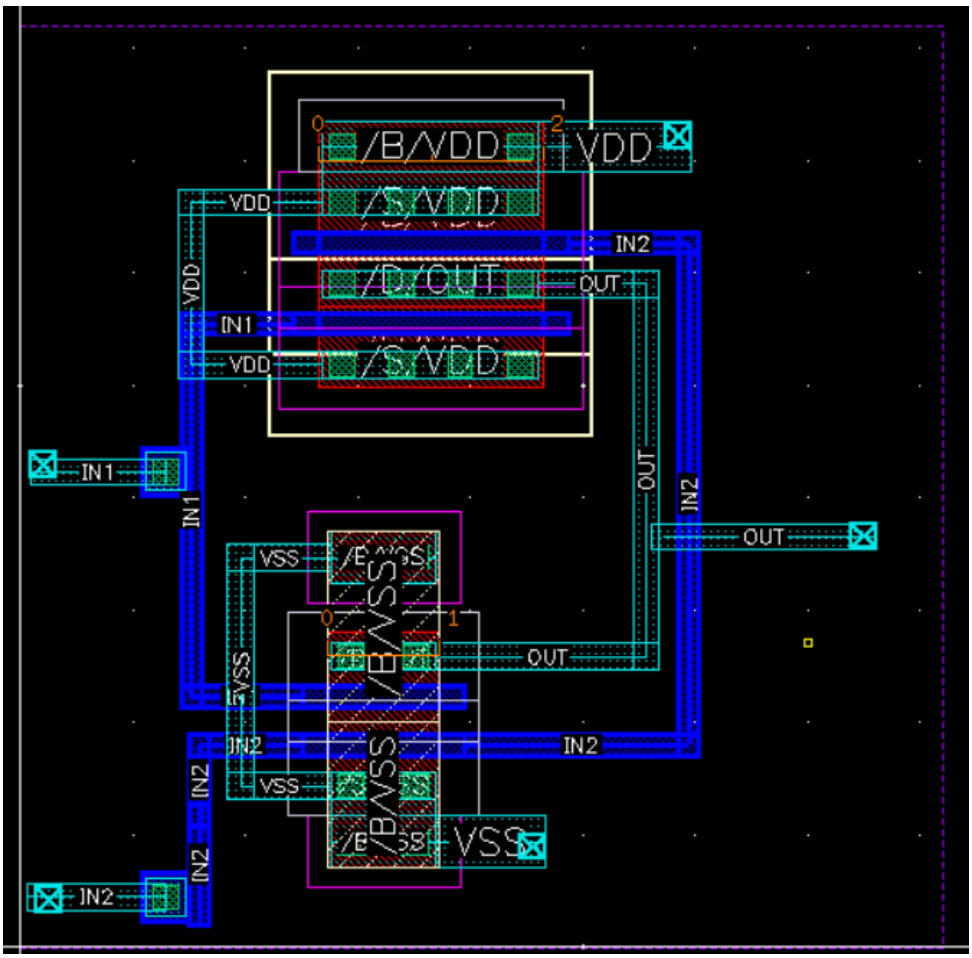


Figure 13: Layout with labeled width

3.1 DRC errors

The DRC errors can be found in Fig.14.

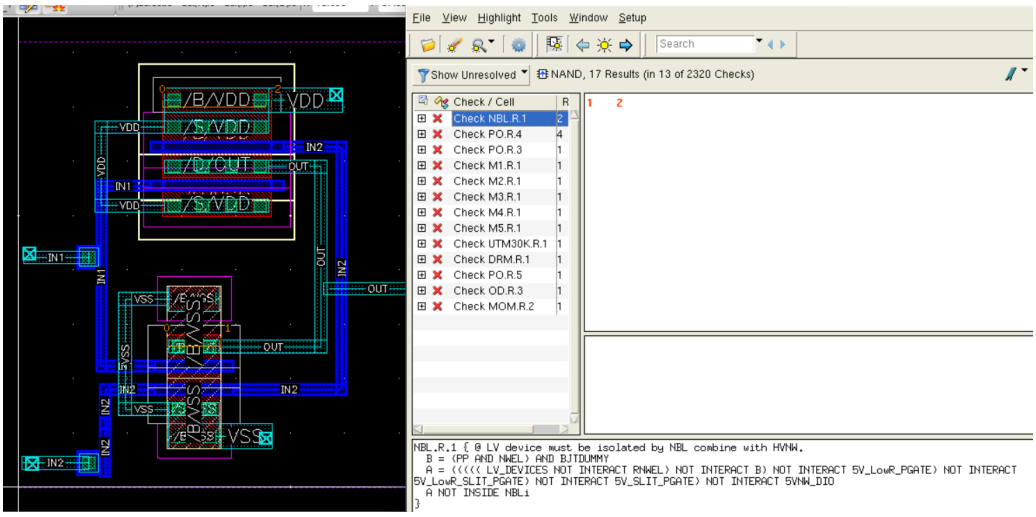


Figure 14: DRC errors of the layout