

EE4610 Digital IC I – Assignments

Schematic Design and Layout in Cadence

Last revised November 2025

This document is a guide for the practical assignments of EE4610 Digital IC Design. The inverter in the pre-exercise is used as an example to show the workflow. While Sections 2.1 and 3.1 are requirements to assignments, you are also welcome to follow in the pre-exercise.

You are allowed to work in three people for the assignments. The assignments are mandatory and must be checked by the teaching assistant during the scheduled sessions.

Refer to the introductory slides for the assignments on Brightspace for more information.

We cover the basic steps of using the Cadence integrated circuit design tool. Some exercises are beneficial to gain a deeper insight into the fabrication process. This document is supposed to be a general overview of the tool for beginners who have not designed any layout before.

In short, two assignments are to be completed:

1. Schematic Design Simulation and Layout Design: NAND Gate, finishing the analysis of propagation delay, rising time falling time, quiescent power, dynamic power of the NAND.
2. Schematic Design of an Adder: finishing the analysis of propagation delay, rising time falling time, quiescent power, dynamic power of the adder.

Good luck and enjoy!

Note: any feedback/comments on the assignment instructions is much appreciated.

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1 | Cadence Usage

We access the Cadence design tool from a remote server, namely ee4610.ewi.tudelft.nl. Refer to the introductory slides for more information. Most students will connect over SSH using MobaXterm.

1.1 Setting Up Cadence

Once your server access has been granted (this will be arranged some days after the groups have enrolled), you can start on the assignments. Please refer to Instruction Manual on brightspace to log in your cadence account.

You can used these commands for your convenience to change your working directory:

Navigation- if you want open a file: cd <file name>

» cd

List of everything-

» ls

Go back-

» cd..

Go into the root-

» cd /

Delete-

» rm

Copy-

» cp

New file-

» mkdir

Delete inside files-

» rm -r

Print work directory-

» pwd

1.2 Local Cadence details

The software and the PDK should be running on each machine where /opt/cad and /data/cad are mounted. If you are interested, you can look around for all kinds of Cadence or PDK documentation by navigating close to the filepaths:

» /opt/ei/DK/tsmc/oa180/mini018BCDG2/216A/PDK_doc/

/opt/cad/DesignKits/cadence/tsmc/tsmc0.18/PDK_doc/

Note: In the following contents, an inverter is given as the example. There are two parts mainly: schematic (Section 2) and layout (Section 3). This manual will guide you through how to get familiar with Cadence basic operation. Please follow the similar process for your assignments. Detailed requirements of the assignments are given in the slides on Brightspace.

2 | Schematic Design and Simulation

2.1 Technical Requirements of Assignments

For this assignment you are required to design a NAND, and observe the characteristics using 'tran' in ADE simulator. For detailed requirements, please check the slides on Brightspace.

Requirements:

- Libraries you can use: tsmc18, analogLib.
- Mosfet Devices: "pmos2V", "nmos2V" in tsmc18.
- (Only for Assignment I) PMOS Width: $[(a+b+c) \bmod 3] + 1$ (unit: μm). If you have no partner, use the last number of your ID.
<For example: your ID: 123456, your partners' ID: 756432 & 124654, the used width for the PMOS is $\bmod[(6+2+4)/3]+1=1\mu m$. The width for the NMOS is 0.5 times the width of PMOS.
- Length: minimum length.
- Generate symbol
- Make a test-bench and observe the output signal

Submit your work to Brightspace which should includes

- Schematic + symbol + description
- Test-Bench + input/output should be clear
- Simulation results and analysis (analysis: propagation delay, rising time falling time, quiescent power and dynamic power of the NAND.)

2.2 Design Process

2.2.1 Library And Schematic Creation

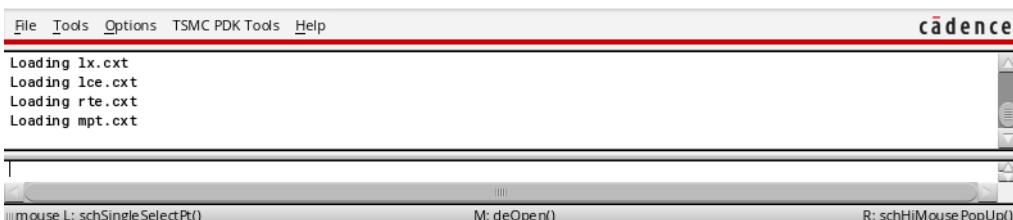


Figure 1: Virtuoso

Step1: Create your own library. When you start the Virtuoso, Fig. 1 will pop out.

- Create your own library by clicking *File > New > Library* in Fig. 1. For example, here "ee4610" is the name of the new library in Fig. 2.
- Don't forget to attach design library to an existing technology library. Click "OK".
- Click "tsmc18" as your technology library.

Step2: Create a new cellview for your schematic

- Start *File > New > Cellview*, and give a new name for your schematic, then Fig. 3 will pop out.
- In Fig. 3, you can use the below shortcuts for your editing:

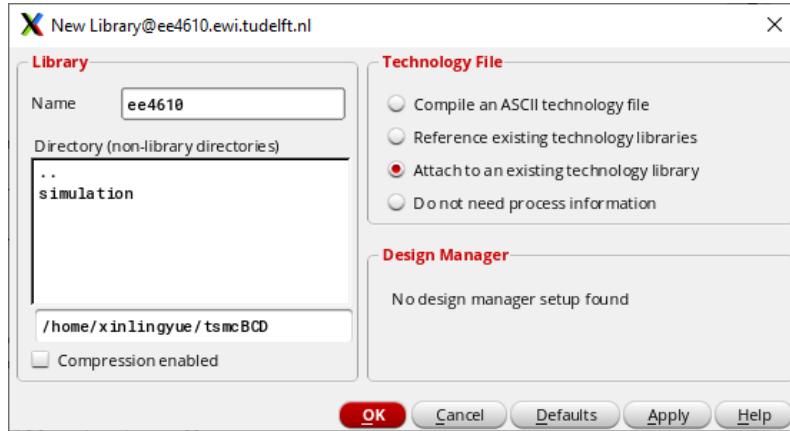


Figure 2: Create your own library

w	Create a wire	m	Move
i	Add instance	s	Stretch
f	Fit the whole design on the screen	c	Copy
l	Add lable for wire	p	Add pin
q	Show properties	SHIFT+z	Zoom out
f	Fit the whole design on the screen	CTRL+z	Zoom in

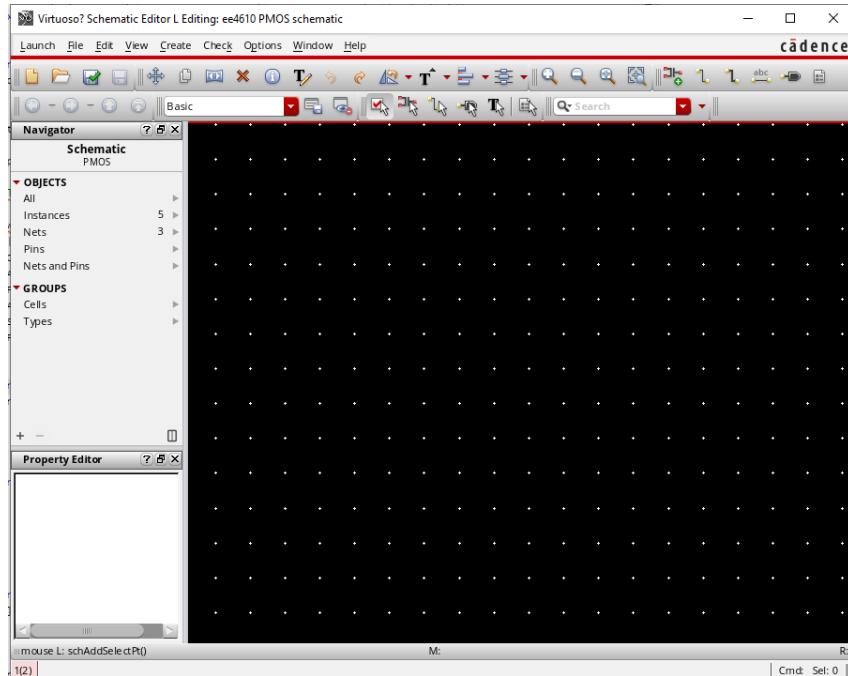


Figure 3: New schematic for exercise

Example For instance, here is an inverter as the example for your reference:

- Firstly, add an instance from tsmc18 library: press "i" in Fig. 3 and click "Browse" in Fig. 4.
- Select the instance from Fig. 5. Press "Enter" and the PMOS (Fig. 6) is displayed in your schematic.

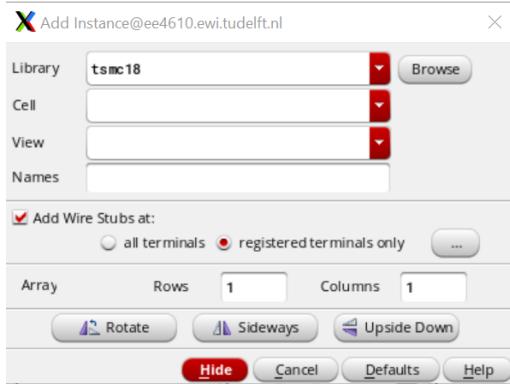


Figure 4: Add instance from tsmc18

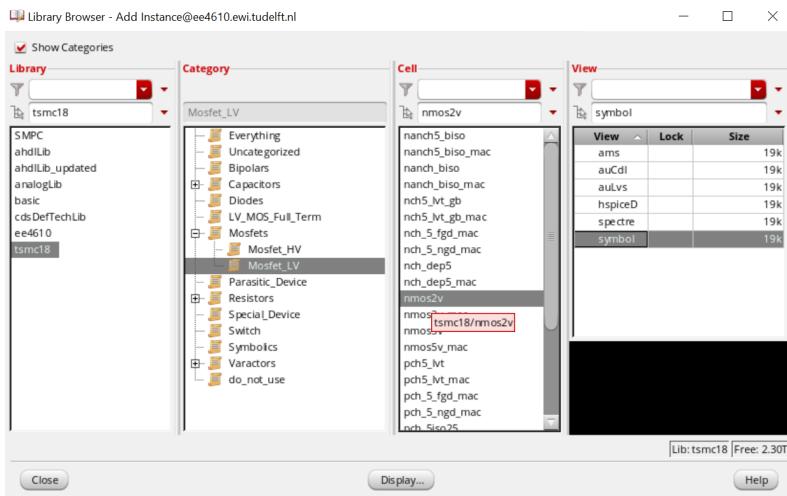


Figure 5: Add instance

By using the similar way, adding NMOS to the cellview, the inverter is completed as is shown in Fig. 7, where the wire label 'VDD' and 'VSS' can be added by pressing 'l'.

- When you left click on the instance, you can change the property of the instance by pressing "q".

2.2.2 Generate Symbol

After you finish the design, according to the input/output signals, you can create pins and generate a symbol for more convenience. Next time, you can use your design by adding symbol directly.

- Define and add "input/output" pins by pressing "p" in Fig. 8.
- Click *Create > Cellview > FromCellview*, and click "OK" in the next two popped out windows. Finally, you will see Fig. 9. You can change the shape and name of the symbol by using previous introduced editing commands.

2.2.3 Make a Test-Bench

- When you are done the symbol, you need to create a new Cellview file for the test-bench. Repeat the Step2 in Section 2.2.1.
- Press "i", choose your built library and find the symbol you already finished.

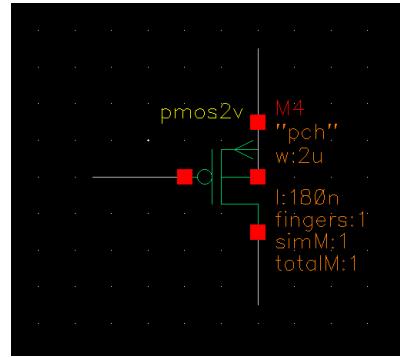


Figure 6: Schematic example

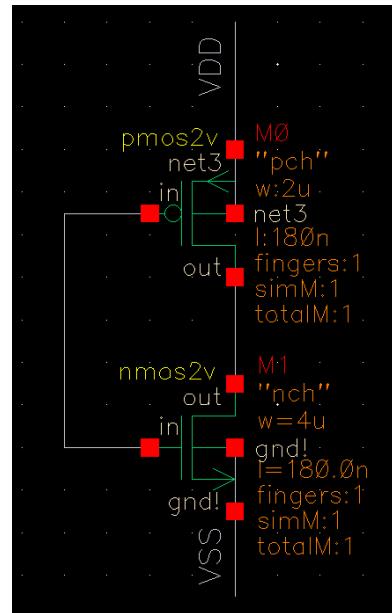


Figure 7: Schematic of an inverter example

- Enter "i", choose some ideal power supply from "analogLib" to test your design. Set your power supply according to the assignments' requirement.
- If you want to open your schematic, click on the symbol and press "Shift+e", then you can go into your symbol and edit the schematic without open a new window.

2.2.4 ADE Simulation Setup

The next step is to set your simulation environment. In this assignment, you are required to use transient simulation. Feel free to play other types of simulations if you like.

- Start *Launch < ADEL*, and click the button in Fig. 11 to choose simulation type. In assignment 1, please select the first one "tran". Set the time and click 'conservative'.
- Follow Fig. 12 to select the signal that you would like to observe by clicking "From Design". Then click the signal in schematic. These selected signals will appear in the simulation window.

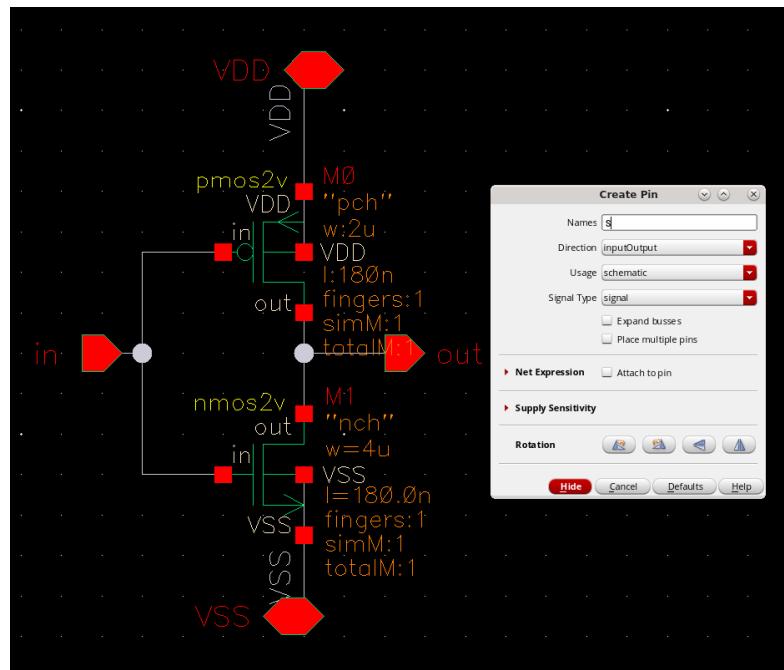


Figure 8: Add Pin

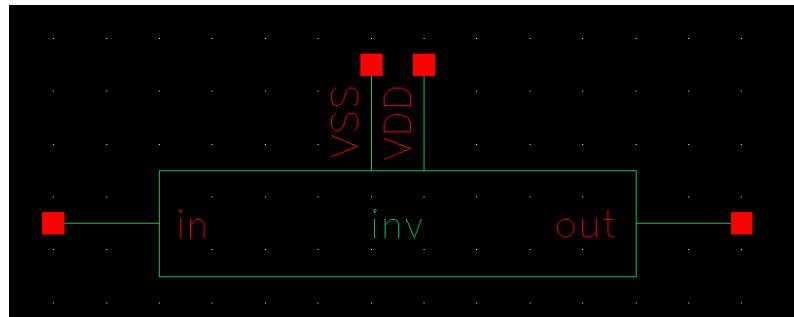


Figure 9: Create symbol

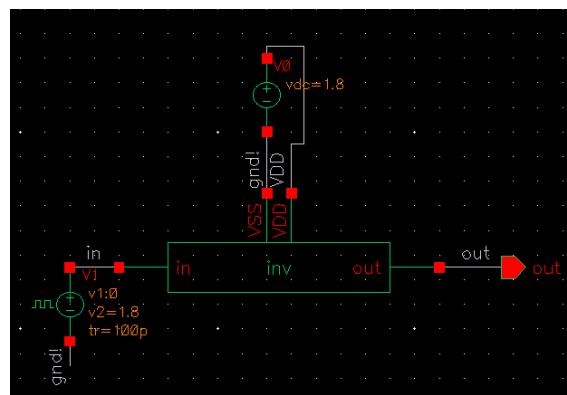


Figure 10: Test-bench

- Finally, click green "run" button, and Fig. 13 will pop out. You can observe your outputs in Fig. 13.

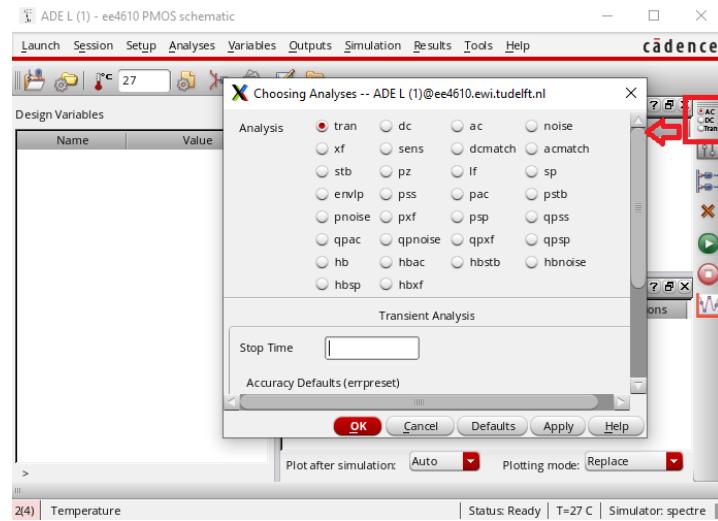


Figure 11: Simulation setup 1

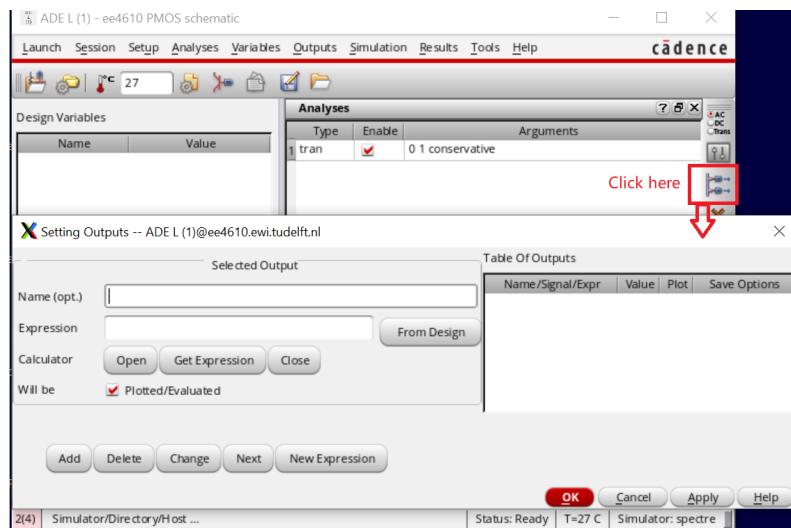


Figure 12: Simulation setup 2

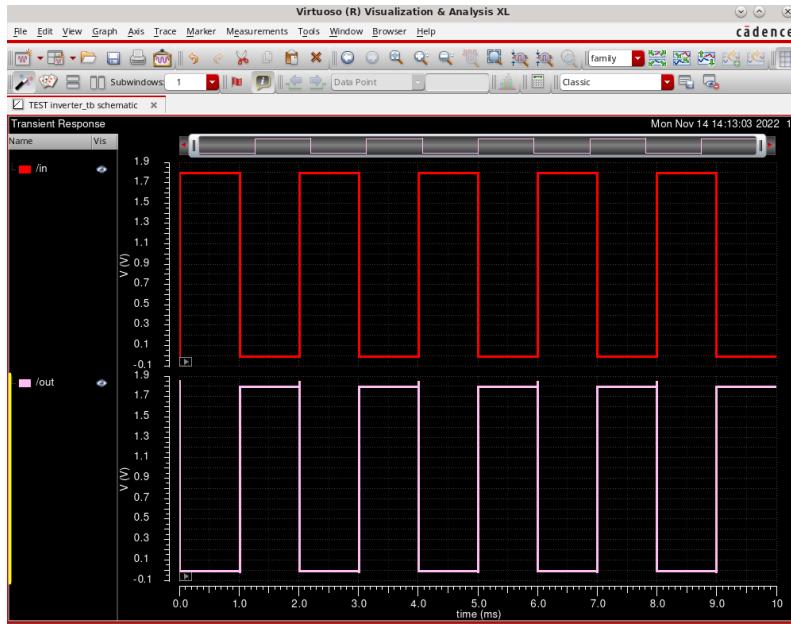


Figure 13: Simulation window

3 | Layout

3.1 Technical Requirements of Assignment 1 Layout

For the second part of your assignment-1 you should perform three parts:

- Calibre Setup;
- Get familiar with layout rules
- DRC-free as possible.

Be aware that this part generally takes more time to complete compared to the first part as we will exercise the most prominent steps in a regular circuit (chip) design cycle, for the first time. In the following subsections, we will guide you through the process in Cadence.

Take screenshots and notes during the process so that the TA can verify that you completed your work. The submission should including these:

- Imported components: use ruler (press "k") to highlight the sizes of the PMOS/NMOS
- Metal/poly wire drawing for correct connection
- Setup process
- DRC clean window

3.2 Layout Guidance

In the following contents, an example of designing the layout of an inverter is presented. For your assignment, you should follows the similar steps.

3.2.1 Start a New Layout

Step1: Start a new layout window

- Open your designed schematic cellview (not test-bench or symbol) and start *Launch > LayoutXL*, then the layout window is presented as in Fig. 14.

Note: Check whether the left layers are all presented to confirm that you have attached to the correct technology.

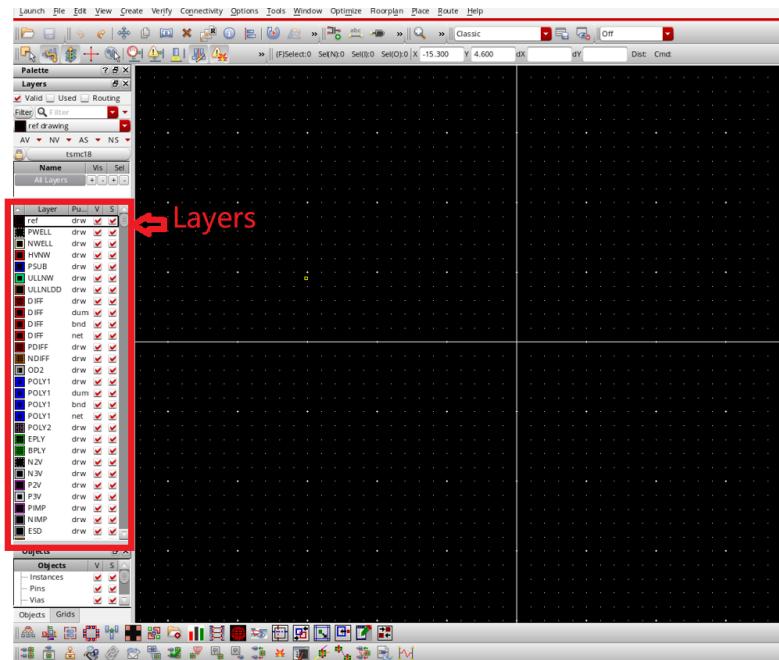


Figure 14: Layout window

Step2: Layout Settings

- The first thing you should do after starting the layout is to fix the grid sizing. Go to *Options > Display*, or press the "E" key which is the shortcut for that, and the options window (Fig 15) will pop up. The X/Y Snap Spacing parameter is a foundry limitation resulted from the ability to place masks on the wafer, if you make a smaller grid, probably when you check DRC of the layout you will find lots of errors about '*offgrid*', if you don't correct this errors the foundry will refuse your fabrication order. The base unit of length in Virtuoso is 1um. The default value of 0.005 (5nm) is fine. Later you may want to adjust the grid spacing as well to help you design layout for our technology. Click "OK" to save your changes or just keep the defaults.

Step3: Import your components

- Click *Connectivity < Update < ComponentsAndNets* to import all designed components. You can used the default settings as shown in Fig. 16. Click "OK".

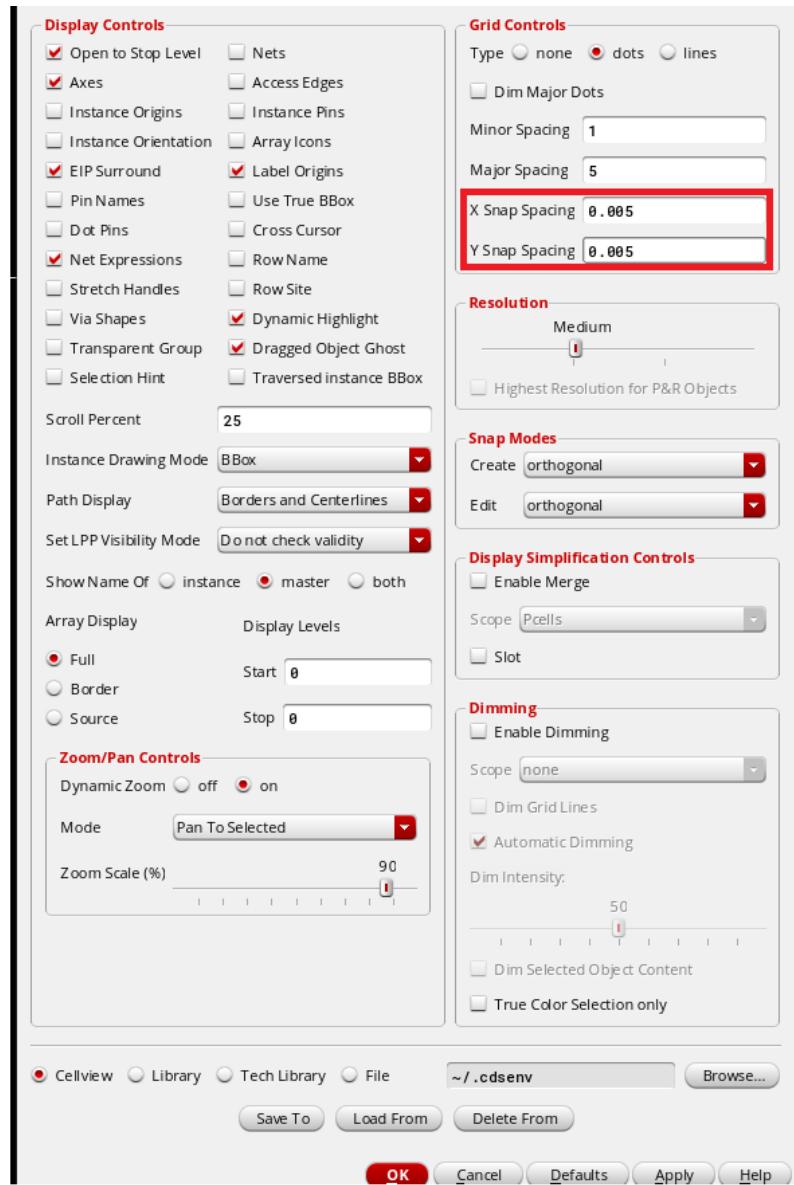


Figure 15: Settings for layout window

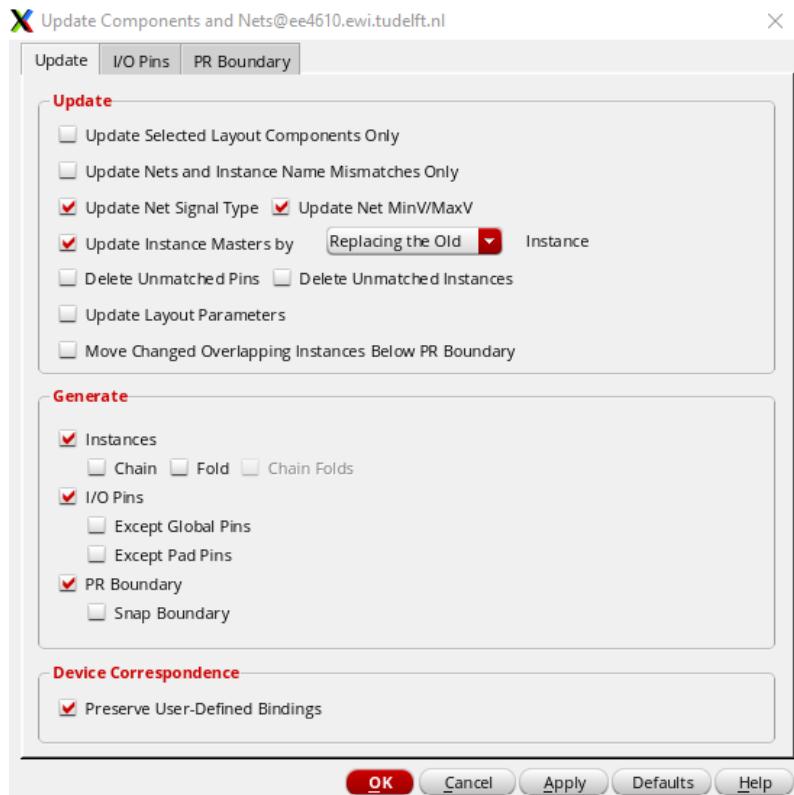


Figure 16: Component import

After import your components, the NMOS and PMOS models are placed here automatically but it doesn't mean layout design is completed. Supply voltage (vdd) and ground (gnd), substrate, pin etc., need to be added and connected. The source, drain, gate and body pickups should be created and finally, labels need to be added.

Step4: Draw metal layers

- In schematic, we use wire to connect different components. Here in layout, we use different metal layers to do the connection.
- Please note that if you connect different layers, you must add corresponding via. This is not required in this assignment, but it is very important for your LVS check.
- The short-cut keys listed below will help you work faster.

Take "r" as a case, before you draw any layer, you should select corresponding layer from the LSW palette window, click it then move the cursor to Virtuoso Layout Editing window to left-click so as to activate it. Press "I" on the keyboard or click the icon for *Rectangle*, sequentially left-click and drag the mouse pointer to define the range. After drawing, do remember to press **Esc** to exit this mode. Detailed explanations for these commands are listed below.

In Fig. 18, you will find the finished layout example.

Edit menu commands

- Rectangle: Create a rectangle of the selected layer in the LSW.
- Move: Click on any object and move it around in the layout.

- Stretch: Click on the edge of a rectangle and size it. Be careful during using it, make sure no object is selected; otherwise the selected object in your previous step will be moved unexpectedly.
- Path: Create a path of the selected layer in the LSW. (Double click to end the path).
- Undo: Undo the previous commands.
- Copy: Create a copy of any object in the layout.
- Properties: Change the properties of objects in the layout. Change the layer definitions and the changes are immediately reflected in the layout.
- Instance: Import another existing cell view into this cell view.

Shortcuts

r	Create a Rectangle	m	Move
s	Stretch	p	Create path
u	Undo	c	Copy
k	Ruler	q	Show properties
i	Add instance	SHIFT+z	Zoom out
f	Fit the whole design on the screen	CTRL+z	Zoom in

NOTE: To zoom in/out in the schematic, use the mouse wheel.

Now, click "check and save" to save your design, and then run "Calibre-DRC".

When you are designing layout, the most important thing you should keep in your mind is the set of DRC rules. The design rules are specific for particular manufacturing processes, which set certain geometric and connectivity restrictions to ensure that the design works correctly. If you don't comply with it, you will face errors and warnings after DRC check.

3.3 Design Rule Check (DRC)

3.3.1 Calibre Setup

DRC is available with Cadence distribution which checks most of the rules. The next step following the completion of layout design is to run DRC to ensure the designed layout meets the design rules and therefore can be manufactured. There are two methods to run DRC, one is Assura and the other is Calibre. Calibre will be used in this laboratory session. However, there is no Calibre menu in the Virtuoso Layout Editing window. Please follow the below steps to integrate Calibre to your Virtuoso:

- In order to make it available we need to exit Virtuoso firstly.
- Download "Calibre Setup" from Brightspace. When you open this file, you will find two documents: ".cdsinit" and "sourceme". Copy them to your working directory ("tsmcBCD" in the example) to replace the original existing version.
- Go back to your working directory and next execute "source sourceme" and restart by typing "Virtuoso &".

When you reopen your Virtuoso, you will find "Calibre" appears on the top tool bar which means you have installed it successfully. Fig. 17 shows the integrated Calibre view.

3.3.2 DRC Clean

After add Calibre successfully, you can run DRC.

- Open your layout window, and select *Calibre > RunnmDRC* to invoke the *Calibre Interactive – nmDRC* window. If this is the first time for you to run DRC, click **Cancel** at **Load Runset File** (if

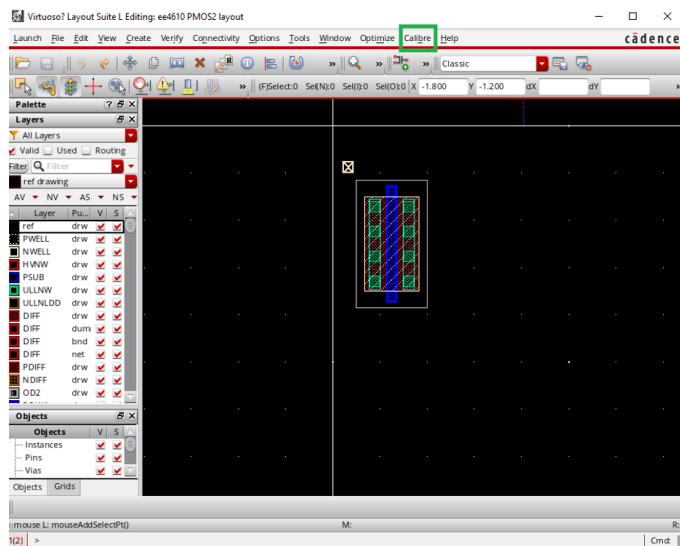


Figure 17: Calibre Interactive

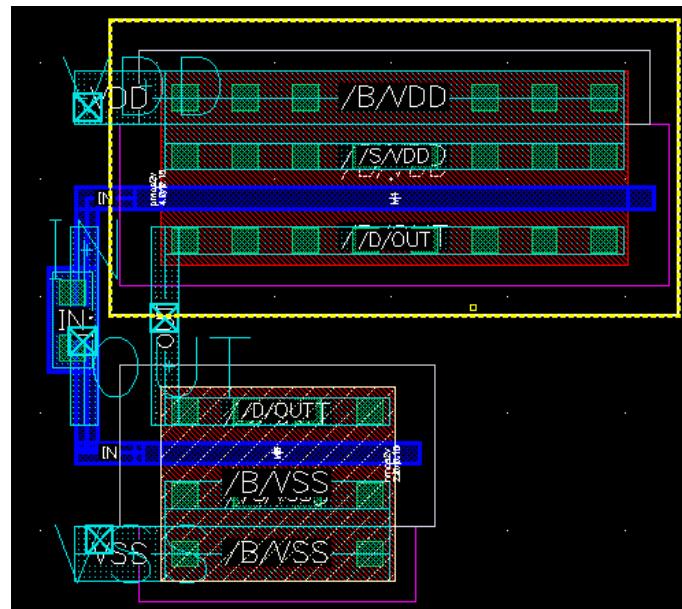


Figure 18: Finished layout example

you saved a runset file before and you want to load it, specify the runset file here).

- Specify *DRC Rule File* and *DRC Run Directory* as shown in Fig. 19 and Fig. 20.
You can define your own run directory to save your DRC results. The DRC Rule File can be found in the local Calibre/DRC directory. The rule file is in:
`/opt/ei/DK/tsmc/oa180/mini018BCDG2/216A/Calibre/drc/calibre.drc`

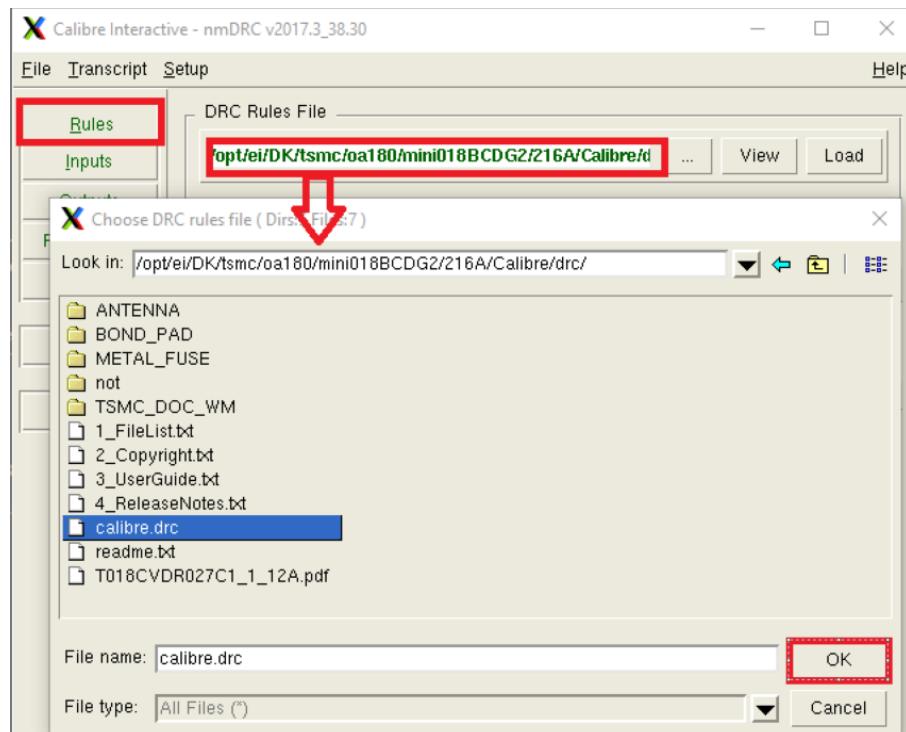


Figure 19: Setup DRC rule

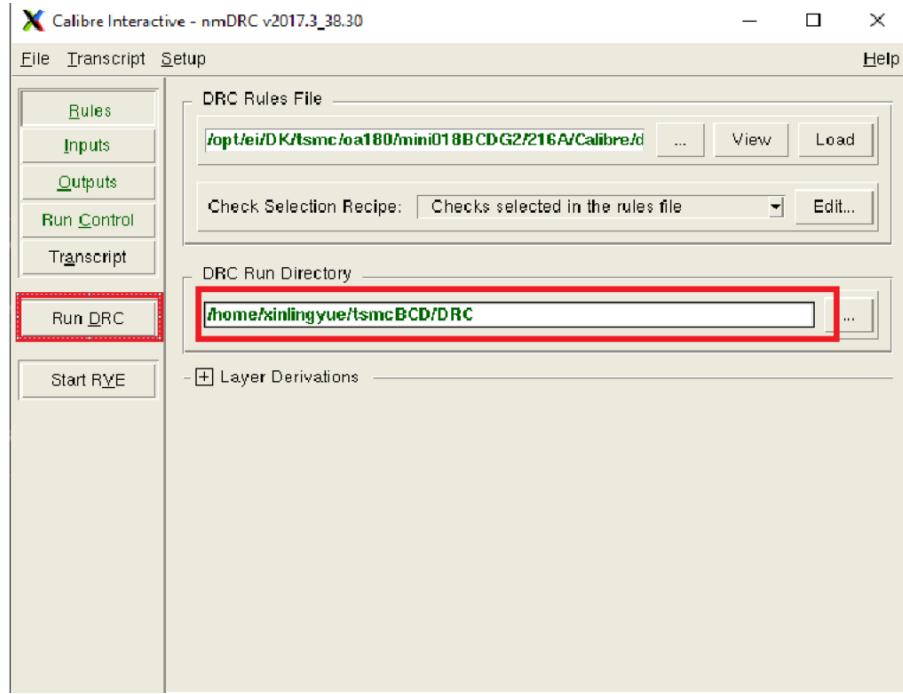


Figure 20: Setup your DRC run directory

- Click **Run DRC** icon on the left of *Calibre Interactive – nmDRC* window. Finally you will have *Calibre – DRC RVE* and *DRC Summary Report* windows with design rule violations as indicated in Fig. 21 and Fig. 22 respectively.
- Correct your layout according to the errors and warnings in *Calibre – DRC RVE window* Fig. 21. Click at the errors to get some information about it at the bottom of *Calibre – DRC RVE* window. At the same time, the location of error will be highlighted in the layout. It should be easy for you to realize what should be modified.
- Repeat correcting layout and running DRC until there is no error shown in *Calibre – DRC RVE* window (Fig.). However, if there are errors belonging to "R" category like:
 - *LV device must be isolated by NBL combine with HVNW*
 - *Min poly area coverage < 14 %*
 - *Minimum density across full chip >=0.14*

you can ignore them until only the errors in Fig. 23 are presented.

The next step would be to run LVS (Layout Versus Schematic) to ensure that the schematic matches the corresponding layout. LVS is not covered in this assignment.

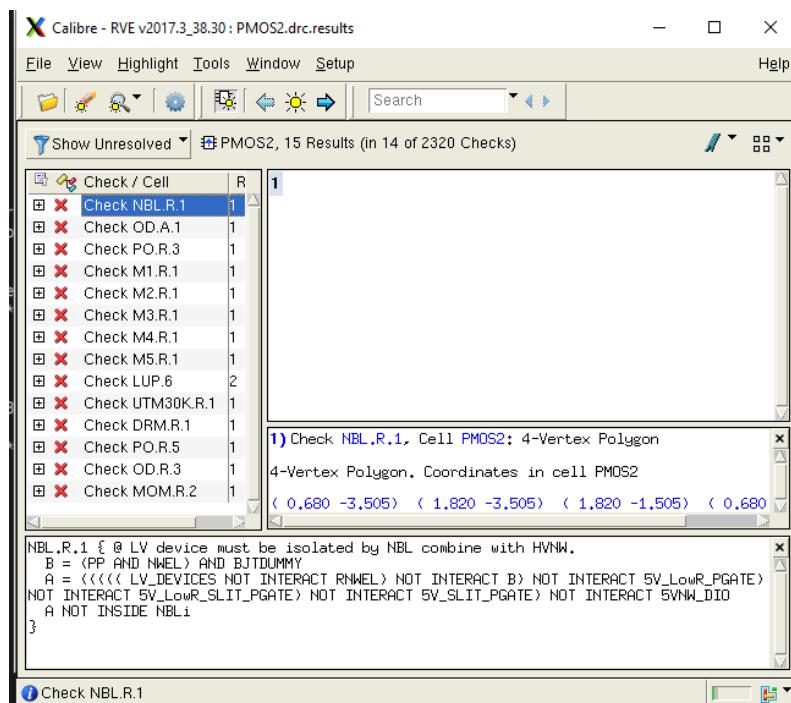


Figure 21: DRC Summary Report 1

DRC Summary Report - PMOS2.drc.summary

```
=====
== CALIBRE:::DRC-H SUMMARY REPORT
=====
Execution Date/Time:      Mon Nov 15 15:33:43 2021
Calibre Version:          v2017.3_38.30   Mon Oct 2 17:38:05 PDT 2017
Rule File Pathname:       /home/xinlingyue/tsmcBCD/DRC/_calibre.drc_
Rule File Title:          -
Layout System:            GDS
Layout Path(s):           PMOS2.calibre.db
Layout Primary Cell:      PMOS2
Current Directory:        /home/xinlingyue/tsmcBCD/DRC
User Name:                xinlingyue
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:  4096
DRC Results Database:    PMOS2.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:     PMOS2.drc.summary (REPLACE)
Geometry Flagging:        ACUTE = YES  SKEW = YES  ANGLED = NO  OFFGRID = YES
                           NONSIMPLE POLYGON = YES  NONSIMPLE PATH = YES
Excluded Cells:          -
CheckText Mapping:        ALL TEXT
Layers:                   MEMORY-BASED
Keep Empty Checks:        YES
-----
---- RUNTIME WARNINGS
----
```

Figure 22: DRC Summary Report 2

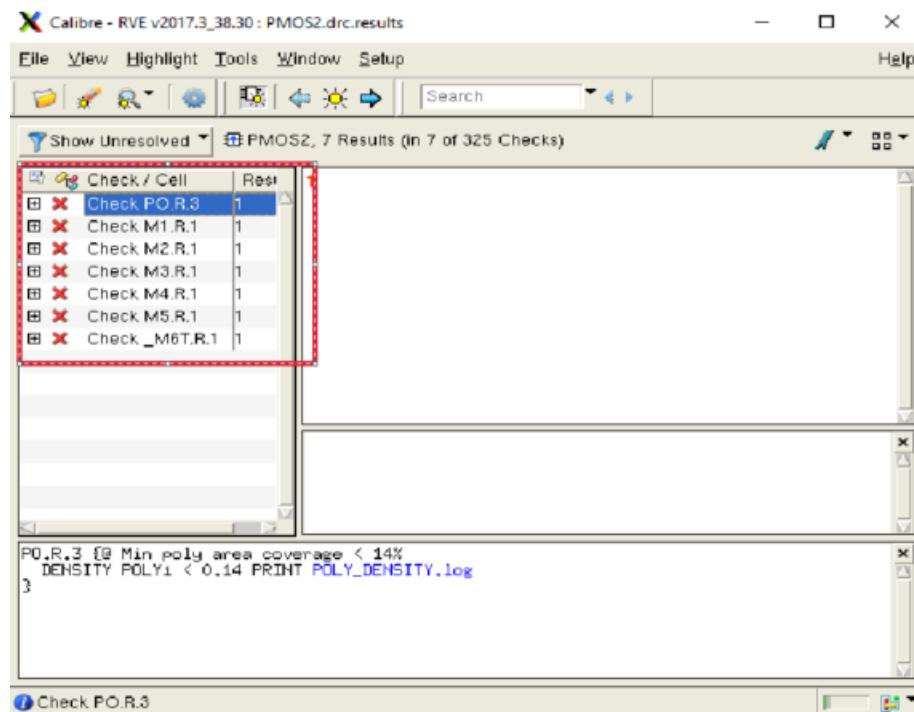


Figure 23: DRC Clean

3.4 “Chip” Design Flow

When you want to design circuits, no matter how large and complicated they are, you should follow this design flow:

1. Design the schematic
2. Simulate the schematic to make sure the function meets the requirements
3. Design layout
4. Physical verification (DRC, LVS, PEX)
5. Post-layout simulation

For this assignment, we do not consider LVS (layout vs. schematic) and PEX (parasitic extraction). However, interested students can refer to http://www.eda.ncsu.edu/wiki/Tutorial:Layout_Tutorial2. You will encounter these steps later on, if you choose to design circuits for microelectronics.