5XCC0 Biopotential and Neural Interface Circuits

Assignment 7

ADC Design and System Simulations

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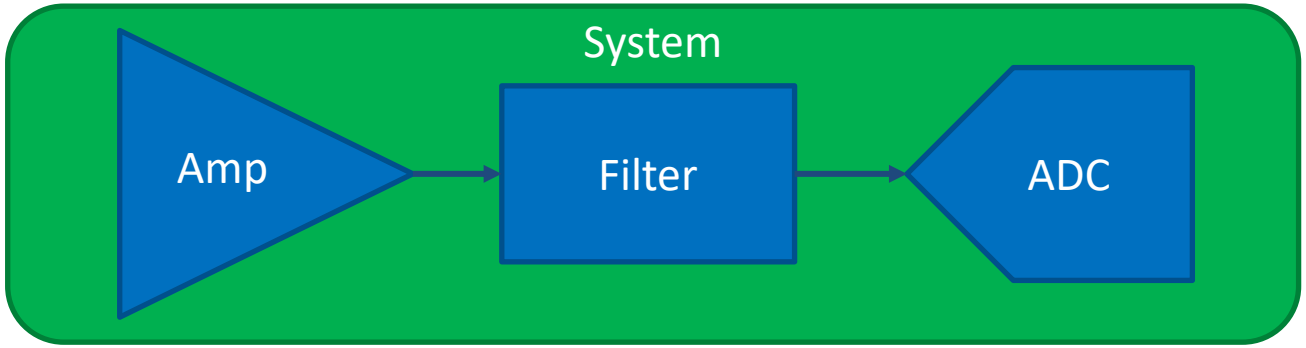
Overall Assignment

- In 6 steps (spread out over 6 weeks), we will design a neural recording interface for AP & LFP recording. The system is composed of an amplifier, a filter, and an ADC.
  - This week, we will focus on step 6: Design of the ADC and overall system test.



Instructions

- The main assignment has 3 parts
  - Analyzing the power consumption of the logic for the ADC
  - Design of the ADC
  - Overall system test

- The final answers need to be entered in CANVAS
  - Carefully check the unit that is asked on CANVAS (e.g.: V, mV, V_{rms}, dB)
  - This will determine your score for this assignment
  - You can enter results twice
  - The correct results will be shown after the deadline

Before You Start: Copy Design Library

- You need to copy a few files by following these steps.
- Close your Cadence session but keep your client to the server connected.
- Open a terminal from the Unix desktop.
- Type the following commands one by one in the terminal:
  - `cd ~/Cadence_GPDK045`
  - `tar xvf ~pharpe/shared/5XCC0_ADC.tar`
  - `echo 'DEFINE 5XCC0_ADC ./5XCC0_ADC' >> cds.lib`

Watch out for the spaces and dots!

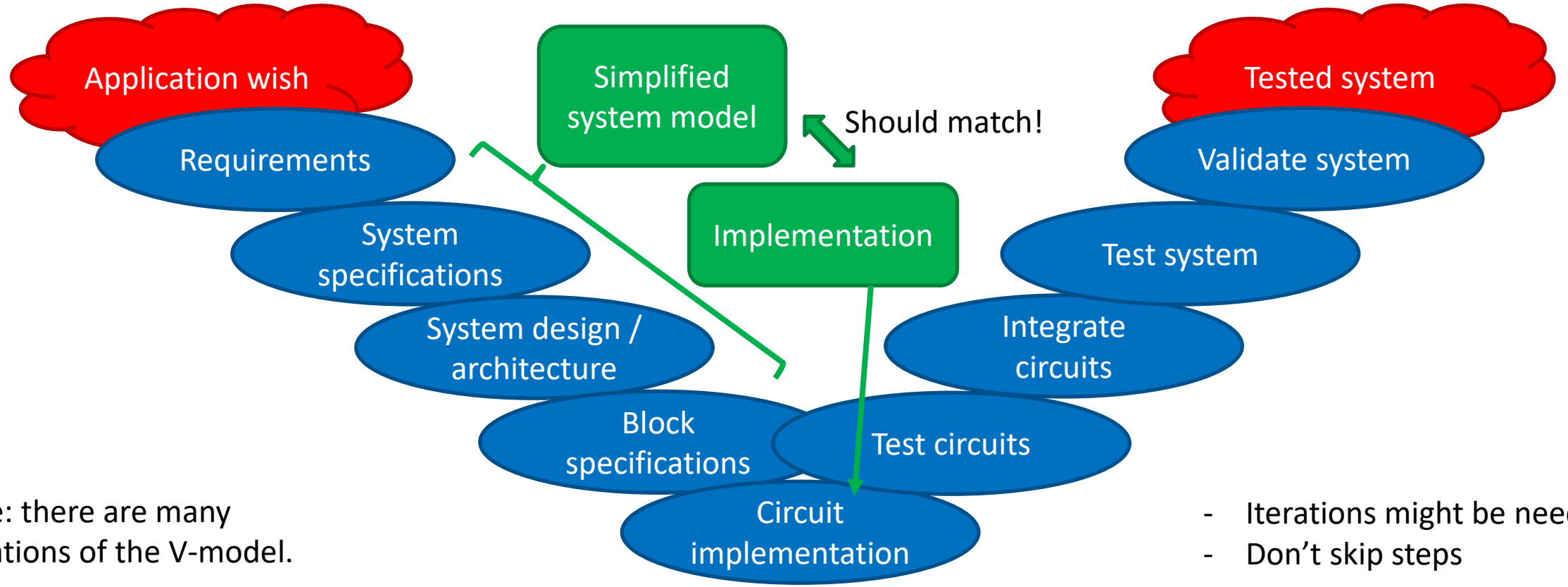
- Close the terminal and start Cadence.
- You should now have a new library 5XCC0_ADC which includes the design of the ADC.

Main Assignment

- According to the V-model (slide 6), this assignment will focus on the circuit implementation (of the ADC) according to the already decided block level specifications. After that, you will put all circuits together and perform system-level testing.
  1. Follow the explanation to optimize the logic and ADC design.
  2. Use the provided Cadence Virtuoso library for simulations.
  3. As a final check: perform system-level testing.
  4. Enter your answers in CANVAS

V-model

- Systematic design methodology to go from an application wish down to a circuit implementation, and up to a tested system



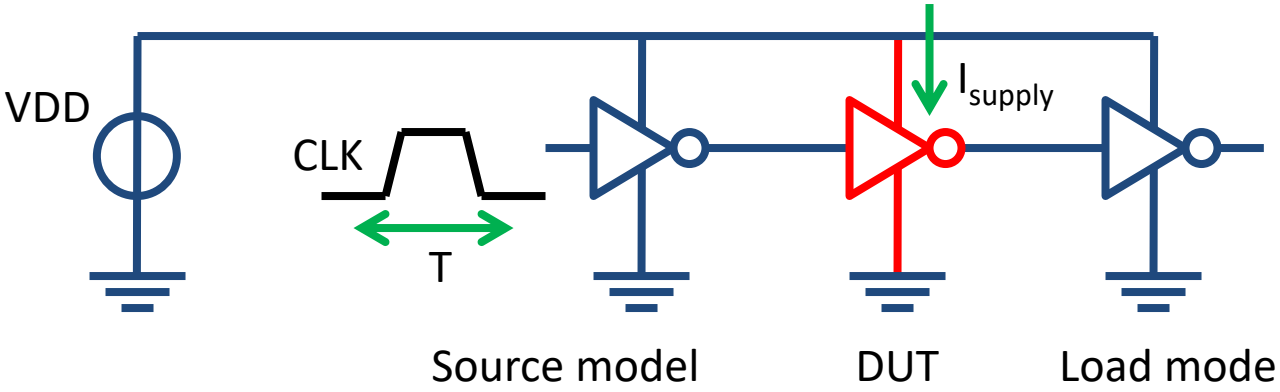
Note: there are many variations of the V-model.

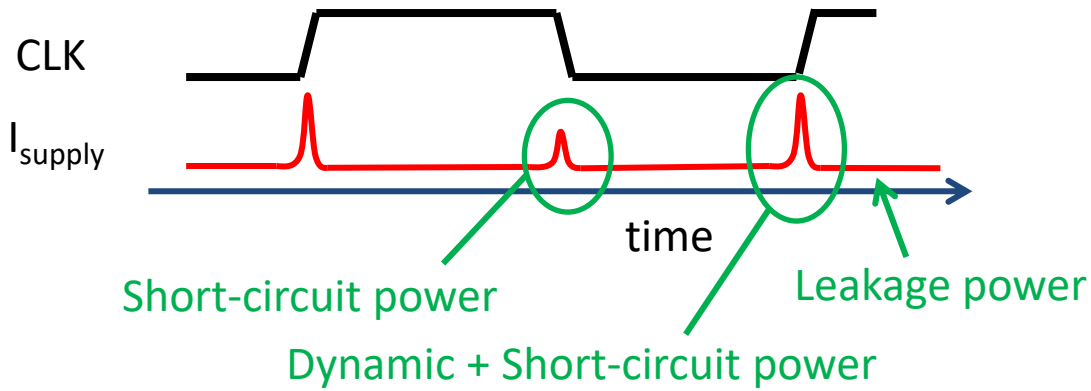
- Iterations might be needed
- Don't skip steps

Step 1: Analyzing the Digital Logic

How to Simulate Power Consumption?

- Transient simulation; model source and load (e.g.: with another logic gate)
  - A good source model is required to have realistic signal transition edges
  - A good load model is required to have a realistic C_L

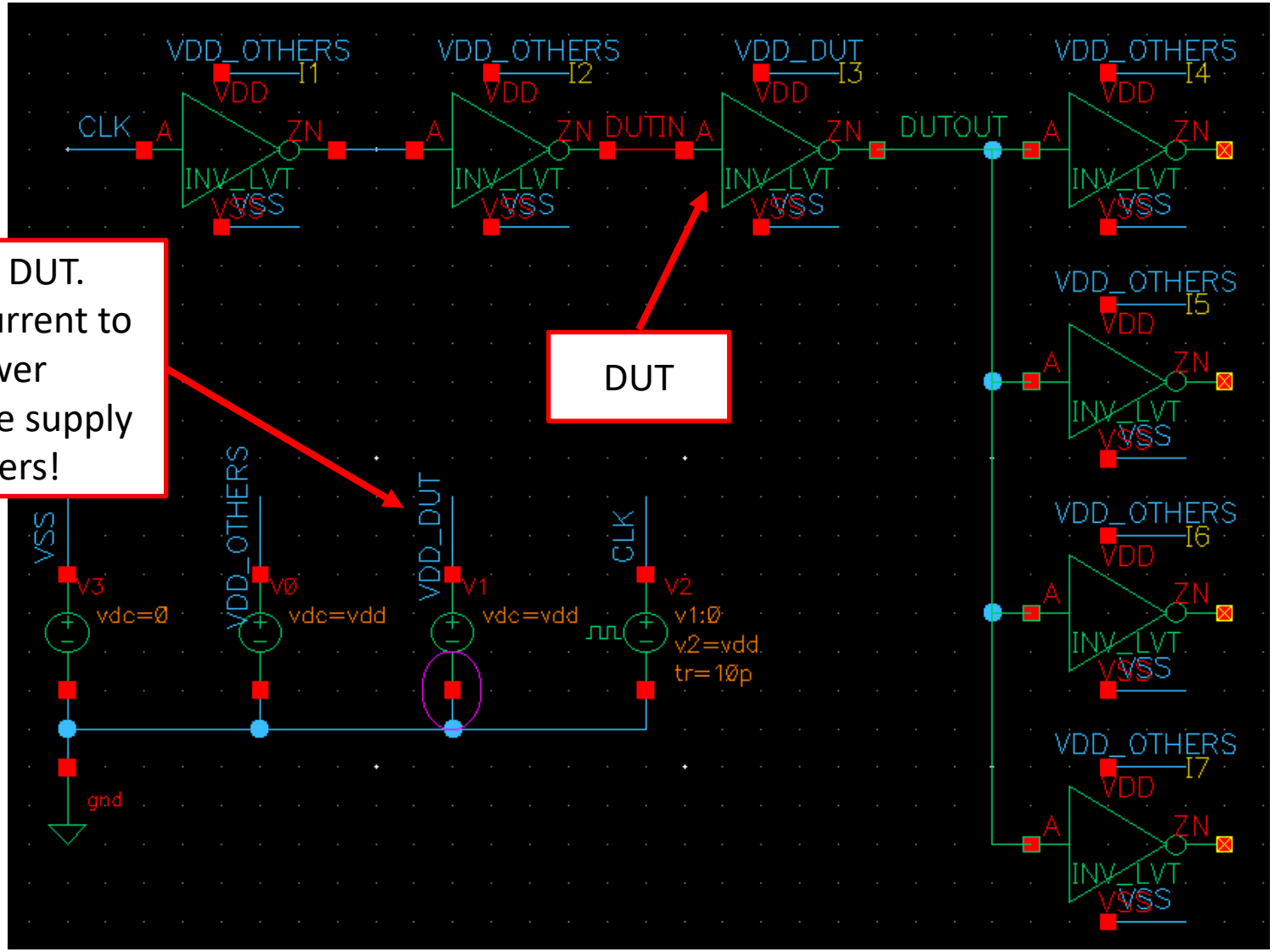




– Integrate over one full period

$$\overline{P} = VDD \cdot \overline{I_{supply}} = \frac{1}{T}\int_0^T VDD \cdot I_{supply}(t)dt = \frac{VDD}{T}\int_0^T I_{supply}(t)dt$$

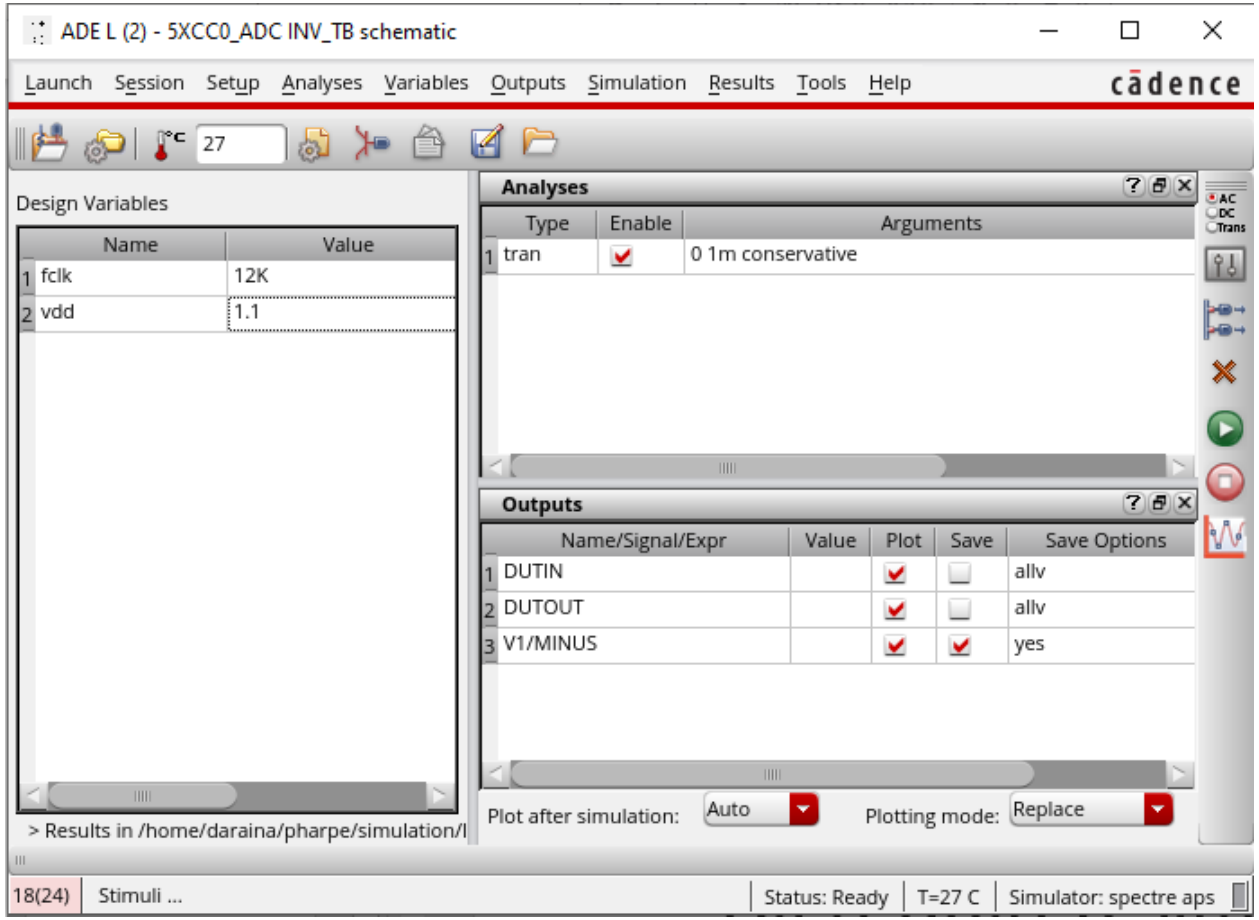
Digital Logic Test Bench: INV_TB



Power supply for the DUT. Check its voltage and current to determine the power consumption. Ignore the supply for the other inverters!

Running Simulations

- To run simulations on the inverter:
  - Open INV_TB schematic
  - Start ADE L
  - Load the existing state (see picture)
- The required simulation will be set up correctly
  - The frequency and supply are set to values that match the ADC design, so we can optimize the logic under the same circumstances.



Questions Digital Logic

Simulate INV_TB and answer the following questions based on the simulated results.

- Question 1: What is the leakage current of the NMOS transistor (in pA)?
- Question 2: What is the leakage current of the PMOS transistor (in pA)?
- Question 3: Calculate, based on your answers from question 1 and 2, the expected average leakage power consumption knowing that VDD is 1.1V, and assuming the clock signal has a 50% duty-cycle (so the NMOS and PMOS are each on for half of the time). Give your answer in pW.
- Question 4: Based on the simulation, what is the total average power consumption (in pW)?
- Question 5: Which component is most critical for the overall power consumption?
- Question 6: Replace all 7 INV_LVT cells by INV_HVT cells (same circuit but using transistors with a higher threshold voltage). What is now the total average power consumption (in pW)?
- Question 7: What else could we do to reduce the leakage power consumption?

Step 2: Optimizing the ADC Design

ADC Specifications

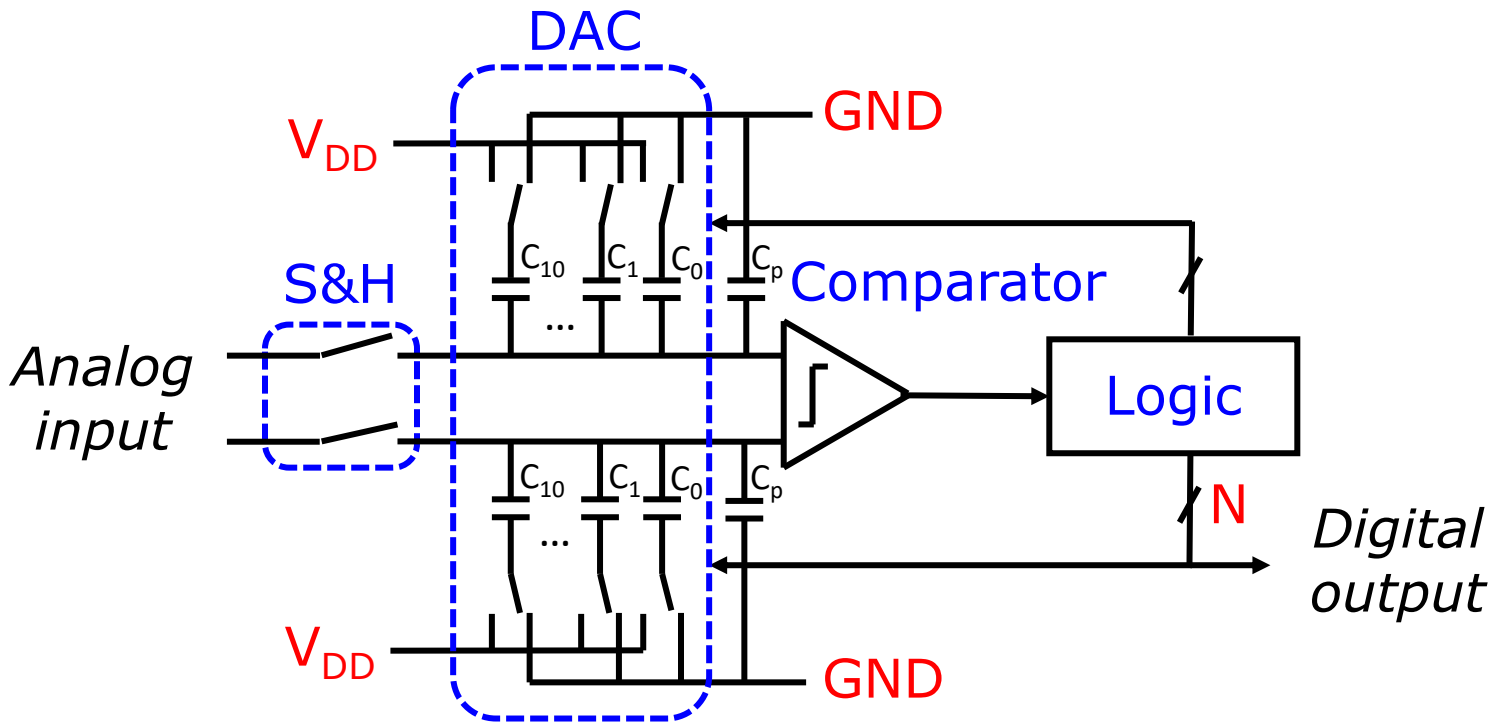
- The table below summarizes the ADC specifications that we found earlier.
- Maybe you had slightly different results, but please use these values from now on!

ADC
IRN = 100μV_{rms}
f_{sample} = 12kHz
Input range = $1V_{pp}$
ENOB = 11.5bit
N = 12bit

- Additionally, you may assume that the supply voltage (VDD) is 1.1V

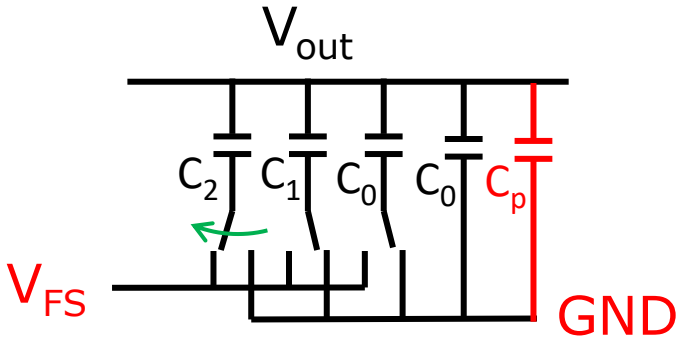
ADC Topology

- 12-bit charge-redistribution SAR ADC with a differential input



Parasitics and Full-Scale Range

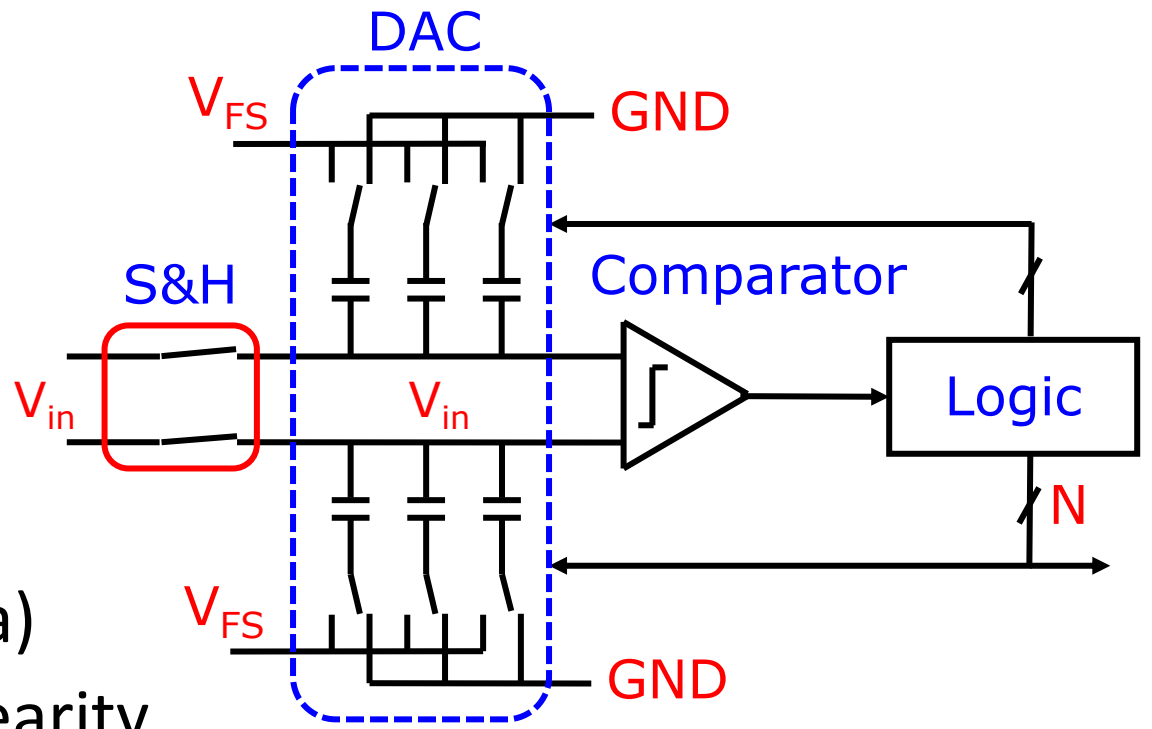
- What happens if we add a parasitic C_p to GND?
- $C_i = 2^i \cdot C_0$ and $C_{sum} = 2^{N-1} \cdot C_0 + C_p = C_{DAC} + C_p$
- What happens when a capacitor is switched from GND to V_{FS}?
  - C_2: $\Delta V_{out} = (C_2 / C_{sum}) \cdot V_{FS} = 4C_0 / (C_{DAC} + C_p) \cdot V_{FS}$
  - C_1: $\Delta V_{out} = (C_1 / C_{sum}) \cdot V_{FS} = 2C_0 / (C_{DAC} + C_p) \cdot V_{FS}$
  - C_0: $\Delta V_{out} = (C_0 / C_{sum}) \cdot V_{FS} = 1C_0 / (C_{DAC} + C_p) \cdot V_{FS}$



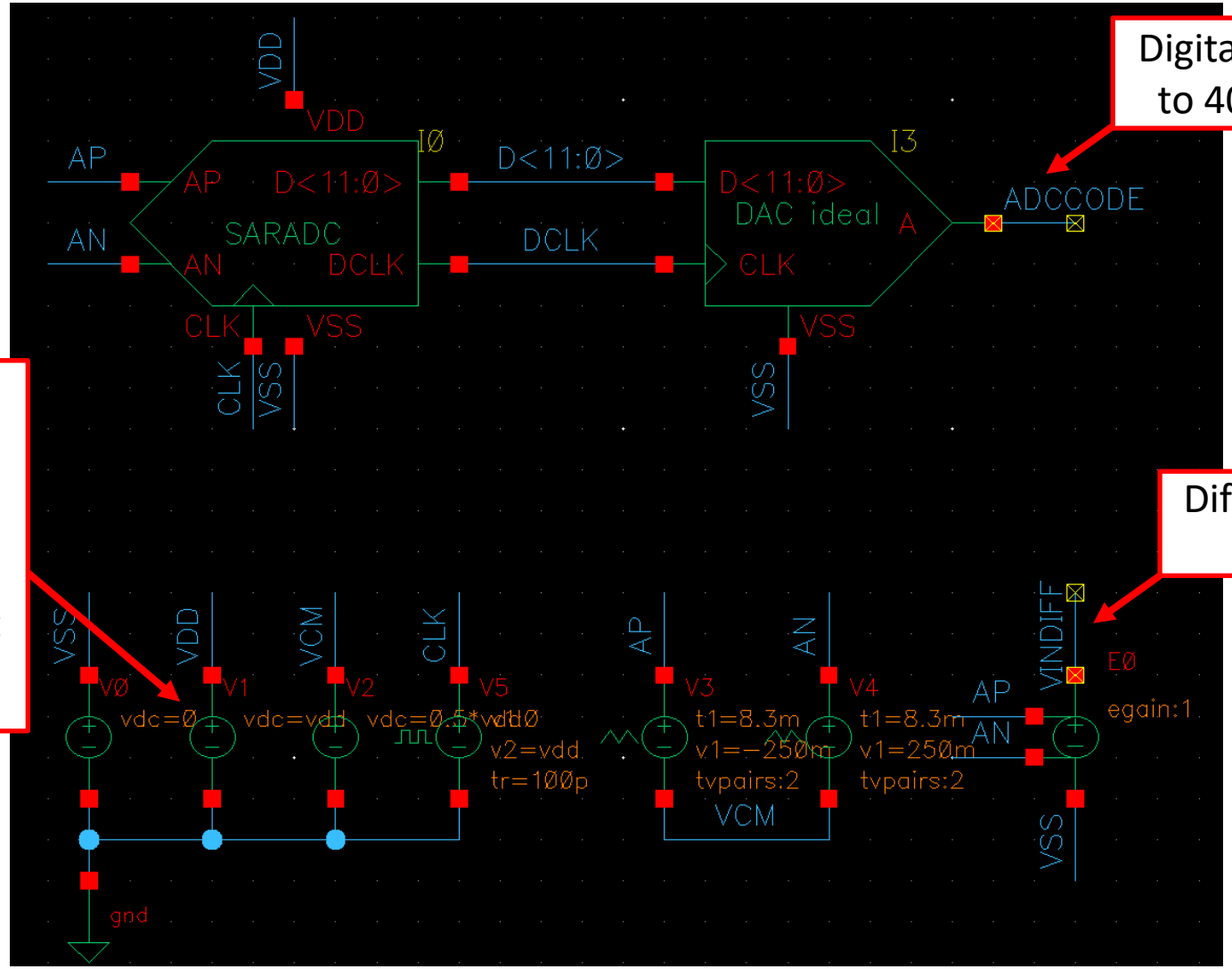
- Steps are still binary-scaled
- Full-scale range is reduced by a factor $C_{DAC} / (C_{DAC} + C_p)$
  - E.g.: if $C_{DAC} = C_p$, the full-scale range becomes $\pm\frac{1}{2}V_{FS}$ instead of $\pm V_{FS}$

DAC: Noise, Linearity, Power Consumption

- Sampling **noise**:
  - $P_n = kT / C_{sum}$ (for one side)
  - $P_n = 2kT / C_{sum}$ (differential)
  - Larger C_{sum} for improved noise
- **Linearity**:
  - Capacitor mismatch ($\sigma_{\%} \propto 1 / \sqrt{\text{Area}}$)
  - More area (larger C's) for better linearity
- **Power consumption**:
  - $E_{DAC} \propto C_{sum} V_{FS}^2 \rightarrow P_{DAC} \propto f_s E_{DAC}$
  - Dynamic power consumption (proportional to f_s), proportional to C_{sum}



ADC Test Bench: ADC_TB



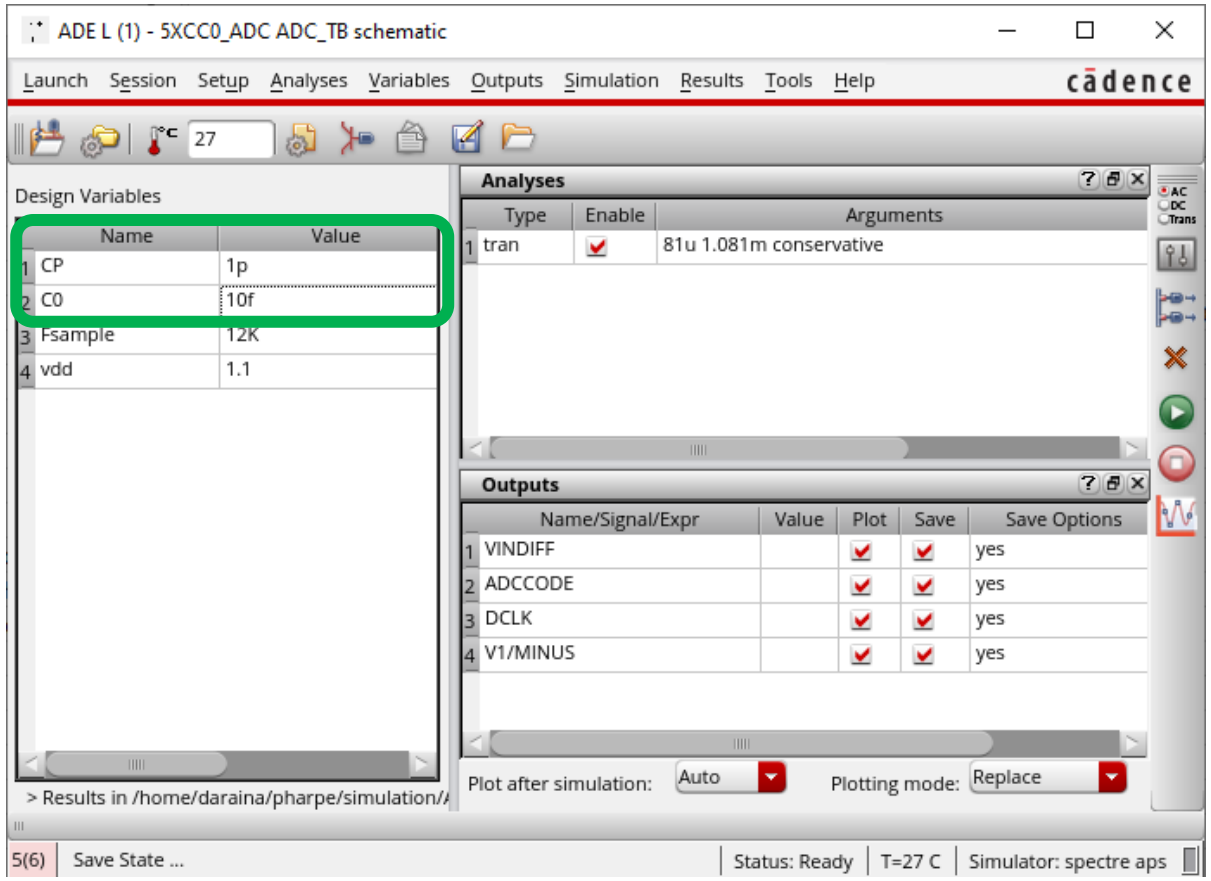
Digital output code (from 0 to 4095 for a 12-bit ADC)

Power supply. Check its voltage and current to determine the overall power consumption. Note: the consumption is dynamic, so you need to check it in the transient simulation!

Differential input voltage (Full-scale sweep)

Running Simulations

- To run simulations on the ADC:
  - Open ADC_TB schematic
  - Start ADE L
  - Load the existing state (see picture)
- The required simulation will be set up correctly
- The goal of this assignment is to find the correct values for C_0 and C_p, and to run simulations to verify the results.
  - All values can be set in ADE L (green box)
  - Results can be observed in the plots
  - The input signal is a $1V_{pp}$ sweep



Questions ADC

According to the block-level requirements, the total IRN of the ADC should not exceed IRN = 100μV_{rms}. Because the ADC is a system in itself (with multiple sub-blocks), this noise budget should again be distributed over the various contributors, such as sampling noise, comparator noise, and quantization noise. For simplicity, we assume that an ADC sampling noise level of 40μV_{rms} is acceptable.

- Question 8: Calculate the required value of C_{sum} (in pF) such that the sampling noise is at a level of 40μV_{rms}.
- Question 9: Calculate the required value of C_p (in pF) such that we achieve the required input range.
- Question 10: Calculate the required value of C_0 (in fF).

Enter the calculated values for C_p and C_0 in ADE L and run the simulation. Answer the following questions based on your simulated results.

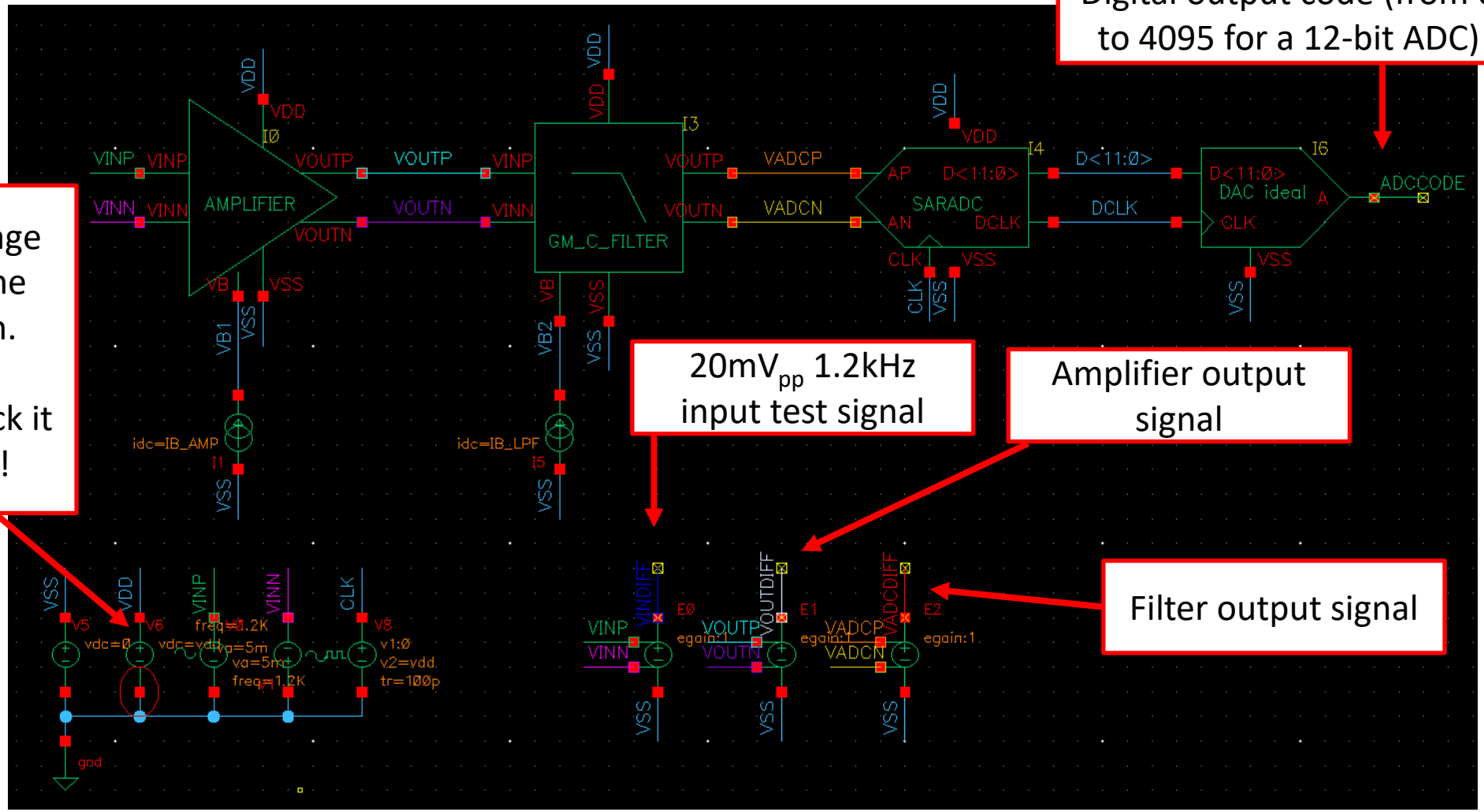
- Question 11: What code range (= max code – min code) is achieved for the 1V_{pp} test signal?
- Question 12: What is the average power consumption of the ADC (in nW)?

Step 3: Overall System Test

System Test Bench: SYSTEM_TB

Digital output code (from 0 to 4095 for a 12-bit ADC)

Power supply. Check its voltage and current to determine the overall power consumption. Note: the consumption is dynamic, so you need to check it in the transient simulation!



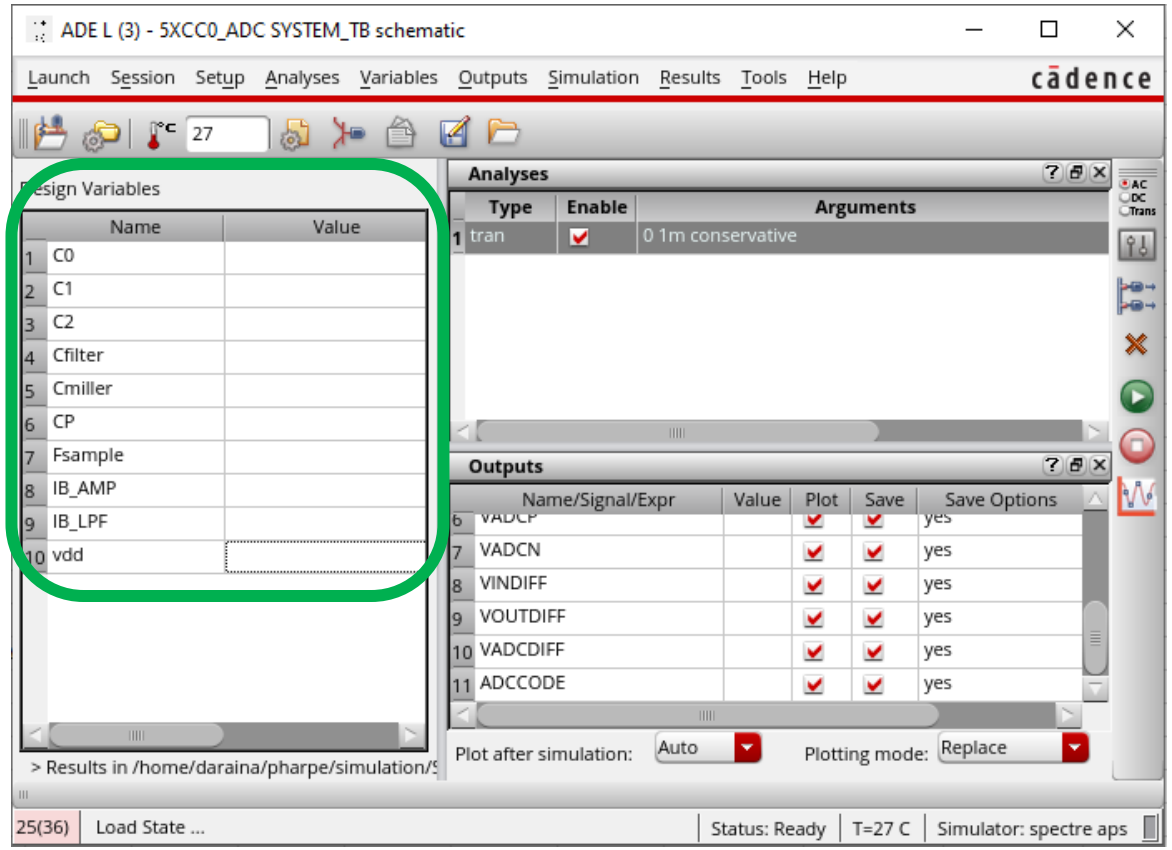
20mV$_{pp}$ 1.2kHz input test signal

Amplifier output signal

Filter output signal

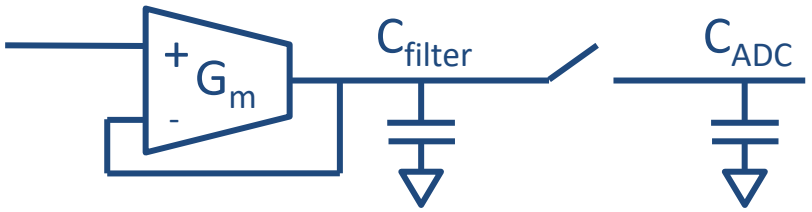
Running Simulations

- To run simulations on the System:
  - Open SYSTEM_TB schematic → Make sure for yourself that the sub-cells (AMP, LPF, ADC) are correct!
  - Start ADE L
  - Load the existing state (see picture)
- The required simulation will be set up correctly
- The goal of this assignment is to **check functionality** of the system
- Set the parameters in the green box according to the values determined in the earlier assignments
  - If you are not sure, ask!



Filter – ADC Loading

- If you like, you could now run the simulation of the entire system, and observe the input signal, the amplifier output signal, the filter output signal, and the ADC output code. However, this simulation takes quite a long time, and will show you that the filter output (which is now connected to the ADC input) is not working well, because the ADC is loading the filter too much.
- Below is a simplified sketch of the situation between filter and ADC (single-ended): the filter output is directly connected to the sampling switch in the ADC, which in turn samples the signal on the capacitance of the ADC.
- The problem is that when the ADC sampling switch is connected, the effective capacitance of the G_m-C filter becomes $C_{filter} + C_{ADC}$, while in the other phase (disconnected switch), it only sees C_{filter}.
- In our design, C_{ADC} is bigger than C_{filter}, and as a result, this effect is rather substantial.
- To solve it, there are two options:
  1. We can add an active buffer (an amplifier with a gain of 1V/V) between filter and ADC to isolate their functions.
  2. We could increase C_{filter} such that it becomes >> C_{ADC}, and then the impact of the ADC on the filter becomes less critical. If we do so, G_m should be changed proportionally, so that G_m/C (and thus the filter bandwidth) remains unchanged.



- We go for option 2: In ADE L, increase the values of C_{filter} and I_{B_LPF} by a factor 10x
  - This should maintain a similar filter bandwidth and solves the ADC loading problem. It increase filter power consumption, but that was quite small compared to the consumption of the overall system.

Step 3: Overall System Test

After changing the filter parameters, run the transient simulation as defined in ADE-L. Check the input signal, the amplifier output signal, the filter output signal, and the ADC output signal one by one to confirm the system is functionally correct. If not, check the circuits and/or the parameters. Once everything looks decent, answer the following questions based on the simulated results.

- Question 13: What code range (= max code – min code) is achieved for the $20mV_{pp}$ input test signal?
- Question 14: What is the power consumption of the entire system (in µW)?