5XCC0 Biopotential and Neural Interface Circuits

Assignment 5

Filter Design

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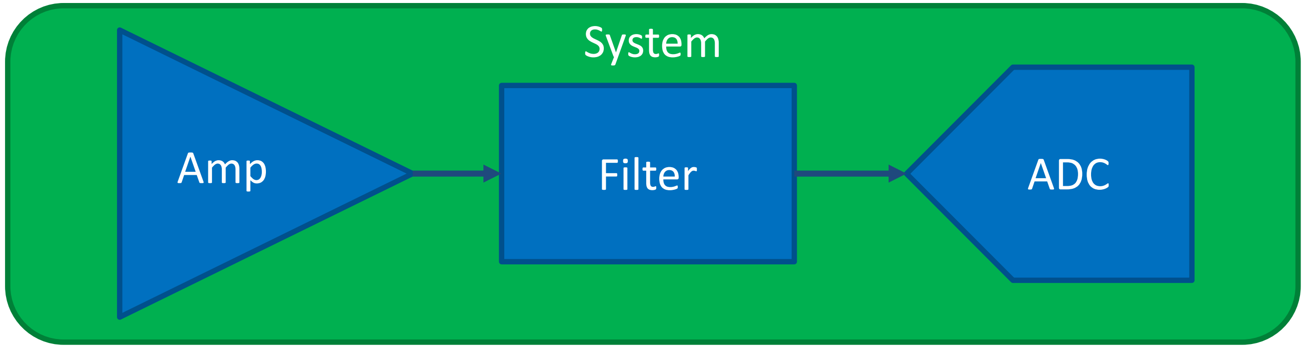
Overall Assignment

- In 6 steps (spread out over 6 weeks), we will design a neural recording interface for AP & LFP recording. The system is composed of an amplifier, a filter, and an ADC.
  - This week, we will focus on step 5: Design of the filter.



- In a separate design assignment (week 6), we will also design a neural stimulation circuit.

Instructions

- First, do the practicing exercises (slide 5 to slide 8)
- After that, do the main assignment (slide 9 and further)
- The final answers need to be entered in CANVAS
  - Carefully check the unit that is asked on CANVAS (e.g.: V, mV, V_{rms}, dB)
  - This will determine your score for this assignment
  - You can enter results twice
  - The correct results will be shown after the deadline

Before You Start: Copy Design Library

- You need to copy a few files by following these steps.
- Close your Cadence session but keep your client to the server connected.
- Open a terminal from the Unix desktop.
- Type the following commands one by one in the terminal:
  - ❑ `cd ~/Cadence_GPDK045`
  - ❑ `tar xvf ~pharpe/shared/5XCC0_LPF.tar`
  - ❑ `echo 'DEFINE 5XCC0_LPF ./5XCC0_LPF' >> cds.lib`

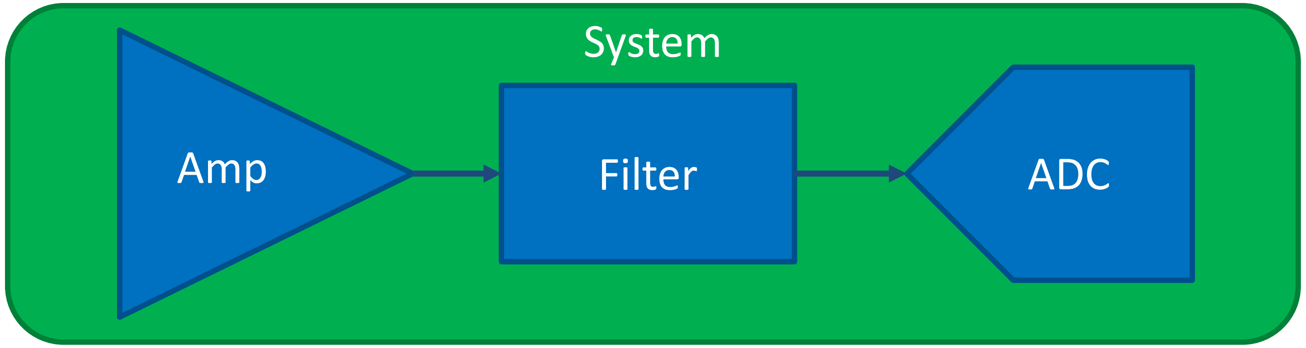
Watch out for the spaces and dots!

- Close the terminal and start Cadence.
- You should now have a new library 5XCC0_LPF which includes the design of the filter.

Part 1: Practicing Exercises

Amplifier Noise Calculation

The figure shows our overall system with some of its specifications:



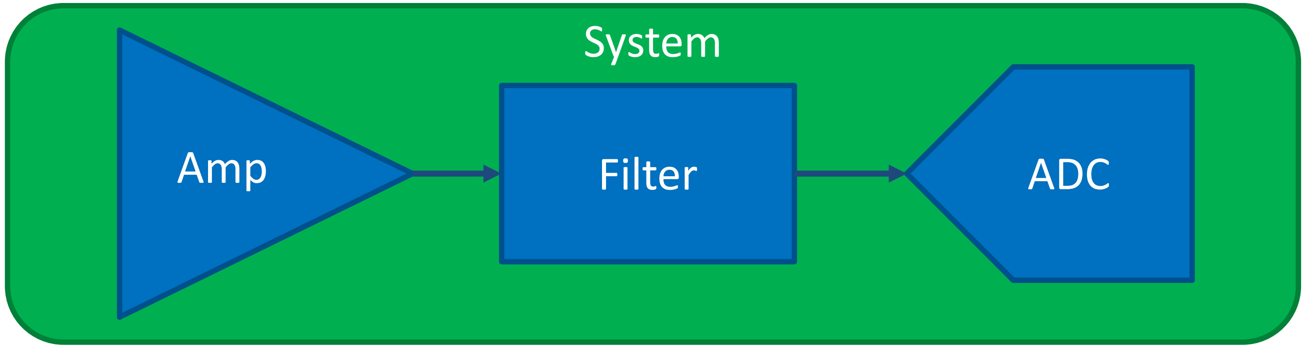
6kHz bandwidth
gain of 50V/V

6kHz bandwidth
gain of 1V/V

12kHz sampling rate

- Question 1: When we calculated the total amplifier noise (in assignment 4), we integrated the noise power spectral density over a bandwidth from 0.5Hz up to 6kHz. Why did we ignore the noise beyond 6kHz?

Filter Noise Calculation



6kHz bandwidth
gain of 50V/V

6kHz bandwidth
gain of 1V/V

12kHz sampling rate

- Question 2: On the other hand, why can we not ignore the filter output noise that occurs beyond 6kHz?
- Question 3: In this context, why might it be a better idea to check the output-referred filter noise instead of the input-referred filter noise?

Integrated Filter Noise

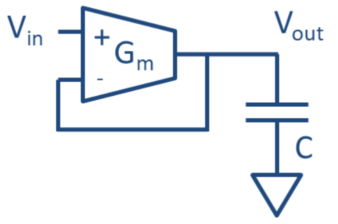
- Assume we have a 1st order G_m-C low-pass filter, where the OTA is given by the circuit below. Please also have a look at lecture 04, where part of the calculation was already performed.
  - For each relevant transistor, the current noise PSD is $S_I^2(f) = 4\ kT\ {}^2/_3 \cdot g_m$.
  - Thus, the input-referred noise voltage PSD is $S_V^2(f) = \alpha\ 8\ kT / 3g_m$, where α depends on the number of transistors that contribute to the noise.
  - The filter characteristic is given by: $H(f) = 1 / (1 + j\ 2\pi f\tau)$, where $\tau = C / g_m$.
  - The integrated output noise power is:

$$P_{noise,out} = \int_{f=0}^{f=\infty} \{S_V^2(f) \cdot |H(f)|^2\} df = \int_{f=0}^{f=\infty} \{\alpha\ 8\ kT / 3g_m \cdot (1 + (2\pi f\tau)^2)^{-1}\} df =$$

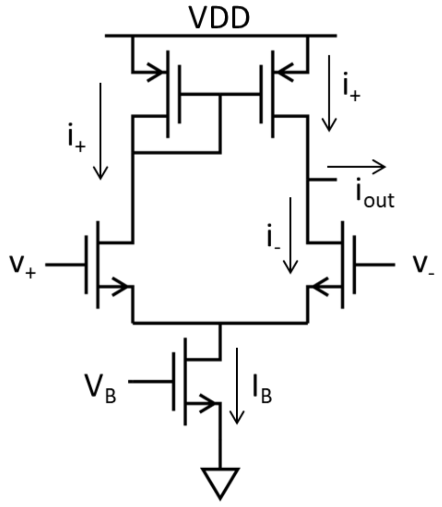
$$\alpha\ 8\ kT / 3g_m \cdot \int_{f=0}^{f=\infty} \{(1 + (2\pi f\tau)^2)^{-1}\} df = \alpha\ 8\ kT / 3g_m \cdot \arctan(2\pi f\tau) \cdot (2\pi\tau)^{-1} \Big|_{f=0}^{f=\infty} =$$

$$\alpha\ 8\ kT / 3g_m \cdot ½\ \pi \cdot (2\pi\tau)^{-1} = ({}^2/_3\ \alpha) \cdot kT / C.$$

  - Conclusion: the integrated noise is proportional to kT/C, but there is a proportionality constant $({}^2/_3\ \alpha)$ that depends on the exact topology.
- Question 4: Assuming $\alpha = 4$, what is the integrated output noise of the filter discussed in exercise 6 of lecture 04? Give your answer in μV_{rms}.



G_m-C filter



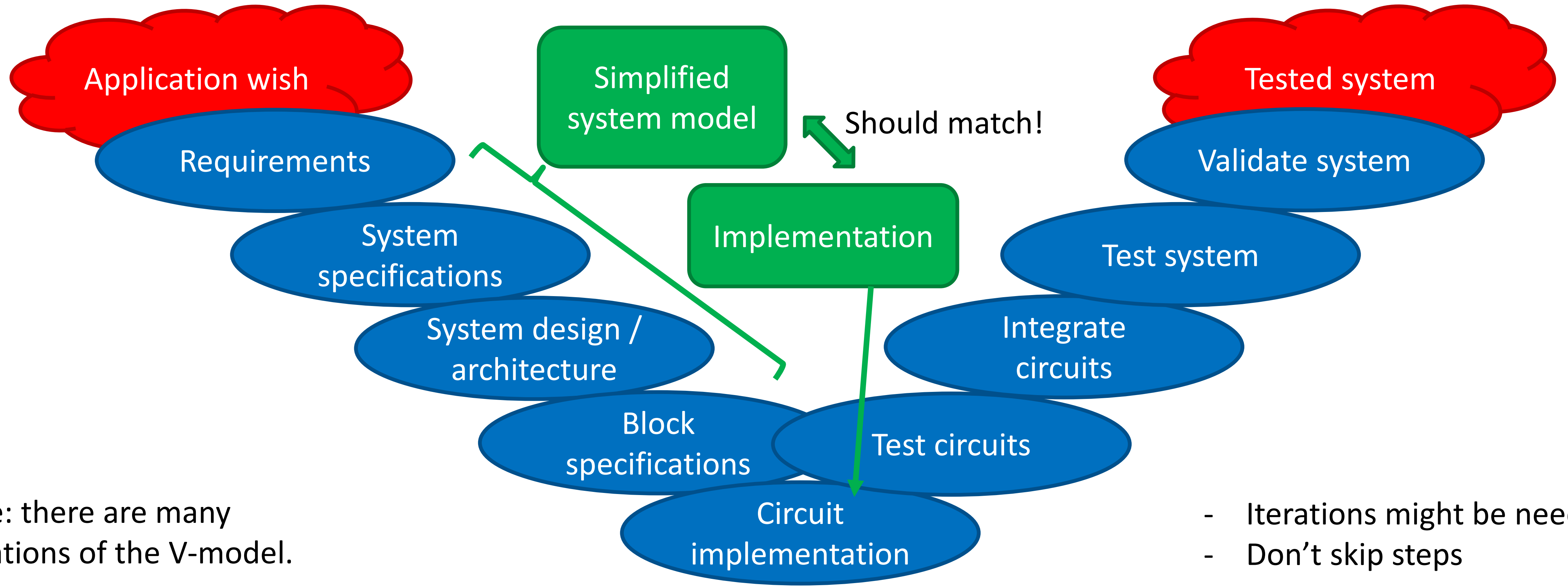
OTA

Part 2: Main Assignment

- According to the V-model (slide 10), this assignment will focus on the circuit implementation (of the filter) according to the already decided block level specifications.
  1. Follow the explanation to dimension the filter step by step.
  2. Use the provided Cadence Virtuoso library to simulate the filter.
  3. Confirm that it meets the block level specifications
     - Minor variations are expected; that is OK.
     - If the results are significantly different; check if all steps were done correctly.
  4. Enter your answers in CANVAS

V-model

- Systematic design methodology to go from an application wish down to a circuit implementation, and up to a tested system



Note: there are many variations of the V-model.

- Iterations might be needed
- Don't skip steps

Filter Specifications

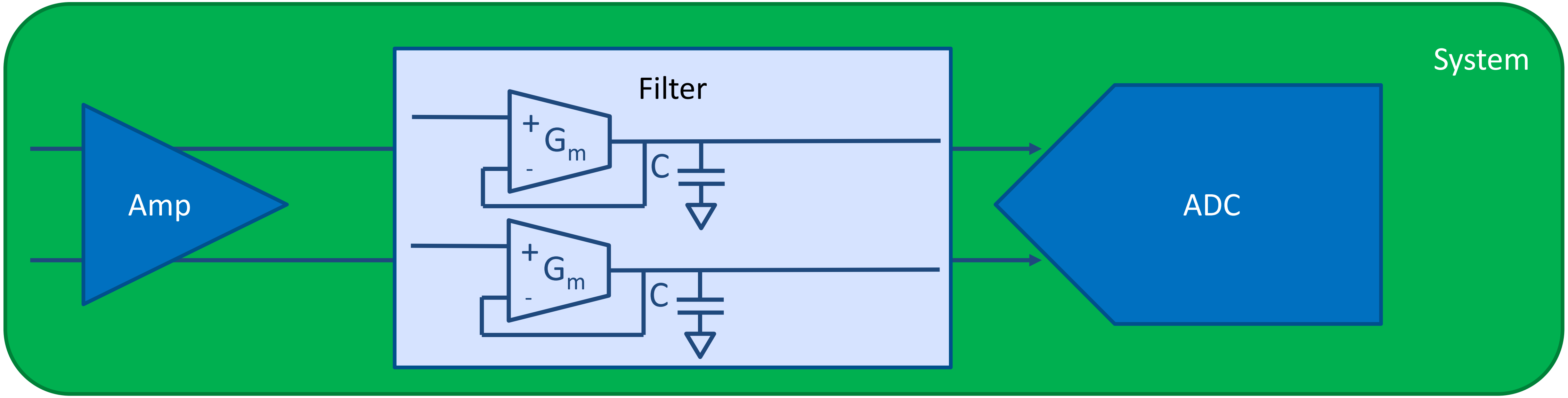
- The table below summarizes the filter specifications that we found earlier.
- Maybe you had slightly different results, but please use these values from now on!

Filter
IRN = $100\mu V_{rms}$
BW = 6kHz
Input range = $1V_{pp}$
Output range = $1V_{pp}$

- Additionally, you may assume that the supply voltage (VDD) is 1.1V

Filter Topology

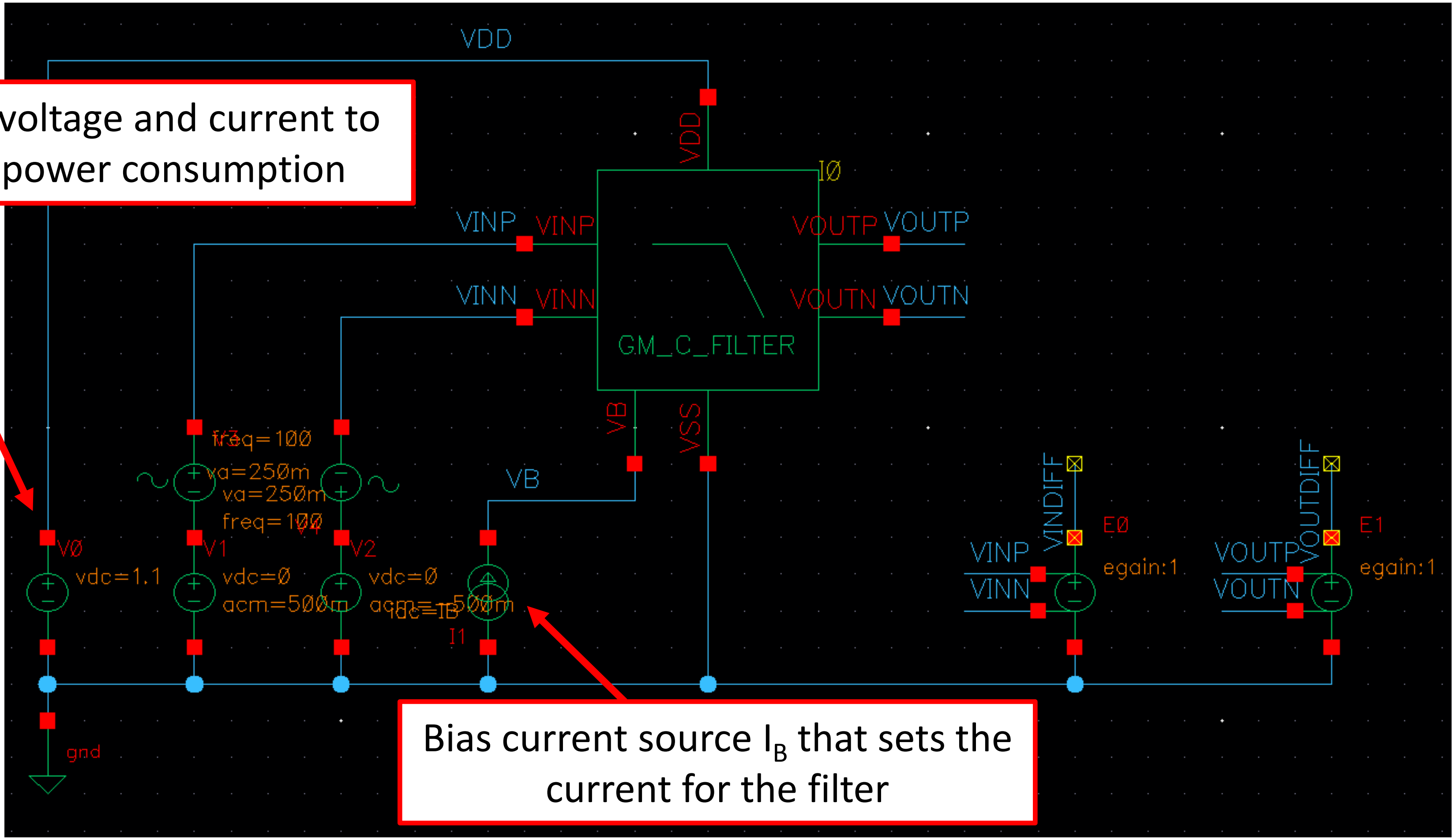
- First-order low-pass filter using G_m-C topology
- Pseudo-differential implementation
  (i.e.: 2 single-ended copies to create a differential system)



FILTER_TB

- Overall test bench to run your simulations on

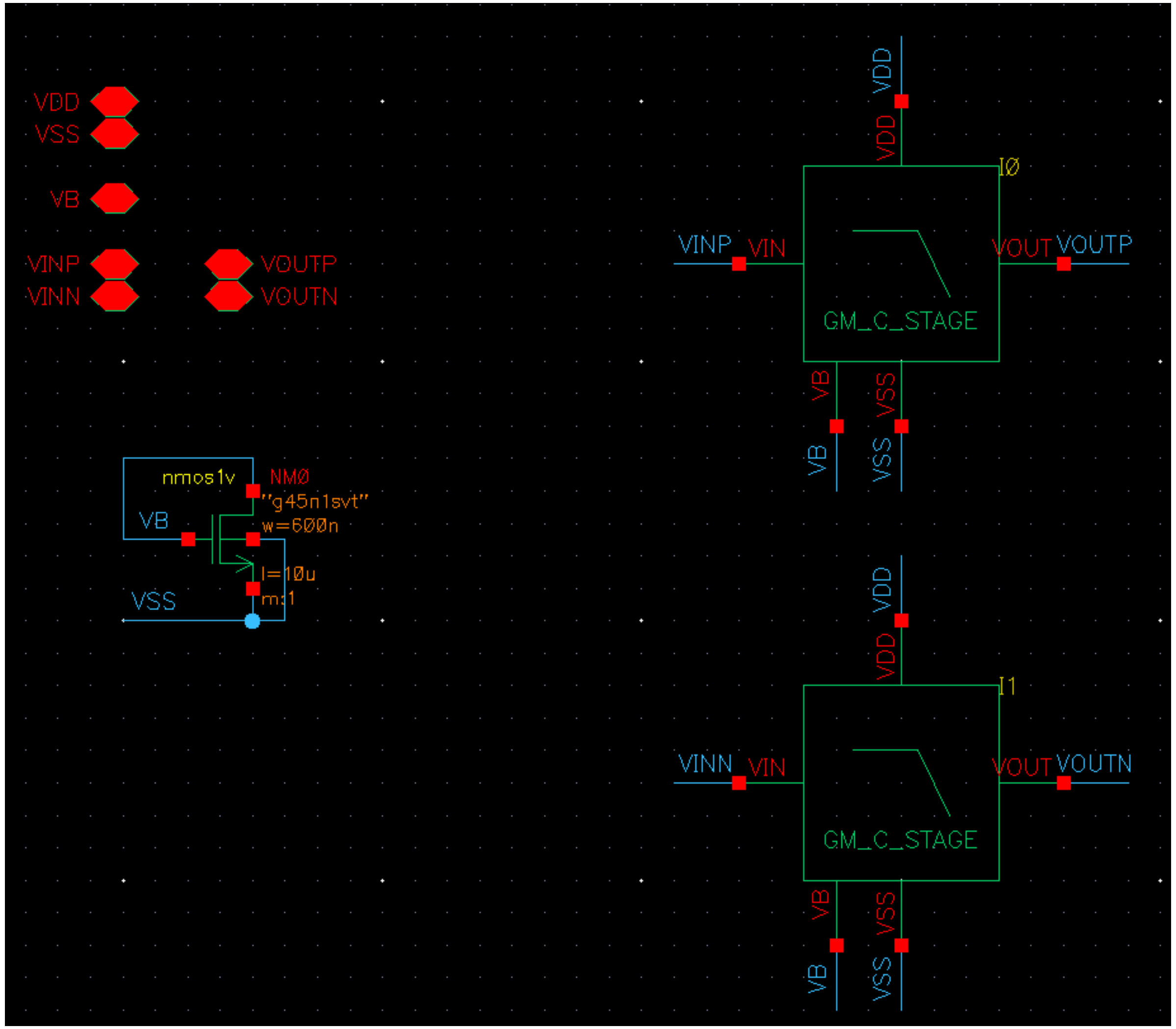
Power supply. Check its voltage and current to determine the overall power consumption



Bias current source I_B that sets the current for the filter

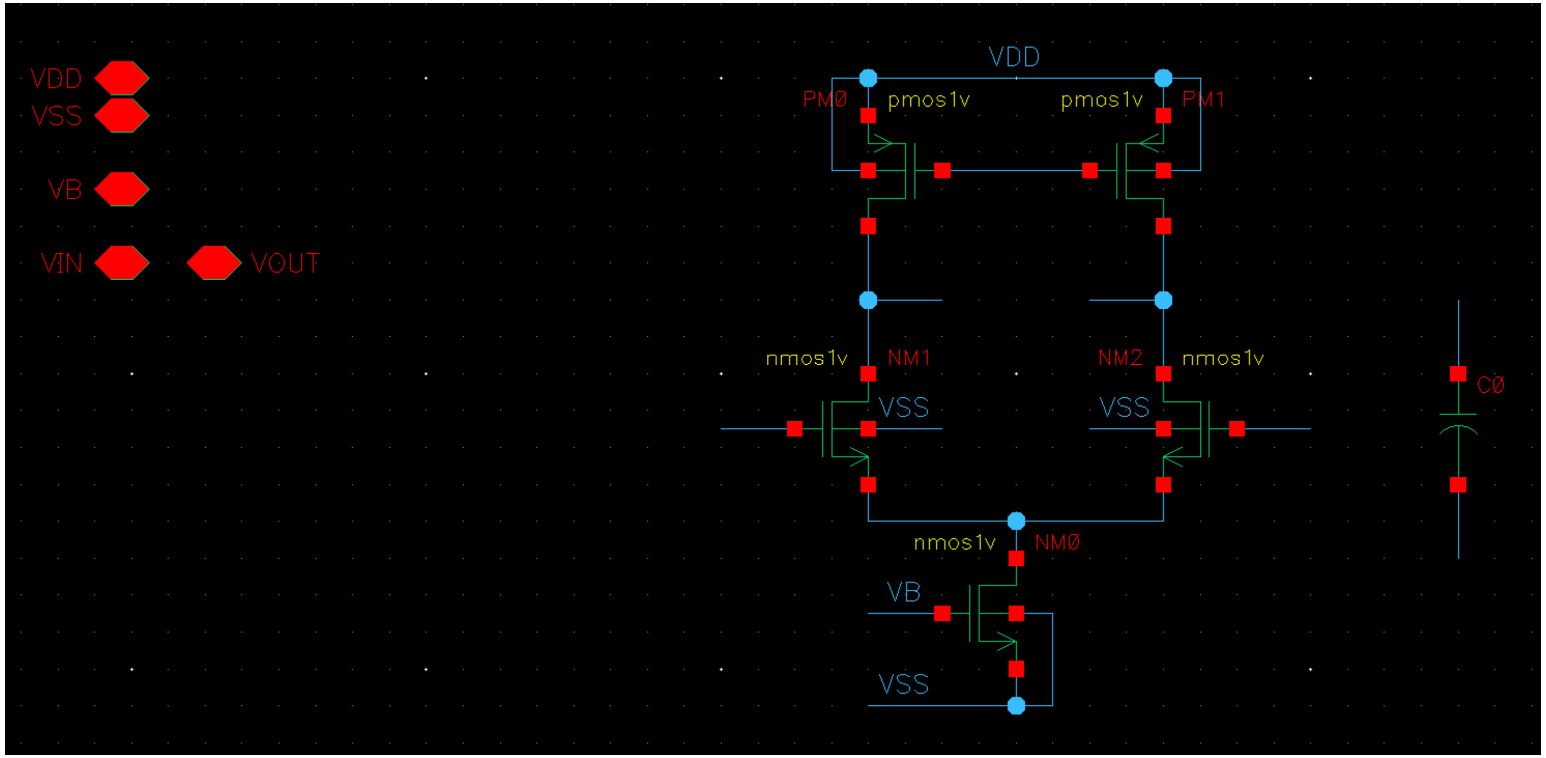
GM_C_FILTER

- Composed of 2 identical G_m-C stages (to make a pseudo-differential design)
- Identical bias current (I_B) is copied to both stages with current mirrors



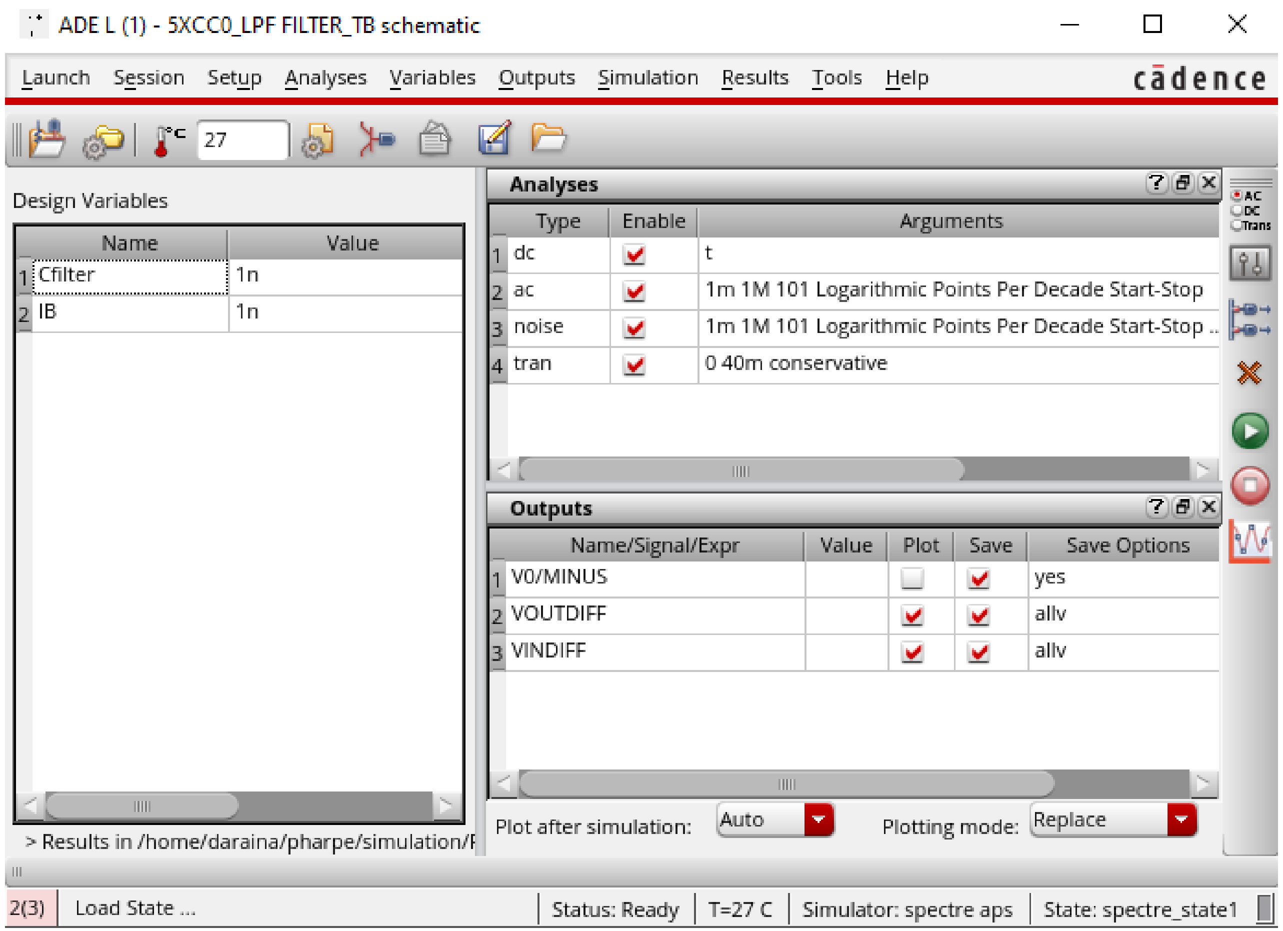
GM_C_STAGE

- A single-ended G_m-C filter
  - Tail current source is set by I_B. The value of the filter capacitance (C_{filter}) is still to be determined.
  - All required components are present and correctly sized
  - You still need to wire the various components correctly to make a 1st order low-pass filter



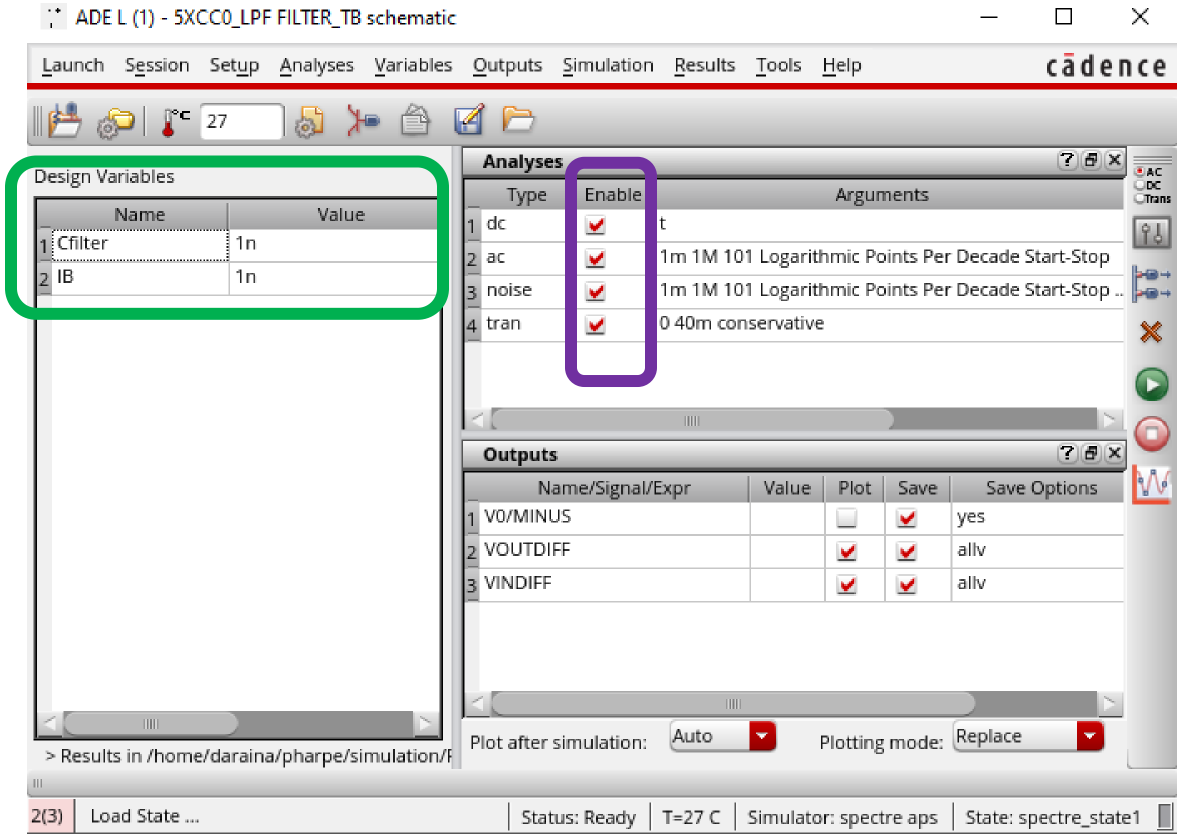
Running Simulations

- To run simulations on the filter:
  - Open FILTER_TB schematic
  - Start ADE L
  - Load the existing state (see picture)
- All required simulations will be set up correctly



Running Simulations

- The goal of this assignment is to find the correct values for C_{filter} and I_B, and to run simulations to verify the results.
  - All values can be set in ADE L (green box)
  - Results can be observed in the plots
  - Analysis types can be enabled/disabled as desired (purple box)



Step 1: Completing the Filter Schematic

Open the schematic GM_C_STAGE and complete the wiring of the system.

Tip: look carefully and compare the design to the one discussed in lecture 04.

Step 2: Calculations

- For this assignment you may assume that:
  - The integrated filter output noise power can be estimated by: $P_{noise} = 7kT / C_{filter}$
    Note that the proportionality constant is quite high here (7), because the topology is differential, which doubles the number of noise sources.
  - The g_m/I_D of the transistors in the OTA can be estimated by $28V^{-1}$.
  - Questions 5 up to 7 require manual calculations. Don't use Cadence simulations yet!

- Question 5: Calculate the filter time constant τ for the desired bandwidth.
  Give your value in µs.
- Question 6: Calculate the required value of C_{filter} to meet the noise specification.
  Round this value to an integer in pF and use the rounded value in your further calculations and simulations. (e.g.: round 1.34pF to 1pF).
- Question 7: Calculate the required bias current I_B of the OTA to get the right value of G_m.
  Round this value to an integer in nA and use the rounded value in your further calculations and simulations. (e.g.: round 3.64nA to 4nA).

Step 3: Simulations

- Open the FILTER_TB, start ADE L, and load the existing state
  - Set the parameters C_{filter} and I_B as determined in Step 2. Use the rounded values.
- Run all simulations that are defined
  - Check from the DC, AC, and transient simulation that your filter works correctly. If not, either the topology or the parameters are incorrect.
  - Integrate the <u>output</u> noise PSD over the <u>entire simulated frequency range</u> to calculate the total output noise power.
  - Use the DC operating point to determine the power consumption.
  - Questions 8 up to 10 should be answered using the simulation results from Cadence.
- Do you (more or less) achieve the requirements (±10% deviations are acceptable)?
- Question 8: What is the simulated bandwidth (-3dB frequency) in kHz?
- Question 9: What is the total integrated output noise in μV_{rms}?
- Question 10: What is the power consumption of the filter in nW?