# 5XCC0 Biopotential and Neural Interface Circuits

## Assignment 4

## Front-end Amplifier Design

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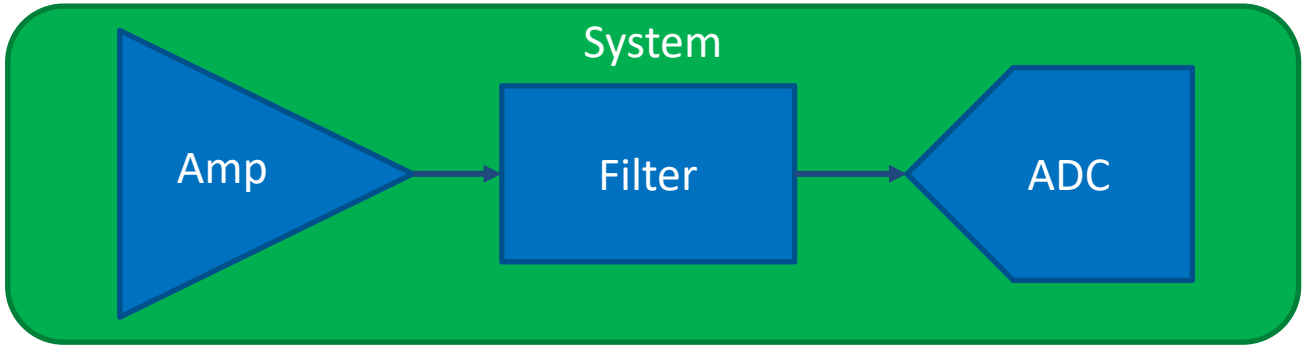
# Overall Assignment

- In 6 steps (spread out over 6 weeks), we will design a neural recording interface for AP & LFP recording. The system is composed of an amplifier, a filter, and an ADC.
  - This week, we will focus on step 4: Design of the front-end amplifier.




- In a separate design assignment (week 6), we will also design a neural stimulation circuit.

# Instructions

- First, do the practicing exercises (slide 5 to slide 10)
- After that, do the main assignment (slide 11 and further)
- The final answers need to be entered in CANVAS
  - Carefully check the unit that is asked on CANVAS (e.g.: V, mV, $V_{rms}$, dB)
  - This will determine your score for this assignment
  - You can enter results twice
  - The correct results will be shown after the deadline

# Before You Start: Copy Design Library

- You need to copy a few files by following these steps.
- Close your Cadence session but keep your client to the server connected.
- Open a terminal from the Unix desktop.
- Type the following commands one by one in the terminal:
  - `cd ~/Cadence_GPDK045`
  - `tar xvf ~pharpe/shared/5XCC0_AMP.tar`
  - `echo 'DEFINE 5XCC0_AMP ./5XCC0_AMP' >> cds.lib`

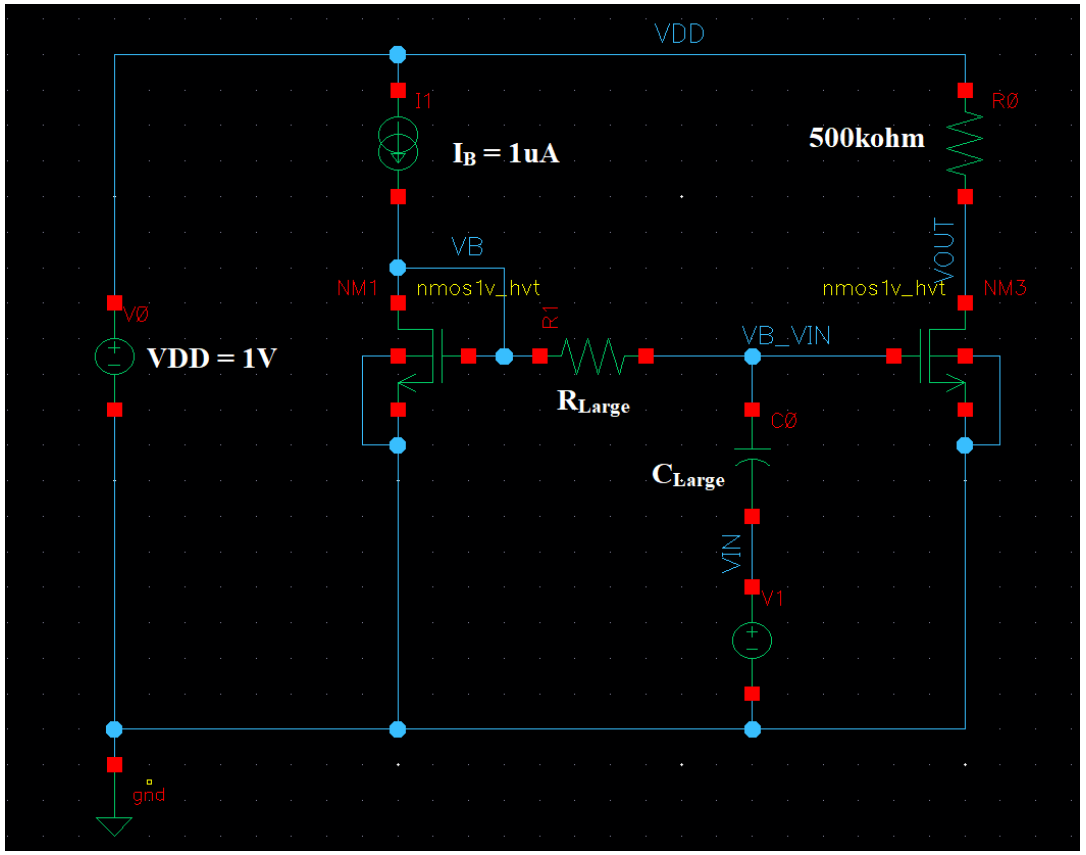
Watch out for the spaces and dots!

- Close the terminal and start Cadence.
- You should now have a new library 5XCC0_AMP which includes the design of the front-end amplifier.

# Part 1: Practicing Exercises

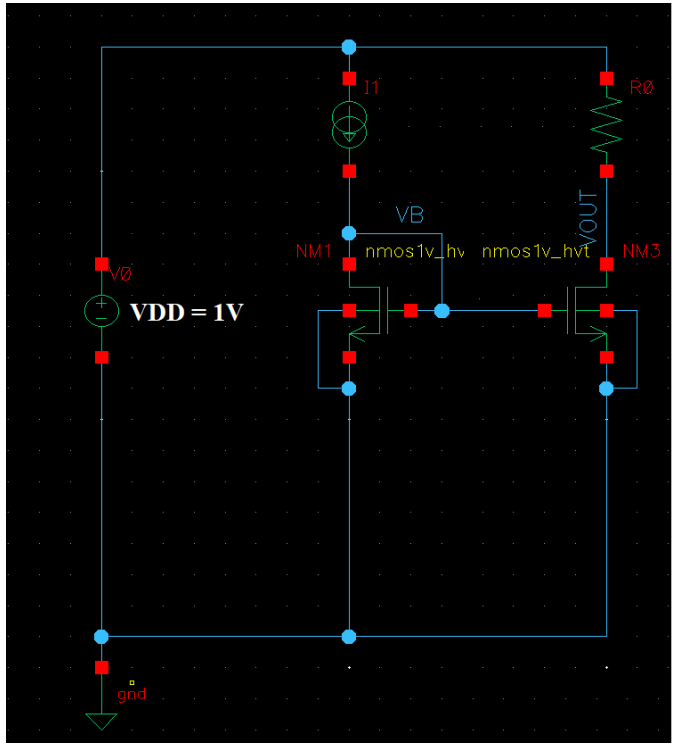
# TRANSISTOR_TB: Weak and Strong Inversion

- In Cadence, open the design “TRANSISTOR_TB”, start ADE L, and load the existing simulator state.
- The schematic is a one-transistor amplifier (NM3) with resistor load (R0).
- Current source I1 and transistor NM1 are used to bias NM3 to $I_B$ = 1µA.
- R0 has a value of 500kΩ.
- $R_{Large}$ and $C_{Large}$ have a very large value and are for simulation purposes only.
  - Because of this, we can simplify the schematic as shown on the next slide

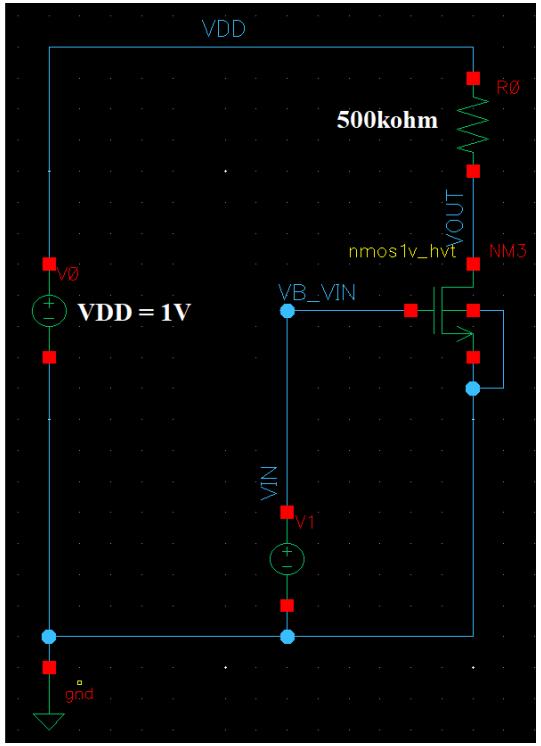


# Simplification of TRANSISTOR_TB

- For DC: $C_{Large}$ is an open. Because there is no DC current flow in $R_{Large}$, there is no voltage drop across $R_{large}$. The circuit now simplifies as shown below.
  - We can see this is a current mirror, so $I_B$ is copied from NM1 to NM3.
- For AC: $C_{Large}$ is a short. Because $R_{Large}$ is large, the gate voltage of NM3 is now controlled by VIN (V1). The circuit now simplifies to the second figure.
  - For AC: this is a 1-transistor amplifier with resistive load.




Simplification for DC




Simplification for AC

# Questions

You may assume that $g_m/I_D$ is 25 in weak inversion.

- Question 1: What is the small-signal gain that you expect from this amplifier with the values given on the previous slides, assuming the transistors are biased in weak inversion?
- Question 2: While the bias current is fixed to 1µA, should we increase or decrease the W/L ratio of the transistors if we want to move the transistors towards weak inversion? Why?

# Simulations

In ADE L, set IB, W, and L as shown below. For each case, check the value of vgs, id, and gm in Cadence (see tip on next slide).

From id and gm, you can calculate the ratio of $g_m/I_D$.

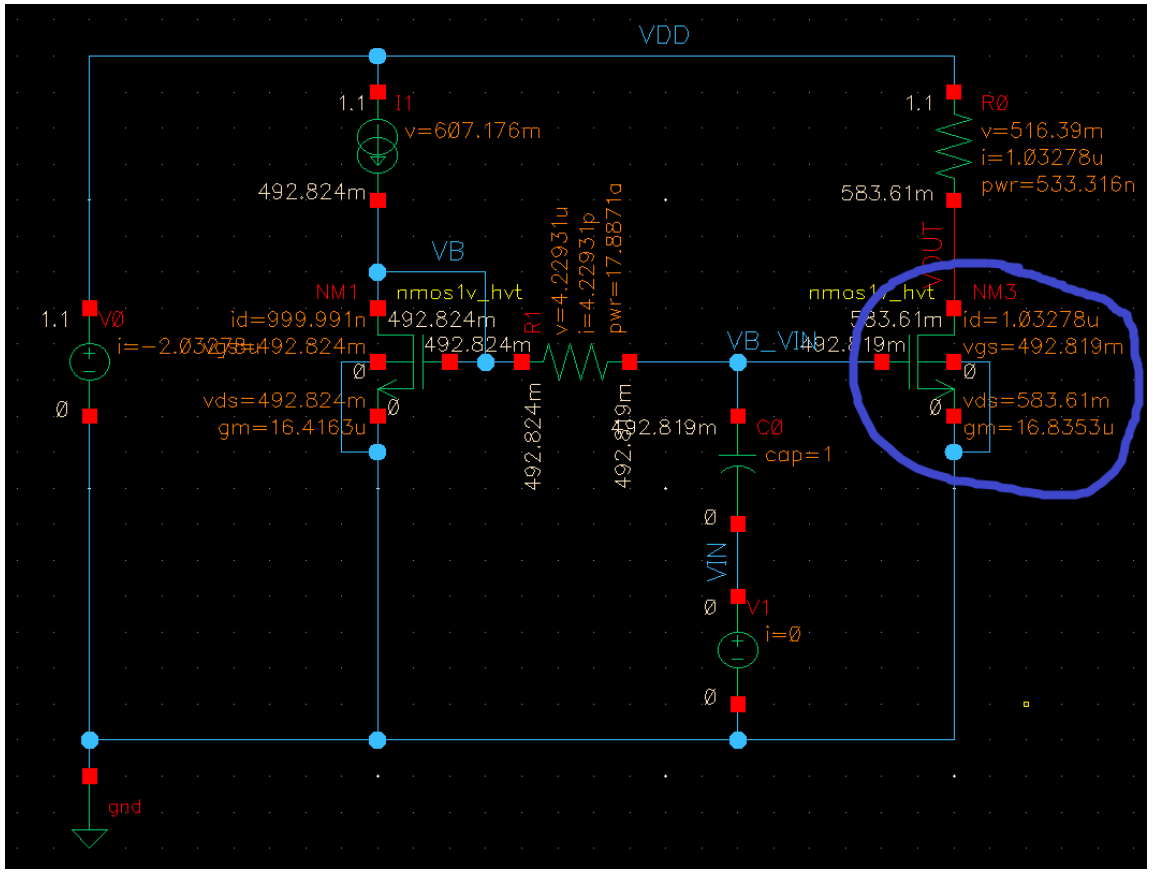
Further, write down the AC small signal gain $A_0$ (from the AC simulation result). Complete the information in the table.

| W [µm] | L [µm] | W / L | $V_{GS}$ [V] | $I_D$ [µA] | $g_m$ [µA/V] | $g_m / I_D$ [$V^{-1}$] | $A_0$ [V/V] |
|---|---|---|---|---|---|---|---|
| 1 | 10 | | | | | | |
| 1 | 1 | | | | | | |
| 10 | 1 | | | | | | |

- Question 3: which of the 3 cases is in weak inversion (or close to it)?
- Question 4: What is the simulated $g_m/I_D$ for that case?

# Tip for Previous Slide

- To check the value of vgs, id, and gm in Cadence, you first run a DC simulation where you save the bias point (that's correctly set if you have loaded the existing state in ADE L).
- After that, you pick the following menu in ADE L: "Results" → "Annotate" → "DC operating points", which will visualize the values on top of the schematic view.

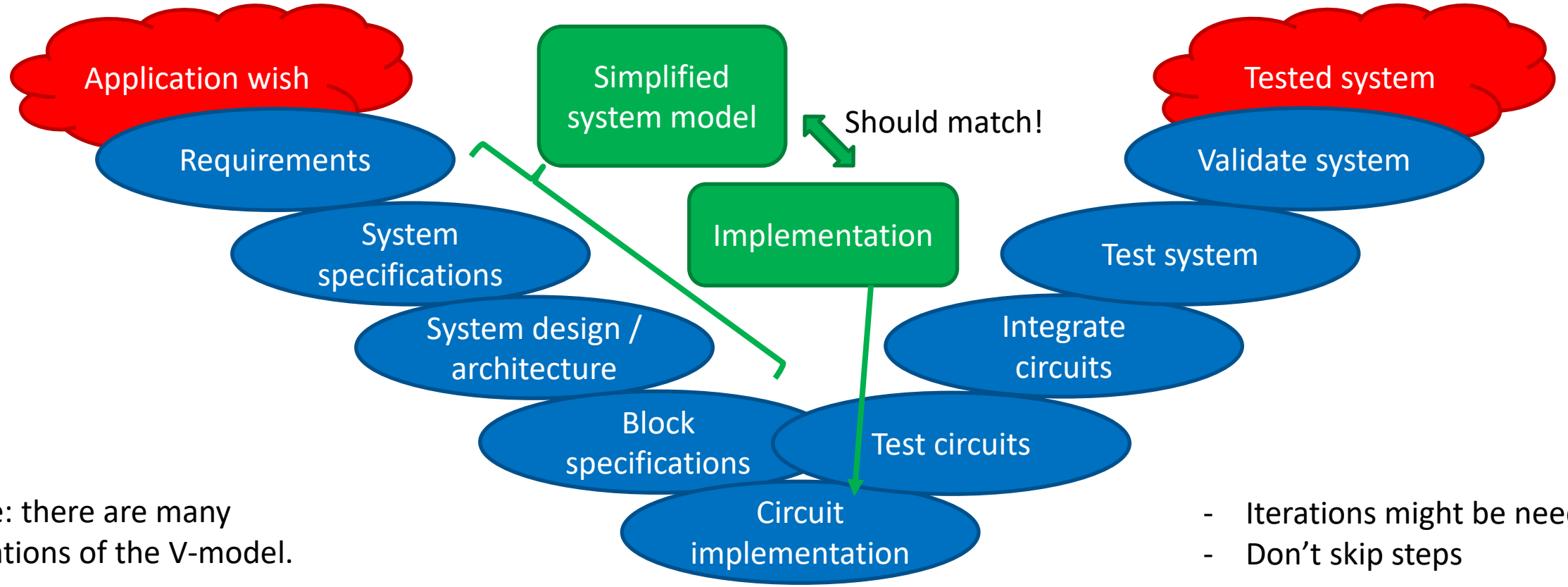


# Part 2: Main Assignment

- According to the V-model (slide 12), this assignment will focus on the circuit implementation (of the front-end amplifier) according to the already decided block level specifications.
  1. Follow the explanation to dimension the amplifier step by step.
  2. Use the provided Cadence Virtuoso library to simulate the amplifier.
  3. Confirm that it meets the block level specifications
     - Minor variations are expected; that is OK.
     - If the results are significantly different; check if all steps were done correctly.
  4. Enter your answers in CANVAS

# V-model

- Systematic design methodology to go from an application wish down to a circuit implementation, and up to a tested system




Note: there are many variations of the V-model.

- Iterations might be needed
- Don't skip steps

# Amplifier Specifications

- The table below summarizes the amplifier specifications that we found earlier.
- Some specs are rounded here, so please use these values from now on!

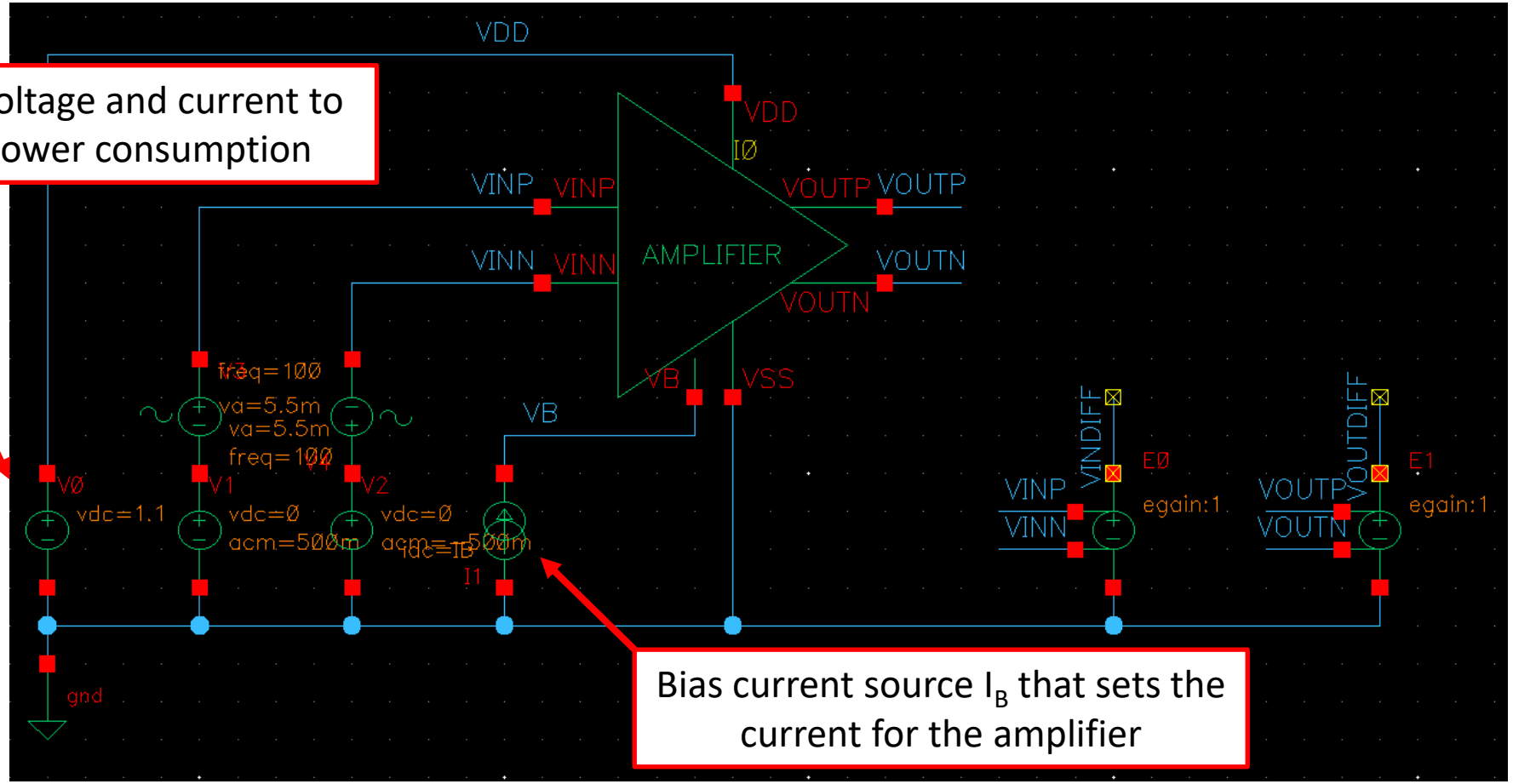
| Amplifier |
| --- |
| IRN = 2.4$\mu V_{rms}$ |
| BW = 0.5Hz – 6kHz |
| Input range = 18$mV_{pp}$ |
| Output range = 1$V_{pp}$ |
| $Z_{in} \geq 32M\Omega$ |
| Gain = 50V/V |

Additional remark: from now on, we'll specify and evaluate the input impedance at 3kHz (the middle of the BW). Also note this is a minimum requirement, so a higher value is fine as well.

- Additionally, you may assume that the supply voltage (VDD) is 1.1V

# AMPLIFIER_TB

- Overall test bench to run your simulations on

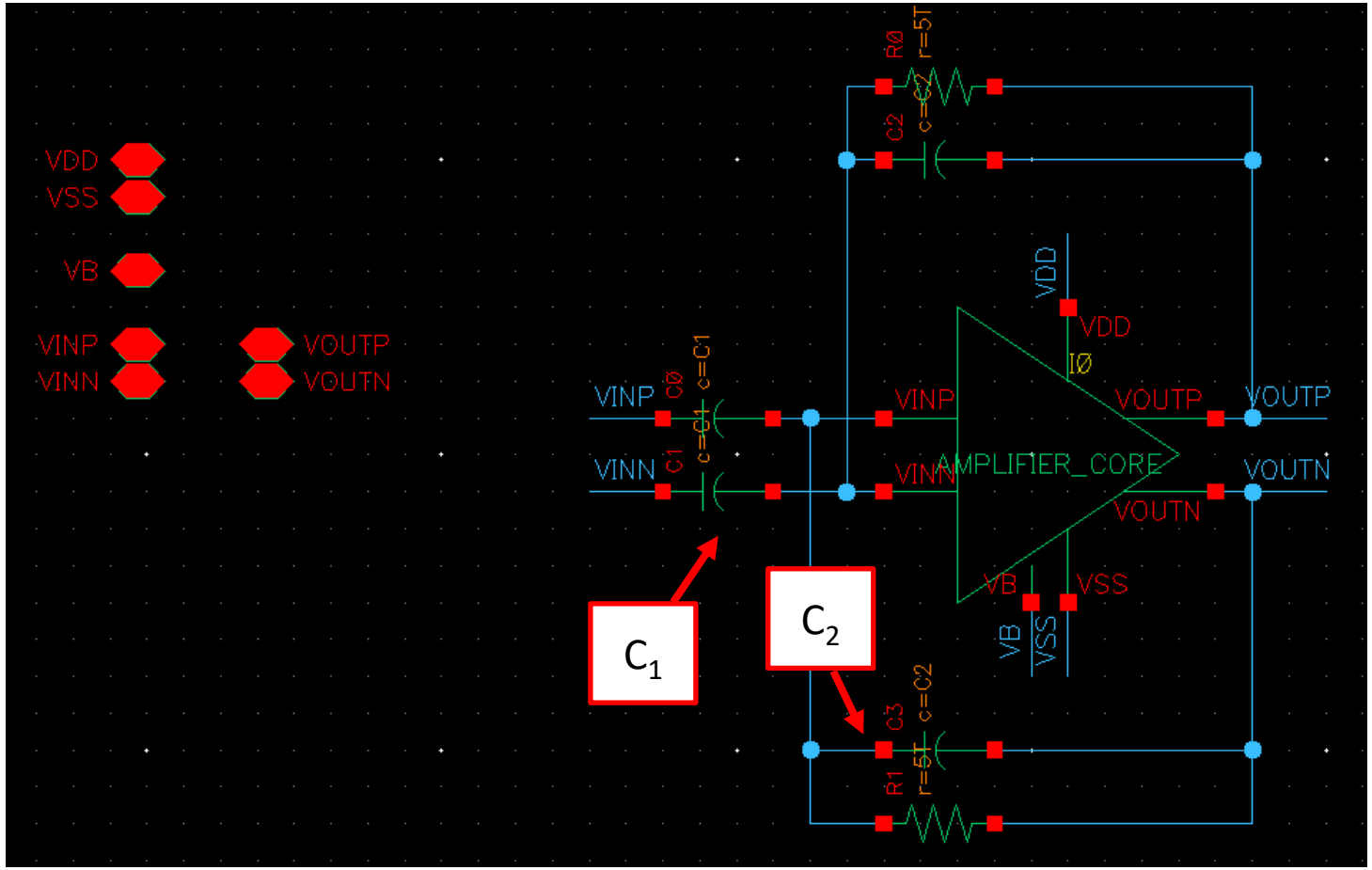



Power supply. Check its voltage and current to determine the overall power consumption

Bias current source $I_B$ that sets the current for the amplifier

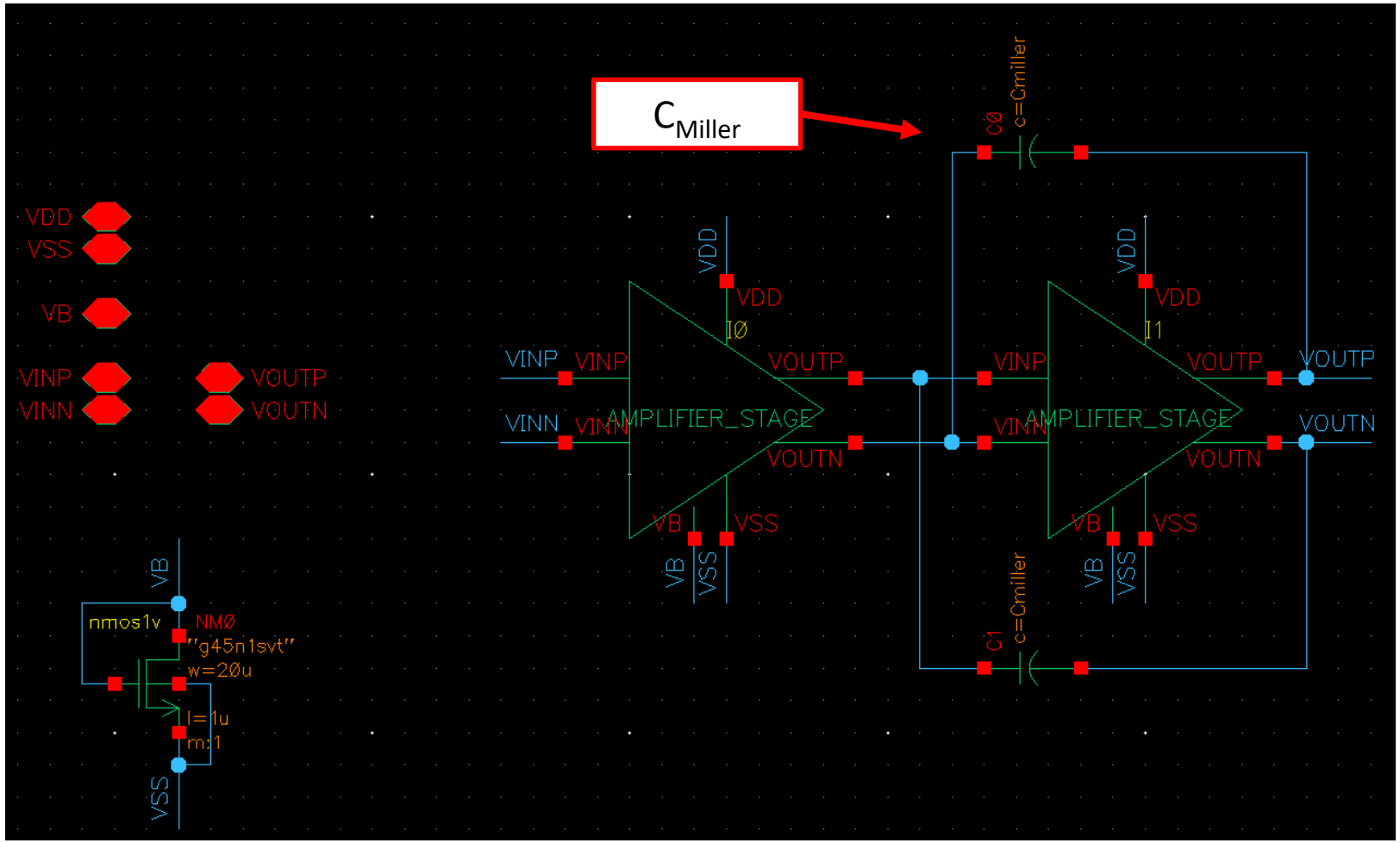
# AMPLIFIER

- Topology: the same as the AC-coupled amplifier in the lecture
  - Capacitors set the gain
  - Resistor is to bias the amplifier (already set)



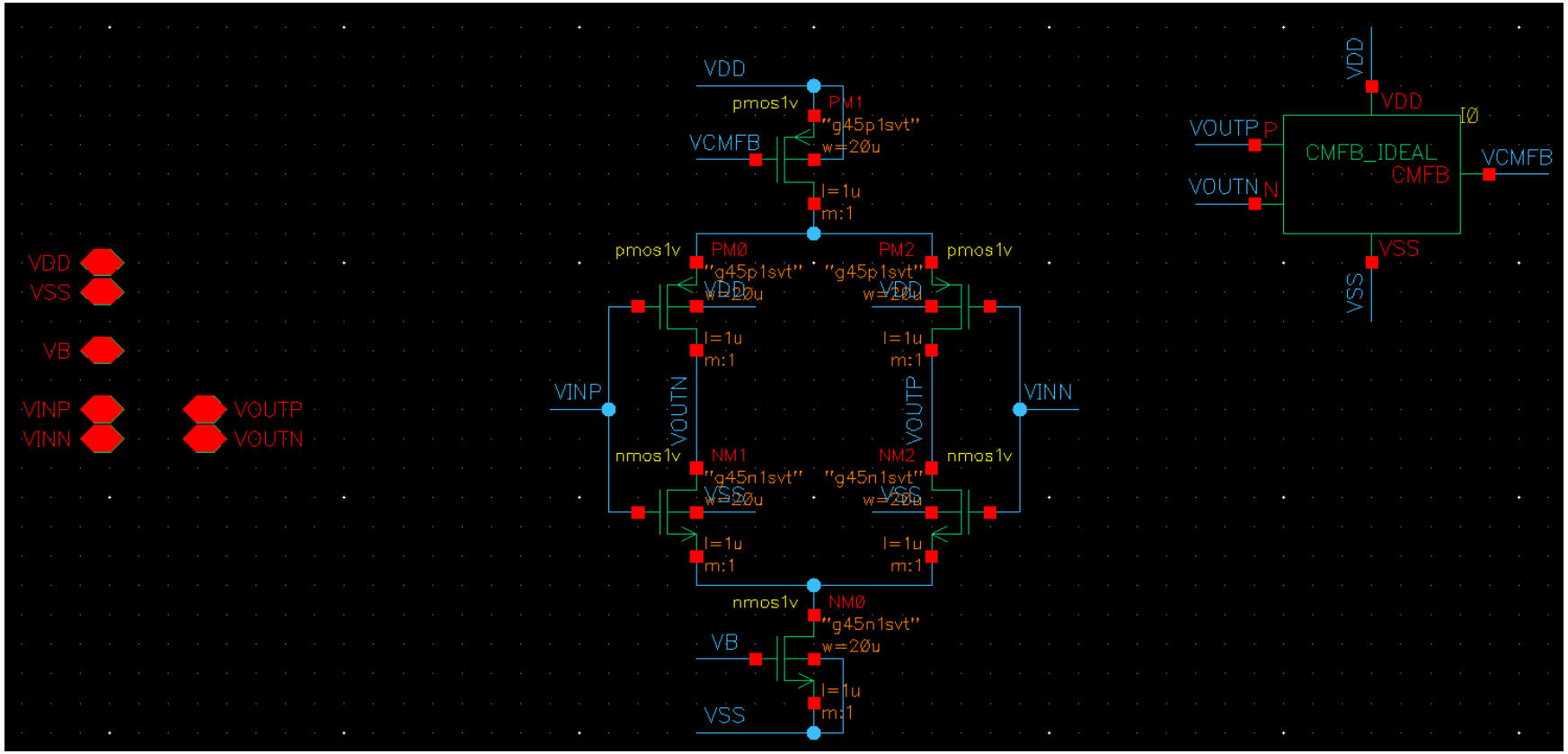
# AMPLIFIER_CORE

- Composed of 2 identical stages in series (to get enough total gain)
- Identical bias current ($I_B$) is copied to both stages with current mirrors
- Miller capacitors are added to the second stage to create a dominant pole which makes the system stable;
  it also limits the bandwidth



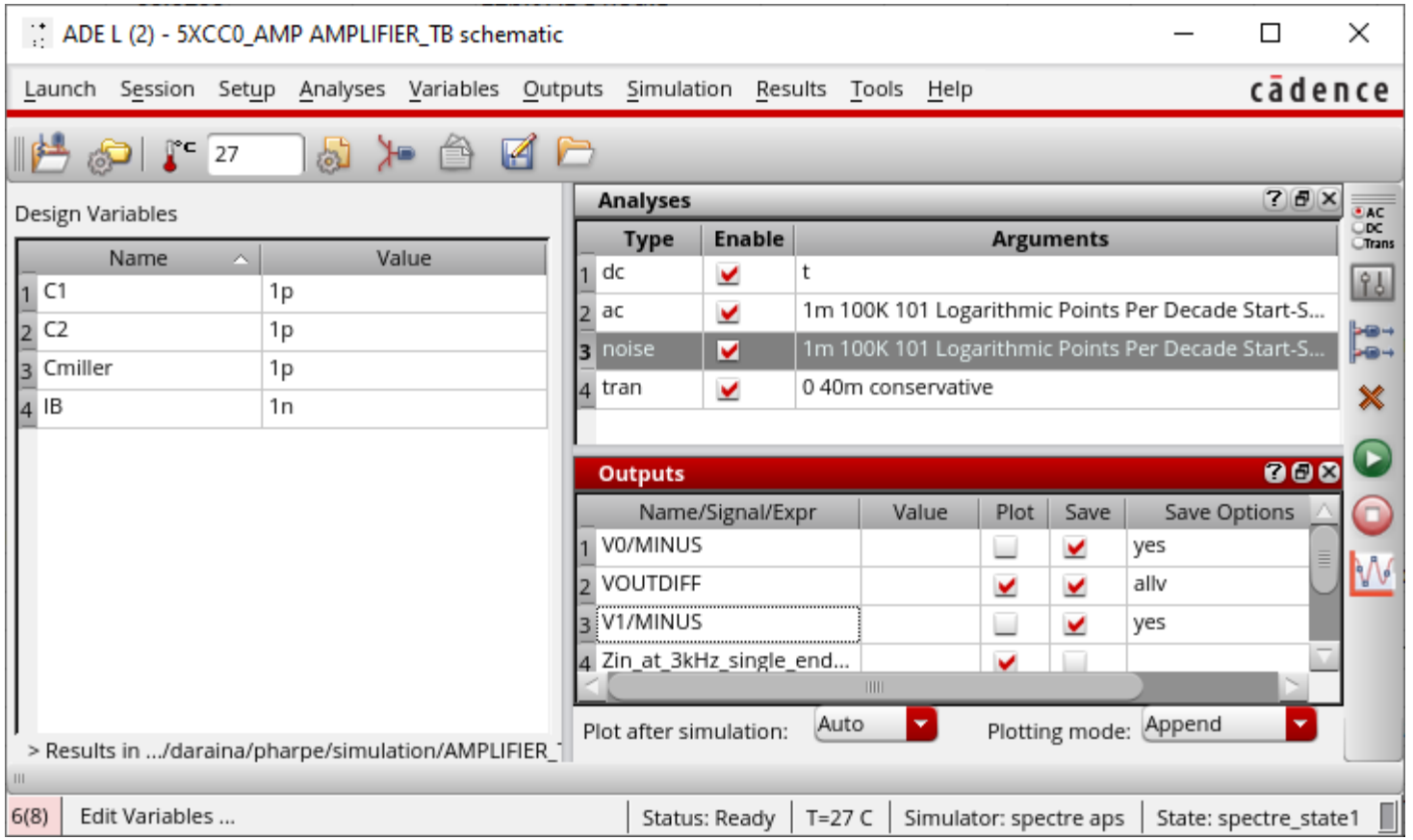
# AMPLIFIER_STAGE

- A differential version of an inverter-based amplifier
  - Tail current source is set by $I_B$
  - Ideal CMFB sets the common-mode to mid-supply



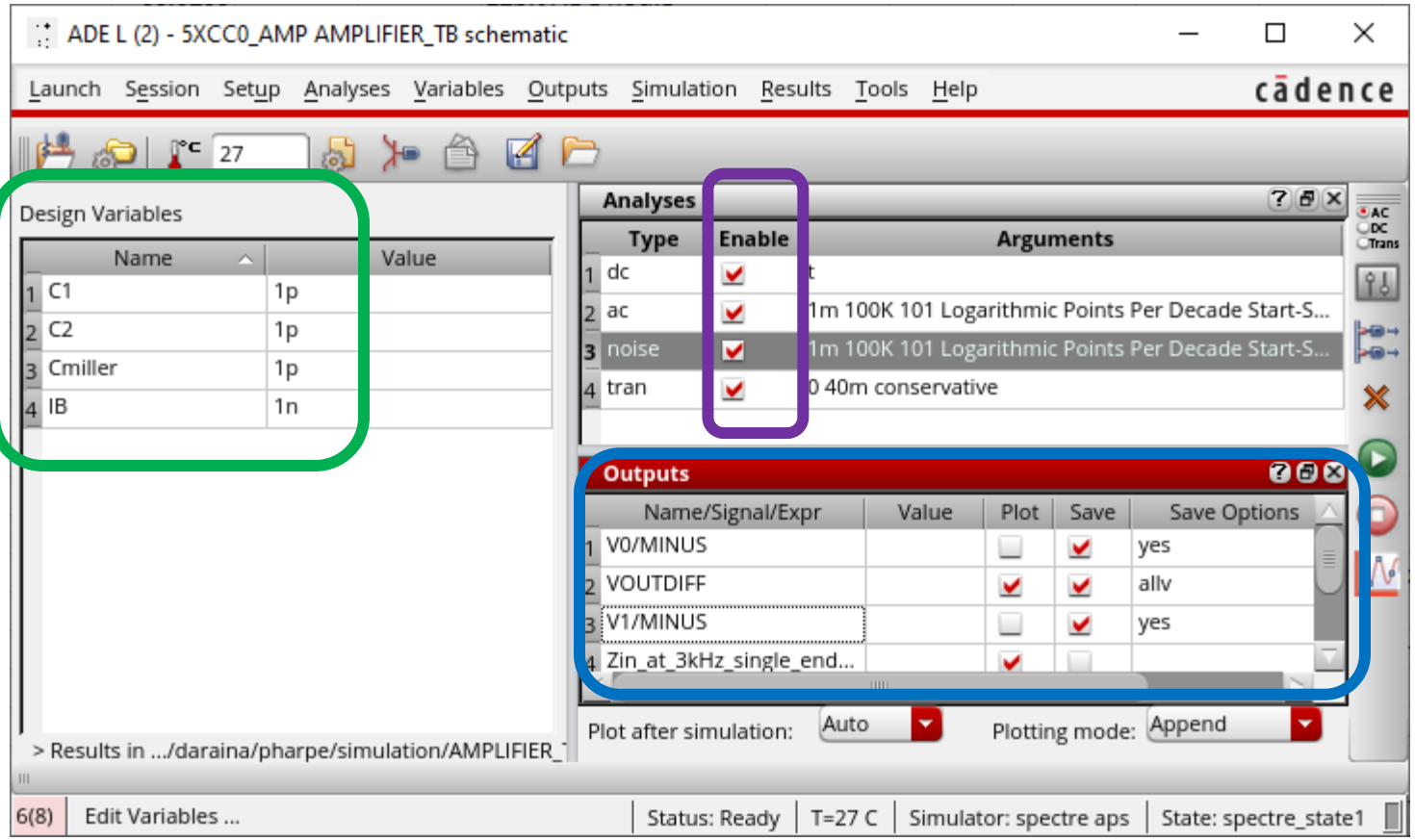
# Running Simulations

- To run simulations on the amplifier:
  - Open AMPLIFIER_TB schematic
  - Start ADE L
  - Load the existing state (see picture)
- All required simulations will be set up correctly



# Running Simulations

- The goal of this assignment is to find the correct values for $C_1$, $C_2$, $C_{Miller}$, and $I_B$, and to run simulations to verify the results.
  - All values can be set in ADE L (green box)
  - Results can be observed in the plots, $Z_{in}$ is calculated automatically (blue box)
  - Analyses types can be enabled/disabled as desired (purple box)



# Step 1: Choosing the Capacitors

Assume that the smallest capacitor that we can use is 1pF. Further assume that we want to minimize the capacitor values (to save area and power, and to increase impedances). With this information, calculate your answers for questions 5, 6, and 7. You don't need to perform any simulations yet.

Question 5: What is the required value for $C_1$? *

Question 6: What is the required value for $C_2$? *

Question 7: What is the calculated (single-ended) input impedance at 3kHz for the selected value of $C_1$?

* For Question 5 and 6, you can ignore the $Z_{in}$ requirement, you only need to consider the gain requirement and respect the minimum value that can be used (1pF).

Since we cannot achieve the desired input impedance, we will add positive feedback: Add 2 capacitors to the AMPLIFIER schematic to create positive feedback to enhance the input impedance. Give these capacitors the same value as $C_2$.

*Note: Questions 5, 6, 7 should be answered before you add this extra positive feedback!*

# Step 2: Choosing the Bias Current $I_B$

- Based on the IRN requirement, we can estimate the required $I_B$
- We assume that the circuit only has shot noise (and no 1/f noise). This is not so realistic, but it makes the design process for the moment more understandable. The 1/f noise in the Cadence setup is also disabled.
- There are quite a few steps involved, so let's go step by step:
- Most likely the 4 input transistors (2 NMOS and 2 PMOS devices) in the first amplifier stage will be the most critical devices for the overall amplifier IRN. Why?
- Assuming this is true, we'll calculate their input-referred noise as function of $I_B$.
- Express the $I_D$ for each of these transistors as function of $I_B$.
- Express the $S_I^2(f)$ of each transistor as function of $I_B$ (assume the formula 2 q $I_D$ for each transistor)
- Why is the total noise current power spectral density for the amplifier $S_{I,total}^2(f) = 4\ S_I^2(f)$?
- Express the $g_m$ of each transistor as function of $I_B$ (assume $g_m/I_D = 25$)
- Why is the total $g_m$ of the amplifier approximately $g_{m,total} = 2\ g_m$?
- Using $g_{m,total}$, calculate $S_{I,total}^2(f)$ back to an input noise voltage $V_{gn}^2(f)$ as function of $I_B$
- Knowing the $V_{gn}^2(f)$ and the bandwidth, what will be the total input referred noise power, and thus the total input referred noise voltage (in $V_{rms}$), as function of $I_B$?
- Equate the last value to the requirement for IRN and solve $I_B$.
- Round $I_B$ to a multiple of 100nA. Use the rounded value for the further steps of this assignment.

Question 8: What is your calculated value for $I_B$?

# Step 3: Simulate to Determine $C_{Miller}$

- Open the AMPLIFIER_TB, start ADE L, and load the existing state
  - Set the parameters $C_1$, $C_2$, and $I_{BIAS}$ as determined in Step 1 to 2
- Run all simulations that are defined
  - Use the DC operating point to check that the 4 input transistors are indeed biased in sub-threshold. How can you confirm that?
  - Use the AC simulation to verify that the gain reaches about 50x.
- Adjust $C_{Miller}$ until the -3dB bandwidth is approximately at 6kHz.
  - Pick the value from this list: 1pF, 5pF, 10pF, 15pF, 20pF
  - Note that the -3dB bandwidth is the frequency at which the gain is reduced by 3dB (i.e. by a factor $\sqrt{2}$) compared to the low-frequency gain
- Question 9: What is your selected value for $C_{Miller}$?

# Step 4: Final Simulations for Verification

- Now all values are set, run all simulations to check the following things:
  - Check the power consumption from the DC operating point of the supply source
  - Check the gain and the BW from the AC simulation
  - Check the input referred noise (in ADE L: Results → Direct plot → Squared input noise), integrate this from 0.5Hz up to 6kHz using the calculator, and recalculate it to $V_{rms}$
  - Check $Z_{in}$ at 3kHz (shown in ADE L as a value)
  - Check that the output range can reach approximately $1V_{pp}$ using the transient simulation
- Is everything more or less correct (±10% deviations are acceptable)?

# Step 5: Enter Simulated Results in Canvas

- Question 10: What is the simulated input-referred noise (in $\mu V_{rms}$)?
- Question 11: What is the simulated single-ended input impedance at 3kHz (in MΩ)?
- Question 12: What is the simulated DC power consumption (in µW)?