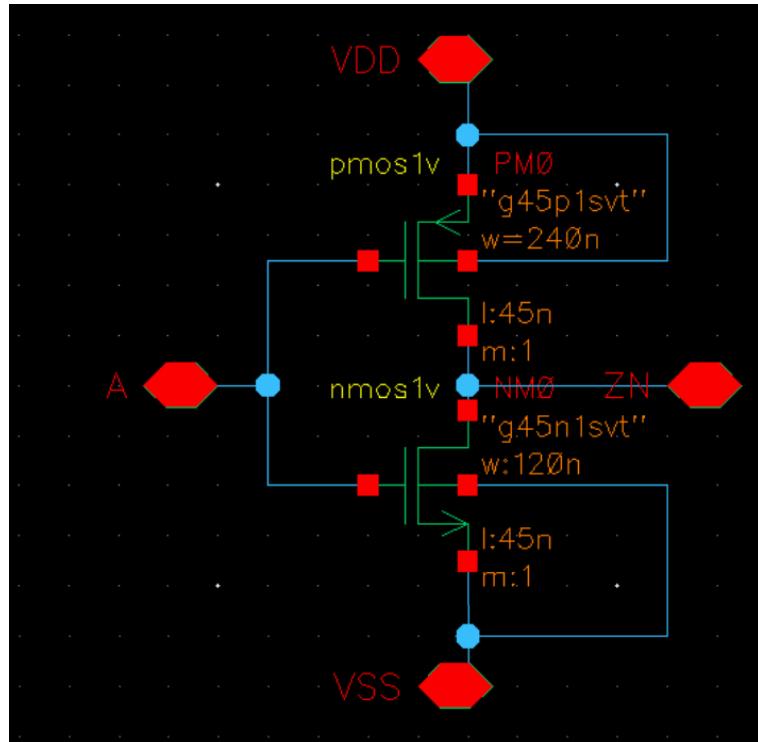
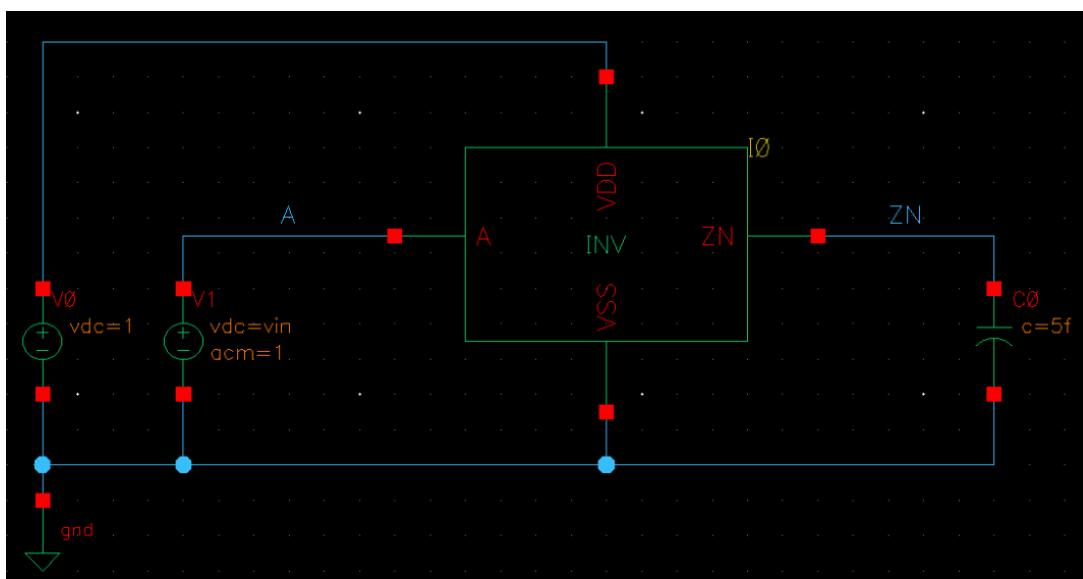


Daniel Tyukov  
1819283

Inverter Schematic:



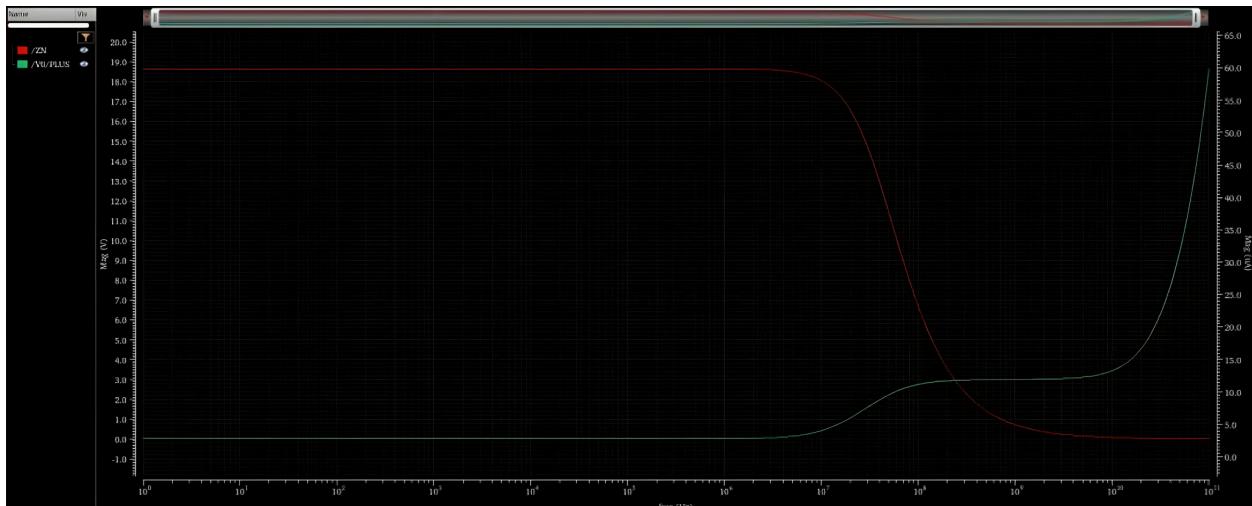
Inverter Testbench:



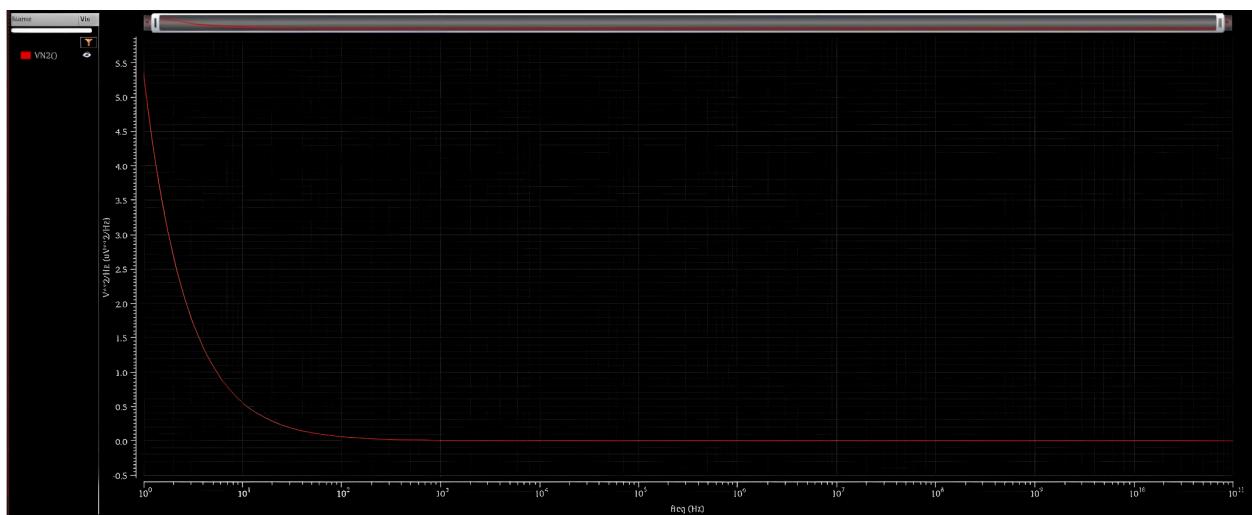
## DC Simulation Results:



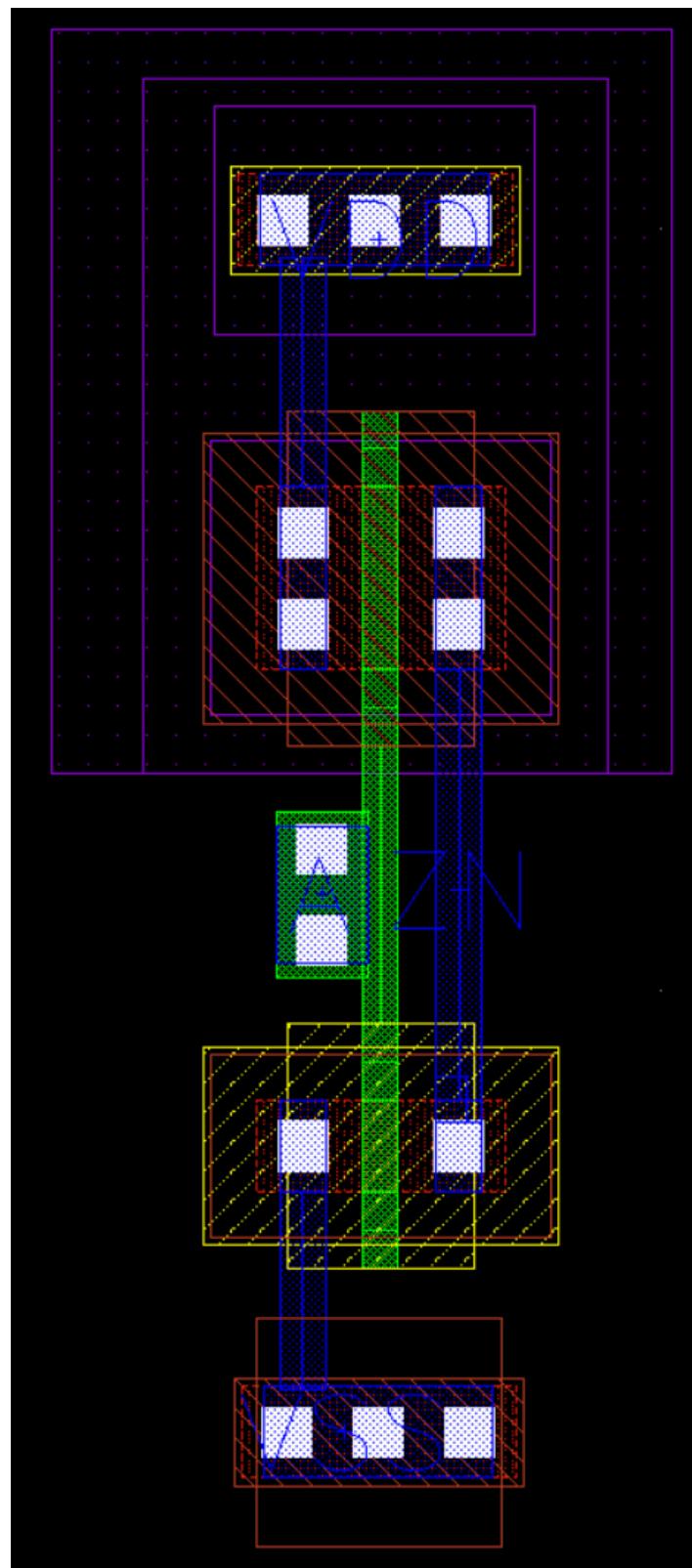
## AC Simulation Results:



## Noise Simulation Results:



**Inverter:**



### DRC Window:



### LVS Result:

Run: "INV"

Run: "INV" from  
/home/daraina/20221525/Cadence\_GPDK045/Assura

Schematic and Layout Match.  
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

Extraction Information:

---

0 cells have 0 mal-formed device problems  
0 cells have 0 label short problems  
0 cells have 0 label open problems

Comparison Information:

---

0 cells have 0 Net mismatches  
0 cells have 0 Device mismatches  
0 cells have 0 Pin mismatches  
0 cells have 0 Parameter mismatches

ELW Information:

---

Total DRC violations: 0

**Yes**   **No**   **Help**





### Parasitics in schematic:

