Computation II - 5EIB0
Lab 0: Setting up the board v1.1

The goal of this lab is to verify that you have a working Virtual Machine (VM) and Pynq board setup. This document assumes that you have installed the computation VM using the "Virtual Machine Installation Guide and Tutorial", and have already completed the "Pynq Basics Tutorial".

Contents

1 Board and VM Configuration

During Computation I you have been booting the board from the SD-card. During the boot process the ARM cores and FPGA are programmed with the predefined state on the SD-card. You are then able to log in to the Linux environment and make software programs that execute on the ARM cores. Unfortunately, (while technically possible) it is not practical to create FPGA designs on the ARM cores of the FPGA.
In Computation II, we will use the JTAG interface to program the hardware designs that you will create, directly into the FPGA. The USB cable that you have already been using in previous tutorials provides access to the JTAG interface. The following instructions explain how to configure your VM and Pynq board to use the JTAG interface.

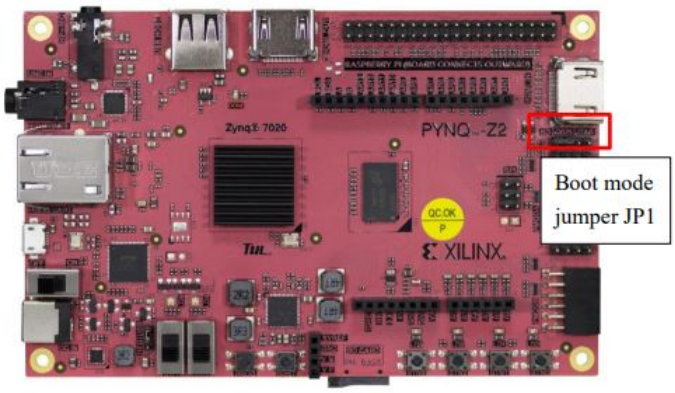

Figure 1: Location of the PYNQ board boot mode jumper highlighted.

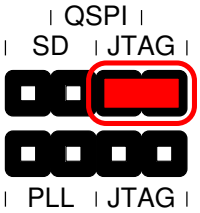

Figure 2: Boot mode jumper configuration for JTAG programming.

Task 1. Make sure that your Pynq board is powered off. Locate the boot mode jumper on your Pynq board, see Figure 1. With the text on the board the correct way up, only one jumper should connect the last two pins on the right side of the top row, see Figure 2.

Task 2. Boot the Computation Virtual machine on your computer. Connect your PYNQ board to your computer using the USB cable. Power the board on using the switch on the board. In the VirtualBox "Devices" menu, select the "USB" sub-menu. Click on the entry "Xilinx TUL [0700]" to connect the board to the VM. You should see a tick beside this entry in the menu when it is connected.

Task 3. Place the file `board_tester.bit` from the OnCourse page in your SharedWork folder.

2 Simple Setup Test

The `board_tester.bit` file is an example of a bitstream file that contains information to configure the FPGA portion of the Zynq chip on your Pynq Board. To verify that your VM and Pynq board are configured correctly, you will program the FPGA using this bitstream from your VM via the JTAG interface. If the test is successful, LEDs LD0-3 will blink continuously.

Task 4. Program the bitstream

1. Open Vivado
2. Click on "Open Hardware Manager".
3. Connect the board, click on "Open Target" and select "Auto Connect".
4. Click on "Program Device".
5. Select the bitstream file (`board_tester.bit`) in the window and click on "Program".
6. If everything went correctly than the LEDs (LD0-3) should be blinking.

Note: If the connection between Vivado and the board stops working, simply power the board off and on again. After power cycling the board, do not forget to reopen the target in Vivado.