

Computation II: embedded system design (5EIB0)

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Started on Thursday, 11 April 2024, 1:24 PM

State Finished

Completed on Thursday, 11 April 2024, 5:33 PM

Time taken 4 hours 9 mins

Grade 13.00 out of 13.00 (100%)

Question 1

Correct

Mark 0.50 out of 0.50

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Fill in the corresponding MIPS code for the following C statement. Assume that the variables i, and j are assigned to registers \$s3 and \$s4 respectively.

C statement: $B[8] = A[i-j];$

MIPS code:

```
sub $t0, $s3, $s4 ✓  
add $t0, $s6 , $t0 ✓  
lw $t1, 16($t0)  
sw $t1, 32($s7 ) ✓
```

Question 2

Correct

Mark 0.50 out of 0.50

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Assume \$t0 holds the value 0x00101000.

Consider the following piece of assembly code:

```
slt $t2, $zero, $t0  
bne $t2, $zero, ELSE  
j DONE  
ELSE: addi $t2, $t2, 2  
DONE:
```

What is the decimal value of \$t2 after these instructions?

Answer: 3



The correct answer is: 3

Question 3

Correct

Mark 0.50 out of 0.50

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Consider the following sequence of instructions.

```
add r5 , r2 , r1  
lw r3 , 4 (r5)  
lw r2 , 0 (r2)  
or r3 , r5 , r3  
sw r3 , 0 (r5)
```

Assume forwarding and hazard detection is not working properly. The programmer has to manually insert **nops** to properly stall the processor. **How many nops should be inserted** by the programmer to this sequence of instructions to ensure correct execution (the minimum number)? Assume 3 stall cycles.

Answer: 8



Question 4

Correct

Mark 0.50 out of 0.50

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consider the following instructions.

Instruction 1: BNE R1, R2, Label

Instruction 2: LW R1, 0(R1)

Which exceptions can each of these instructions trigger? For each of these exceptions, specify the pipeline stage in which it is detected.

Select one:

- a. Instruction 1: invalid target address (EX)
- b. Instruction 1: invalid data address (MEM)
- c. Instruction 1: invalid data address (EX)
- d. Instruction 1: invalid target address (MEM)

- Instruction 2: invalid data address (MEM) ✓
- Instruction 2: invalid target address (EX)
- Instruction 2: invalid target address (MEM)
- Instruction 2: invalid data address (EX)

Your answer is correct.

The correct answers are: Instruction 1: invalid target address (EX)
address (MEM) Instruction 2: invalid data address (EX)

Instruction 2: invalid data address (MEM), Instruction 1: invalid target

Question 5

Correct

Mark 0.50 out of
0.50

 Flag question

Select all the statements that are **true**.

Select one or more:

- a. The following is a necessary, but not sufficient, condition for coherence: *writes to the same location are serialized. Two writes to the same location by any two processors are seen in the same order by all processors.* ✓ True.
- b. The following is a necessary, but not sufficient, condition for coherence: *a read by a processor P to a location X that follows a write by P to X, with no other writes of X by another processor occurring between the write and the read by P, may return the written value or the values that was previously contained in X.*
- c. In a multiprocessor system, the value read in a cache is always the same as the value read in its corresponding memory address.
- d. The following is a necessary, but not sufficient, condition for coherence: *a read by a processor to location X that follows a write by another processor to X returns the written value if the read and write are sufficiently separated in time and no other writes to X occur between the two accesses.* ✓ True.
- e. A *write invalidate protocol* can be used to maintain coherence between caches and main memory ensuring that no other readable or writable copies of an item exist when the *write occurs*. ✓ True.

Your answer is correct.

The correct answers are: A *write invalidate protocol* can be used to maintain coherence between caches and main memory ensuring that no other readable or writable copies of an item exist when the *write occurs*., The following is a necessary, but not sufficient, condition for coherence: *a read by a processor to location X that follows a write by another processor to X returns the written value if the read and write are sufficiently separated in time and no other writes to X occur between the two accesses.*, The following is a necessary, but not sufficient, condition for coherence: *writes to the same location are serialized. Two writes to the same location by any two processors are seen in the same order by all processors.*

Question 6

Correct

Mark 0.75 out of
0.75

 Flag question

Consider a write-back direct-mapped cache with 64-bit address. It uses bits 0-1 for Offset, bits 2-11 for the Index and the remaining address bits 12-63 as Tag.

What is the cache block size in (4-byte) words?

Answer: 16



The correct answer is: 16

Question 7

Correct

Mark 0.75 out of
0.75

 Flag question

Consider a write-back direct-mapped cache with 32-bit address. It uses bits 0-4 for Offset, bits 5-9 for the Index and the remaining address bits 10-31 as Tag.

How many entries does the cache have?

Answer: 32



The correct answer is: 32

Question 8

Correct

Mark 0.75 out of
0.75[Flag question](#)

Consider a write-back direct-mapped cache with 32-bit address. It uses bits 0-4 for Offset, bits 5-9 for the Index and the remaining address bits 10-31 as Tag.

What is the total cache size (counting all bits), in bits?

Answer: 

The correct answer is: 2816

Question 9

Correct

Mark 0.50 out of
0.50[Flag question](#)

Assume the breakdown of dynamic instructions into various instructions categories as follows:

R-Type	BEQ	JMP	LW	SW
40%	25%	5%	25%	5%

Also, assume the following branch prediction accuracies:

Always-Taken	Always-Not-Taken	2-Bit
45%	55%	85%

Calculate the exact extra CPI due to the mispredicted branches with the Always-Taken predictor. Assume that branch outcomes are determined in the EX stage (meaning that the number of stall cycles due to a mispredicted branch is 3), that there are no data hazards, and that no delay slots are used.

Answer: 

The correct answer is: 0.4125

Question 10

Correct

Mark 0.50 out of
0.50[Flag question](#)

Consider a microprocessor with $CPI_{ideal} = 4$, an instruction cache Icache and a data cache Dcache.

The Icache miss rate is 4%, while the Dcache miss rate is 4%.

The percentage of load and store instruction is 37%.

The miss penalty is 38 cycles.

Calculate the Slowdown of the processor, in terms of $CPI_{with\ cache\ miss}/CPI_{ideal}$. Use 2 decimal ciphers in your answer (2 becomes 2.00, 3.0151 becomes 3.02).

Answer: 

The correct answer is: 1.5206 +/- 0.1

Question 11

Correct

Mark 0.25 out of
0.25[Flag question](#)

Suppose a 4-way set-associative cache has a capacity of 32 KiB (1 KiB = 1024 bytes) and each block consists of 64 Bytes. What is the total number of blocks in the cache? What is the number of sets?

Total number of blocks : Number of sets : 

Your answer is correct.

Question 12

Correct

Mark 0.50 out of
0.50

[Flag question](#)

Consider a microprocessor with $CPI_{ideal} = 3$, an instruction cache Icache and a data cache Dcache.

The Icache miss rate is 2%, while the Dcache miss rate is 9%.

The percentage of load and store instruction is 35%.

The miss penalty is 45 cycles.

As in the previous question, calculate the Slowdown of the processor, in terms of $CPI_{with\ cache\ miss}/CPI_{ideal}$.

Consider then to double the processor's clock frequency. Calculate the new $CPI_{double\ freq}$ and calculate the Speedup in terms of $T_{exec-with\ cache\ miss}/T_{exec-double\ freq}$. **Submit the Speedup as your answer.**

Use 2 decimal ciphers in your answer (2 becomes 2.00, 3.0151 becomes 3.02).

Answer:



The correct answer is: 1.3929273084479 \pm 0.1

Question 13

Correct

Mark 0.50 out of
0.50

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Consider a microprocessor with $CPI_{ideal} = 3$.

Assume that 10% of the instructions are branches.

The percentage of taken branches is 41%.

The penalty when a branch is taken is 1 cycle(s), while when the branch is not taken there is no penalty.

Calculate the Slowdown of the processor, in terms of $CPI_{with\ branches}/CPI_{ideal}$.

Use 2 decimal ciphers in your answer (2 becomes 2.00, 3.0151 becomes 3.02).

Answer:



The correct answer is: 1.0136666666667 \pm 0.010136666666667

Question 14

Correct

Mark 0.50 out of
0.50

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In this configuration, the access times and hit rates are the following:

Processor	Execution Time (ns)	2
L1 Cache	Time (ns)	26
	Hit Rate (%)	74
L2 Cache	Time (ns)	202
	Hit Rate (%)	67
L3 Cache	Time (ns)	1544
	Hit Rate (%)	51
Main Memory	Time (ns)	29018
	Hit Rate (%)	100

What is the Average Memory Access Time (in nanoseconds)? Use at least 2 decimal digits in your answer.

Answer: 1430.97



The correct answer is: 1430.969956 +/ 14.30969956

Question 15

Correct

Mark 0.50 out of 0.50

Flag question

What is the result in the terminal when running the following code?

```
#include <stdio.h>
#include <unistd.h>
#include <sys/types.h>

int main(){
    pid_t pid_value;
    printf("PID before fork(): %d\n", (int)getpid());

    pid_value = fork();
    if (pid_value!=0){
        printf("Parent. PID = %d\n", (int)getpid());
    }
    else{
        printf("Child. PID = %d\n", (int)getpid());
    }
}
```

Select one:

- a. PID before fork(): 1169
Parent. PID = 1170
Child. PID = 0
- b. PID before fork(): 1434
Child. PID = 0
- c. PID before fork(): 342 ✓
Parent. PID = 342
Child. PID = 343
- d. PID before fork(): 1315
Parent. PID = 1316

Your answer is correct.

PID before fork(): 342

Parent. PID = 342

Child. PID = 343

Question 16

Correct

Mark 0.75 out of 0.75

Flag question

Consider three branch prediction schemes: predict not taken, predict taken, and dynamic prediction. Assume that they all have zero penalty when they predict correctly and two cycles when they are wrong. Assume that the average predict accuracy of the dynamic predictor is 90%. Which predictor is the best choice for the following branches?

A branch that is taken with 5% frequency

Predict non taken



A branch that is taken with 70% frequency

Dynamic prediction



A branch that is taken with 95% frequency

Predict taken



Your answer is correct.

The correct answer is: A branch that is taken with 5% frequency → Predict non taken, A branch that is taken with 70% frequency → Dynamic prediction, A branch that is taken with 95% frequency → Predict taken

Question 17

There are three different types of hazards events:

Correct
Mark 0.75 out of 0.75
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- A Structural ✓ hazard occurs when a required resource is busy.
A Data ✓ hazard occurs when a instruction needs to wait for a previous one to finish loading or storing a register.
A Control ✓ hazard occurs when the next instruction is not directly known.

One method of resolving data hazard is called [Forwarding] ✓, in which the missing data element is retrieved from internal buffers.

[Stall](#) [Instruction](#) [Pipeline](#) [Forwarding](#) [Control](#) [ALU](#) [Structural](#) [Data](#)

Your answer is correct.

The correct answer is:

There are three different types of hazards events:

A [Structural] hazard occurs when a required resource is busy.

A [Data] hazard occurs when a instruction needs to wait for a previous one to finish loading or storing a register.

A [Control] hazard occurs when the next instruction is not directly known.

One method of resolving data hazard is called [Forwarding], in which the missing data element is retrieved from internal buffers.

Question 18

Correct
Mark 0.50 out of 0.50
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Consider the 5-stage pipelined MIPS processor, as described in the book, running the following code (9 instructions):

```
lw $t0, 64($zero)
lw $t1, 0($t0)
lw $t2, 4($t0)
add $t5, $t5, 8
add $t3, $t1, $t2
sw $t3, 12($t0)
lw $t4, 8($t0)
add $t5, $t1, $t4
sw $t5, 16($t0)
```

How many cycles are required for the execution of this code when **no forwarding** circuitry has been implemented? Assume **3 stall cycles** in case of RaW dependencies. Omit the 4 cycles required to fill the pipeline.

Answer: 23 ✓

The correct answer is: 23

Question 19

Correct
Mark 0.50 out of 0.50
[Flag question](#)

Consider the 5-stage pipelined MIPS processor, as described in the book, running the following code (8 instructions):

```
lw $t1, 0($t0)
lw $t2, 4($t0)
add $t3, $t1, $t2
add $t3, $t2, $t3
sw $t3, 12($t0)
lw $t4, 8($t0)
add $t5, $t1, $t4
sw $t5, 16($t0)
```

How many cycles are required for the execution of this code with **all possible forwarding (bypassing)** and **remaining hazard detection** circuitry implemented? You may omit the 4 cycles required to fill the pipeline. (Hint: Carefully check all the RaW dependencies).

Answer: 10 ✓

The correct answer is: 10

Question 20

Correct
Mark 0.25 out of 0.25
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Consider the following sequence of instructions, which involves one or more load-use hazards:

```
lw $t0, 0($a0)
addi $t0, $t0, 1
sw $t0, 0($a0)
addi $a0, $a0, 4
```

How many data hazards cannot be resolved by forwarding?

Answer: 1



The correct answer is: 1

Question 21

Correct

Mark 0.25 out of 0.25

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The target of a j instruction (unconditional jump) is computed in the ID stage of the 5-stage MIPS pipeline. How many instructions must be flushed each time a j instruction is executed?

Answer: 1



The correct answer is: 1

Question 22

Correct

Mark 0.50 out of 0.50

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The following code is run on the 5-stage MIPS pipeline with full forwarding. Branch targets and decisions are resolved in the ID stage, and branches are always predicted not taken.

```
# a0 = head node of list
li $v0, 0
loop:
    beq $a0, $0, done
    lw $t0, 0($a0)
    add $v0, $v0, $t0
    lw $a0, 4($a0)
    j loop
done:
    # other code
```

If the linked list has length 10000, how many cycles will the above code take to execute?

Answer: 70000



The correct answer is: 70007 +/- 10

Question 23

Correct

Mark 0.50 out of 0.50

[Flag question](#)

The code is converted into a do-while form as follows. Code is run on the 5-stage MIPS pipeline with full forwarding. Branch targets and decisions are resolved in the ID stage, and branches are always predicted not taken.

```
# a0 = head node of list
li $v0, 0
loop:
    lw $t0, 0($a0)
    add $v0, $v0, $t0
    lw $a0, 4($a0)
    bne $a0, $0, loop
    # other code
```

If the linked list has length 10000, how many cycles will the above code take to execute?

Answer: 80000



The correct answer is: 80004 +/- 10

Question 24

Correct

Mark 0.50 out of

The code is restructured into the following form. Code is run on the 5-stage MIPS pipeline with full forwarding. Branch targets and decisions are resolved in the ID stage, and branches are always predicted not taken.

```
loop:
```

0.50

[Flag question](#)

```

lw $t0, 0($a0)
lw $a0, 4($a0)
add $v0, $v0, $t0
bne $a0, $0, loop

```

If the linked list has length 10000, how many cycles will the above code take to execute?

Answer: 60000



The correct answer is: 60004 +/- 10

Question 25

Correct

Mark 0.50 out of 0.50

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Assume that individual stages of the MIPS data-path have the following latencies:

IF	ID	EX	MEM	WB
150ps	200ps	250ps	500ps	150ps

Furthermore we assume that the instructions executed by the processor have the following distribution:

alu	beq	lw	sw
13%	18%	29%	40%

What is the maximum frequency in a pipelined MIPS processor (in GHz)?

Answer: 2



The correct answer is: 2 +/- 0.2

Information

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