Computation II: embedded system design (5EIB0)

Started on	Wednesday, 10 April 2024, 1:46 AM
State	Finished
Completed on	Wednesday, 10 April 2024, 2:15 AM
Time taken	28 mins 52 secs
Grade	**5.00** out of 5.00 (**100**%)

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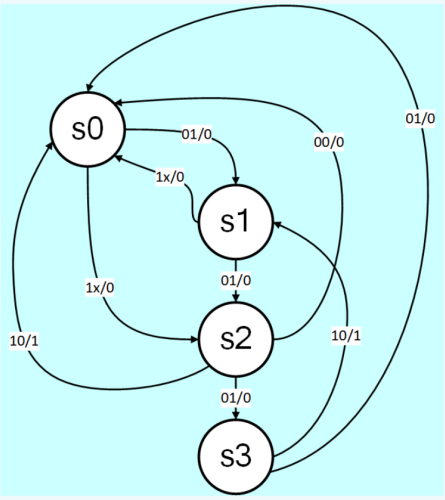
Question **1**
Correct
Mark 1.00 out of 1.00
Flag question

The following diagram represents the states transition of a Mealy FSM. The format of the transition represented on the edges is *inputs (2 bits) / output (1 bit)*. At each positive edge of the *clock* signal it will check the values of its inputs and move to the corresponding state. The input combinations that are not represented in the diagram correspond to self-edges, which are not shown. The output value of a self edge is always 0. The *reset* signal always reset the FSM to the state *s0*.



Which are the states reached by the following testbench? Does the output value change?

```
/* ..... */
reg [1:0] input_signal;
reg reset;
reg clk;
wire out;
fsm_mealy UUT #() (.clk(clk), .reset(reset), .input_signal(input_signal), .out(out));

always @ 10 clk <= ~clk;
initial begin
clk = 0;
input_signal = 2'b0;
reset = 1;
#5 reset = 0;
#10 input_signal = 2'b01;
#40 input_signal = 2'b10;
#20 input_signal = 2'b11;
#20 input_signal = 2'b10;
/* ..... */
```

Select one or more:

- a. s0 ✔
- b. s1 ✔
- c. s2 ✔
- d. s3
- e. The output is always 0.
- f. The output is 1 for 1 cycle. ✔

Your answer is correct.
The correct answers are: s0, s1, s2, The output is 1 for 1 cycle.

Question **2**
Correct
Mark 1.00 out of 1.00
Flag question

Select the correct State Element for each of the following waveforms.

1) D Latch ✔
2) Gated S-R Latch ✔

3) S-R Latch ✔

4) D Flip Flop ✔

Your answer is correct.

The correct answer is:
Select the correct State Element for each of the following waveforms.

1) [D Latch]

2) [Gated S-R Latch]

3) [S-R Latch]

4) [D Flip Flop]

Question 3
Correct
Mark 1.00 out of 1.00
Flag question

You are tuning the branch prediction method of a 5-stage pipelined MIPS processor to suit a particular application. This application is composed of the following proportion of instructions/types of instruction:

```
R-Type 35%
   BEQ 30%
   JMP  5%
    LW 25%
    SW  5%
```

Having performed some benchmarking of the application for three different types of branch predictor, you find the following branch prediction accuracies:

```
    Always-Taken 40%
Always-Not-Taken 60%
          2-Bit 95%
```

Calculate the exact extra CPI (i.e. do not round the result) due to the mispredicted branches with the Always-Taken predictor. Assume that branch outcomes are determined in the EX stage, that there are no data hazards, and that no delay slots are used.

(**Hint: wrong prediction results in 3 stall cycles)**

Answer: 0.54 ✔

The correct answer is: 0.54

Question 4
Correct
Mark 1.00 out of 1.00
Flag question

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2
200ps	250ps	20ps	90ps	90ps	70ps	15ps	10ps

The table above shows the latencies of a processor's datapath.

If only the processor's Instruction Fetch unit has been implemented to be able to fetch consecutive instructions, what would the cycle time of this unit be? Give your answer in ps.

Answer: 250 ✔

The correct answer is: 250

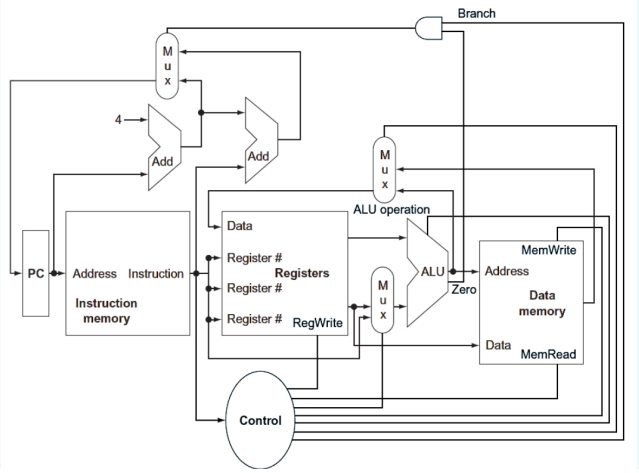
Question 5
Correct
Mark 1.00 out of 1.00
Flag question

The basic single-cycle MIPS implementation from the textbook shown in the Figure below can only implement some instructions. New instructions can be added to an existing ISA. Consider the new instruction:

```
LWI Rt, Rd(Rs)
```

Interpretation: Reg[Rt] = Mem[Reg[Rd]+Reg[Rs]]

Which existing blocks (if any) can be used for this instruction?



Select one or more:

- a. No existing block can be used for the new instruction.
- b. Register Write Port. ✔
- c. Data Memory. ✔
- d. Branch.
- e. Register Read Ports. ✔
- f. ALU. ✔
- g. Instruction Memory. ✔

Your answer is correct.

The correct answers are: Instruction Memory., Register Read Ports., ALU., Data Memory., Register Write Port.

Finish review

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