Flip-Chip for Millimeter-Wave and Broadband Packaging

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Abstract— **Emerging markets for mm-wave wireless and sensor systems as well as high bit-rate components demand for cost-effective packaging solutions. Flip-chip is one of the most promising approaches in this regard combining high-volume potential with excellent high-frequency performance. The talk presents the different flip-chip concepts in use, focusing on the microwave characteristics and approaching the subject from the designer's point of view. Basic electromagnetic properties of the interconnects as well as consequences for chip and package design are discussed. As carrier substrates, conventional ceramics, thin-film, and LTCC-multilayer approaches are covered. Experimental results for various applications document feasibility and capabilities in the frequency range up to 100 GHz.**

Index Terms—**Flip-chip; mm-waves; packaging; multi-chip modules.**

I. Introduction

The millimeter-wave frequency range is receiving increasing interest. Broadband radio links and distribution networks around 40 GHz as well as automotive radar systems at 77 GHz form landmarks for new markets above 30 GHz. And because these are commercial applications which follow the rules of the market, cost and volume have become crucial parameters for system development.

A particularly critical issue in this regard is module packaging, i.e., the way to assemble and connect several MMICs in a multi-chip environment in order to build the mm-wave front-end. The requirements on the packaging scheme are obvious: the interconnects should provide good mm-wave performance (that means primarily: low reflections and low insertion loss) and, at the same time, they should allow for low-cost fabrication. Among the multichip packaging techniques available, the flip-chip approach is considered to be the most promising candidate to meet these requirements.

A similar situation is found in broadband electronics operating at 40 Gbps and more. In contrast to the classical mm-wave systems such as radio links and radars, which are essentially of the narrow-band type, high bit-rate optoelectronics demand for broadband solutions covering the entire range from almost DC to frequencies of 50 GHz and beyond. This puts constraints on the interconnect which are much more challenging than in the conventional mm-wave world.

Is the flip-chip approach the solution to this demand for an interconnect, which shows low parasitics, is broadband, and cheap as well? This has been discussed now for some time and there are a lot of arguments around. It is the purpose of this talk to shed some light on the technical background and to highlight the key issues. This will be done from the designer's point of view. Accordingly, flip-chip technology will be discussed only briefly but the emphasis will be on the electromagnetic effects and the design issues relevant for the higher GHz range.

II. High-Frequency Characteristics of the Flip-Chip Interconnect

The basic flip-chip scheme is illustrated in Fig. 1. The MMIC chip is mounted upside down on a carrier substrate by using metallic bumps as interconnects.

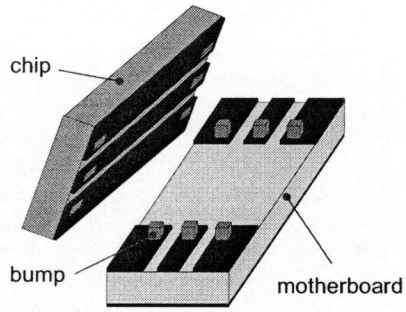

Fig. 1. The flip-chip approach: mounting a flipped chip onto a motherboard using bump interconnects (simplified coplanar geometry with thru-line on chip).

From the electromagnetic point of view, the flip-chip structure affects mm-wave and broadband circuit behavior in mainly two ways:

First, due to flipping, the surface of the motherboard comes close to the chip surface, separated only by an air gap as thick as the bump height. This causes dielectric loading (for a non-metalized motherboard surface) and detunes the chip, the amount of which is determined by the bump height. Thus, from the detuning point of view, bump height should be large. The actual dimensions required depend on the size and the type of structures on the chip. Assuming a coplanar waveguide with

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50 µm ground-to-ground spacing, for instance, bump heights down to 15 µm are acceptable (resulting errors in phase constant and impedance range below 1.5 %). Situation gets worse when using an underfiller between chip and motherboard.

Second, the bump transition itself acts as a discontinuity and causes reflections. For this effect, the bump diameter represents the most critical parameter: the smaller the diameter, the lower the reflection level. On technological reasons, bump height is limited to values slightly smaller than the diameter at maximum. Thus, bump diameter, height, and the size of the corresponding upper and lower pad are not independent.

A closer look reveals that, for the typical mm-wave geometries, it is not the bump height, which determines reflection to first order, but the bump-pad size. The pads on the motherboard and on the chip cause dielectric loading of the transition, which can be identified as the main source of reflections.

The resulting return loss can be considerably improved by layout optimization and suitable compensation techniques, which are well known from wire bonding. But, in contrast to that case, already simple compensation measures yield good broadband behavior over tens of GHz.

It should be noted here that it is not only the bump transition which determines mm-wave characteristics but also the transmission-line concepts on chip and motherboard, which play an important role. For the chip, this refers to the decision between microstrip and coplanar. On the motherboard side, a variety of solutions are available, from the conventional ceramics substrate to LTCC solutions with multi-level wiring or thin-film transmission lines.

III. What Can be Achieved?

The conclusion from the above considerations reads: for optimum mm-wave characteristics, keep bump diameter and pad size as small as possible, depending on the flip-chip process available. As a rule of thumb: For bump diameters in the 30 µm range one achieves excellent broadband characteristics up to mm-wave frequencies. Fig. 2 presents measured data of such a back-to-back structure including two interconnects (the chip contains a homogeneous coplanar line). Broadband features with a return-loss level beyond 20dB from DC to 80 GHz are obtained [1], which demonstrates the potential of the flip-chip concept.

For larger bump diameters in the range 50…80 µm, a similar performance can be achieved when applying appropriate compensation techniques. The resulting bandwidth then still spans 20…30 GHz, which is sufficient for most applications. Published data (e.g., [2,3,4,5]) supports the excellent performance of flip-chip-mounted chips up to W-band frequencies.

IV. The Multi-Chip Module Approach

This basic performance of flip-chip interconnects is greatly influenced by the module approach applied, i.e., the carrier-substrate type and the transmission-line structures used. Parasitic moding, for instance, is a critical issue for mm-wave packaging and needs to be accounted for in design. Thus, interconnect, carrier substrate and housing have to be included into the considerations before the high-frequency performance can be assessed properly. An interesting flip-chip derivative in this regard is the so-called hot-via structure [6], where the chip is placed face-up and the signal line is connected through a via to the backside (which, in particular, yields good compatibility with microstrip chips). A similar approach uses the so-called direct-backside interconnect technology [7].

Among the solutions for the carrier substrate, the following three choices are of specific importance:

- Ceramic and softboard carrier substrates with microstrip or coplanar waveguide
- Thin-film substrates with BCB dielectric employing thin-film microstrip line.
- LTCC substrates with multi-layer capabilities and a variety of line geometries

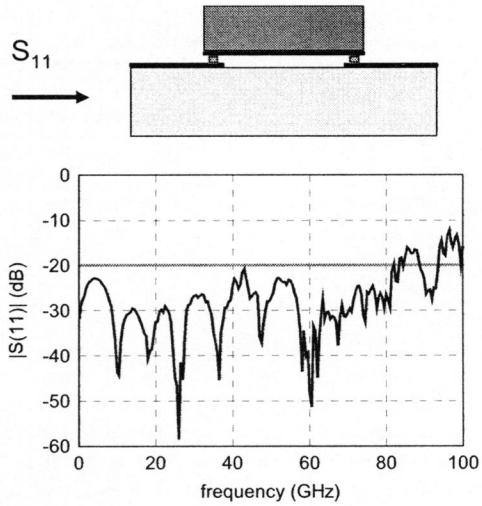

Fig. 2. Input reflection of optimized flip-chip interconnect against frequency (back-to-back structure as shown).

V. Further Aspects and Conclusions

The above considerations focus on the electrical behavior, which, however, is only one part of the whole story (though an important one). Beyond this, the thermal issues must be accounted for. Because the backside of the flipped chip is free, one should consider including thermal bumps near the heat sources. The thermal bumps do not have electrical functions but act as heat sink to the motherboard surface. Also, thermal mismatch between chip and motherboard can be a problem. In this case, an underfiller between chip and motherboard improves reliability (but increases chip detuning).

One should note at this point that, for substrates with low thermal conductivity such as GaAs, flip-chip even offers advantages in heat sinking for power devices. For practical examples see, e.g., [8,9,10]. However, there is still some work to do to have flip-chip power modules fully developed.

These statements emphasize that development of a multi-chip approach is a really multi-disciplinary project, which

must not be restricted to electrical properties but has to include the relevant thermal, mechanical, technological, and, not to forget, cost issues.

Regarding the status of mm-wave packaging so far, flip-chip is widely discussed and implemented into prototypes, but it is not yet common. One reason is that applying this technology implies major investments, which range from assembly-line equipment and foundry requirements (providing bumped chips) to the basics of chip design (moving from microstrip to coplanar).

What will be the future? Flip-chip clearly offers excellent potential in realizing high-frequency interconnects at moderate processing efforts. Hence, in the opinion of the author, for high-performance circuits such as broadband modules the flip-chip technique is a must. Furthermore, the increasing market share of mm-wave Si chips with their surface-oriented wiring will exert a push towards flip-chip equally. The same is true for high pin-count digital ICs, which demand for flip-chip mounting with miniaturized bump interconnects not because of the high-frequency properties but because of the necessity to accommodate a large number of interconnects on a given chip size.

So, this author expects to see more and more flip-chip solutions. On the other hand, there will not be a single flip-chip approach but many different versions adapted to fit the special needs. Some of them may even come without the classical bump, as SMD-like approaches.

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