Developing a Process for System-in-Package Integration of Large-Scale DAC Arrays

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***Abstract*—This work explores a flip-chip–based system-in-package (SiP) strategy that is targeted for the integration of large digital-to-analog converter (DAC) arrays in high-frequency applications, particularly in cutting-edge radar and wireless communication systems. The strategy leverages gold stud bump bonding coupled with thermocompression flip-chip assembly on interposer substrates to achieve dense and compact interconnections among various integrated circuit (IC) dies, including both silicon and III–V semiconductor technologies. This project conducts a complete literature survey of alternative interconnection methods, creates laboratory recipes for gold bump and bonding, and then constructs an interposer-based demonstrator. The process is characterized via electrical measurement, notably resistance and high-frequency response, and assessed via yield, mechanical reliability, and manufacturability. The findings identify significant design limitations—among them alignment accuracy, bump size, and interposer flatness—that have a dramatic effect on yield for pitches below 100 µm. The results demonstrate the feasibility of a high-density system-in-package solution, suggesting that more studies are needed with the goal of enhancing multi-chip interposers for millimeter-wave applications.**

I. Introduction

Heterogeneous integration becomes more and more important for high-power, high-speed, and high-density electronic systems. As mm-wave and sub-THz frequency ranges are addressed with contemporary radar and communication architectures, the virtues of flip-chip integration become apparent: fewer bond wires reduce parasitic inductance, smaller interconnect footprint enables higher I/O density, and high-bandwidth materials translate to improved thermal management. Coincident with this is that the inclusion of multiple IC processes (i.e., CMOS, InP) in a single package results in new design horizons relative to performance, as the optimal characteristics of each technology can be leveraged to advantage. The research includes design and demonstration of a system-in-package (SiP) integration flow for large DAC arrays, exploring methods that combine high-speed digital and analog/RF front ends within one multi-chip module. The paper aims at [1] gold ball bump deposition and their size tailoring to fine-pitch interconnects; [2] designing a low-loss, high-flatness interposer or substrate that can propagate mm-waves with minimal parasitics; and [3] developing a reliable flip-chip bonding process using thermocompression or ultrasonic welding with gold. A literature review explains the inadequacies of wire bonding at such frequencies, which motivates our chosen approach. This paper also outlines practical fabrication procedures, such as sputtering or evaporation techniques for metallization, wet etching techniques for the realization of fine gold traces, and the subsequent reliability testing—to achieve maximum bump adhesion and minimum contact resistance. The paper concludes by proposing a way forward for using the acquired knowledge to inform future research in system-in-package technology, including the development of more complex interposer designs and packaging for higher frequencies.

References

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