A High Throughput and Reliable Thermal Compression Bonding Process for Advanced Interconnections

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Abstract

In this study, a liquid phase contact thermal compression bonding (LPC TCB) process was investigated for fine-pitch copper pillar with solder cap flip chip packages. It offers a high throughput and reliable interconnection with a controllable solder height. A series of LPC TCB experiments using both Chip-on-substrate (CoS) and Chip-on-chip (CoC) packages were performed. The bonding profiles clearly indicate that a high throughput, UPH (units per hour) of 1.2k, could be achieved compared with UPH of ~600 for a conventional TCB-flux process. The results on cross section examination, interfacial microstructure, shear strength and failure mode demonstrated that excellent wetting and robust solder joint could be achieved using LPC TCB process. With a bond head (BH) cooling step, a precise solder height could be obtained based on a pre-determined bonding level, while without a BH cooling step, the solder height remained at a constant value regardless the bonding level. The restoring force from the surface tension was calculated to explain this phenomenon. Finite element analysis (FEA) was also carried out to predict the joint fatigue life for the packages bonded with different solder thickness values.

1. Introduction

The increase in functionality together with miniaturization of electronic devices has driven the development of fine pitch copper pillar with solder cap flip chip packages. Both mass reflow (MR) and thermal compression bonding (TCB) have been used as chip assembly approaches. With continuously reducing the pitch size, solder volume, and also increasing tendency to package warpage caused by thin die/substrate and CTE mismatch, there is a growing need for using TCB process in order to achieve high assembly yield and high-level of package reliability [1,2]. However, low throughput is a major limitation for TCB process.

In this study, a new TCB-flux process, namely, liquid phase contact (LPC) TCB approach was proposed and studied. The significant difference of the LPC TCB process from the traditional TCB-flux process was that the solder cap on the copper pillar had been heated to a molten state before contacting the bond pad/lead on the substrate under a small force. The bonding cycle time for LPC TCB with or without BH cooling step was greatly reduced compared with the traditional TCB-flux process, therefore a high throughput assembly process could be achieved. Another advantage of LPC TCB process was that the solder thickness (stand-off height) after assembly could be precisely controlled, which is very important for the subsequent underfill process and reliability consideration.

2. Experimental Procedure

2.1 Test Vehicles

In this study, two kinds of test vehicles were used for CoS and CoC bonding, as summarized in Table 1.

Table 1 Test vehicles

	CoS	CoC
Die	Bump diameter: Ø60μm Height: 25μmCu/27μm solder Bump pitch: 160μm	Bump diameter: Ø40μm Height: 25μm Cu/17μm solder Bump pitch: 160μm
	Bump diameter: Ø40μm Height: 25μmCu/17μm solder Bump pitch: 160μm	
Substrate	BT metallization: CuOSP Cu lead width:18μm Cu pad diameter: Ø80μm Cu lead/pad thickness: 15μm	Surface finish: Cu Cu pad diameter: Ø60μm Cu pad thickness: 10 μm
		Surface finish: SOP Cu pad diameter: Ø40μm 25μmCu/17μm Solder

For CoS bonding, the chip size was 5.0mm×5.0mmx0.15mm. As shown in Figure 1, the chip had a 31x31 area array of Cu pillar with SnAg solder cap. The pillar diameter was 40 or 60μm, the heights for Cu pillar and solder cap were 25μm and 27μm, or 25μm and 17μm, respectively. The bump pitch was 160μm. The solder composition was 97.5% Sn and 2.5% Ag. The BT substrate had a CuOSP metallization with both BOP and BOL structures. The pad diameter was 80μm, while the lead width was 18μm.

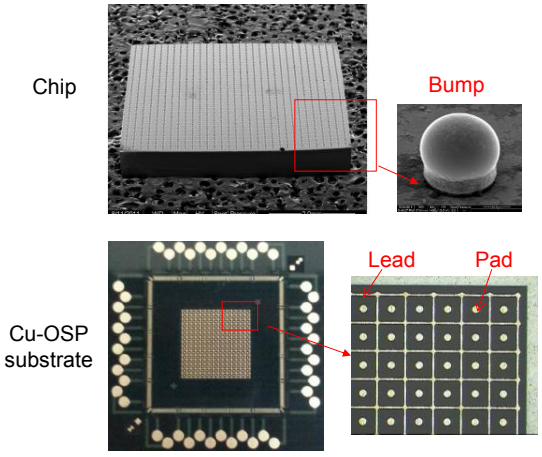

Figure 1 CoS test vehicle

For CoC bonding, the top die had 40μm pillar diameter with 25μm Cu pillar height and 17μm solder height. The

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bottom die had two surface metallizations: bare Cu and solder on pad (SOP). For the die with Cu finish, the pad diameter was 60µm and the pad thickness was 10µm. For the die with SOP finish, the pad diameter was 40µm and the solder height was 17µm.

2.2 LPC TCB Process

As shown in Figure 2, LPC TCB process has following operation sequences

(a) Flux was printed or sprayed on the substrate

(b) BH picked up a die from the carrier at an elevated temperature, which is below the solder melting point.

(c) The BH heated up to a temperature higher than the solder melting point.

(d) The chip was aligned with the substrate.

(e) After the vision alignment, the chip contacted and wetted on the substrate at a predetermined bonding level.

(f) After a certain bonding time, the BH could move away at the bonding temperature or cooled down to a temperature below the melting point of solder.

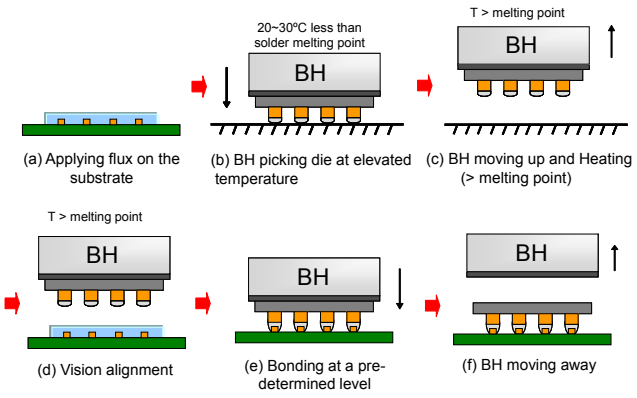

Figure 2 Process flow of LPC TCB Process

Figure 3 compares the bonding steps between the conventional TCB-flux process and LPC TCB process. For the conventional TCB-flux process, the flux was applied on the die by a flux dipping method. The dipping temperature was lower than 100°C due to the flux wicking and evaporation issues under high temperatures. A large temperature increment, such as from 100ºC to 250°C for SnAg solder, was required after the chip contacting with the substrate. The heating time needed depends on the heating capacity/heating rate of the heater. However for LPC TCB process, the standby temperature of the bond head was relatively high, only 20~30°C lower than the solder melting point. The temperature heating up could occur during the bond head moving up and the vision alignment. The whole bonding cycle for LPC process could be less than 4 seconds. In some circumstances, if the required stand-off height was near the solder equilibrium level, the cooling step could be omitted. The bonding cycle could be further reduced to 3 seconds or even less. The UPH could be as high as 1.2k for a single bond head configuration, compared with UPH of ~600 for a conventional TCB-flux process.

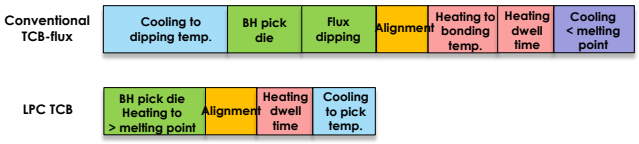

Figure 3 Bonding steps of conventional TCB-flux and LPC TCB processes

3. Experimental Results and Discussion

3.1 Bonding quality evaluation

Bonding temperature, bonding force, bonding time, bonding level, and cooling step are major process parameters for TCB LPC process, which need to be optimized. Cross sections of CoS and CoC bonded samples (Figures 4a and 4b, respectively) show excellent solder wetting with a solder thickness variation less than 2 µm. It is noted higher temperatures for both bond head and work holder were required for CoC bonding. This is because silicon has a higher thermal conductivity (149W/m·K) than organic materials (BT: 0.35W/m·K), for CoC bonding heat from the bond head could be dissipated rapidly into the bonding stage by the bottom silicon chip. The amount of additional heat required was controlled by the thickness and size of the bottom chip.

The solder joints obtained from LPC TCB process were evaluated together with the samples assembled using MR and conventional TCB-flux processes. Figure 5 shows the interfacial microstructure using three bonding processes. For as-bonded condition, a very thin intermetallic compound (IMC) layer, about 1µm, could be detected for both LPC TCB and conventional TCB-flux processes. For the MR process, IMC was relatively thick, about 2.0µm. This is due to the longer liquidus time during MR process.

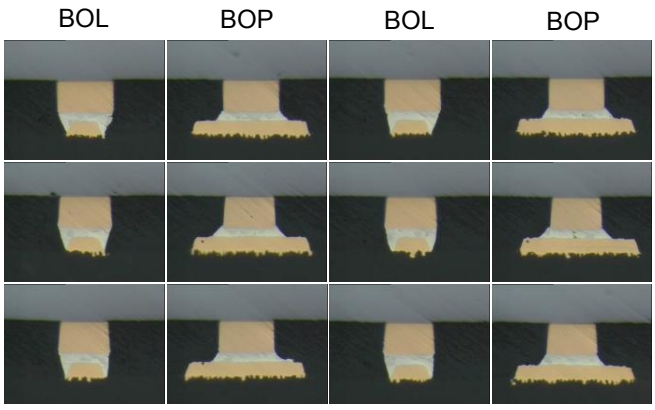

Figure 4a Cross section images of CoS packages
Stand-off height:45.6 (left) →46.2 (center) →46.4µm (right)
(Bonding conditions: WH:80ºC, BH:260ºC, BT: 1.0s)

Short thermal aging and 3 times reflow tests were performed to examine the IMC growth behavior. After thermal aging at 150°C for 4 hours, the IMC growth was limited, only 0.1~0.2µm, while significant IMC growth (3µm for LPC TCB and traditional TCB-flux processes, and 4µm

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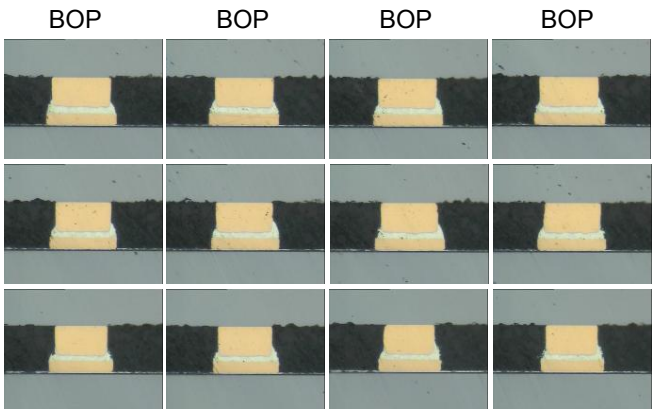

Figure 4b Cross section images of CoC packages
Stand-off height:38.4 (Left)→37.6 (center)→38.1µm (right)
(Bonding conditions: WH:120ºC, BH:350ºC, BT: 1.0s)

for MR process) was observed after 3 times reflow. The scallop-like Cu_6Sn_5 could be found at the bonding interfaces for all three bonding processes.

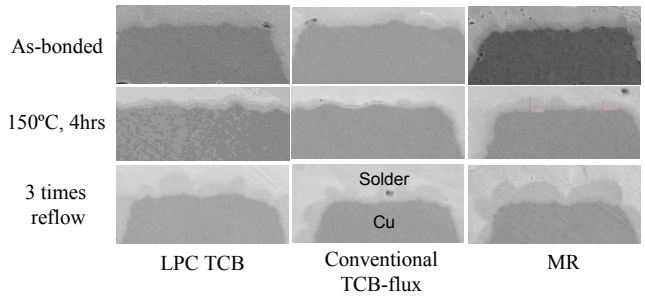

Figure 5 Interfacial microstructure for LPC TCB, conventional TCB-flux and MR Processes

Die shear test was also performed to evaluate the joint integrity. High values of shear force, ranged from 13.0kgf to 15.0kgf were obtained for all three processes under as-bonded conditions. The fracture occurred inside the solder layer. Compared with as-bonded condition, there was only a little change in shear force after thermal aging at 150ºC for 4 hours, a relatively large drop in shear force was detected after multiple reflow (shear force after reflow: 10.0kg to 13.0kg).

The results on interfacial microstructure, shear strength and failure mode indicate that LPC TCB process could provide an excellent solder joint.

3.2 Stand-off height control

Stand-off height control is important to facilitate the subsequent underfill process and to achieve excellent joint reliability. Coplanarity adjustment, precise position control and thermal management are the key controlling factors. Compared to the conventional TCB-flux process, there was no bonding tool heat-up step after the die contacted with the substrate for LPC TCB process. Thermal expansion induced by the bonding tools could be neglected. Because of the relatively short bonding time, the substrate temperature was low, hence the thermal expansion of the substrate was also less than that in the conventional TCB-flux process.

In addition, only a small bonding force (<1kg) was required in LPC TCB process since the solder was in the molten state during bonding. The small bonding force could also minimize the elastic deformation of the substrate to maintain an accurate stand-off height.

In following sections, effects of two bond parameters (cooling step, bonding temperature) on the solder height are reported and discussed.

3.2.1 Effect of cooling step

As explained previously, after bonding the bond head could move away from the die at the bonding temperature (without a cooling step), or the bond head cooled down to a temperature below the solder melting point before moving away (with a cooling step). Different solder height values could be obtained under these two conditions.

The pictures on the left in Figure 6 show that without a cooling step the final solder height was almost the same for the samples bonded at different pre-determined bonding levels (from 4µm to 20µm), while the solder heights were consistent with the bonding levels if the BH cooled down to 200ºC before releasing (the pictures in the middle), which were also in good agreement with the simulation results predicted using Surface Evolver model (the pictures on the right).

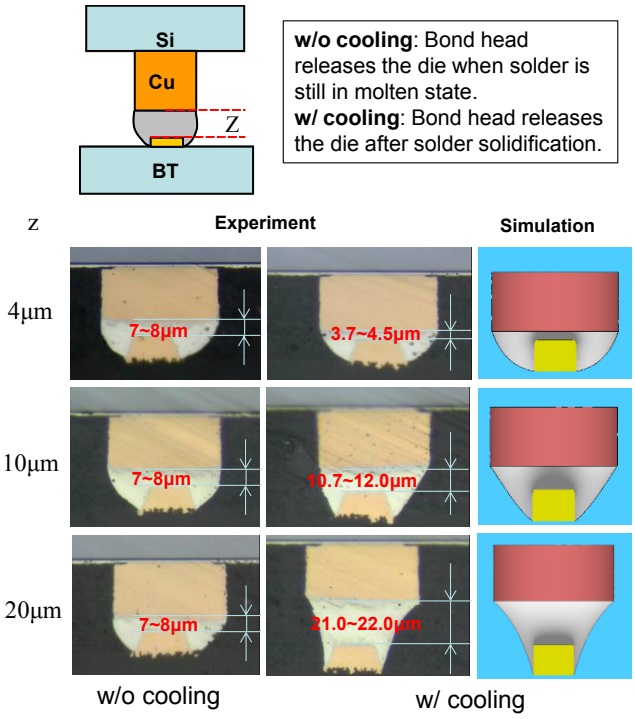

Figure 6 Cooling effect on solder height at different bonding levels for CoS packages

In order to understand how the restoring force driving the molten solder to the equilibrium height after BH was removed at the temperature above the solder melting point, Surface Evolver model was used to calculate the force generated by the surface tension of liquid solder. Based on the principle of virtual work, the restoring force at z direction is the rate of change of energy with respect to the solder thickness [3]. In

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this study, the central difference scheme was used for calculating the restoring force.

Figure 7 shows the relationship between the restoring force and the solder thickness. When the solder was compressed the force was repulsive, while if the solder was elongated it was attractive. There was one equilibrium point, at which the net force was zero. This point was the equilibrium solder thickness without any external force exertion. If the pre-determined bonding level was 4µm, the chip moved up to the equilibrium height driven by the repulsive force after the bond head moving away from the die top. While for the samples bonded at bonding levels of 10µm and 20µm, the chip moved down to the equilibrium height by the attractive force. That's why the solder height maintained the same regardless the bonding level.

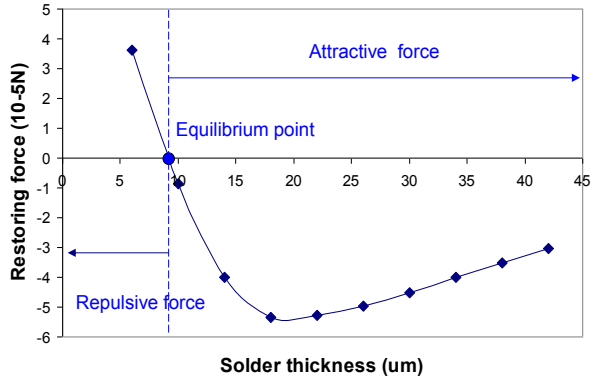

Figure 7 Restoring force vs. solder thickness

3.2.2 Effect of bonding temperature

It should be noted that in aforementioned cases the bonding temperature was high enough that no solder solidification occurred during the bonding process. If the bonding temperature was relatively low, the molten solder might solidify, or partially solidify, as the BH contacting with the substrate. The final stand-off height at the low bonding temperature could be higher than that at the high bonding temperature. As shown in the Figure 8, 8 µm and 15 µm solder heights were obtained for bonding temperatures at 280ºC and 250ºC, respectively. Similar phenomenon was also observed for CoC bonding (Figure 9).

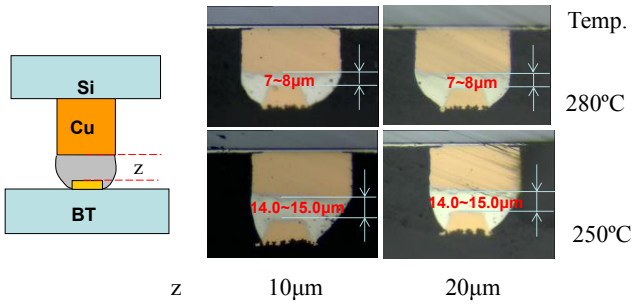

Figure 8 Temperature effect on solder height for CoS packages (w/o cooling)

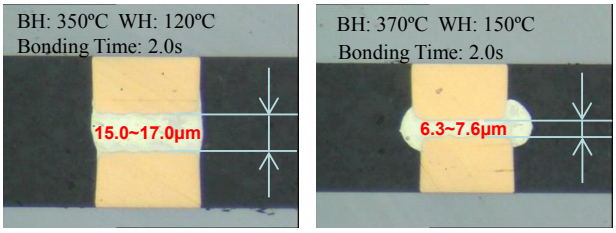

Figure 9 Temperature effect on solder height for CoC packages (w/o cooling)

4. Thermal Fatigue Life Estimation

Bump geometry is the dominant factor that affects solder joint reliability. As shown in Figure 10, the flip chip assembly was modeled as a three-dimensional slice that captured the construction along a diagonal path from the geometric center to corner. In this model, there were two kinds of bumps: BOP and BOL. The joint geometries with 10µm solder thickness were first simulated by Surface Evolver. The simulated geometries were then imported into the commercial finite element analysis (FEA) tools Ansys 14.0 for life prediction. The critically affected bumps were meshed finely, while the others were meshed coarsely. Thermal cycle loads recommended by IPC-970, were applied on all the nodes. The temperature ranged from -55ºC to 125°C with 12 minutes ramp-up time and 3 minutes dwell time. Totally three cycles were simulated in the current model. The material properties used were listed in Table 2.

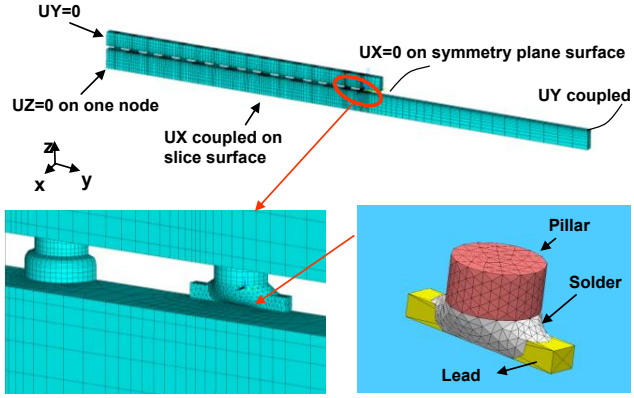

Figure 10 Slice model of a CoS flip chip package. (Underfill is not shown so the BOP and BOL solder joints can be seen.)

Table 2 Material properties

Material	CTE (ppm/K)	Young's Modulus (GPa)	Poison's Ratio
Copper[4]	16.3	121	0.34
BT substrate[5]	16	25.5	0.37
Silicon chip[6]	2.7	131	0.28
Solder: SnAg[4]	21.5	49	0.40
Underfill[4]	29	7.6	0.32

As shown in Equation (1), a double power law model [7] was used to study the evolution and accumulation of irreversible strains and energies of solder bumps.

$$\dot{\varepsilon_{cr}} = A_1 \exp\left(\frac{-H_1}{kT}\right)\left(\frac{\sigma}{\sigma_n}\right)^{n1} + A_2 \exp\left(\frac{-H_2}{kT}\right)\left(\frac{\sigma}{\sigma_n}\right)^{n2} \quad (1)$$

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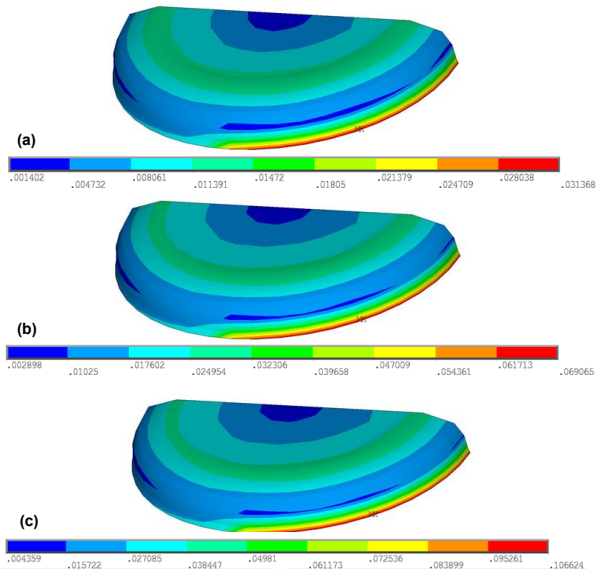

Figure 11 Creep strain contours for outmost BOP solder joint. (a) 1st cycle. (b) 2nd cycle. (c) 3rd cycle

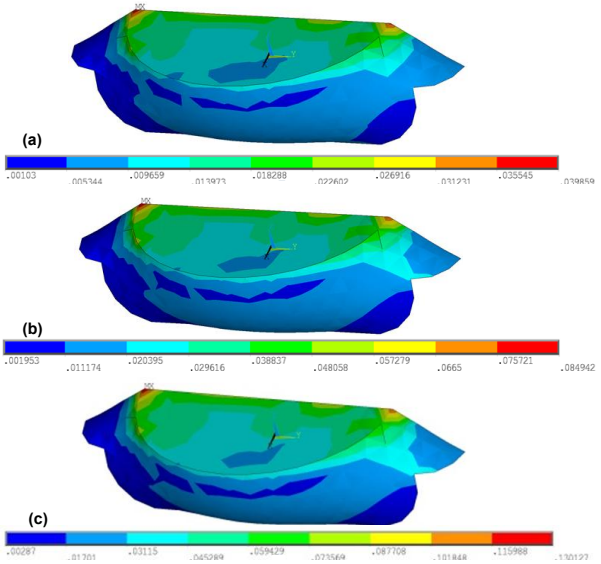

Figure 12 Creep strain contours for outmost BOL solder joint. (a) 1st cycle. (b) 2nd cycle. (c) 3rd cycle

where $\dot{\varepsilon_{cr}}$ is creep strain rate, A_1 and A_2 are power law multipliers, H_1 and H_2 are activation energies, σ is applied stress, n_1 and n_2 are stress exponents, T is the absolute temperature, k is Boltzmann's constant. The values of all these parameters for SnAg solder were listed in Table 3.

Table 3 Creep data of SnAg solder [7]

A_1=4E-7s^{-1}, H_1/k = 3223, n_1 = 3.0
A_2=1E-12s^{-1}, H_2/k = 7348, n_2 = 12
σ_n = 1 Mpa,

The life prediction model [7] is expressed as

$$N_f = (0.0468\varepsilon_{acc})^{-1} \quad (2)$$

where N_f is the number of cycles to failure and ε_{acc} is the accumulated creep strain per cycle.

The accumulated creep strain contours of the outmost BOP solder joint for the first cycle, second cycle, and third cycle are, respectively shown in Figures 11(a), 11(b), and 11(c). It can be seen that the accumulated creep strain was stabilized at the second cycle. The maximum creep strain occurred at the interface between the circumferential solder joint and the OSP Cu-pad.

The accumulated creep strain contours of the outmost BOL solder joint for the first cycle, second cycle, and third cycle are, respectively shown in Figures 12(a), 12(b), and 12(c). Again, it can be seen that the accumulated creep strain was stabilized at the second cycle. The maximum creep strain occurred at the interface between the solder joint and the Cu-pillar and at a localized area.

The crack paths for estimating the average thermal fatigue life of the outmost solder joint are shown in Figure 13 (a) for the BOP case and Figure 13(b) for the BOL case. It can be seen that for the BOP solder joint the crack path was assumed to be along the circumference between the solder joint and the OSP Cu-pad. On the other hand, the crack path for the BOL solder joint was assumed to be along the circumference between the solder joint and the Cu-pillar. The calculated average accumulated creep strain vs. time is shown in Figure 14 and the thermal fatigue life prediction is shown in Table 4. It can be seen that the average accumulated creep strain for the outmost BOP solder joint (0.0148) is smaller than that for the outmost BOL solder joint (0.0167) and thus the thermal fatigue life of the BOP solder joint (1441 cycles) is longer than that of the BOL solder joint (1281 cycles). This could be due to the larger distance-to-neutral point and less solder volume to resist thermal fatigue of the BOL solder joint.

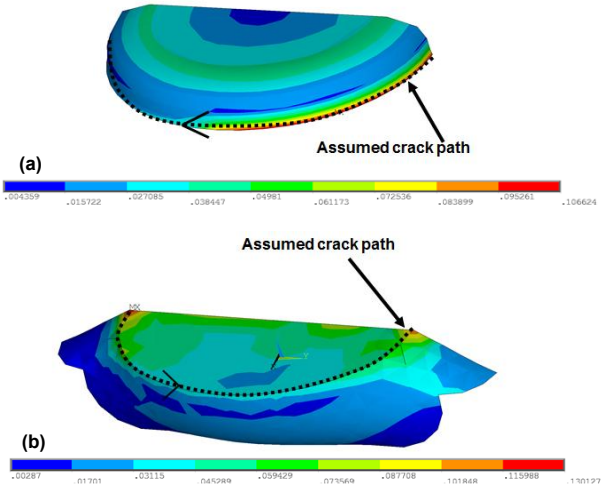

Figure 13 Crack paths for calculating the average accumulated creep strain per cycle. (a) BOP solder joint. (b) BOL solder joint

Table 4 Predicted Thermal Fatigue Lives

Solder thickness (μm)	ε_{acc}		N_f	
	BOP	BOL	BOP	BOL
10	0.0148	0.0167	1441	1281
20	0.0105	0.0151	2029	1418

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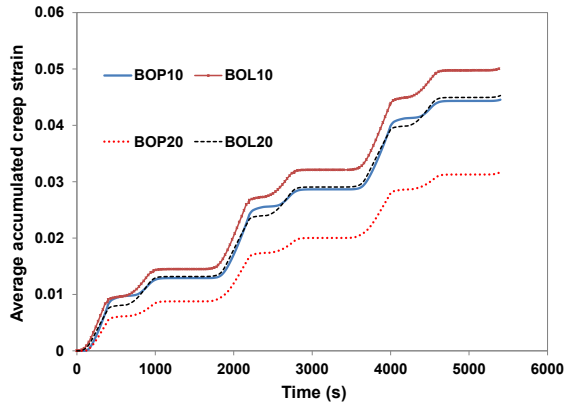

Figure 14 Average accumulated creep strain vs. time

Besides the 10µm solder joint height, 20µm solder joint height was also considered. The simulation results are shown in Figure 14 and Table 4. It can be seen that when the standoff height of the solder joint increased (from 10µm to 20µm): (1) the average accumulated creep strain decreased (from 0.0148 to 0.0105 for the BOP case and 0.0167 to 0.0151 for the BOL case), and (2) the thermal fatigue life increased (from 1441 to 2029 cycles for the BOP case and 1281 to 1418 cycles for the BOL case).

4. Conclusions

A LPC TCB process has been developed for the assembly of fine-pitch copper pillar with solder cap flip chip packages. Some important results are summarized in the follows.

- LPC TCB process is a high throughput method; UPH of 1.2k could be achieved, compared with UPH of ~600 for a conventional TC-flux process.
- The results on cross section examination, interfacial microstructure, shear strength and failure mode demonstrated that excellent wetting and robust solder joint have been achieved using LPC TCB process.
- With a cooling step in the bonding profile, a precise solder height can be obtained based on the pre-determined bonding level.
- Without a BH cooling step, the solder height remained at a constant value (the equilibrium level) regardless the bonding level.
- Solder height can be influenced by the maximum bonding temperature. The higher the bonding temperature the lower the solder height.
- FEA simulation and simple life prediction results indicated that for both BOP and BOL solder joints, the thermal fatigue life increased with increased solder height. Also, their average values are greater than 1,000 cycles. Thus these solder joints are reliable for most of the operating and environmental conditions.

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