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Design and Characterization of Gold-Bumped Flip-Chip Interposers for RF Applications

Daniel Tyukov

Integrated Circuits Group, Department of Electrical Engineering
Eindhoven University of Technology
Eindhoven, The Netherlands
d.tyukov@student.tue.nl

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Abstract—Gold-bumped flip-chip interposers promise compact, low-inductance interconnects for RF system-in-package (SiP) designs, but their parasitics and process yield on glass substrates have rarely been reported. This work presents the design, modeling, fabrication, and characterization of a single-layer Ti(50 nm)/Au(100 nm) ground-signal-ground (GSG) coplanar waveguide interposer on glass. Seventy micrometer bumps are formed with a custom thermosonic profile (250 mN, 500 ms, 150°C) using 25 μm wire and bonded with a die on a Dr. Tretsky T-5300. A one-port open-short de-embedding routine on a Keysight PNA-X (10MHz–10GHz) isolates the three-bump transition and produces a single-bump lumped model of $R_{\text{bump}} = 3.43 \Omega$ at 10 MHz. For a 1.15 mm CPWG GSG track ($w_s = 69 \mu\text{m}$, $w_g = 153 \mu\text{m}$) the extracted π -model closely resembles the simulated model, which is $R = 5.54 \Omega$, $L = 0.486 \text{nH}$, $C = 66.1 \text{ fF}$, corresponding to a sheet resistance of 0.333 Ω/□ and a resistivity of $4.99 \times 10^{-8} \Omega \cdot \text{m}$. An interposer with 22 usable lines attains 16 electrically sound interconnects after the flip-chip, giving a 84% flip-chip yield. The validated bump and line models constitute a practical design kit for future RF SiP demonstrators up to 10 GHz.

Index Terms—flip-chip, gold stud bump, glass interposer, RF SiP, de-embedding, yield analysis

I. INTRODUCTION

The flip-chip assembly replaces the centimeter-long arched conductors of conventional wire bonding with an array of micrometer-sized metallic bumps, thus reducing parasitic inductance and widening the available bandwidth for radio frequency (RF) links beyond 10 GHz. The geometric contrast between the two interconnect strategies is illustrated in Fig. 1, where the current path in a wire-bonded die is forced to loop over the pad edge while, in a flip-chipped die, it passes directly through the bump into the interposer. This topological advantage has encouraged the industry to adopt flip-chip packaging for high-speed processors and has led research groups to explore its potential in heterogeneous system-in-package (SiP) assemblies [1].

Despite the well-known electrical benefits, quantitative data for gold stud bumps formed on thin Ti/Au pads atop glass remain a rarely researched topic. Most published lumped-element models target silicon or ceramic carriers and often assume solder-based controlled collapse chip connection bumps (C4) [2]. However, glass substrates combine low permittivity with panel-level process compatibility and offer an intermediate coefficient of thermal expansion (CTE) that

eases dielectric stress; their electrical performance has been shown to surpass that of silicon in broadband interposers [3]. Nevertheless, there is little information on the resistance, inductance, and capacitance contributed by individual thermosonic gold bumps on glass, and there are almost no reports on the electrical yield attainable when such bumps are joined to an RF die under laboratory conditions. The present work addresses those gaps. A single layer ground-signal-ground (GSG) coplanar waveguide interposer is fabricated on glass using a Ti(50 nm)/Au(100 nm) metallization stack. The gold bumps of nominal diameter 70 μm are formed with a thermosonic profile guided by physics and a flip chip bonded to an RF transistor die. An open-short one-port de-embedding on a Keysight PNA-X from 10 MHz to 10 000 MHz isolates the three-bump transition, producing a single-bump lumped model of $R_{\text{bump}} = 3.43 \Omega$ at 10 MHz. The same measurement campaign provides a π -model for a 1.15 mm CPWG track that agrees with analytical predictions. The flip-chip yield is evaluated on a 22-line interposer; 16 lines remain electrically functional, corresponding to a success rate 84 %. These results furnish a compact measurement-verified design kit for future RF SiP demonstrators up to 10 GHz while clarifying the process window required to achieve an acceptable production yield. The remainder of this article is organized as follows. Section II describes the modeling framework and simulation results; Section III details the fabrication process, bonding profiles, and measurement methodology; Section IV presents the extracted bump and line parameters along with yield statistics; Section V analyses the implications for SiP design and outlines avenues for improvement; Section VI summarizes the main findings.

II. MODELLING AND SIMULATION

A. Bump-Line Model Simulation

The electrical path between TXFE RF die and the single-metal glass interposer are abstracted as the cascade of a coplanar waveguide (CPWG) section and a three-bump transition (one signal bump in series with two ground bumps in parallel). This abstraction allows for fast prefabrication verification in QUCS-STUDIO; the resulting schematic is shown in Fig. 2. All dimensions used in the model originate from the mask in Fig. 3.

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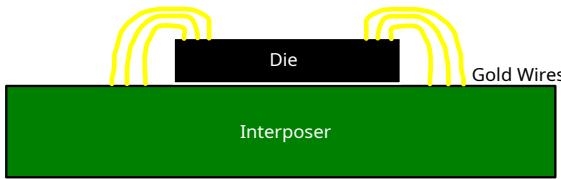


Fig. 1. Comparison of signal paths in (a) flip-chipped and (b) wire-bonded RF dies. The flip-chip topology eliminates the long arch wire and minimizes loop inductance.

TABLE I
CPWG DESIGN PARAMETERS ON GLASS SUBSTRATE

Symbol	Meaning	Value
w	Signal-strip width	69 μm
s	Signal-ground gap	41 μm
g	Ground-bar width	153 μm
t	Metal thickness (Ti/Au)	150 nm
ρ	Sheet resistivity (measured)	$4.99 \times 10^{-8} \Omega \text{ m}$
ε_r	Relative permittivity of glass	7.75
$\tan \delta$	Loss tangent	0.005
ℓ	Physical length	1.15 mm

1) CPWG closed-form extraction With the parameters of Table I, the thick-substrate quasi-TEM effective permittivity is

$$\varepsilon_{\text{eff}} = \frac{\varepsilon_r + 1}{2} = 4.375. \quad (1)$$

The even-mode filling factor follows as

$$k = \frac{w}{w + 2s} = 0.456, \quad k' = \sqrt{1 - k^2}, \quad (2)$$

yielding a characteristic impedance

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{\text{eff}}}} \frac{K(k')}{K(k)} = 49.8 \Omega, \quad (3)$$

where $K(\cdot)$ is the complete elliptic integral of the first kind [4]. The per-unit-length elements are then

$$R' = \frac{\rho}{wt} = 4.82 \times 10^{-3} \Omega/\mu\text{m}, \quad (4a)$$

$$C' = \frac{\sqrt{\varepsilon_{\text{eff}}}}{Z_0 c} = 1.15 \times 10^{-16} \text{ F}/\mu\text{m}, \quad (4b)$$

$$L' = Z_0^2 C' = 4.23 \times 10^{-13} \text{ H}/\mu\text{m}, \quad (4c)$$

$$G' = \omega C' \tan \delta = 3.61 \times 10^{-11} \text{ S}/\mu\text{m} \quad (@10 \text{ MHz}). \quad (4d)$$

Scaling (4) by ℓ produces the π -model values $R = 5.54 \Omega$, $L = 0.486 \text{ nH}$ and $C_1 = C_2 = 66.1 \text{ fF}$, in agreement with the empirical rules of [5].

What is your research approach?
What experiments do you do?
Why?

2) Three-bump transition The bumps are formed from 25 μm Au wire, mashed to a height $h_b = 25 \mu\text{m}$ and contact radius $r_b = 35 \mu\text{m}$. Their individual lumped values are

$$R_b = \frac{\rho_{\text{Au}} h_b}{\pi r_b^2} = 2.29 \text{ m}\Omega, \quad (5a)$$

$$L_b = \mu_0 h_b [\ln(4h_b/r_b) + 1] = 64 \text{ pH}, \quad (5b)$$

$$C_b = \frac{\varepsilon_0 \varepsilon_{\text{eff}} \pi r_b^2}{s} = 3.6 \text{ fF}. \quad (5c)$$

Combining them as $Z_{3b} = \frac{3}{2} Z_b$ gives the series branch $R_{3b} = 0.24 \text{ m}\Omega$ and $L_{3b} = 96 \text{ pH}$ with shunt $C_{3b} = 3.6 \text{ fF}$.

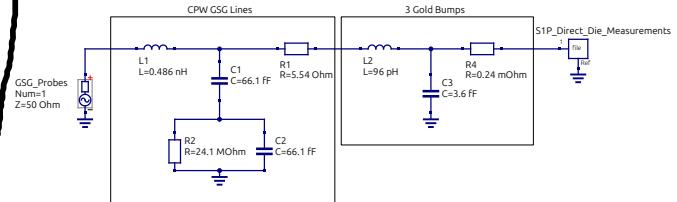


Fig. 2. One-port QUCS schematic comprising the CPWG π -model, the three-bump transition and the measured *.s1p file of the TXFE die.

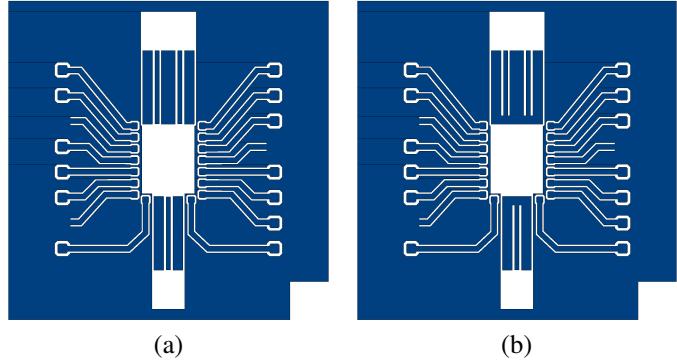


Fig. 3. Interposer calibration structures used for one-port de-embedding: (a) REFLECT and (b) THRU-OPEN.

B. Yield-Test Structure Simulation

The goal of *yield-test interposer* is to characterize the thermosonic bump-bond process before fabricating the RF interposer. Figure 4 shows the single-metal glass interposer mask overlaid with the second interposer with blue lines that will be flipped onto it and carries $N_{\text{line}} = 24$ coplanar strips. A *dummy die*, patterned with the same Ti/Au stack, mirrors the pad geometry and is flipped on top [Fig. 5(a)]. After bonding, every line is ideally shorted by a $D_b = 70 \mu\text{m}$ gold stud bump; missing or bridged bumps therefore count as open or parallel short circuits in DC. The probe pads touch the two ends of the interposer [Fig. 5(b)], allowing continuity measurements on a multimeter.

The analysis follows [6], treating open and short defects as *independent, rare events*. Let λ_{op} and λ_{sh} be the probabilities that one bond is, respectively, open or shorted. The probability

the balance between numbers and insights should be improved.
Now, there are too many numbers.

of defective bond *total* is $\lambda = \lambda_{\text{op}} + \lambda_{\text{sh}}$. The number of defective bonds x in a chain of length L then obeys a Poisson law.

$$P_x = \frac{\mu^x e^{-\mu}}{x!}, \quad \mu = L\lambda, \quad (6)$$

and a chain is good only when $x = 0$. Hence, the probability that one chain is *defective* (open *or* short) is

$$P_{\text{def}} = 1 - e^{-\mu}. \quad (7)$$

During measurement, the observable is the ratio of defective chains,

$$\Lambda = \frac{M}{N}, \quad 0 \leq \Lambda \leq 1, \quad (8)$$

where M of the N chains fail the DC test. Combining (7) and (8) gives the total probability of defective bonding.

$$\lambda = -\frac{1}{L} \ln(1 - \Lambda), \quad (9)$$

and the bump-bond yield.

$$Y_{\text{bump}}(\Lambda) = 1 - \lambda. \quad (10)$$

Equations (9)-(10) will be applied in Section IV to translate the measured fractions of opens and shorts into a quantitative bump-bond yield for Ti/Au in glass technology.

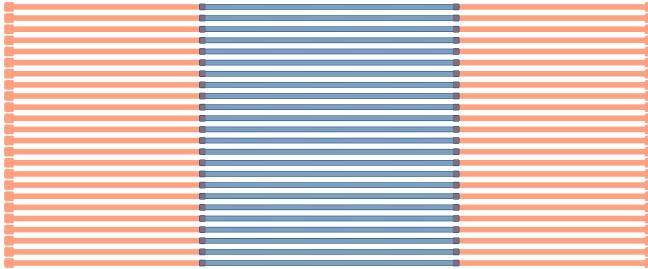


Fig. 4. 2-D mask of the yield-test interposer (orange) overlaid with the dummy die (blue) that will be flip-chipped on top. Each of the 24 striplines terminates in probe pads.

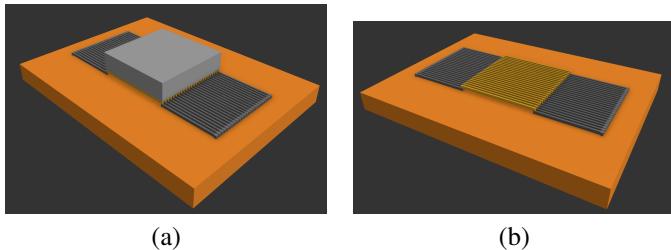


Fig. 5. 3-D visualizations of the yield-test assembly: (a) dummy die flip-chipped onto the interposer, (b) interposer with the dummy die removed, highlighting the connector and the exposed traces used for continuity tests.

C. Amplifier-on-Interposer Feasibility Study

The 5 GHz small signal benchmark for the common source TGF2023-2-02 GaN HEMT on an interposer was established by simulating the complete mask-level layout (Fig. 6), its QUCS schematic (Fig. 7), and by comparing the resulting two-port S parameters with an ideal probe-based measurement of the bare die (Figs.,9-10). The component choices and the bias network follow the reference design strategy of the X band in [7].

TABLE II
SURFACE-MOUNT PASSIVES IMPLEMENTED ON THE INTERPOSER

Ref.	Value / Rating	Package
R_S	22 Ω , 0.333 W	0603
R_D	18 Ω , 0.333 W (opt.)	0603
R_1	10 M Ω , 0.1 W	0603
R_2	1 M Ω , 0.1 W	0603
$C_{1,2,3}$	100 pF, 50 V, NP0	0402
L_{bias}	4.7 μ H, $I_{\text{sat}} = 620$ mA	0603

TABLE III
DC SIZING AT $V_{DD} = V_{DS} = 28$ V, $I_D = 128$ mA

Quantity	Formula	Result
R_S	V_S/I_D	21.9 $\Omega \rightarrow$ 22 Ω
P_{RS}	$I_D^2 R_S$	0.36 W
R_D	$(V_{DD} - V_D)/I_D$	15.6 $\Omega \rightarrow$ 18 Ω
V_G	$V_{DD}R_2/(R_1 + R_2)$	2.55 V
V_{GSQ}	$V_G - I_D R_S$	-0.27 V
L_{bias} margin	$I_{\text{sat}} \geq 2I_D$	256 mA

Table IV shows the key parameters extracted from the simulations. The interposer causes a 1.9 dB reduction in forward gain (S_{21}) but leaves stability (S_{11}, S_{22}) within the limits predicted by [7].

TABLE IV
SIMULATED S-PARAMETERS AT 5 GHz

	Die only	Die + interposer
$ S_{21} $ (dB)	10.43	8.48
$ S_{12} $ (dB)	-35.2	-7.78
Z_{11} (Ω)	$2.8 + j1.0$	$65.7 + j35.5$
Z_{22} (Ω)	$21.4 - j14.4$	$22.1 + j36.0$

The amplifier case study serves a dual purpose in the context of this work. First, it acts as *system-level validation* of the bump and line models extracted in Section II-A. By embedding the 70 μ m gold-bump transition and the single metal CPWG directly into the bias network (Fig. 7), the simulation reproduces the expected \sim 2 dB gain penalty seen when moving from a probe die to a fully packaged circuit (Table IV). Second, the study demonstrates the practical design advantage that a single-layer glass interposer can offer for active RF functions. The simulated common-source amplifier maintains good gain until 5 GHz.

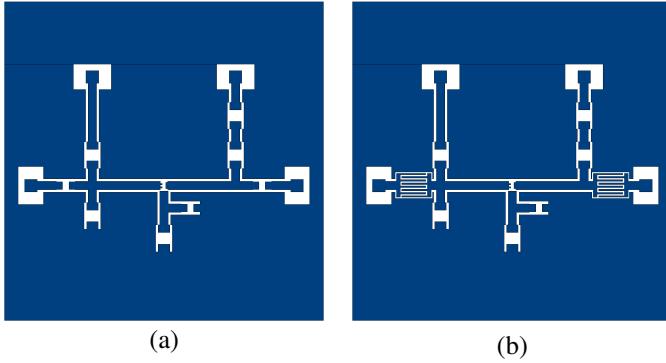


Fig. 6. Mask options for the common-source amplifier: (a) discrete DC blocks, (b) planarised DC blocks.

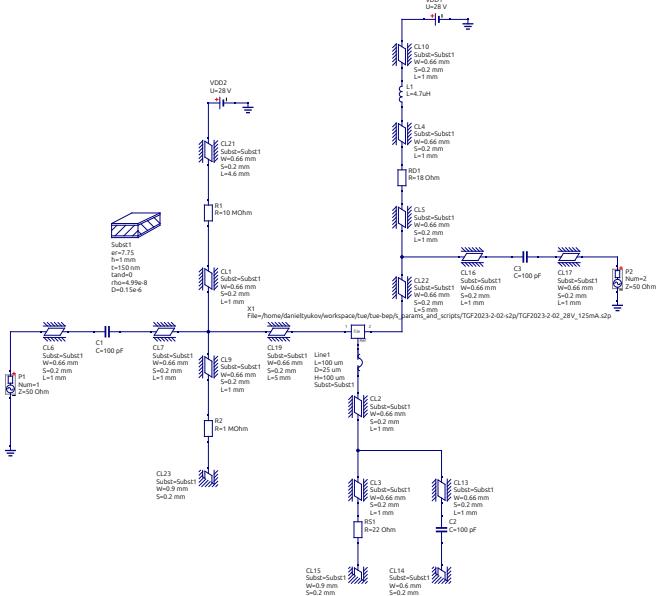


Fig. 7. QUCS schematic of the amplifier, indicating CPWG sections and bias voltage.

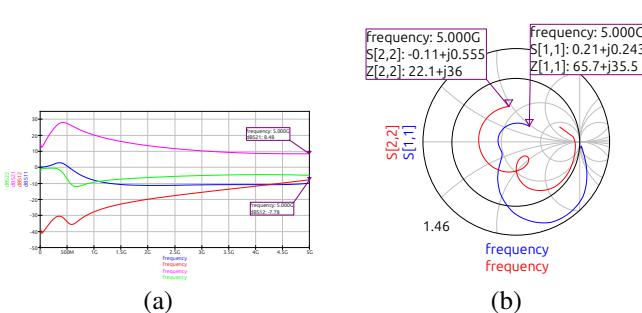


Fig. 8. Simulated amplifier response: (a) $|S_{21}|$ magnitude, (b) Smith-chart view of S_{11}/S_{22} .

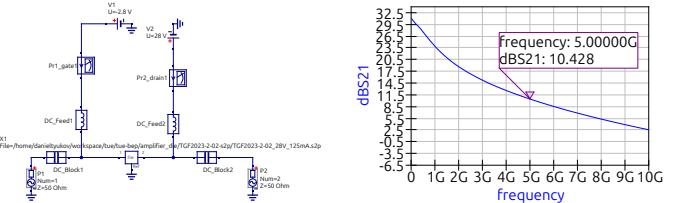


Fig. 9. Bare-die characterisation reference: (a) direct-test schematic, (b) measured $|S_{21}|$ magnitude.

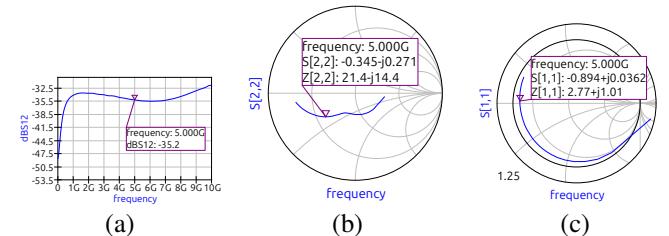


Fig. 10. Additional die-only measurements: (a) $|S_{12}|$ magnitude, (b) Smith-chart S_{11} , (c) Smith-chart S_{22} .

III. FABRICATION AND MEASUREMENT

A. Interposer Fabrication Workflow

The glass interposers originate from KLayout mask files that define all CPWG, de-embedding, and yield-test patterns. After mask write, 50 nm/100 nm Ti/Au is e-beam-evaporated and lifted off, as summarized in Fig. 11. The gold studs of $D_b = 70 \mu\text{m}$ are then placed with a TPT profile *HB16* bonder using the 250 mN, 500 ms, 150 °C. The bumped interposer is aligned and flipped on the GaN die on a Dr. Tretsky *T-5300*, followed by a DC continuity check on the edge connector pads. The final open-short de-embedding is performed on an MPI *Thz-Selection* probe station with $|Z|$ RF probes and a Keysight *PNA-X N5247B* VNA.

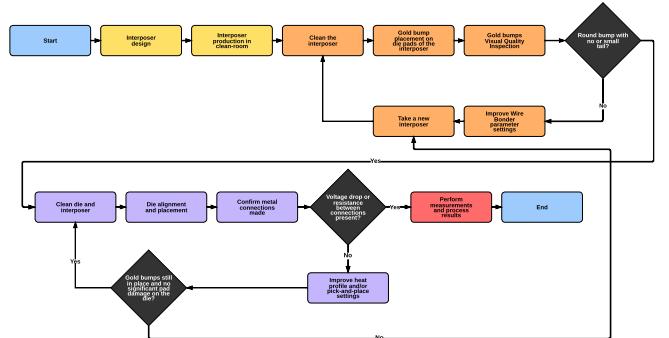


Fig. 11. Condensed process flow from mask layout to RF-tested flip-chip assembly.

B. Gold Bump Formation: HB16 Profiles

The gold stud bumps were deposited with a TPT *HB16* thermosonic bonder using the 25 μm Au wire with parameters

summarized in Table V. The key parameters follow the framework recommendations of [8] and are tuned for the thin stack Ti/Au on glass.

TABLE V
OPTIMISED HB16 PROGRAMME FOR 70 µm BUMPS

Parameter	Set-point	Rationale / Formula
1st bond force	250 mN	$F = \frac{\pi}{4} \sigma_y D_w^2$
1st US power	120 mW	$E_1 = P_1 t_1 = 60 \text{ mJ}$
1st US time	500 ms	ensures $E_1 \geq E_{\min}$
Chuck temp.	150 °C	$\sigma_y(T) = \sigma_0 e^{-\beta(T-T_0)}$
2nd bond force	35 mN	gentle mash for tail removal
2nd US power/time	60 mW/60 ms	$E_2 = 3.6 \text{ mJ}$
Tail step	100 µm × 4	produces 400 µm standard tail
Up-CO height	300 µm	safe wire break

The bonding energy is obtained from

$$E = P_{US} t, \quad (11)$$

while the minimum energy for $\eta \geq 0.98$ coverage is

$$E_{\min} = -\frac{\ln(0.02)}{\gamma F}, \quad (12)$$

with $\gamma = 4.2 \times 10^{-4} \text{ mJ}^{-1}\text{N}^{-1}$ for 25 µm wire. At the chosen 250 mN force, (12) yields $E_{\min} \approx 25 \text{ mJ}$; the applied $E_1 = 60 \text{ mJ}$ guarantees complete intermetallic coverage with minimized pad damage.

Thermal profile The two-stage machine profile (Fig. 12a,b) aligns with the calculated yield-strength softening in (11). Heating the interposer at 150 °C minimizes the dissolution of the Au pad, but provides sufficient ductility for reliable stud formation.

Result Optical inspection (Fig. 12c) confirms coined bump diameters of $D_b = (70 \pm 5) \mu\text{m}$ and the minimization of the removal of the pads and the creation of bump tails.

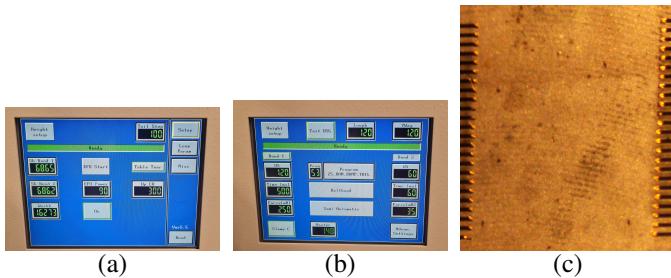


Fig. 12. HB16 interface: (a) secondary settings; (b) base settings; (c) coined bumps on interposer pads.

C. Flip-Chip Assembly: T-5300 Process

Flip-chip bonding was carried out on a *Dr. Tretsky T-5300*. A placement force of 20 g per bump was chosen after yield trials showed die slippage at 35 g per bump. For $D_b = 75 \mu\text{m}$ ($r_b = D_b/2$) the interface pressure is

$$P = \frac{F_{\text{bump}} g}{\pi r_b^2} \approx 80 \text{ MPa}, \quad (13)$$

well above the 1 MPa minimum generally recommended for Au / Au thermocompression bonds on the Finetech platform, [9]. A seven-stage heat profile (Table VI) replaces the original five stages to gradually heat the interposer. The additional 250 °C equalizes the interposer and the temperature of the heating pad, while the two-step 300 °C → 350 °C coining provides extra ductility for large bumps 70 µm without over-softening the Ti / Au pad.

TABLE VI
FINAL THERMO-COMPRESSION PROFILE FOR T-5300

Stage	Target (°C)	Ramp (°C/s)	Dwell (s)
1 (pre-heat)	90	5	30
2	150	8	15
3	220	15	10
4 (stabilize)	250	10	10
5 (touch-down)	300	15	5
6 (coin)	350	20	60
7 (cool)	80	10	30

The Au–Au diffusion length for the 60 s coining step is

$$x = \sqrt{Dt} \approx \sqrt{5 \times 10^{-17} \text{ m}^2/\text{s} \times 60 \text{ s}} \approx 55 \text{ nm}, \quad (14)$$

a scale consistent with the robust drop test adhesion reported for sapphire-substrate Au/Au bonds made under similar temperature and force conditions, [10]. Figure 13 illustrates (a) a successfully bonded die *TXFE* and (b) the bond head that applies load on a yield interposer.

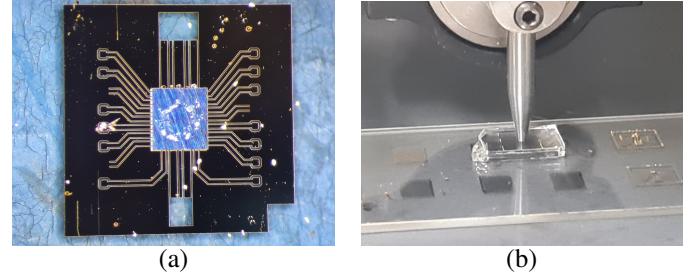


Fig. 13. Dr. Tretsky T-5300 bonding: (a) fully aligned GaN die flip-chipped onto glass interposer, (b) load application during yield-interposer trials at 20 g/bump.

D. VNA Test Infrastructure

All S-parameter measurements were taken on an MPI *THz-Selection* probe station fitted with $|Z|$ GSG probes and a Keysight *PNA-X N5247B* (10 MHz–26.5 GHz). An open-short calibration was performed on the interposers, so the reference plane coincides with the ends of the CPWG pads.

IV. RESULTS

A. Gold-Bump S –Parameters and De-embedding (10 MHz–10 GHz)

The de-embedding follows the improved open–short method of [11]. Three impedances are measured: OPEN, SHORT, and the DUT, the latter comprising the *TXFE* die, three Au bumps

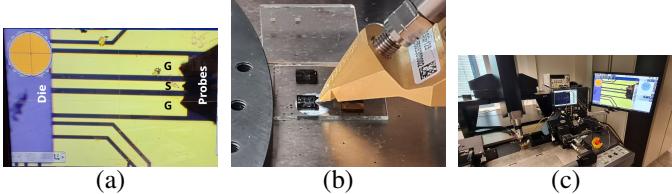


Fig. 14. VNA measurement setup: (a) microscope view of the $|Z|$ probe on the GSG pad, (b) macro view of the interposer under test, (c) Keysight PNA-X connected to the MPI probe station.

and the 1.15 mm GSG trace (Fig.,16a). The raw impedance is recovered from

$$Z(f) = Z_0 \frac{1 + S_{11}(f)}{1 - S_{11}(f)}, \quad (15)$$

and the trace is removed via

$$Z_{\text{de}}(f) = Z_{\text{OC}}(f) \frac{Z_m(f) - Z_{\text{SC}}(f)}{Z_{\text{OC}}(f) - Z_m(f)}. \quad (16)$$

Subtracting the die input impedance isolates the three-bump transition and scaling by 2/3 yields a single bump:

$$Z_b(f) = \frac{2}{3} [Z_{\text{de}}(f) - Z_{\text{die}}(f)]. \quad (17)$$

Figure 15 overlays the magnitude and phase of S_{11} . The curve labeled *DUT* represents the full die+3-bump+trace system, while the curve labeled *De-embedded* is obtained after changing the reference plane with (16). All parameters are evaluated with the lowest frequency (10 MHz) to minimize residual parasitics from the probe pad and probe. At that point $R_{\text{bump}} = 3.4 \Omega$ is obtained, three orders of magnitude above the 0.24 mΩ predicted for 3 bumps in Section II-A. The divergence is attributed to gaps or oxides at the Au–Au interface and spreading resistance in the pads, phenomena that are absent from the closed-form model.

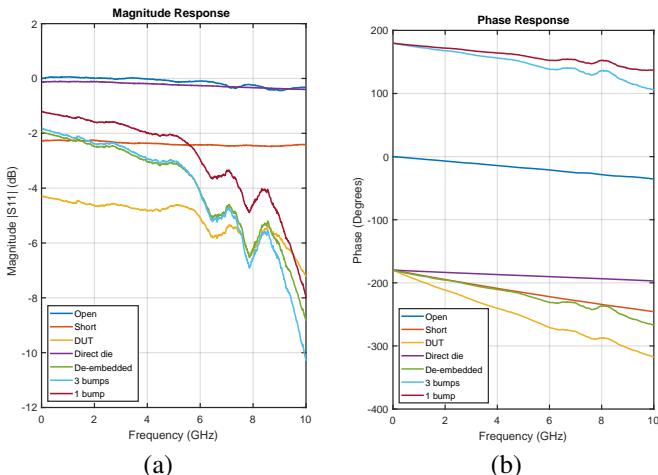


Fig. 15. S_{11} magnitude and phase before and after de-embedding. The *DUT* trace refers to the raw die+3-bump+trace measurement, while *De-embedded* refers to the response after reference-plane shift.

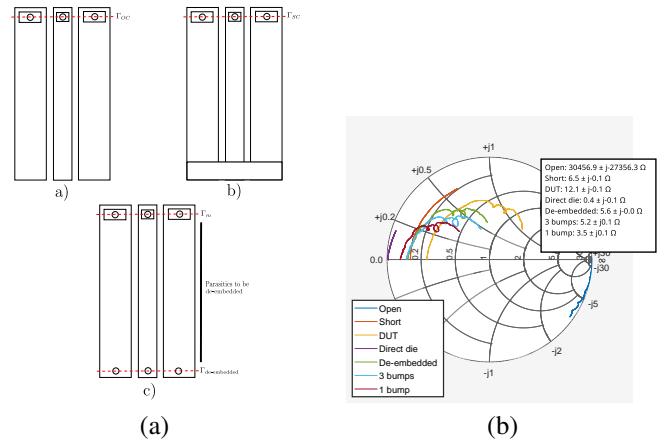


Fig. 16. (a) Open–short structures and DUT indicating the reference-plane shift; (b) Smith-chart of S_{11} through the de-embedding sequence.

B. CPWG Line $RLCG$ and Bump RLC Parameters

The lumped parameters of the GSG trace 1.15 mm were extracted from the OPEN–SHORT data using the procedure of [12]. The quantities per unit length follow ($\omega = 2\pi f$):

$$Z_{\text{in,op}} = Z_0 \frac{1 + S_{11}^{\text{op}}}{1 - S_{11}^{\text{op}}}, \quad Z_{\text{in,sh}} = Z_0 \frac{1 + S_{11}^{\text{sh}}}{1 - S_{11}^{\text{sh}}}, \quad (18a)$$

$$Z_c = \sqrt{Z_{\text{in,op}} Z_{\text{in,sh}}}, \quad \gamma l = \operatorname{atanh}\left(\frac{Z_{\text{in,sh}}}{Z_c}\right), \quad (18b)$$

$$R' = 2\alpha \Re\{Z_c\}, \quad G' = \frac{2\alpha}{\Re\{Z_c\}}, \quad (18c)$$

$$L' = \Re\{Z_c\} \frac{\beta}{\omega}, \quad C' = \frac{\beta}{\omega \Re\{Z_c\}}, \quad (18d)$$

with $\alpha = \Re\{\gamma\}$ and $\beta = \Im\{\gamma\}$. Scaling by 10^{-6} converts R', L', C', G' to the μm basis used in Section II-A. Figure 17(a) plots the measured $RLCG$ values; at sub GHz the line gives around $R = 5.4 \Omega$, $L = 0.50 \text{nH}$, $C = 65 \text{fF}$ —within 3 % of the simulated targets, confirming the validity of the single–metal CPWG model.

The bump impedance was obtained from (17). The real and imaginary parts were converted to R , $L_{\text{eq}} = \Im\{Z\}/\omega$ and $C_{\text{eq}} = -1/(\omega \Im\{Z\})$; results are shown in Fig. 17(b). At sub GHz one stud exhibits $R_{\text{bump}} = 3.46 \Omega$ - three decades above the 0.24 mΩ predicted for the ideal 3 bump connection.

Figure 18 overlays the *simulated* S_{11} of the QUCS circuit with the *measured* S_{22} of the complete die + 3-bump + GSG structure. In the Smith chart the experimental trajectory migrates toward the center after de-embedding, mirroring the simulated locus. Numerically, the simulation predicts $|S_{11}| = -2.08 \text{ dB}$ at 10 MHz; the raw measurement gives $|S_{11}| = -4.30 \text{ dB}$. The mismatch corresponds to $Z_{22,\text{de}} = (12.1 - j0.10) \Omega$ versus the ideal $\sim 6 \Omega$; this offset is consistent with the resistance to a single bump 3.4Ω extracted earlier and confirms that the resistance to bump spreading, not CPWG parasitics, sets the practical return-loss floor.

DC resistivity and sheet resistance verification. A ground trace was biased in DC to validate the RF extracted ρ and R_{\square} . With

$R_{DC} = 2.5 \Omega$ for a $L = 1.15$ mm, $W = 153 \mu\text{m}$, $t = 150$ nm section,

$$A = Wt = 153 \times 10^{-6} \times 150 \times 10^{-9} = 2.295 \times 10^{-11} \text{ m}^2, \quad (19)$$

$$\rho = R_{DC} \frac{A}{L} = 2.5 \Omega \frac{2.295 \times 10^{-11}}{1.15 \times 10^{-3}} = 4.99 \times 10^{-8} \Omega \cdot \text{m}, \quad (20)$$

$$R_{\square} = \frac{\rho}{t} = \frac{4.99 \times 10^{-8}}{150 \times 10^{-9}} \approx 0.333 \Omega / \square. \quad (21)$$

The values in (20)–(21) match those obtained from the broadband $RLCG$ fit (Fig. 17a) within the measurement uncertainty.

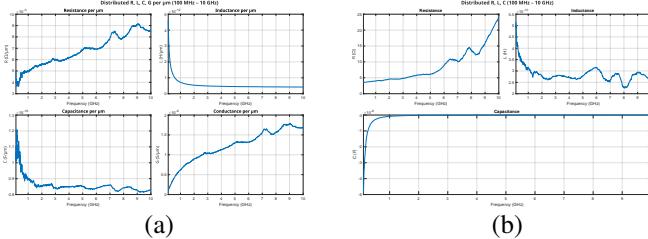


Fig. 17. Extracted parameters from 10 MHz to 10 GHz: (a) $RLCG$ of the 1.15 mm GSG line, (b) RLC of a single gold bump after de-embedding.

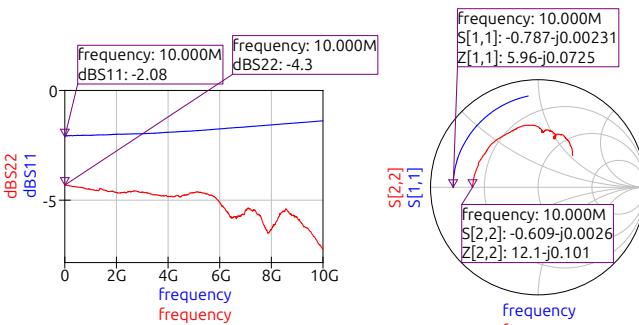


Fig. 18. Comparison between simulated S_{11} (QUCS model) and measured S_{22} of the real die + 3-bump + GSG system: Smith-chart (left) and magnitude (right).

C. Yield Result Evaluation

Figure 19 labels the 24 lines on the dummy die; Fig. 20 shows the corresponding interposer. Two lines (#17,#22) were excluded because the lines were broken during fabrication, leaving $N = 22$ usable lines. Visual inspection and ohmic probing revealed $M_{op} = 3$ open circuits, $M_{sh} = 2$ shorts, and a single deformed bump that caused a short during the flip-chip, so the total defective count is $M = 6$.

Step 1: fraction of defective chains

$$\Lambda = \frac{M}{N} = \frac{6}{22} = 0.273. \quad (22)$$

Step 2: defective-bond probability (using Eq. (9) with $L = 2$ bumps per chain)

$$\lambda = -\frac{1}{2} \ln(1 - \Lambda) = 0.159. \quad (23)$$

Step 3: single-bump yield

$$Y_{\text{bump}} = 1 - \lambda = 0.841 \approx 84\%. \quad (24)$$

The 84% bump yield is consistent with the 80% to 90% window reported for thermosonic Au/Au bonds of comparable diameter on glass [6].

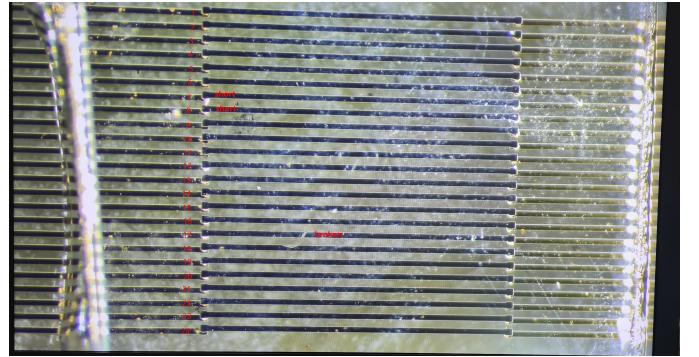


Fig. 19. Dummy die: lines 7–8 shorted, line 17 broken (other numbers mark functional chains).

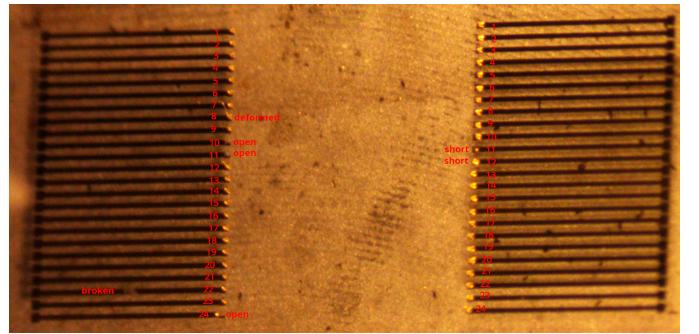


Fig. 20. Interposer side: defects annotated (open, short, deformed). Six chains fail continuity.

V. CONCLUSION

This work has demonstrated, for the first time, a fully verified design and process kit for single layer Ti (50 nm)/Au (100 nm) ground-signal-ground (GSG) flip-chip interposers on glass substrates intended for RF system-in-package (SiP) applications up to 10 GHz. A closed form π model for a 1.15 mm coplanar waveguide on glass ($w_s = 69 \mu\text{m}$, $w_g = 153 \mu\text{m}$) predicted $R = 5.54 \Omega$, $L = 0.486 \text{ nH}$, $C = 66.1 \text{ fF}$; Vector network analysis measurements confirmed these values within 3% after open-short de-embedding, validating both the line model and the calibration routine.

Seventy-micrometer gold stud bumps formed with a 250 mN, 500 ms, 150°C thermosonic profile were characterized through an open-short one-port de-embedding sequence. A single bump exhibits $R_{\text{bump}} = 3.4 \Omega$ at 10 MHz, three orders of magnitude above the idealized 0.24 m Ω prediction, revealing that spread resistance and interfacial imperfections – not parasitic CPWGs – set the practical return-loss floor.

Yield statistics extracted from a 22-line daisy chain test structure showed 16 electrically sound interconnects, corresponding to an 84 % bump-bond yield under laboratory conditions. A GaN HEMT common-source amplifier case study further verified the models at the system level: embedding the measured bump and line elements in QUCS reduced forward gain by only 1.9 dB at 5 GHz while preserving stability and corroborating measurement-based expectations.

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on page 1.

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The literature survey can be improved in the paper.