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Study on Flip Chip Assembly of High Density Micro-LED Array

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INTRODUCTION

Flip chip assembly technology is an attractive solution for high I/O density and fine-pitch microelectronics packaging. Recently, high efficient GaN-based light-emitting diodes (LEDs) have undergone a rapid development and flip chip bonding has been widely applied to fabricate high-brightness GaN micro-LED arrays [1]. The flip chip GaN LED has some advantages over the traditional top-emission LED, including improved current spreading, higher light extraction efficiency, better thermal dissipation capability and the potential of further optical component integration [2, 3]. With the advantages of flip chip assembly, micro-LED (μLED) arrays with high I/O density can be performed with improved luminous efficiency than conventional p-side-up micro-LED arrays and are suitable for many potential applications, such as micro-displays, bio-photonics and visible light communications (VLC), etc. In particular, μLED array based selif-emissive micro-display has the promising to achieve high brightness and contrast, reliability, long-life and compactness, which conventional micro-displays like LCD, OLED, etc, cannot compete with. In this study, GaN micro-LED array device with flip chip assembly package process was presented. The bonding quality of flip chip high density micro-LED array is tested by daisy chain test. The p-n junction tests of the devices are measured for electrical characteristics. The illumination condition of each micro-diode pixel was examined under a forward bias. Failure mode analysis was performed using cross sectioning and scanning electron microscopy (SEM). Finally, the fully packaged micro-LED array device is demonstrated as a prototype of dice projector system.

EXPERIMENT AND DISCUSSION

Two types of array devices are fabricated in this study, including the 80×60 GaN micro-LED array chip with each pixel having a diameter of 35μm on a 50μm pitch and the 240×160 silicon micro-element array chip with each pixel having a diameter of 20μm on a 30μm pitch as fine-pitch, high IO number bonding test vehicle. 80×60 micro-LED arrays was designed by all pixels in the same row share a common n-contact, and silicon substrate as control backplane was designed and fabricated by the same pixel counts of bumps in 4,800 counts of 80×60 arrays which share a common p-contact metal line in the same column. With this configuration, packaged 80×60 devices can be addressed in passive matrix driving. 240×160 array chips were designed in all pixels individually and silicon substrate with 8 daisy chain design for reference bonding test vehicle. The Karl Suss FC150 machine was used for bonding of GaN micro-LED array chip onto silicon substrate. The schematic illustrations of micro-LED arrays and silicon substrate were showed in Fig. 1, and also schematic illustration of 240×160 testing vehicle with daisy chain in cross-sectional view shown in Fig. 2. Specificiations of substrates and chips were also shown in Table 1 and Table 2 respectively. Both two types of array devices were performed by thermo-compression bond process and capillary flow under-fills after bonding. The bonding quality and failure mode analysis of high I/O density flip chip micro-LED array were performed by daisy chain testing and cross-sectional scanning electron microscopy (SEM). The electrical and illumination condition of each micro-diode pixel were examined under current-voltage (I-V) measurement.

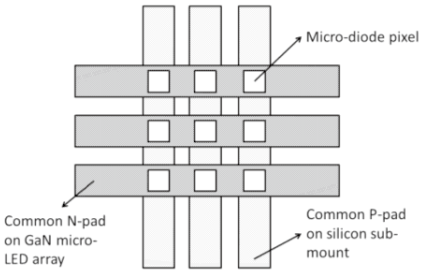

Fig. 1 Schematic illustration of micro-LED array bonded on silicon sub-mount (plan view).

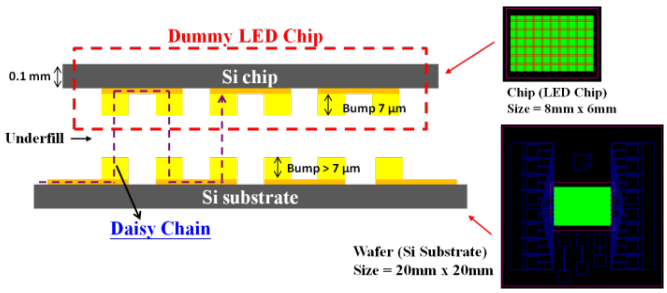

Fig. 2 Schematic illustration of 240x160 testing vehicle with daisy chain (cross-sectional view)

240x160 dummy device testing

The bonding process is optimized by varying the bonding pressure, temperature and time. The parameters were therefore set to 4.63Mpa -250℃-90sec. The result is that each daisy chain including 2400 I/Os has resistance of 28.7±9.6Ω, which means the resistance of single I/O is approximately 12mΩ and shows good electrical property in this bonding condition therefore.

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Table 1 Specifications of two type silicon substrates

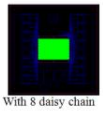
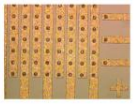
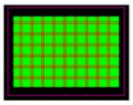
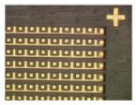
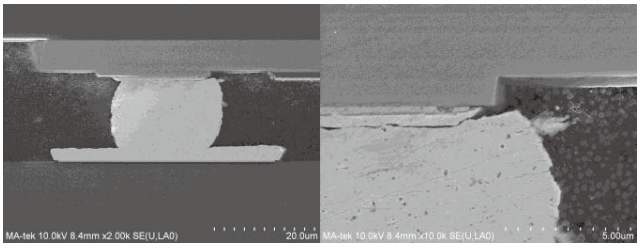
Resolution	240x 160	80 x 60
Substrate material	Silicon	Silicon
Line pitch / spacing	30 μm / 10 μm	50 μm / 15 μm
Line material	Au	Au
No. of bumps	38,400	4, 800
Bump height	10um	10um
Line height	---	3um
Substrate	 With 8 daisy chain testing points	

Table 2 Specifications of two type chips

Resolution	240x 160	80 x 60
Chip size	7.2mm x 4.8mm	4mm x 3mm
Chip material	Silicon	GaN on Sapphire
Bump pitch /spacing	30 μm / 10 μm	50 μm / 15 μm
Bump type	Au	Au
No. of bumps	38,400	4, 800
Bump height	10μm	<3μm
Chip		

80x60 real microLED device packaging

Fig. 3 showed the cross-sectional SEM diagram of bonded interface between pixel of micro-LED array and Au bump of silicon substrate. From the SEM diagram, we can see the failure mode of peelings near the reflected p-contact layer on GaN microLEDs which was considered mainly coming from the larger CTE mismatch between GaN and Silicon materials. Besides, non-uniform bonding interface between pixel of micro-LED array and bump of silicon substrate also contributes to the failures. Fig. 4 shows the illumination condition of GaN micro-LED array bonded onto silicon substrate under a forward current of 0.1 mA. With the non-optimized bonding condition, the electrical and luminous efficiency were restricted due to the increasing interface resistance.



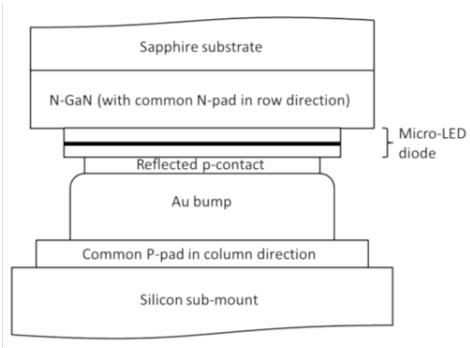


Fig. 3 Cross-sectional scanning electron microscopy diagram and schematic illustration of bonded interface between pixel of micro-LED array and Au bump of silicon substrate.

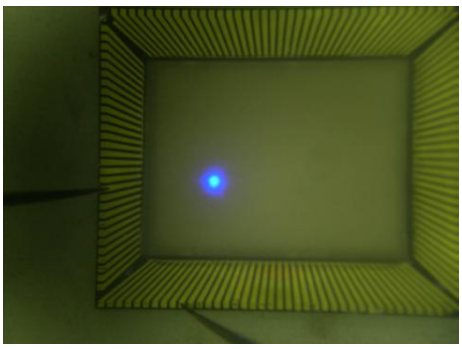


Fig. 4 Illumination condition of GaN micro-LED array bonded onto silicon substrate under a forward current of 0.1 mA.

SUMMARY

GaN micro-LED array devices with flip chip assembly package have been demonstrated and examined in this study. Both 80×60 micro-LED arrays with 4,800 pixel counts, 35 μm in pixel size and 50 μm in pixel pitch and 240×160 bummy micro-LED arrays (silicon) with 38,400 pixel counts, 20 μm in pixel size and 30 μm in pixel pitch were fabricated. After flip chip assembly process, micro-LED chips were bonded onto the silicon sub-mount via Au-Au bonding. Although high I/O density of GaN micro-LED array flip chip assembly package has been demonstrated, the large CTE mismatch between GaN and silicon materials is considered as the main reason of the failures. Therefore the low temperure and pressure assembly is a solution, Indium bump assembly for example [4].

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