Glass Interposer Substrates: Fabrication, Characterization and Modeling

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Abstract

There is growing interest in applying glass as a substrate for 2.5D/3D applications. Glass has many material properties that make it well suited for interposer substrates. Glass based solutions provide significant opportunities for cost benefits by leveraging economies of scale as well as forming substrates at design thickness.

A lot of work is being done to validate the value of glass as an interposer substrate. One important area is the electrical performance of glass relative to silicon. Because glass is an insulator, it is expected to have better electrical performance than silicon. Electrical characterization and electrical models demonstrate the advantages of the insulating properties of glass, and its positive impact on functional performance. Further advantages are anticipated in reliability performance, because of the ability to adjust thermal properties such as coefficient of thermal expansion (CTE) of glass. Modeling results demonstrating these improvements will be presented.

Additionally, significant progress has been made in the demonstration of glass interposer fabrication. Fully patterned wafers and panels with through holes and blind holes are being fabricated today. Leveraging existing downstream processes for metallization on these substrates is also important for cost effectiveness and ease of transition into production. Progress on demonstrating the ability to leverage existing downstream processes to make functional glass interposers using both through and blind via technology will be presented.

Introduction

Over the past several years, the semiconductor industry has seen some tremendous developments in using glass as an interposer substrate. Glass has many properties that make it an ideal material for interposer substrates such as: ultra-high resistivity, low dielectric constant, ultra-low electrical loss and adjustable coefficient of thermal expansion (CTE) that allows management of warp of 3D-IC stacks. Regardless of technical performance, any glass based solution must also provide cost advantages in substrate material, via formation, and subsequent processing.

Interposer technology plays an important role for 2.5D/3D integration. There is a great deal of activity to develop manufacturing infrastructure for interposers based on through silicon via (TSV) technology. While manufacturability of TSVs continues to improve, there are some difficult challenges around cost and electrical performance that are prompting consideration of alternative solutions for interposer applications. Glass interposers provide a number of opportunities for improved performance and cost.

Glass describes a broad material set, with a wide range of properties driven by composition and forming methodologies. Compositional changes allow tailoring of various properties, such as mechanical, thermal, electrical, optical characteristics, along with chemical durability. As an insulator, glass substrates provide a platform for high performance with low loss for increased signal integrity, particularly at higher frequencies. Copper interconnects designed in glass (TGV) instead of Silicon (TSV) also eliminate the need for an oxide barrier layer, which provides the benefit of cost reduction and reduced complexity.

One of the challenges facing silicon is the management of warp due to thermal deformation in assembly and use. This issue is mainly driven by coefficient of thermal expansion (CTE) mismatch and is a significant reliability concern. A notable advantage of glass compared to silicon is the ability to tailor the CTE by adjusting composition, which improves the ability to manage stack warpage.

Below we provide results showing progress made in developing downstream processes such as TGV metallization and laying down redistribution layers (RDL). In addition, we show some of the advantages given by the ability to adjust the CTE with results from finite element analysis of various interposer designs.

Glass Substrates

For 2.5D and 3D-IC interposer technology application, the substrate surface flatness and TTV are critical factors, as they will impact yields in device fabrication. The advantages given by Corning Incorporated's fusion forming process for supplying substrates for electronics applications, particularly interposers, has been previously reported. [1, 2] Supplies of 300mm diameter wafers with TTV < 2 μm are readily available today. Because the fusion process is capable of delivering sheets several meters in size, high volume scaling of quality wafers and panels for the semiconductor industry is also easily achievable. In addition to scaling glass substrate size, it is possible scale the process to deliver ultra-slim flexible glass to thicknesses down to ~100 um. Providing large substrates in wafer or panel format at 100 um thickness gives significant opportunities to reduce manufacturing costs of interposers.

Glass Interposer Demonstrators

The ability to provide glass substrates in a cost effective manner as described above is very important. It is also important to be able to leverage existing equipment and processes to transform these glass substrates into functional interposers. Previously we have described the ability to provide precision holes in glass [1], as well as initial demonstrations of metalizing the substrates [2-4].

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Fig. 1. Manufacture of high quality ultra-slim flexible glass provides substantial opportunities to deliver substrates for TGV that do not require post processing.

Collaborative work with the Industrial Technology Research Institute (ITRI) in Taiwan was done using blind vias in 300 mm diameter glass wafer substrates. Corning provided the glass wafers with blind holes, and ITRI performed the design, via fill and subsequent metallization processes. A number of factors which influences the via filling performance, especially the non-optimized plating will lead to the voids inside the via. The void defect will impact current density, chip performance and the life time of the chip. Therefore, it is very important to understand the quality of the Cu filling within TGV substrates. A PVD process was used to sputter an adhesion layer (Ta) on the via sidewall, and afterward a Cu seed layer was applied, followed by a conformal Cu plating process for filling the via. Good Cu filling within the smooth sidewall profile is demonstrated in figure 2a. The redistribution layer (RDL) is also demonstrated in figure 2b, which exhibited very good adhesion through the hatch test.

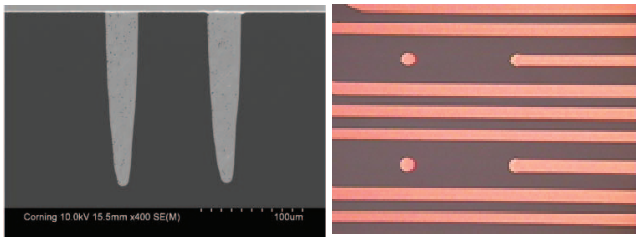

Fig. 2. X-SEM- Cu filling performance (2a, left) and RDL routing (2b, right) with TGV substrate based on Corning fusion glass.

In addition to filling the vias, ITRI incorporated coplanar waveguide and micro-strip structures onto the glass substrate and made similar structures in silicon. Figure 3 shows the glass and silicon interposer devices manufactured at ITRI.

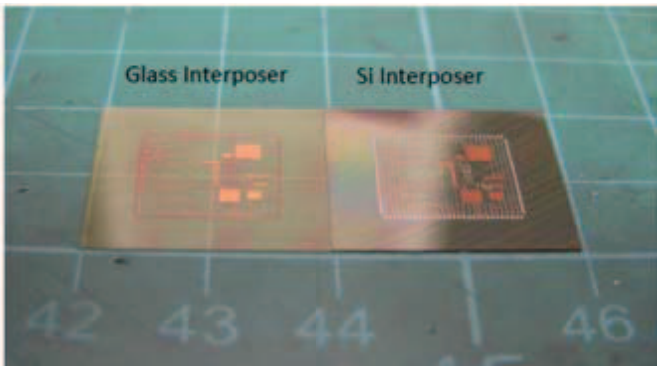

Fig. 3. Glass and Silicon Interposer Test Vehicles (ITRI)

Figure 4 demonstrates example results from this work. Figure 4a shows the microstrip lines included in the interposer design and Fig. 4b shows the results from testing the insertion loss in both glass and silicon substrates. There are curves showing the loss for lines 0.9 – 2.1 mm long. As expected, the loss is significantly lower in glass substrates than it is in silicon substrates. One important aspect of this work is that tools used to metallize the glass substrates are the same as those used in the industry today to metallize silicon substrates, with only minor process modifications.

As mentioned above, glass material properties are determined by the specific composition, making it possible to tailor glass composition to achieve a targeted CTE; thus enabling management of stack warp. Previously, we have shown examples of the material properties of two fusion formed glass types, in which it is possible to achieve very different CTE values while maintaining similar mechanical properties [1]. Other characteristics, such as electrical properties and chemical durability, may also be adjusted by optimizing the glass composition. Understanding these effects and finding the best way to manage these factors is an important consideration in TGV applications. Below we review results from applying CTE modifications to the interposer substrate to understand how that will affect stack warp.

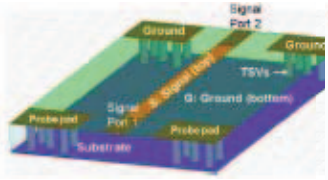

Fig. 4a: Microstrip line structure.

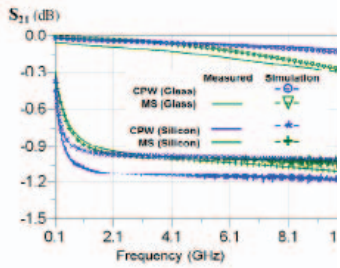

Fig. 4b: Insertion loss for glass and silicon interposers. Insulation properties of glass have significant advantages in reducing insertion loss.

Leveraging CTE to Manage Warp

Finite element analysis (FEA) has been applied in an effort to understand how the CTE of different glass compositions affect the warpage of a package with glass interposer. In addition, a comprehensive design of experiments (DOE) based regression analysis was conducted using finite element analysis to understand the factors and interactions that affect the package warpage. In this effort, a well-known package design [5] is used in this study. The finite element model developed is a three dimensional model with quarter symmetry used to represent the whole package. The reference temperature at which the package is assumed to be stress free is 150 C. and the strains are estimated at the final temperature of 25 C. This implies that the strains and stresses are estimated for temperature difference of 125 C. Constitutive relation for all the materials is linear and elastic. Silicon is modeled as an anisotropic material and BT substrate is modeled as orthotropic material. All other materials are modeled as isotropic. The package is discretized using a quadratic solid element with 20 nodes. Each node has three degrees of freedom, which are translations in x-, y- and z-directions. The microbumps are in the order of 30 microns in height and 50 microns in diameter approximately. The microbump consists of three layers [6] : a) copper layer towards the IC side b) electrodless Nickel immersion gold towards the interposer side with c) 99% Sn in between. These are surrounded by the underfill. Due to the differences in the scale of these joints, it is not practical to model every fine detail. Instead, a homogeneous layer representing microbumps and the underfill can be modeled with effective properties. The effective properties are estimated using separate finite element models. In these separate models, a unit cell comprising of a micro-bump and the underfill is modeled and a unit displacement is applied. The stress and strain resulting from this load is used to estimate the effective modulus and CTE in different directions. Similarly, the effective material properties of C4 joints layer are estimated. Figure 5 below shows the schematic of the finite element model on the whole package.

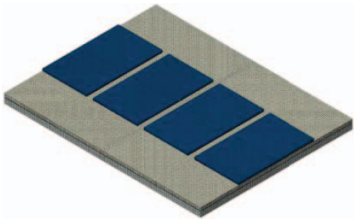

Fig. 5a: Isometric view of the entire package.

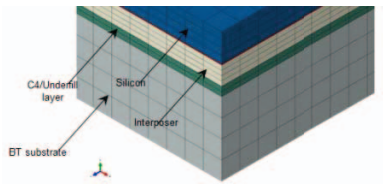

Fig. 5b: Close-up view through the package thickness

Figure 6 below shows the warpage of a package with four chips on a glass interposer substrate.

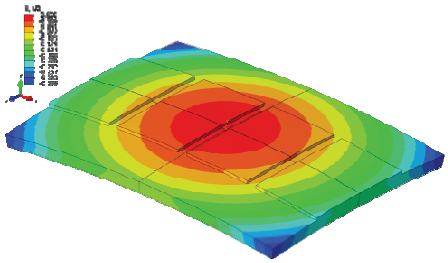

Fig. 6: Warpage of the Package.

Figure 7 below shows the variation of the package with varying CTE and the thickness of the interposer.

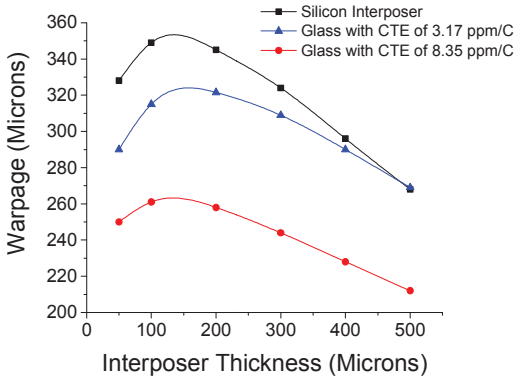

Fig. 7: Warpage vs. Interposer Thickness

At a given interposer CTE, the package warpage decreases with interposer thickness. However, if the interposer thickness decreases beyond 100 microns, it does not appear to contribute to the package warpage and the substrate completely determines the behavior. The warpage decreases with increasing interposer CTE because as the CTE of interposer increases, the difference between the interposer and substrate CTE decreases and therefore, the warpage decreases. Next, a DOE was set up using Box-Wilson central composite design. A Box-Wilson Central Composite Design contains an embedded factorial or fractional factorial design with center points that is augmented with a group of `star points' that allow estimation of curvature. Commercially available software, MINITAB, is used in this study to set up the DOE and analyze the results. Table 1 below shows the factors and their ranges considered in this study.

It can be observed that the CTE and thickness of interposer, substrate thickness and their interactions play a significant role in affecting package warpage. The mean effects of interposer modulus and thickness of flip-chip joints are minimal for package warpage. The advantage of the glass interposer is that its CTE can be engineered depending on its interactions with its thickness and substrate thickness. In addition, the interposer CTE can be adjusted such that the C4 joints reliability and microbump reliability is optimized. This is clearly a significant advantage compared to alternate materials for interposer.

Table 1 below shows the material properties of different materials used in the package.

Table 1: FEA Material Properties

Material	Elastic Modulus (MPa)	Poisson Ratio	CTE (ppm/C)
Silicon	See Table 2 below	NA	2.6
Interposer (Glass A, B)	73600 (A) 71700 (B)	0.23 (A) 0.21 (B)	3.17 (A) 8.35 (B)
Substrate	x,z = 29647-39.438T y = 12962-17.168T	xy,zy = 0.39 xz=0.11	16 (in-plane) 84 (out-of-plane)
Microbump and Underfill Effective Properties	20705	0.3	40
C4 joints and Underfill Effective Properties	8517.8	0.35	25

Table 2: Anisotropic properties of Silicon [5]

Constant	C11=C22	C12	C13	C33	C44	C55	C66
Value [GPa]	194.5	35.7	64.1	165.7	79.6	79.6	50.9

Conclusions

The electrical performance of glass, and tunability of other material properties such as CTE and chemical durability, generates tremendous incentive for using glass as a TGV substrate for 2.5D and 3D applications.

Moreover, the fusion forming process provides excellent attributes such as a pristine surface, low warp/ TTV, and can create a wide range of substrate sizes and thicknesses. These attributes provide glass with additional advantages for low manufacturing cost and scaling to large dimensions.

With glass substrates of different sizes, thicknesses, and compositions, we have developed a via formation process that meets a wide range of TGV requirements. This via formation process does not create flaws in the glass interposer, so the inherent strength of the glass substrate is retained.

The work reported here also show that existing metallization technology can be leveraged to generate very good Cu filling performance. A continuous seed layer and void-free Cu filling were observed. The RDL results also show that metal can be smoothly plated on the glass. The ability to generate well-formed and filled TGV has been demonstrated, and fully populated test vehicles using glass interposers have been created. These test vehicles indicate that good electrical, thermal and reliability performance can be achieved using glass interposers. Finite element analysis also shows that an appropriate choice of interposer CTE, which is adjustable using glass composition, can have a beneficial impact on the total warp of a 3D-IC stack. With glass, opportunities for truly cost-effective interposer solutions with improved reliability exist, and work continues to move these solutions closer to commercialization.

Acknowledgments

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