# Comparison of the "Pad-Open-Short" and "Open-Short-Load" Deembedding Techniques for Accurate On-Wafer RF Characterization of High-Quality Passives

Luuk F. Tiemeijer, Ramon J. Havens, André B. M. Jansman, and Yann Bouttement

***Abstract*—The impedance errors remaining after applying the industry standard "open-short," a "pad-open-short," and a "open-short-load" deembedding scheme on a 0.43-nH 20-GHz high-$Q$ single-loop inductor test structure are investigated using real $S$-parameter data taken up to 50 GHz. Since the latter two deembedding schemes both correct for all parasitic elements of the test structures, they are, at least in principle, error free. The accuracy of the "open-short-load" deembedding scheme, however, critically depends on how well the reactive part of the load resistance is accounted for. This issue makes the more simple "pad-open-short" deembedding scheme an attractive choice because the required split between external and internal capacitances is easy to make, either based on process and layout information or from measurements done on a "pad" dummy structure.**

***Index Terms*—Calibration, deembedding, integrated circuits, on-chip inductors, on-wafer microwave measurements.**

## I. Introduction

With THE increasing operating frequencies of many wireless communication standards, the demands on the accuracy of on-wafer $S$-parameter measurements become increasingly stringent. Since there are only limited possibilities to reduce wafer probing parasitics by down scaling of the on-wafer test structures, highly accurate deembedding schemes become a necessity. The most basic deembedding method is the simple "open" deembedding scheme, which was first introduced in 1987 [1]. In this technique, the pad capacitance is measured on an "open" test structure, and used to correct the measurement taken on the device-under-test (DUT). To include interconnect resistance and inductance, the "open-short" deembedding method was introduced in 1991 [2]. This method is now regarded as the industry standard and requires two dummy test structures. However, this approach and alternatives [3], [4], employing a few more dummy structures, assume a specific lumped-element circuit approximation, which reduces deembedding accuracy at high frequencies [5].

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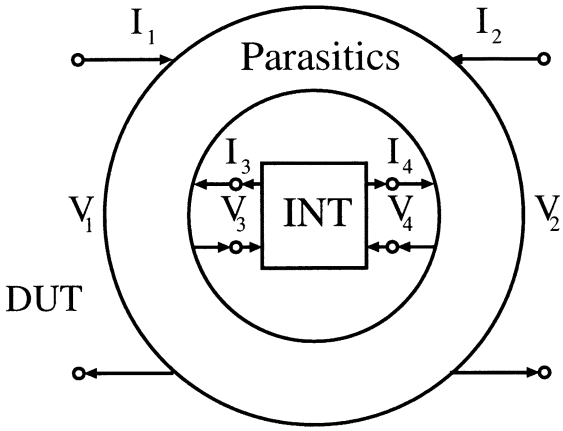


Fig. 1. Illustration of the general four-port description of the parasitics to be deembedded. The DUT is measured at ports 1 and 2, whereas the intrinsic device (INT) is connected to ports 3 and 4.

In this paper, we compare the benefits of two deembedding strategies employing one additional dummy test structure. The first one is a "pad-open-short" strategy, which is a three-step version of the four-step approach introduced in [6]. The second one is an "open-short-load" strategy, which is a simplified and rationalized version of the approaches proposed in [7] and [8]. We will first show that both approaches consider all relevant parasitics in a general manner and, thus, are, at least in theory, well suited to provide better accuracy at high frequencies.

## II. Four-Port Parasitic Deembedding Theory

To generalize the deembedding problem and avoid potential errors by simplifications, a four-port system calibration methodology was introduced in [8]. In this methodology, the *I–V* relationships between the extrinsic and intrinsic ports (Fig. 1) are expressed in a $4 \times 4$ $Y$-matrix according to

$$\begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} = \begin{pmatrix} Y_{11}Y_{12}Y_{13}Y_{14} \\ Y_{21}Y_{22}Y_{23}Y_{24} \\ Y_{31}Y_{32}Y_{33}Y_{34} \\ Y_{41}Y_{42}Y_{43}Y_{44} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix}. \quad (1)$$

The notation can be significantly simplified by defining $V_e$ and $I_e$ to represent the extrinsic voltage and current vectors, and $V_i$

and $I_i$ to represent the intrinsic voltage and current vectors. This reduces the above equation to

$$\begin{pmatrix} I_e \\ I_i \end{pmatrix} = \begin{pmatrix} Y_{ee} Y_{ei} \\ Y_{ie} Y_{ii} \end{pmatrix} \begin{pmatrix} V_e \\ V_i \end{pmatrix} \tag{2}$$

where $Y_{ee}, Y_{ei}, Y_{ie}, Y_{ii}$ are four $2 \times 2$ matrices. Using these, the desired intrinsic device $Y$-parameters $Y^{\mathrm{INT}}$ and measured extrinsic $Y$-parameters $Y^{\mathrm{DUT}}$ can be related as [8]

$$Y^{\mathrm{DUT}} = Y_{ee} - Y_{ei}(Y^{\mathrm{INT}} + Y_{ii})^{-1} Y_{ie}. \tag{3}$$

In [8], a procedure requiring five dummy structures is further given to find all 16 variables of the four $2 \times 2$ matrices. The industry standard "open-short" deembedding method uses only two of these dummy structures, an "open" where $Y^{\mathrm{INT}}_{\mathrm{open}} = 0$, and a "short" where $(Y^{\mathrm{INT}}_{\mathrm{short}})^{-1} = 0$. Applying this, one obtains

$$Y^{\mathrm{OPEN}} = Y_{ee} - Y_{ei}(Y_{ii})^{-1} Y_{ie} \tag{4}$$

and

$$Y^{\mathrm{SHORT}} = Y_{ee} \tag{5}$$

In the "open-short" method, the deembedded device parameters $Y^{\mathrm{OS}}$ are calculated by

$$Y^{\mathrm{OS}} = \left( \left( Y^{\mathrm{DUT}} - Y^{\mathrm{OPEN}} \right)^{-1} - \left( Y^{\mathrm{SHORT}} - Y^{\mathrm{OPEN}} \right)^{-1} \right)^{-1}. \tag{6}$$

Substituting (3)–(5) in (6), it is seen that the result of this method can be related to the intrinsic device $Y$-parameters as

$$Y^{\mathrm{OS}} = Y_{ei}(Y_{ii})^{-1} Y^{\mathrm{INT}} (Y_{ii})^{-1} Y_{ie}. \tag{7}$$

The four-port deembedding procedure outlined in [8] is far too general. One can safely assume the $4 \times 4$ parasitics matrix to be symmetrical, thus reflecting the reciprocal nature of the interconnect connecting the intrinsic device with the test-structure pads. For reciprocal interconnect, we have $Y_{ee} = Y_{ee}^T, Y_{ii} = Y_{ii}^T$, and $Y_{ie} = Y_{ei}^T$. This allows us to simplify the above relation into

$$Y^{\mathrm{OS}} = A Y^{\mathrm{INT}} A^T \tag{8}$$

where $A = Y_{ei}(Y_{ii})^{-1}$. For the usual on-wafer test structures, at low frequency, the dominant parasitics are the interconnect resistances. At these frequencies, standard "open-short" deembedding is correct and the $A$ matrix equals the unitary matrix. Once we know the four elements of the matrix $A$, we are able to derive the intrinsic device $Y$-parameters at any frequency from the result obtained after the standard "open-short" deembedding. To find these four elements, we need two additional "left" and "right" resistive dummy structures where

$$Y^{\mathrm{INT}}_{\mathrm{left}} = \begin{pmatrix} 1/R_l & 0 \\ 0 & 0 \end{pmatrix} \tag{9}$$

and

$$Y^{\mathrm{INT}}_{\mathrm{right}} = \begin{pmatrix} 0 & 0 \\ 0 & 1/R_r \end{pmatrix} \tag{10}$$

and where $R_l$ and $R_r$ represent the values of the resistances in these structures. With these dummy structures, the $A$ matrix can be found solving

$$Y^{\mathrm{OS}}_{\mathrm{left}} R_l = \begin{pmatrix} a_{11}^2 & a_{11}a_{21} \\ a_{11}a_{21} & a_{21}^2 \end{pmatrix} \tag{11}$$

and

$$Y^{\mathrm{OS}}_{\mathrm{right}} R_r = \begin{pmatrix} a_{12}^2 & a_{12}a_{22} \\ a_{12}a_{22} & a_{22}^2 \end{pmatrix}. \tag{12}$$

There are two possible solutions for $a_{11}$ and $a_{22}$, but we can select the correct ones by requiring the $A$ matrix to be continuous over frequency and equal to unity at low frequency. Since many practical on-wafer test structures are drawn with identical left and right ports, the reciprocal four-port parasitic deembedding scheme is still too general. When the left and right ports are identical, the number of independent parameters in the symmetrical $4 \times 4$ parasitics matrix reduces from 10 to 6. As a result of this, the number of independent parameters in the $A$ matrix reduces from 4 to 2 since we will have $a_{11} = a_{22}$ and $a_{21} = a_{12}$, and we can omit the second resistive load dummy structure because it does not provide any new information. Alternatively, a symmetric "load" dummy structure with two resistive elements where

$$Y^{\mathrm{INT}}_{\mathrm{load}} = \begin{pmatrix} 1/R & 0 \\ 0 & 1/R \end{pmatrix} \tag{13}$$

can be used. With this "load" dummy structure, the $A$ matrix can be found solving

$$Y^{\mathrm{OS}}_{\mathrm{load}} R = \begin{pmatrix} a_{11}^2 + a_{21}^2 & 2a_{11}a_{21} \\ 2a_{11}a_{21} & a_{11}^2 + a_{21}^2 \end{pmatrix} = B. \tag{14}$$

Compared to (11), finding the elements of $A$ is now a bit more complicated, but the system $A^2 = B$ can still be solved and we can again select the correct roots by requiring the $A$ matrix to be continuous over frequency and equal to unity at low frequency. When it is known beforehand that the intrinsic device to be characterized is also symmetrical, the matrix multiplications commute, and the correction required on the "open-short" result simplifies to

$$Y^{\mathrm{OS}} = B Y^{\mathrm{INT}} \tag{15}$$

were we do not need to resolve the $A$ matrix anymore. To summarize, the above refinements of the four-port parasitic theory shows that we can deembed any reciprocal parasitic four-port structure surrounding our intrinsic device by first characterizing four dummy test structures. In many practical cases, however, when both ports are drawn identical, a simplified four-port deembedding scheme can be applied. This scheme requires only three dummies, which are: 1) an "open"; 2) a "short"; and 3) either a "left," "right," or "load" test structure.

## III. Three-Step Parasitic Deembedding Theory

In the three-step deembedding approach [5], the equivalent-circuit model of Fig. 2 with nine unknown impedances is assumed for the parasitics. Using this model, the desired intrinsic

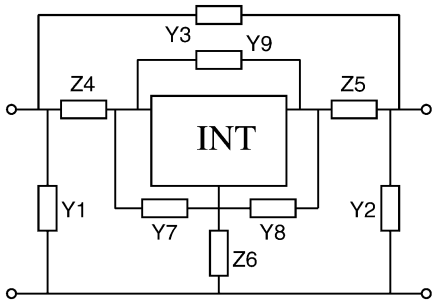


Fig. 2. Illustration of the parasitics assumed in the three-step deembedding approach. No *a priori* assumptions are made on the nature of these nine impedances.

device $Y$-parameters $Y^{\mathrm{INT}}$ and the measured extrinsic $Y$-parameters $Y^{\mathrm{DUT}}$ are related as

$$Y^{\mathrm{DUT}} = \left(\left(Y^{\mathrm{INT}} + Y_I\right)^{-1} + Z_S\right)^{-1} + Y_E \tag{16}$$

where

$$Y_E = \begin{pmatrix} Y_1 + Y_3 & -Y_3 \\ -Y_3 & Y_2 + Y_3 \end{pmatrix} \tag{17}$$

$$Z_S = \begin{pmatrix} Z_4 + Z_6 & Z_6 \\ Z_6 & Z_5 + Z_6 \end{pmatrix} \tag{18}$$

$$Y_I = \begin{pmatrix} Y_7 + Y_9 & -Y_9 \\ -Y_9 & Y_8 + Y_9 \end{pmatrix}. \tag{19}$$

For the open and short dummies, where $Y^{\mathrm{INT}}_{\mathrm{open}} = 0$ and $(Y^{\mathrm{INT}}_{\mathrm{short}})^{-1} = 0$, respectively, one obtains

$$Y^{\mathrm{OPEN}} = \left((Y_I)^{-1} + Z_S\right)^{-1} + Y_E \tag{20}$$

$$Y^{\mathrm{SHORT}} = (Z_S)^{-1} + Y_E. \tag{21}$$

It is easily seen that once $Y_E$ is known, one can find the other two unknown matrices $Z_S$ and $Y_I$ using the information provided by the open and short dummy structures. A straightforward solution here is to add a "pad" dummy structure, which only contains the probe pads and is especially designed to directly measure $Y_E$ through

$$Y^{\mathrm{PAD}} = Y_E. \tag{22}$$

An alternative approach is to derive the ratio between $Y_E$ and $Y_I$ from the probe pad and interconnect line dimensions and the process parameters and then use the low-frequency approximation

$$Y^{\mathrm{OPEN}} \approx Y_I + Y_E \tag{23}$$

to get a good estimate for $Y_E$. After that, we can recover the intrinsic device $Y$-parameters $Y^{\mathrm{INT}}$ using

$$Y^{\mathrm{INT}} = \left(\left(Y^{\mathrm{DUT}} - Y_E\right)^{-1} - Z_S\right)^{-1} - Y_I. \tag{24}$$

We can use the same approach to correct noise-figure data taken on active DUTs by subtracting the noise correlation matrices of $Y_E, Z_S$, and $Y_I$ from that of the DUT using the techniques described in [9]. For the general four-port deembedding scheme, this is less obvious. The three-step deembedding approach is almost as general as the reciprocal four-port deembedding scheme since it incorporates nine unknown impedances, whereas the four-port scheme assumes ten unknown impedance. When we assume $Y_{32} = Y_{41}$ and, thus, $Y_{ie} = Y_{ei}$, it is straightforward to show that the four $2 \times 2$ matrices of the four-port deembedding theory and the three $2 \times 2$ matrices of the three-step deembedding theory are related by

$$Y_{ee} = Y_E + (Z_S)^{-1} \tag{25}$$

$$Y_{ii} = Y_I + (Z_S)^{-1} \tag{26}$$

$$Y_{ie} = Y_{ei} = -(Z_S)^{-1}. \tag{27}$$

This allows us to conclude that when both ports are drawn identical, the four-port and three-step deembedding approaches are equivalent and equally accurate. Even when this is not the case, the differences will be small because asymmetric device connections will mainly affect $Y_I$, asymmetric probe placement will mainly affect $Y_E$, and $Y_{32}$ and $Y_{41}$ are expected to be small anyway. It could, therefore, be seen as a matter of preference whether an "open-short-load" or a "pad-open-short" procedure is used. In practice, however, the nonideality of the dummy structures and their impact on the final result needs to be considered in order to make the correct choice between these two alternatives. This will be the topic of the remainder of this paper.

## IV. Dummy Nonidealities

In commercially available RF-probe calibration substrates, laser trimming is used to bring the resistors of the 50-$\Omega$ load standards within a fraction of a percent of their target value, whereas the geometry is chosen such that the reactive parts coming from the inductance and self-capacitance cancel each other over a wide range of frequencies. This is clearly not feasible for the polysilicon resistors in an on-wafer "load" dummy structure. However, we may safely assume the $A$ and $B$ matrices to equal unity at low frequency, and base the final correction on the actual resistance values. "Open-short" deembedding cannot provide the reactive part of the intrinsic load impedances since it is not seen at low frequencies, whereas at high frequencies, the $A$ and $B$ matrices no longer equal the unitary matrix. The typical parasitic capacitance to the substrate of these polysilicon resistors, which can be as high as 30 fF [10] and may have a strong frequency dependence due to the substrate resistance, has to be accurately characterized and accounted for in order for the "open-short-load" deembedding scheme to produce accurate results. It is possible to minimize the parasitic capacitance of the resistors by down-scaling. However, due to design rule limitations and process uncertainties it will be difficult to know the reactive part of the intrinsic load impedances better than within a few femtofarads. At several tens of gigahertz, this may translate into significant phase errors of the eigenvalues of the $A$ and $B$ matrices, which, in turn, will adversely affect measured quality factors [11] and power gains. For the commercially available RF-probe calibration standards, "open" residual capacitance and "short" inductance are well known and accounted for in the calibration procedure. In the standard "open-short" deembedding approach, these dummy imperfections are usually neglected and absorbed in the intrinsic device. However, care

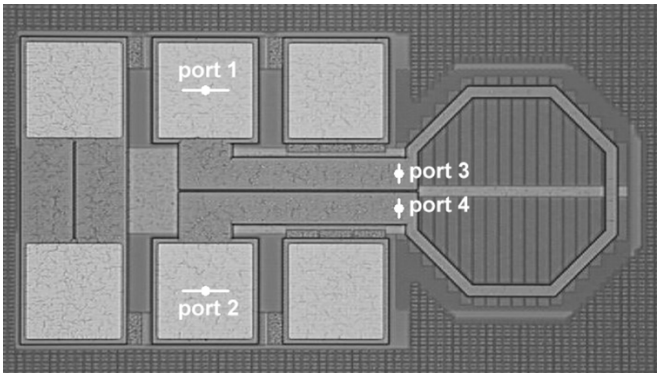


Fig. 3. On-wafer test structure for a 0.43-nH 20-GHz high-$Q$ single-loop inductor. The probe-pad pitch is 125 $\mu$m. The inductor outer diameter and track widths are 200 and 10 $\mu$m, respectively. The positions of the external ports 1 and 2 and internal ports 3 and 4 are indicated.

has to be taken that the intrinsic device is not over-corrected due to a (lossy) intrinsic open fringe capacitance or a resistance found in the short dummy, which is not present in the DUT. For a "pad" dummy structure, nonidealities seem to be less of an issue because its main purpose is to get an estimate for the ratio between $Y_E$ and $Y_I$.

## V. Measurements and Verification

The deembedding errors at high frequency of the standard "open-short" deembedding procedure can be seen when advanced high-speed bipolar transistors or MOSFET devices are characterized, but are most pronounced for high-quality passives [5] such as on-wafer inductors. We will, therefore, compare the "open-short-load" and "pad-open-short" deembedding procedures for the 0.43-nH 20-GHz high-$Q$ single-loop inductor shown in Fig. 3. Due to its small size, this is an extremely difficult device to characterize because its intrinsic impedance is overwhelmed by the test-structure parasitics, and the parasitic crosstalk between the two ports is not negligible. This inductor originates from a set of inductor structures for which results were reported in [12], was realized in a BiCMOS process featuring a 3-$\mu$m-thick top metal layer with a sheet resistivity of 10 m$\Omega$, and employs a ground shield made of polysilicon bars to prevent substrate loss. "Open," "short," and "load" dummy structures were realized in the usual way by removing the inductor, its polysilicon shield and the center tap connection. The signal pads were realized in the two top metal layers and are shielded from the substrate by a buried n+ layer with a sheet resistivity of 25 $\Omega$. The interconnect is realized in the top metal only and is shielded from the substrate by the first metal layer with a sheet resistivity of 60 m$\Omega$. The load resistances at the end of the interconnect lines were realized in n-type polysilicon, measure $1.9 \times 6.6$ $\mu$m with heads, and $0.6 \times 6.6$ $\mu$m without heads, and have a nominal resistance of 30 $\Omega$. After line-reflect-reflect-match (LRRM) calibration with automated load inductance extraction [13] for all structures, $S$-parameters have been measured up to 50 GHz with a port power level of $-10$ dBm. To ensure identical probe placement for the DUT and the dummies, a semiautomatic test bench is used. Results for the three dummy structures are shown in Fig. 4. The characteristic impedance of the on-wafer microstrip

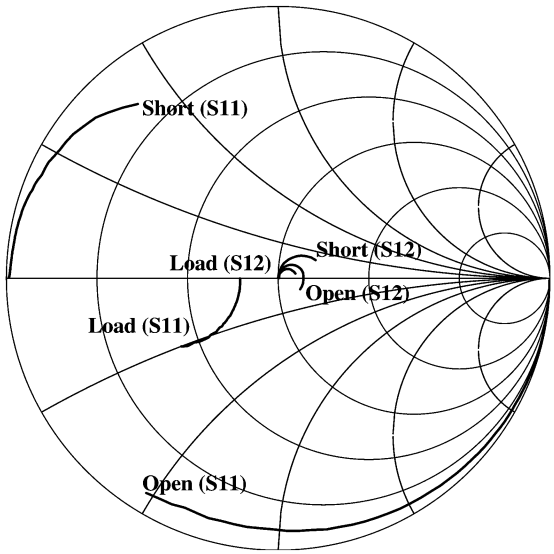


Fig. 4. $S$-parameters measured up to 50 GHz on the "open," "short," and "load" dummy structures. The characteristic impedance of the interconnect lines is 23 $\Omega$, the load resistances are 36 $\Omega$. The parasitic crosstalk between the two ports is acceptable, but certainly not negligible.

TABLE I
Comparison of Test-Structure Parasitics Calculated From Process Data and Extracted From Measured $S$-Parameters. The Agreement Is Within the Normal Process Variations

| Capacitance / Resistance | calculated | extracted |
|---|---|---|
| pad - ground | 52.2 fF | 54.5 fF |
| pad - ground | 17 ohm | 15 ohm |
| interconnect - ground | 46.2 fF | 48.2 fF |
| interconnect - interconnect | 9.1 fF | 11.3 fF |
| intrinsic load | 30 ohm | 36 ohm |
| intrinsic load | 2.5 fF | ? |

lines connecting to the inductor appears to be approximately 23 $\Omega$. From process parameters, the pad and interconnect parasitics depicted in Table I are found, which agree well with the values extracted from $S$-parameter data measured on the open dummy structure. In this extraction, the ratio between pad and interconnect capacitances is assumed to be the same as for the calculated capacitances. Applying "open-short" deembedding on the $S$-parameter data measured on the "load" dummy structure, the load resistance value was found to be somewhat higher (Table I) than predicted. A considerable difference was found for the parasitic parallel capacitance of the load resistance using a standard layout extraction tool (1.1 fF) and a two-dimensional (2-D) electrostatic field solver (2.5 fF, Table I). The latter was taken as the "correct" value. Since a "pad" structure was not available in the experiment, $Y_E$ was synthesized using the extracted parameters listed in Table I and contains the full extracted pad capacitance with its series resistance and half the extracted interconnect line capacitances.

In comparing results, we restrict ourselves to the differential impedance

$$Z_{\text{dif}} = \left(Z_{11}^{\text{INT}} - Z_{12}^{\text{INT}} - Z_{21}^{\text{INT}} + Z_{22}^{\text{INT}}\right) \tag{28}$$

and differential $Q$

$$Q_{\text{dif}} = \text{Im}(Z_{\text{dif}})/\text{Re}(Z_{\text{dif}}). \tag{29}$$

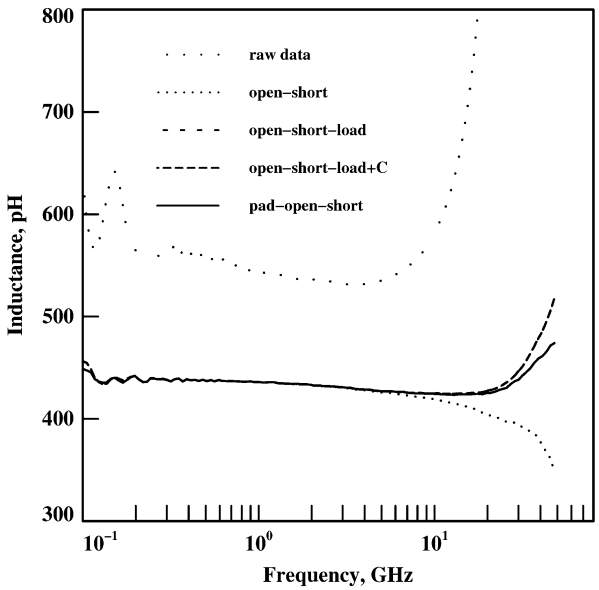


Fig. 5. Inductance of the 0.43-nH single-loop inductor versus frequency. Only "open-short-load" and "pad-open-short" deembedding procedures reproduce the expected increase in inductance beyond 20 GHz when the inductor is approaching its resonance frequency.

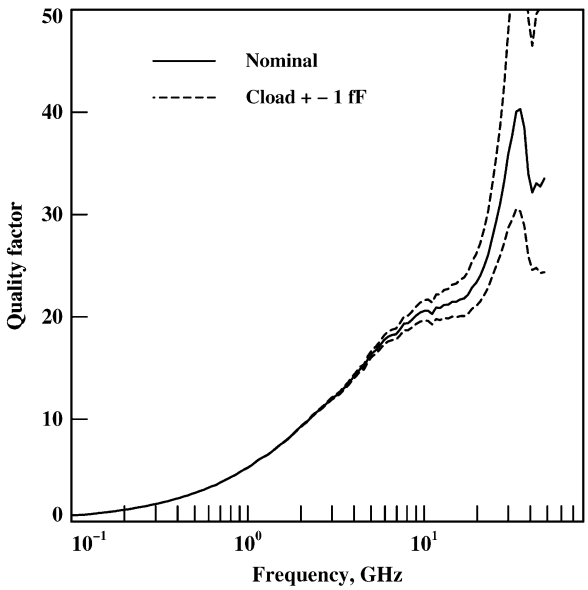


Fig. 7. Differential $Q$ factor of the 0.43-nH single-loop inductor versus frequency as obtained with "open-short-load" deembedding. The dashed lines represent a sensitivity analysis where the estimated load capacitance has been modified by $+$ and $-$ 1 fF.

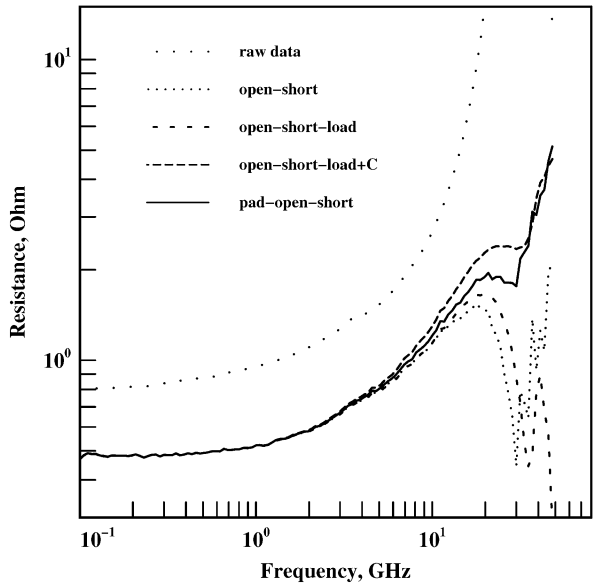


Fig. 6. Resistance of the 0.43-nH single-loop inductor versus frequency. Both "open-short" and "open-short-load" deembedding produce unphysical artefacts beyond 20 GHz. "Pad-open-short" deembedding produces better results (solid line). When the 2.5-fF parallel capacitance of the load resistances is accounted for ("open-short-load+C") , similar results are obtained.

Figs. 5 and 6 show the inductance $(\mathrm{Im}(Z_{\mathrm{dif}})/\omega)$ and ac resistance $(\mathrm{Re}(Z_{\mathrm{dif}}))$ of the 0.43-nH single-loop inductor versus frequency. Two types of "open-short-load" deembedding are compared. In the standard version, the actual polysilicon resistance values found with "open-short" deembedding are used while the reactances are set to zero. In the improved version, the parallel capacitance of 2.5 fF calculated with the 2-D electrostatic field solver is also accounted for. It can be seen that only "open-short-load" and "pad-open-short" deembedding procedures recover the expected increase in inductance beyond 20 GHz when the inductor is approaching its resonance frequency. For the ac resistance, both "open-short" and standard "open-short-load" deembedding procedures yield unphysical artefacts beyond 20 GHz. In fact, due to the skin effect, a monotonic increase with frequency would be more in line with expectations. Here, the improvement in deembedding accuracy obtained from the standard "open-short-load" methodology over the "open-short" result is marginal. The "pad-open-short" deembedding however, produces fairly realistic results, as shown by the solid line in Fig. 6. Only when the 2.5-fF parallel capacitance of the load resistances is accounted for are similar results obtained for the "open-short-load" deembedding technique. The intrinsic load parasitic inductance has not been calculated. Including this inductance will improve the agreement between the two deembedding approaches because it partly compensates the load parasitic capacitance. Using lumped-element equivalent-circuit modeling, the dip in the series resistance observed around 30 GHz could be attributed to a fringe capacitance of the "open" dummy coupling to the lossy substrate, which is not seen in the actual inductor structure. Since the amount of energy dissipated at the end of the open dummy interconnect lines is difficult to quantify, for clarity, it was chosen not to correct for this effect.

## VI. Sensitivity Analysis

As shown in Section V, it is essential to accurately account for the reactive parts of the load resistances to apply the "open-short-load" deembedding scheme successfully. To obtain quantitative figures for this, a sensitivity analysis was conducted. Fig. 7 shows the $Q$ factor of the 0.43-nH single-loop inductor versus frequency obtained after "open-short-load" deembedding. To see the impact of the parasitic load capacitance, its estimated value has been varied by $+$ and $-$ 1 fF. As a result of this, the peak $Q$ factor is seen to vary from 40

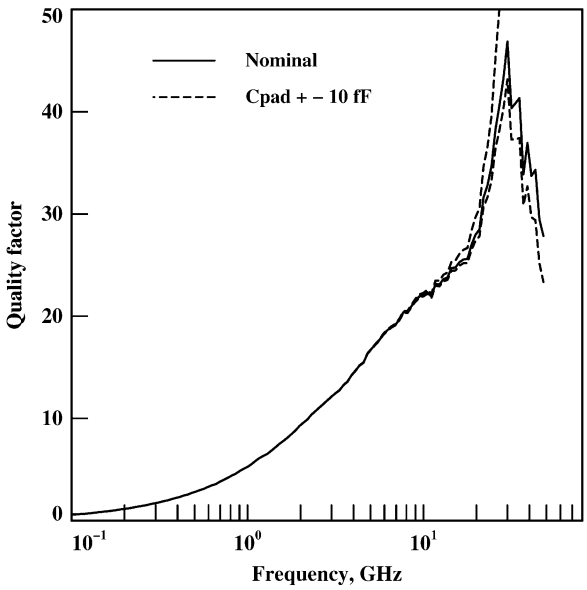


Fig. 8. Differential $Q$ factor of the 0.43-nH single-loop inductor versus frequency as obtained with "pad-open-short" deembedding. The dashed lines represent a sensitivity analysis where the pad-to-ground and interconnect-to-ground capacitances were enhanced/decreased by + and − 10 fF.

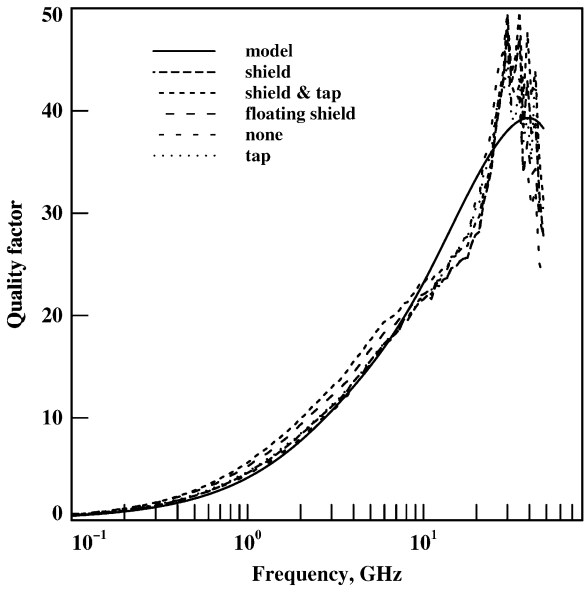


Fig. 9. Differential $Q$ factors measured on five different versions with and without a shield and with and without a grounded center tap of the 0.43-nH single-loop inductor versus frequency as obtained with "pad-open-short" deembedding.

to 30 and 60. At 20 GHz, the variation is from 24 to 21 and 27. This is quite large given the fact that, in practice, it will already be extremely difficult to know the reactive part of the load resistance within this 1 fF. Fig. 8 shows the $Q$ factor of the 0.43-nH single-loop inductor versus frequency obtained after the "pad-open-short" deembedding. To see the impact of the pad capacitance, its estimated value has been varied by + and − 10 fF. To comply with (23), the estimated pad series resistance and interconnect capacitance values had to be varied by a similar amount in the opposite direction. Due to this compensation effect, the impact of this significant modification of the pad capacitance on the $Q$ factor is small. Although the peak $Q$ factor is seen to vary significantly, at 20 GHz, the variation is only from 28.4 to 27.8 and 30.5, which is per femtofarad deviation 25 times less than for the previous case. Finally, Fig. 9 gives a comparison of the $Q$ factor measured on inductor versions with and without polysilicon ground shields and with and without a grounded center tap. Although grounding the center tap significantly changes the raw $S$-parameters measured on the inductor structure, the $Q$ factor derived from the differential impedance is not affected. The $Q$ factor predicted by our scalable inductor compact model reported in [12] is included for reference. The overall agreement is fairly good. The remaining differences are caused by nonidealities of the "open" and "short" dummy structures. For inductors with larger inductance values and lower $Q$ factor values, these minor artefacts were not seen [12].

## VII. Summary and Conclusions

In this paper, we have investigated the practical benefits of adding a load dummy structure to the industry standard "open" and "short" dummy structures. We have found that the benefits of including this dummy structure are marginal unless the reactive part of its impedance is accurately accounted for. This cannot be done without any prior process knowledge and is susceptible to errors. We fear that this is also the case for the more general five-dummy scheme proposed in [8]. Almost identical results were obtained using a three-step "pad-open-short" approach, basically a simplified version of our earlier work [5], which requires only two dummy structures since the fraction of the total open dummy capacitance also seen in the pad dummy structure can easily be estimated with only modest process knowledge. A sensitivity analysis shows that the impact of errors in the estimated pad capacitance in the "pad-open-short" approach is 25 times less than the impact of errors in the estimated parasitic capacitance of the load resistance in the "open-short-load" approach. This makes the "pad-open-short" deembedding scheme an attractive alternative because the required split between external and internal capacitance generally is fairly simple to make either based on process and layout information or from measurements done on a "pad" dummy structure. Applying both deembedding approaches on the same dataset provides a powerful tool to check their validity, and that of the deembedded data.

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