BEP Daniel Tyukov 2024-2025 B

WEDNESDAY, 12 FEBRUARY 2025

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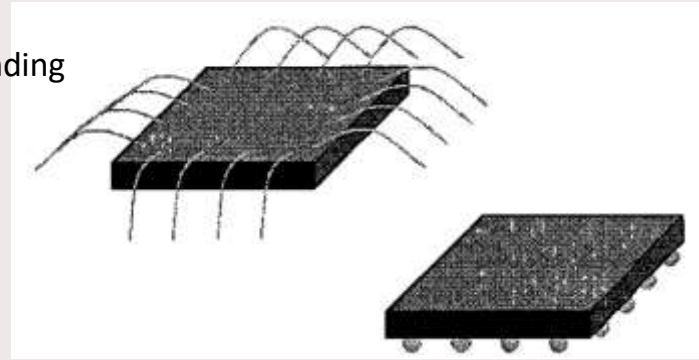
TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY

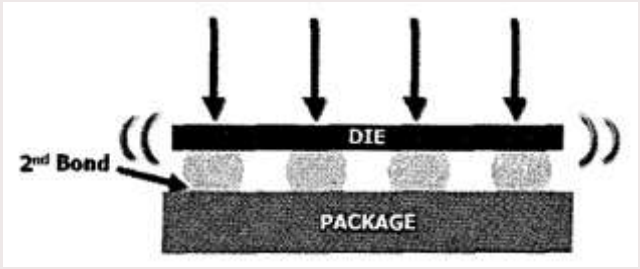
Flip chip technology [1]

- Shorter connections → increased speed/bandwidth
- Higher pad density → enables array
- Co-integration of different substrates → electronic/photonic integration

Wire bonding



Flip chip



The gold bumps

- To attach the die to the package, we use gold ball bumps. These act as a glue and connection between the pads of the die and the package.
- In the previous setup we've attached these gold bumps to the package and flip the chip onto it to attach it.
- The ball bumps are created using the wire bonding machine and placing the start and end of the wire in the same location.
- Any combination of heat, pressure and ultrasound can be used the attach the die to the package.

The interposer

- For integration of large arrays of DACs and connecting them to a photonic beamformer, we require an interposer
  - The DAC array is a 2D grid, whereas the beamformer is a 1D array. Implementing the DAC in a 1D array is possible in theory, but the cost of the silicon chips makes this unviable.
- An interposer is comparable to a PCB, but higher quality. At the TU/e we can produce single gold layer interposers on a glass substrate.
- Compared to PCBs the interposer is much flatter. This allows for the use of flip chipping.

Objectives

- Characterization of interposer
  - How do different production methods impact
    - the interposers performance?
    - the connection yield?

- Flip chip
  - What is the typical yield of the connections during flip chipping?
  - What is the quality of the connections between the chip and interposer?
    - DC resistance (statistical distribution?)
    - Frequency response

Deliverables and meetings

- BEP marketplace
  - Code of conduct
  - Initial planning (PRV 52)
  - Revised planning (PRV 53)
  - Intermediate Paper (graded, but weight 0%)
  - Reflection report (PRV43)
  - Final paper (PRV33)
  - Presentation (PRV23)

Deliverables and meetings – cont'd

- Weekly meetings with Timo, bi-weekly meetings with Marco
- Paper drafts are possible and advised but not required.

- Academic writing workshop (PRV33)
- Information skills session (PRV63)

- Please send your specific dates and deadlines to t.m.matray@tue.nl, as these change for each BEP project.

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References

1. J. Jordan, "Gold stud bump in flip-chip applications," 27th Annual IEEE/SEMI International Electronics Manufacturing Technology Symposium, San Jose, CA, USA, 2002, pp. 110-114, doi: 10.1109/IEMT.2002.1032735.