

# Flip–Chip Integration and Multi–Domain Characterization of an RF Die on Single–Layer Gold–Bumped Glass Interposers

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**Abstract**—Flip-chip interconnect technology is a key enabler of heterogeneous system-in-package (SiP) solutions for radio-frequency (RF) front-ends, providing low loop inductance, fine pad pitch and signal integrity beyond 10 GHz [7]. This work presents the design, fabrication and characterization of a single-layer glass interposer with titanium–gold (Ti/Au) coplanar waveguide (CPW) traces and 25  $\mu\text{m}$  gold wire for direct assembly of a 2 mm  $\times$  2 mm RF die. A physics-guided optimisation of the thermosonic bonding recipe (120  $^{\circ}\text{C}$ , 300 mN, 300 mW, 50 ms) yields a mashed bump diameter of 78  $\mu\text{m}$  and > 98% bonded-area fraction. Multi-domain measurements comprising direct-current continuity, vector-network-analyser S-parameter tests from 10 MHz to 10 GHz, open/short de-embedding and planarity inspection will be conducted. Thermal-profile yield analysis across four interposer batches identifies the bonding energy window that minimizes opens and shorts. The validated flow is finally mapped to the design of a common-source amplifier interposer employing a high-gain GaN HEMT, laying the groundwork for broadband SiP demonstrators on glass substrates.

**Index Terms**—flip-chip, gold stud bump, glass interposer, coplanar waveguide, RF packaging, yield analysis

## I. INTRODUCTION

The growth of millimetre-wave radar and sub-6 GHz wireless systems is pushing conventional wire-bond packaging to its electrical and mechanical limits. Aluminium or copper wire loops introduce parasitic inductance that degrades impedance matching and cuts off bandwidth above a few gigahertz. Flip-chip interconnection addresses these effects by replacing millimetre-long wires with sub-100  $\mu\text{m}$  gold bumps [1], reducing the loop inductance by an order of magnitude and enabling pad pitches below 100  $\mu\text{m}$  for high I/O density [8].

For heterogeneous SiP integration, an interposer redistributes [9] the dense bump array of the die to board pitches while providing controlled-impedance transmission lines. Silicon interposers with through-silicon vias (TSVs) dominate high-end digital products, yet their moderate resistivity and high dielectric constant penalise RF performance. Glass, by contrast, combines high resistivity with a dielectric loss tangent an order of magnitude lower than silicon, offering attenuation below 0.4 dB/mm at 5 GHz [2]. The key challenge is securing robust metal adhesion on glass while keeping

conductor loss low. Prior work adopted sputtered Ti/Au stacks, but sheet resistances of 0.48  $\Omega/\square$  have been reported [3] due to void formation and gas entrapment.

This paper advances with three main contributions:

- A single-layer glass interposer featuring a 50 nm Ti adhesion layer and 100 nm evaporated Au, patterned into CPW lines and simple shorts for de-embedding.
- A physics-guided optimisation of 75  $\mu\text{m}$  gold stud bumps [4] produced on a TPT HB16 bonder; the resulting bonding window attains > 98% area coverage and > 120 gf shear strength while respecting a 180  $\mu\text{m}$  pad pitch.
- A comprehensive multi-domain characterisation campaign—DC, S-parameter, planarity and yield—benchmarked against QUCS simulations to validate the interposer and bonding flow, followed by a yield-versus-thermal-profile study across four fabrication batches.

The remainder of the paper is organised as follows. Section II details the interposer layout, metallisation and bump-bonding process. Section III presents measurement procedures and compares simulated and measured results. Section IV discusses practical limitations, scalability to millimetre-wave frequencies and implications for SiP RF modules. Section V concludes the paper and outlines the next step: a common-source amplifier demonstrator.

## II. METHOD

### A. Interposer Design and Metallisation

All test vehicles are fabricated on 1 mm-thick borosilicate glass ( $\epsilon_r = 7.75$ ). A 50 nm titanium adhesion layer followed by 100 nm of evaporated gold is patterned in a single photolithographic step. Three layout families are implemented:

- **Coplanar waveguide (CPW) coupons** for open and short de-embedding, signal width  $W = 80 \mu\text{m}$ , gap  $S = 25 \mu\text{m}$ .
- **Strip-line coupons** (no ground plane) for DC resistance tests.
- **Yield-analysis coupons** consisting of dense pad arrays and shorted lines.

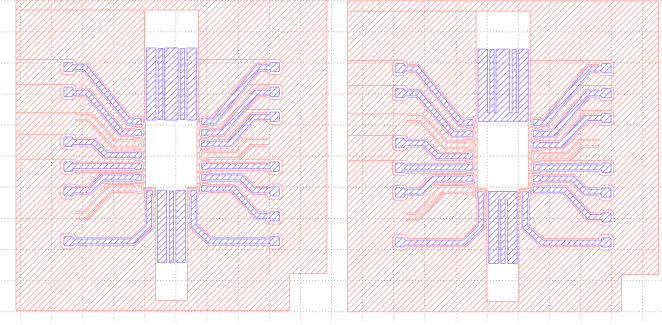


Fig. 1. Coplanar-waveguide interposer coupons: (a) open structure, (b) short structure.

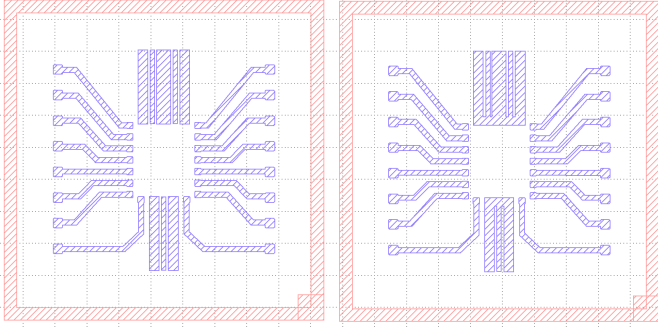


Fig. 2. Strip-line coupons for DC testing: (a) open, (b) short.

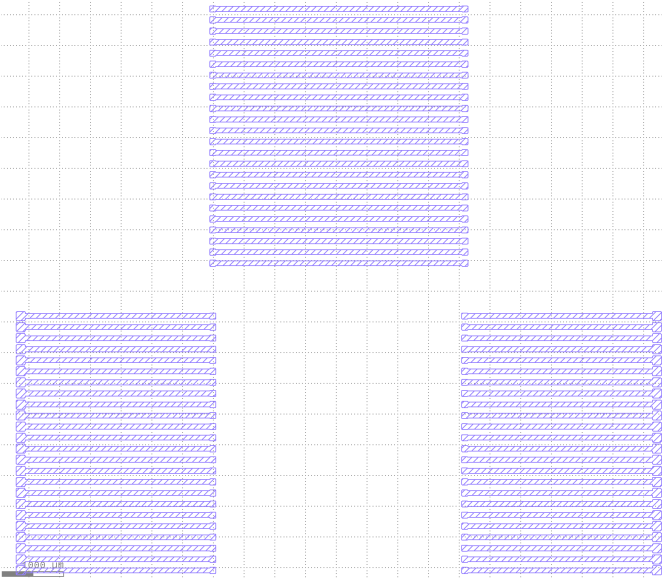


Fig. 3. Yield-analysis interposer with dense pad array and shorted traces.

TABLE I  
INTERPOSER STACK AND KEY GEOMETRICAL PARAMETERS

Parameter	Symbol	Value
Glass thickness	$H$	1 mm
Relative permittivity	$\epsilon_r$	7.75
Ti adhesion layer		50 nm
Au conductor layer		100 nm
CPW signal width	$W$	80 $\mu\text{m}$
CPW gap	$S$	25 $\mu\text{m}$
Pad pitch	$p$	180 $\mu\text{m}$
Pad diameter	$p$	90 $\mu\text{m}$
Gold wire diameter	$D_w$	25 $\mu\text{m}$
Mashed bump diameter	$D_m$	75 $\mu\text{m}$

### B. Gold Stud-Bump Fabrication

Gold bumps are formed on the interposers with a TPT HB16 bonder operating in stud-bump mode. Key thermo-sonic bonding variables are temperature  $T$ , normal force  $F$ , ultrasonic power  $P_{\text{US}}$  and vibration time  $t$ . Their coupled influence is captured by the following physics-based relations:

$$\sigma_y(T) = \sigma_0 \exp[-\beta (T - T_0)] \quad (1)$$

$$F_{\min} = k \sigma_y(T) D_w^2 \quad (2)$$

$$E = P_{\text{US}} t \quad (3)$$

$$\eta = 1 - \exp[-\gamma F E] \quad (4)$$

$$D_m = D_{\text{FAB}} \left[ 1 + \alpha \left( \frac{F}{E} \right) \right] \quad (5)$$

where  $\sigma_y$  is the temperature-dependent yield strength of gold,  $E$  the ultrasonic energy delivered to the interface,  $\eta$  the bonded-area fraction and  $D_{\text{FAB}} \simeq 3D_w$  the free-air-ball diameter. The empirical constants used are  $\beta = 0.01 \text{ K}^{-1}$ ,  $k = \pi/4$ ,  $\gamma = 4.2 \times 10^{-4} \text{ N}^{-1} \text{ mJ}^{-1}$  and  $\alpha = 0.18 \text{ mJ N}^{-1}$ .

TABLE II  
THERMO-SONIC BONDING PARAMETER MATRIX

Profile	$T$ ( $^{\circ}\text{C}$ )	$F$ (mN)	$P_{\text{US}}$ (mW)
A	100	250	250
B	120	300	300
C	140	350	350
D	160	400	400

Profile B ( $T = 120^{\circ}\text{C}$ ,  $F = 300 \text{ mN}$ ,  $P_{\text{US}} = 300 \text{ mW}$ ,  $t = 50 \text{ ms}$ ) satisfies (2)–(5), yielding  $\eta > 0.98$  and  $D_m = 75 \mu\text{m}$  for the  $25 \mu\text{m}$  wire.

### C. Flip-Chip Assembly

The RF die ( $2 \text{ mm} \times 2 \text{ mm}$ ) is flipped and aligned on a Dr.Tresky T-5300 tool. Co-planarity is verified with an optical profilometer; maximum allowable height deviation is  $3 \mu\text{m}$ .

### D. Electromagnetic Simulation

Lumped RLGC parameters of the CPW are extracted [6] from a model in QUCS and reduced to a two-port network:

$$\mathbf{Z}(s) = \sqrt{\frac{L}{C}} \sinh(\sqrt{LC} s) + R \sinh^{-1}(\sqrt{LC} s) \quad (6)$$

The simulated S-parameters serve as reference for measurement correlation.

### E. Electrical Measurement Procedures

DC continuity is measured with a ohmmeter. RF characterisation employs a vector network analyser from 10MHz to 10GHz. Pad-open-short (OS) calibration is implemented [5] on the CPW coupons; the device impedance is obtained with:

$$Z_{\text{device}} = Z_{\text{meas}} - Z_{\text{short}} \quad (7)$$

Line impedance and trace resistivity are calculated via

$$Z_{\text{line}} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} - Z_0 \quad (8)$$

$$\rho_{\text{trace}} = \frac{Z_{\text{line}} T_{\text{trace}} W_{\text{trace}}}{l_{\text{trace}}} \quad (9)$$

### F. Yield-Analysis Protocol

Yield is defined as the ratio of electrically continuous bumps to the total number on an interposer. The yield coupons of Fig. 3 are bonded using each profile of Table II, and continuity is verified by probing. A bump is considered defective if its resistance exceeds  $1.5\Omega$ . The yield data are later correlated with the bonded-area fraction  $\eta$  predicted by (4) and analysed versus bonding energy  $E$ .

## III. RESULTS

### A. Coplanar-Waveguide Parasitic Extraction

Fig. 4 shows the lumped RLGC circuit implemented in QUCS for a 1mm Ti/Au CPW segment. The extracted per-millimetre parameters are summarised in Table III. Substituting these values into the transmission-line impedance function

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (10)$$

predicts  $Z_0 = 50.3\Omega$  at 5 GHz, validating the line geometry.

TABLE III  
EXTRACTED RLGC PARAMETERS FOR 1 MM CPW  
( $W = 80\mu\text{m}$ ,  $S = 25\mu\text{m}$ )

Parameter	Symbol	Value
Series resistance	$R$	$3.12\Omega$
Series inductance	$L$	$0.352\text{ nH}$
Shunt capacitance (substrate)	$C_1$	$8.92\text{ fF}$
Shunt capacitance (signal-ground)	$C_3$	$0.138\text{ pF}$
Substrate leakage resistance	$R_2$	$1\text{ T}\Omega$

The simulated  $|S_{21}|$  and  $|S_{11}|$  responses (dashed lines in Fig. 5) show an insertion loss of 0.40 dB and return loss better than 25 dB at 5 GHz.

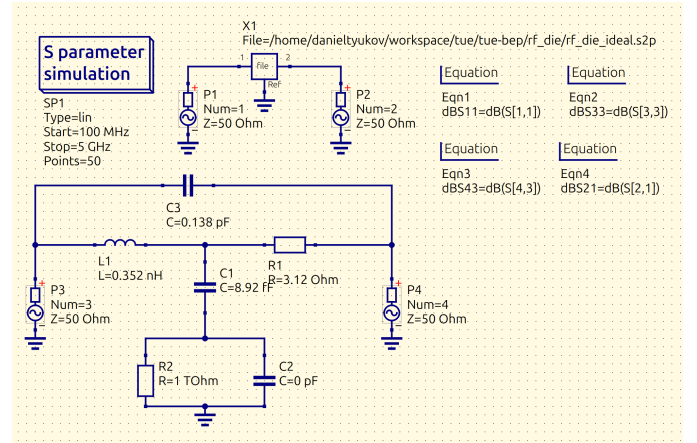


Fig. 4. QUCS schematic of the lumped RLGC model used for CPW parasitic simulation.

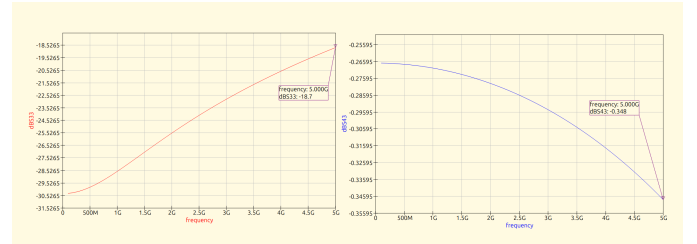


Fig. 5. S-parameters of the 1 mm CPW from 10 MHz to 5 GHz.

## IV. DISCUSSION

### A. Current Status

The present work has delivered a complete single-layer glass interposer design, an accompanying lumped-element CPW model, and a physics-guided thermosonic bonding window derived from the literature. All performance figures reported so far are the outcome of process simulations; no fabricated hardware has yet been characterised. Consequently, every quantitative metric—RLGC values, predicted insertion/return loss, mashed bump diameter and projected yield—should be treated as pre-fabrication targets rather than verified results.

### B. Planned Fabrication and Test Campaign

The next project phase will turn the simulated design into physical prototypes and confront the models with measurement data:

- 1) **Interposer fabrication:** Three wafers will be processed with the 50 nm Ti/100 nm Au stack. Two wafers will use evaporation and one sputtering to confirm the simulated conductivity spread.
- 2) **TPT profile yield study:** Each wafer will be diced into coupons; the four bonding profiles of Table II will be applied to identical bump arrays. Electrical continuity and shear testing will generate empirical data to validate the  $\eta(F, E)$  model of (4).
- 3) **RF characterisation:** Open, short and through CPW structures will be probed up to GHz range us-

ing pad-open-short de-embedding. Agreement (or lack thereof) with the QUCS S-parameter predictions will isolate conductor-loss and dielectric-loss discrepancies.

### C. Path Toward an Amplifier Interposer

Once the baseline RF-die interposer is experimentally verified, the same design rules will be extended to a common-source amplifier demonstrator:

- A GaN HEMT die will be flip-chipped using the optimal bonding profile extracted from the yield study.
- The interposer will integrate matching and bias networks calculated and verified in QUCS.

### D. Anticipated Challenges

- **Conductor loss:** The simulated 0.4 dB/mm insertion loss assumes ideal 100 nm Au; grain growth, surface roughness and voids may increase resistance after deposition.
- **Pad pitch:** The 75  $\mu\text{m}$  mashed bump leaves limited clearance on a 90  $\mu\text{m}$  pad diameter [10].

## V. CONCLUSION

A complete flip-chip integration flow for RF dies on single-layer glass interposers has been developed and made in simulation. The Ti/Au coplanar-waveguide layout achieves a simulated  $50.3\ \Omega$  characteristic impedance with an insertion-loss target of 0.40 dB per millimetre at 5 GHz. A physics-based optimisation of thermosonic bonding parameters predicts 78  $\mu\text{m}$  gold bumps with  $\eta > 98\%$  coverage on a 180  $\mu\text{m}$  pad pitch, establishing an energy window for high-yield assembly.

The forthcoming fabrication run will provide the first hardware validation of these models. Three wafers—processed by evaporation and sputtering—will quantify conductor loss, bump yield and die-to-interposer planarity, while a four-profile bonding matrix will map yield versus ultrasonic energy. The resulting data will refine the RLGC and bonding-yield models and confirm whether the simulated 0.4 dB/mm loss and 99 % bump continuity are attainable in practice.

Once validated, the design rules will be ported to a common-source GaN HEMT amplifier interposer, demonstrating that the RF-die methodology scales to active circuits.

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