Process Development and Characterization of Flip-Chip Technology

W.M. Beelaerts van Emmichoven, 1459635

***Abstract*— Flip-Chip Technology offers a very large number of connections and reduced propagation time for signals compared to Wire Bonding. In order to produce Flip-Chip Technology at the TU/e, a process was created. This process consist of 4 stages: interposer design and production, bump placement, die placement and measurements. It was discovered that gold evaporation is the best production method for the interposer due to consistent bump placement and having the least resistivity. Moreover, it was discovered that 25μm gold wire made bump placement more reliable, but requires a pitch size larger than 90μm. In the die placement stage, a heat profile was found that resulted in confirmed metal connections.**
[1]

***Index Terms*—Flip-Chip, Process, Interposer, Die, Gold bumps, Testing, Electrical characterization**

I. Introduction

The concept of Flip-Chip Technology, first introduced by IBM in the 1960s, involves placing the die face down on a carrier material (substrate or interposer) using metal bumps instead of traditional bonding wires [2]. This technique allows for more connections per surface area and shorter connections which reduces resistance, inductance and capacitance, improving signal propagation time and thus chip performance [3], [7]–[9].

In order to make these connections reliable, 4 options for connecting the interposer and the die with metal bumps can be considered. These options are Thermal Compression bonding, Eutectic bonding, Ultrasonic bonding and Solder Bump bonding. Starting with Thermal Compression bonding, heat and force are applied to connect the bumps. Next is Eutectic bonding, which uses an intermediate solder alloy to form a continuous bond between two surfaces and is used often in die packaging for systems that are sensitive to outgassing of standard die attach materials [6]. Ultrasonic bonding uses high-frequency vibrations to bind the surfaces, which is suitable for temperature-sensitive dies because of the friction generated heat used for bonding is local. Finally, Solder Bump bonding re-flows solder balls to connect the die.

These benefits, choosing a suitable bonding technique and the research into the characteristics of the metal bumps and the interposer tracks play a vital role in the integration of, for example, On-Chip Arrays such as LED arrays [1]. That is because the type of connection between two or more dies significantly impacts the practical use due to connection specific limitations. In the field of On-Chip Arrays, the amount of connections that must be made reliably can reach a few thousand connections. Since Flip-Chip Technology offers an increased number of connections, the limitations and requirements of Flip-Chip Technology, along with how any substrate or interposer would affect the signals sent between dies, is of great interest. Due to this interest, the Integrated Circuits (IC) research group of the TU/e would benefit significantly from having a specified process for Flip-Chip Technology.

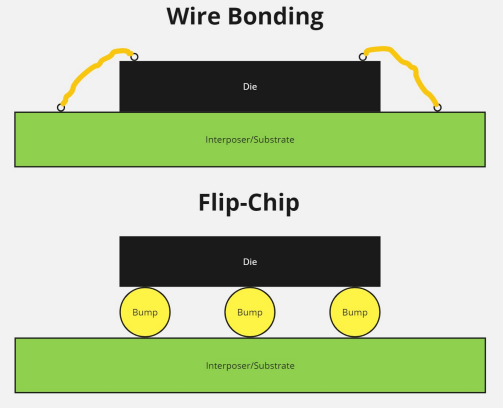

Fig. 1. Wire Bonding (top) and Flip-Chip Technology (bottom) visualized.

This paper describes the creation and developments made to obtain such a process, which can be used to speed up future research requiring Flip-Chip Technology. In section II the essentials and setup of the process are described. Section III describes the steps of the process, any obstacles that were faced and results that are obtained in each stage of the process. Finally, in section IV several conclusions are drawn about the process and recommendations are given for any steps that still need to be investigated to obtain a complete process.

II. Process setup

The essential components in Flip-Chip Technology are the bumps and interposer, for both of which the material of choice is gold due to its high conductivity. The process utilizes university resources, with the interposers produced in the clean-room on campus and the remainder of the process carried out in the Electronics lab at Flux 8.070, which houses the necessary machines.

Three setups are used in the Electronics lab for producing bumps, placing the die, and testing the interposer and bumps. Gold bumps are made with the TPT 16 Wire Bonder using two gold wire diameters: 25μm and 17μm. The bump diameter is approximately three times the wire diameter, with smaller wire sizes used for higher bump density [8].

[1]This paper is written as part of a Bachelor End Project in the department of Electrical Engineering of the TU/e, in the period of 02-09-2024 → 17-01-2025 and was supervised by G. Radulov.

The Wire Bonder has several parameters to optimize, varying by mode. Of the four modes available, only Ball Bump and Ball Wedge are of interest.

- Ball Bump Mode: Creates a bump with a tail that can potentially cause shorts during die placement. A coining tool can flatten the tails to reduce the risk of a short circuit being formed.
- Ball Wedge Mode: Cuts off the tail, leaving a well-rounded top, which is preferred to reduce short circuit risk.

In both modes, parameters like ultrasound (US) power, time, force, and stage heater temperature need optimization. For Ball Wedge mode, these parameters are split between Bond 1 and 2. A necessary addition to the Wire Bonder is a camera for inspection and capturing images.

After making the bumps, the die is placed using the Tresky T-5300, which offers high precision alignment with its beam-splitter, allowing to simultaneously view the die and interposer. The machine uses a nozzle to create a vacuum in pick-mode, lifting the die. The substrate heater also has a vacuum to hold the interposer in place. Once aligned, the pick-and-place mover can be lowered to make contact with the bumps. Upon reaching the set force it locks the mover for the duration set and then blowing off the die. The substrate and/or nozzle heater is heated using a specific heat profile and optimizing the heating profile, placement time, and placement force is essential for reliable connections.

Finally, the setup for testing the characteristics of the interposer and bumps uses a Keysight PNA-X N5247B Vector Network Analyser (VNA) with a frequency range of 10 MHz to 110 GHz. For this project, only up to 10 GHz is investigated. The VNA connects to extenders with coaxial cables leading to 125μm pitch GSG probes. Calibration is done using the ISS-101-190 substrate for OSLT (open-short-load-through) calibration, moving the reference plane from the VNA to the probes. Measurements are taken on an open and a shorted test structure on the interposer. These obtained S-parameters are used to extract the S-parameters of the bumps using the OS (open-short) de-embedding method once a die is successfully placed. The chosen die has a known 100Ω resistance for accurate measurements. Figures 2 and 3 show the Wire Bonder, Tresky T-5300, and VNA setup.

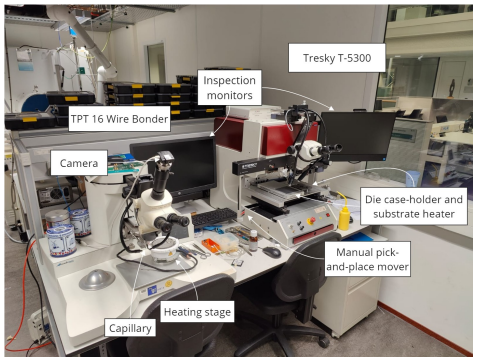

Fig. 2. Lab setup for the TPT 16 Wire Bonder and Tresky T-5300 used to place the bumps and the dies.

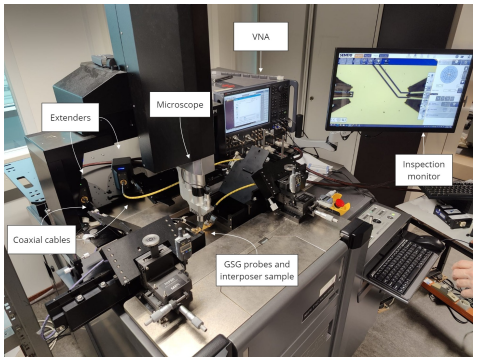

Fig. 3. Lab setup of the VNA used for characterization of the bumps and interposer.

III. Process Developments

A. Interposer design and production

Fig. 4 and 5 show the flowchart of the Flip-Chip process in which each colour represents a different stage of the process. The first stage is the design and production of the interposer. The interposers serve as a redistribution layer for the connections of the die and are designed such that the DC and AC characteristics of the interposer and bumps can be obtained, but also the trade-off between bump density, yield and reliability can be investigated. This results in the 3 designs shown in Fig. 7, 8 and 9. The designs are made in Altium with a 90μm pitch. Design 1 and 3 serve the same purpose, but design 1 has a different pad-ring lay-out due to the first design being made for a different die than design 2 and 3 are. The purpose of design 1 and 3 is to investigate the trade-off between the bump density, yield and reliability. The pitch size in the pad-ring of design 1 has a pad size of 70μm and 20μm spacing. For design 2 and 3 this is 60μm and 30μm respectively. Moreover, all designs have a trace width that matches the pad size. The purpose of design 2 is to investigate the interposer and bump characteristics. This design has 4 test structures, 2 line structures and 2 die structures. In both structure types, the top structures are shorted to ground and the bottom structures are open circuit. The open line test structure is used to obtain the an equivalent RLC model of the transmission line. Furthermore, the top die structure is used to obtain the S-parameters of the short circuited transmission lines and the bottom die structure to obtain the open circuit transmission line S-parameters. These measurements are to be used in the de-embedding method described in Section II to obtain the characteristics of the bumps. Ideally, the impedance of the transmission lines matches characteristic impedance, which is 50Ω. The program Qucs is used to find the dimensions of the trace such that the impedance is close to matching the characteristic impedance. This resulted in a spacing 20μm for the Coplanar Waveguide (CPWG) in design 2, as can be seen from the results of the line-calculator in Fig. 6. It does not match perfectly, but since the de-embedding method mathematically removes the impedance of the transmission lines from the measurements of the complete structure this is no problem.

With the designs finished, samples are made in the clean-

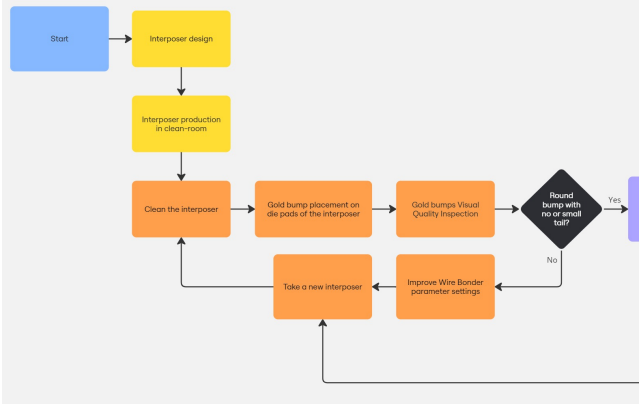

Fig. 4. First half of the flowchart of the Flip-Chip process showing the sequence of steps to follow for obtaining a desired result.

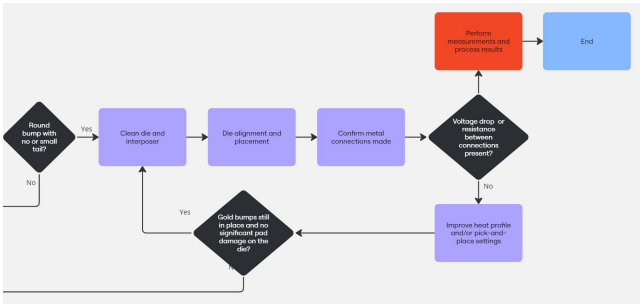

Fig. 5. Second half of the flowchart of the Flip-Chip process showing the sequence of steps to follow for obtaining a desired result.

room, which was done in 3 batches. In the first batch Cr(15nm)/Au(100 nm) electrodes were patterned on cleaned glass substrates by photolithography and the subsequent lift-off process of the negative photoresist (AZ nLOF 2035). This batch contained 2 samples of each design and the gold was placed by method of gold sputtering. Unfortunately, the samples had some minor imperfections in the form of small random black spots. Moreover, the gold layer thickness of the first and second sample where 111 and 104 nm respectively. The second batch was made of Ti(50nm)/Au(100 nm) and contains 4 samples of each design. 2 of these are made by method of gold sputtering and the other 2 are made with gold evaporation. These sputtering samples contained only a few smaller black spots as production conditions where improved. Finally, the third batch is made with the same materials as batch 2 and contains 2 gold evaporation samples, which served as back-up samples. Fig. 10 shows the production of the samples before the photolithography stage and Fig. 11 shows the finished product.

B. Bump placement

The second stage in the process is the bump placement, shown in orange in Fig. 4. After many attempts of finding only inconsistent results with long tails, it was decided to discuss the consistency with Accelonix, the company that makes both the Wire bonder and Tresky T-5300. Eventually, a base setting for the parameters was found. The bumps produced on their

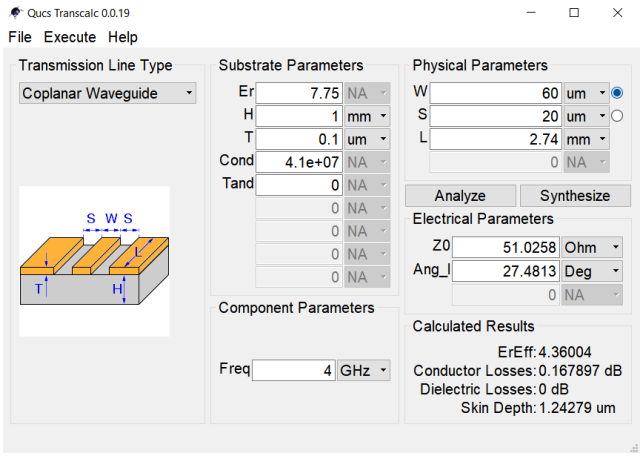

Fig. 6. Result for the spacing of the CPWG calculated in the line-calculator in Qucs.

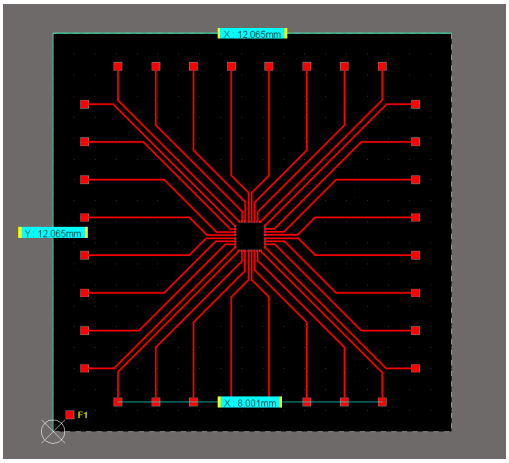

Fig. 7. First interposer design for specific signal amplifier die including scale reference.

standard substrate yielded good visual results in terms of well-rounded bumps with no tail. These recommended base settings and visual proof are shown in Fig. 12.

Working with these settings for 25μm wire on design 1 of the first and second batch yielded good, but inconsistent results as the bumps often would not stick to the surface. However, when the same settings where applied to design 1 of the gold evaporation sample of batch 2, it yielded consistent and good results as can be seen in Fig. 13. Unfortunately, when placing the bump centre too far off the centre of the pad and too close to the edge, the pad/trace broke off. The Wire Bonder has no automatic way to ensure good alignment, making proper alignment highly susceptible to the skill of its operator. Although it was not possible to automate this, a workaround was found to improve alignment and make it less dependent on the operator's skill. When viewing the bumps through the camera of the setup in the Thorlabs application, a test area was used to place a bump. By moving the cursor of the computer to the centre of the placed bump it is easier for the operator to place a bump more precisely and thus increasing the yield.

In terms of density, the wire diameter and EFO power

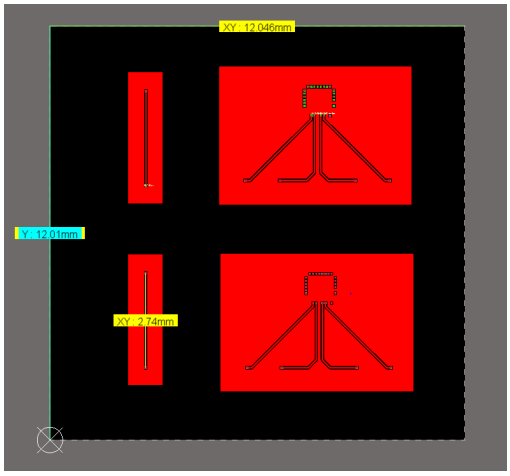

Fig. 8. Second interposer design for generic die including scale reference.

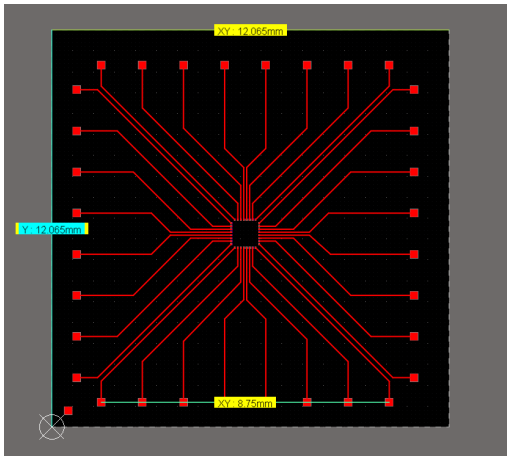

Fig. 9. Third interposer design for generic die including scale reference.

determine the bump size and thus density. Bumps made with 25μm wire (Fig. 13) had good yield and reliability, but faced density issues. When placing bumps on adjacent pads, the capillary might land on a neighbouring bump, coining it, or place the bump too far to the side, ripping off the pad. To address this, a 17μm gold wire was used, reducing bump size and thus preventing interference with neighbouring bumps by creating more space in between the bumps. This change enabled bumps to be properly placed on a 90μm pitch size with a good quality of bumps. However, the capillary clogged more frequently and could only be unclogged by placing it upside-down and using USG to vibrate out the material through the large hole of the capillary, through which the wire is meant to be inserted. Several parameter adjustments, including reducing EFO and US power, were attempted but were unsuccessful in resolving the issue.

Although the bump quality is inspected visually, the size of the bump is very important in determining what the highest density could be. By writing a script in Matlab that applies circle detection to distinguish the bumps from the interposer and its traces, it not only automatically detects the bumps but also finds the diameter of the bumps in number of pixels.

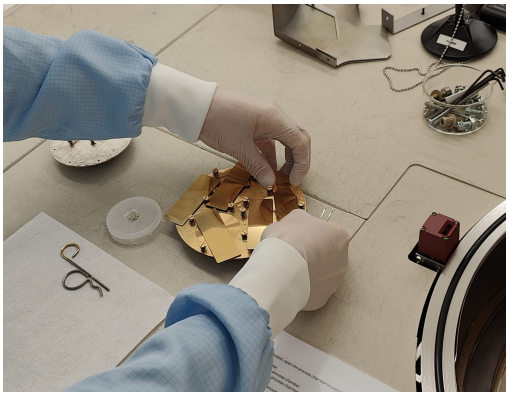

Fig. 10. Production of the interposer in the clean-room at intermediate stage.

Fig. 11. Finished interposers ready for bump placement and testing.

All that remains is to determine the conversion rate. This is done by taking a picture of a known length object and measuring the amount of pixels that spans the length of the object. This object was a 2x2 mm die and was measured in the Thorlabs application to be 1166 pixels in length. In (1) CR is the conversion rate in μm per pixel, W is the known width of the reference object and N_{px} is the number of pixels that span the known width. This resulted in a conversion rate of 1.715μm/px. Using this conversion rate, it was determined that for the 25μm gold wire, the bumps were in the range of 67-78μm diameter, which was expected as it is around 3 times the wire diameter [8].

Assuming that a bump is placed perfectly in the centre of a 70μm pad, it has a 4μm overshoot to either side in the worst case scenario, leaving only 12μm spacing between the bumps assuming the adjacent bump is placed with the same conditions. In a practical sense, it was determined not to be enough space. As the 25μm wire yielded the best results, working with this wire size requires a larger pitch size. Increasing the spacing from 20 to 30μm or pad size from 70 to 80μm and thus increasing the pitch to 100μm would allow for a larger space to operate in and thus increase the yield. Depending on the requirements, it should be decided to either increase the spacing or pad size or even consider moving to 110μm pitch size to further increase the yield as this would increase the reliability of the process.

$$CR = \frac{W}{N_{px}} = \frac{2000}{1166} \approx 1.715 \mu m/px \quad (1)$$

After determining the need for a larger pitch size, the bumps were placed on design 2 of an evaporation sample of batch 2. Unfortunately the bumps where no longer well-rounded and instead had a cone-like shape. Although a significant amount

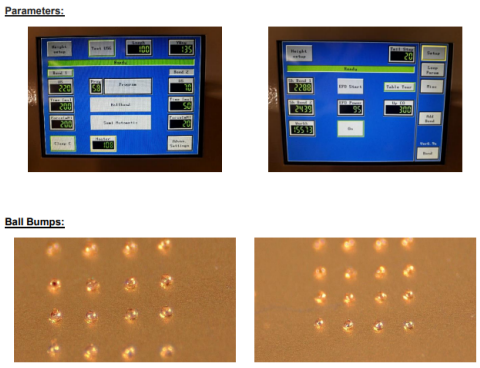

Fig. 12. Base settings and visual proof of high quality bumps on standard substrate of Accelonix.

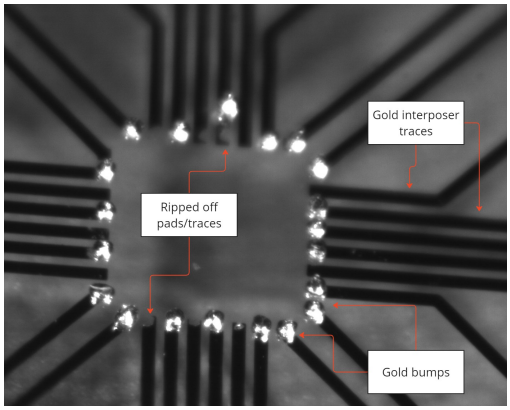

Fig. 13. Bump placement on gold evaporation sample of batch 2, yielding good bump quality but also containing ripped off traces.

of time was spent to find the right parameter settings for large gold surface area bump placement, the time constraints of the project were too narrow to obtain them.

C. Die placement

The third stage of the process is die placement. As discussed in the previous subsection, the 17μm wire had practical problems, but nonetheless it was possible to place bumps on all of the pads of design 1 of an evaporation sample. Thanks to the beam-splitter, it was possible to achieve near-perfect alignment of the die with the interposer. However, the main challenge in the die placement was figuring out a suitable heat profile. Based on the research in [4] and [5], multiple heat profiles were tested, which eventually lead to a semi-successful heat profile. Fig. 14 shows the heat profile that managed to connect the die to the bumps. Taking a standard multimeter, a forward voltage drop of 107 mV was measured between IO and GND pins, measured by placing the handheld probes on the large pads. When measuring between two of the IO pins, a resistance of 69Ω was measured. These measurements confirm that a metal connection was made without any shorts.

Unfortunately, the next day the die had broken off, potentially indicating that even though the connection was good, the quality could be improved. It is, however, worth noting that the die placed was 2x2 mm and contained 3 different pad-rings

	Semi-successful attempt heat profile settings			**Heating profile settings recommended by Accelonix**	
	Stage 1	Stage 2	Stage 3	Stage 1	Stage 2
Segment type	Heat	Heat	Cooling	Heat	Cool
Start trigger	-	Wait for Touchdown	-	Wait for Touchdown	-
Start delay [ms]	0	0	0	0	0
Duration [ms]	40000	30000	40000	60000	0
Ramp/Slope [C/s]	10	10	-	30	-
Target temperature [C]	220	270	40	300	40
Wait for completion	Not selected	Not selected	Not selected	Not selected	Selected
Wait target	-	-	-	-	-
Logic	-	-	-	-	SKIP_EXEC
	Placement settings			**Placement settings**	
Place force [g]	600			500	
Place duration [ms]	40000			30000	

Fig. 14. The heat profile settings of a semi-successful die placement attempt and later discussed but untested recommendations from Accelonix.

$R_{sh}[\Omega/square]$	$\rho_{trace}[S/m]$	$R_{line}[\Omega]$	$L_{line}[nH]$	$C_{line}[pF]$
0.3797	$3.9858 \cdot 10^{-8}$	18.2017	1.6193	0.0346
0.3491	$3.6363 \cdot 10^{-8}$	16.6058	2.2481	0.0428
0.4796	$5.0230 \cdot 10^{-8}$	22.9383	2.4980	0.0507
0.4812	$5.0071 \cdot 10^{-8}$	22.8657	2.0889	0.0528

TABLE I
RESULTS TABLE FOR INTERPOSER CHARACTERISTICS, TOP 2 ROWS ARE FOR THE EVAPORATION SAMPLES AND THE BOTTOM 2 FOR THE GOLD EVAPORATION SAMPLES.

of which only 1 was used that matched the pad-ring on the interposer, because it was designed for that one. Consequently, only about 1/4 of the surface area of the die had connection with the bumps, leaving the other 3/4 of the surface area as overhang. The stress this causes on the bumps is likely to be the main reason for the die breaking off. Because of the failure, the heating profile was discussed with Accelonix to work out a suitable profile. Accelonix made a recommendation that was not able to be tested, because the Tresky T-5300 entered error mode when a temperature target above 270°C was set. The recommended settings are also shown in Fig. 14. Unfortunately, the machine error could not be resolved within the time constraints of the project.

D. Measured results

The final stage of the process involves performing measurements and analysing the results. The primary focus after production is to evaluate the characteristics of the interposer and determine the RLC values of the transmission lines. More specifically, the values of interest are the sheet resistance (R_{sh}), resistivity (ρ_{trace}), line resistance (R_{line}), line inductance (L_{line}), and line capacitance (C_{line}) of the interposers. Additionally, the differences between the two production methods will be assessed. After calibration of the VNA, the S-parameters are measured at 4 distances, which are 25, 100, 500 and 2740μm respectively, the latter being the full length of the transmission line in design 2. This procedure is performed a total of four times: twice for different gold sputtering samples and twice for different gold evaporation samples. The gold sputtering samples include one from batch 1 and another from batch 2, while the gold evaporation samples are from batch 2 and batch 3, respectively. The obtained S-parameters are then processed in Matlab. As the first measurement is at 10 MHz, (2) shows that this frequency is low enough to consider the results to be DC, because λ_{trace} is much larger than the length of the traces. In (2) λ_{trace} is the wavelength of the electrical signal in the trace, λ_{vacuum} the wavelength of a something

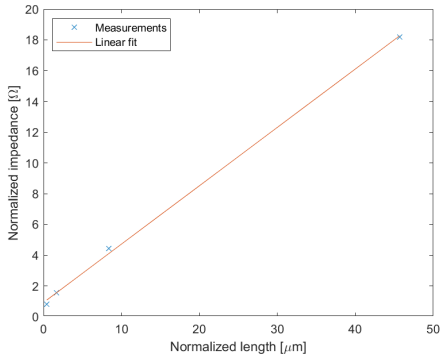

Fig. 15. Plot of the measured resistances normalized to the trace width against the normalized length of the measurement

propagating in a vacuum, $\epsilon_{r,gold}$ the relative permittivity of gold, c the speed of light and f the frequency of the signal.

By applying (3) to the first entry of each measurement (where Z_0 is the characteristic impedance of 50Ω and $S_{1,1}$ is a specific entry in the measured S-parameters at 10 MHz), the line impedance is determined. A linear fit of the real part of the line impedance (the line resistance) is performed to estimate the contact resistance and sheet resistance (R_{sh}) with minimal error. Fig. 15 shows the plot of measured line resistances and its linear fit for normalized length, demonstrating that the linear fit accurately represents R_{sh}. The trace resistivity (ρ_{trace}) is calculated using (4), with Z_{line} as the line impedance, T_{trace} as the gold layer thickness, W_{trace} as the trace width, and l_{trace} as the line length. Furthermore, R_{line} is found from the real part of Z_{line}, L_{line} is determined using (5) at 10 MHz (the lowest VNA measurement frequency), and C_{line} is determined using (6) at 10 GHz (the highest VNA measurement frequency) and its corresponding S-parameter. At DC frequencies, inductance dominates the imaginary part of the RLC model, while at high frequencies, capacitance is dominant. The values of R_{sh}, ρ_{trace}, R_{line}, L_{line}, and C_{line} are shown in Table I.

$$\lambda_{trace} = \frac{\lambda_{vacuum}}{\sqrt{\epsilon_{r,gold}}} = \frac{c}{f\sqrt{\epsilon_{r,gold}}} = \frac{3 \cdot 10^8}{10^4\sqrt{6.9}} = 11.42 \cdot 10^3 [m] \tag{2}$$

$$Z_{line} = Z_0 \frac{1 + S_{1,1}}{1 - S_{1,1}} - Z_0 \tag{3}$$

$$\rho_{trace} = \frac{Z_{line} \cdot T_{trace} \cdot W_{trace}}{l_{trace}} \tag{4}$$

$$L_{line} = \frac{im\{Z_{line}\}}{2\pi f_l} \tag{5}$$

$$C_{line} = \frac{im\{1/Z_{line}\}}{2\pi f_h} \tag{6}$$

The resistivity of pure gold (ρ_g) is $2.041 \cdot 10^{-8}$ S/m. Evaporator samples have resistivity factors of 1.953 and 1.782, while gold sputtering samples have significantly higher factors of 2.461 and 2.454. Higher resistivity yields higher resistance, indicating that gold evaporation is better for both resistivity and bump placement. The difference in resistivity is due to production methods as sputtering produces less densely packed gold with more impurities, while evaporation packs gold more densely.

IV. Conclusion

Despite not completing the process due to time constraints, a sequence of steps has been established for the Flip-Chip process. The evaporation production method of the interposer is preferred over sputtering because of its consistent bump placement and reduced resistivity. During bump placement, the obtained base parameter settings yielded high-quality bumps on small gold surface areas but poor quality on larger areas. The 25μm gold wire was more reliable than the 17μm wire, which had clogging issues. A pitch size of 90μm was impractical for the 25μm gold wire and increasing it to 100μm or even 110μm would greatly improve yield. Moreover, a semi-successful heat profile was found for die placement, requiring further improvement for greater consistency and reliability.

Setting up the process required a significant amount of time, leaving some issues unfinished within the time frame set for the project. The issues that still require investigation in future research are:

- Optimizing parameter settings for consistent, well-rounded bumps on large gold surface areas.
- Improving the heat profile and die placement settings.
- Investigating the AC characteristics of design 2.
- Exploring the DC and AC characteristics of the bumps.

The improvements and issues of the production steps are recommended to be worked out in collaboration with Accelonix.

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