5XCC0 Biopotential and Neural Interface Circuits

Low-Power System Design

Pieter Harpe

Outline

- System design methodology: V model
- Risk management
- Optimization for low power at different levels
- System-level optimization and trade-offs
- Analog, mixed-signal, and digital circuits
  - Signal definitions, optimization strategies
- Summary

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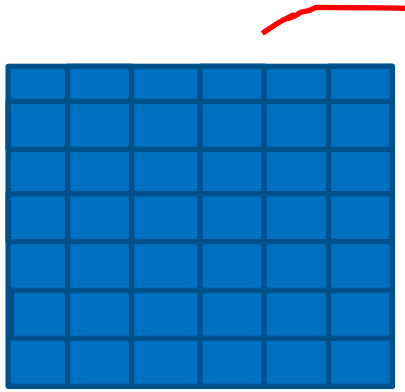
From Application to Circuit Implementation

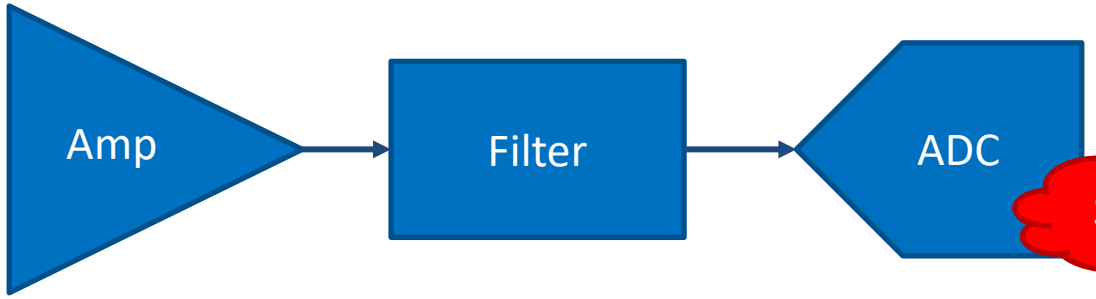
- Conventional: analog outputs → Many cables



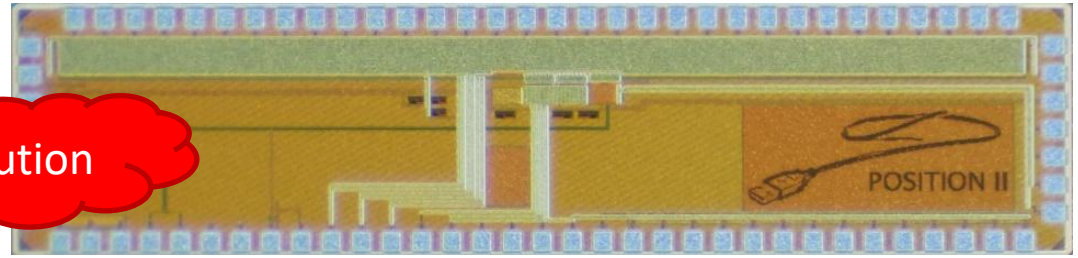
Ultrasound transducer array

Application wish

- Future: digitization at the tip → Few cables

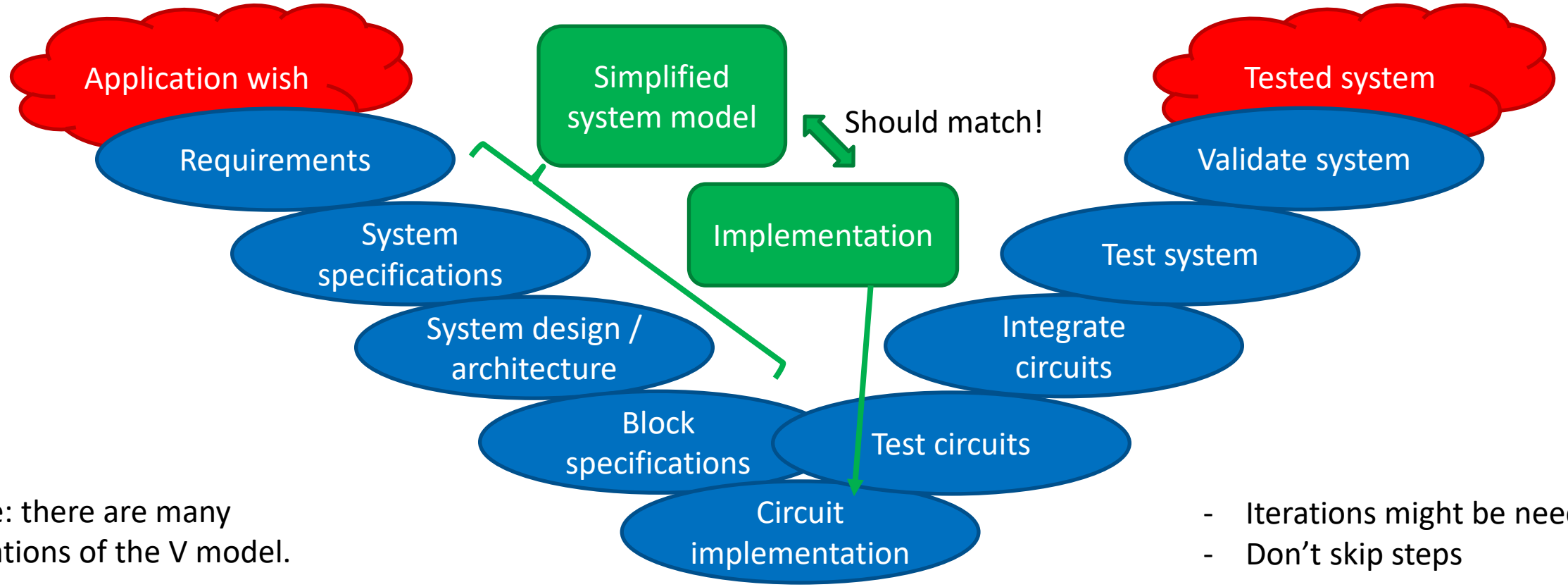


In-probe digitizers for ultrasound catheters (ICE)



V Model

- Systematic design methodology to go from an application wish <u>down</u> to a circuit implementation, and <u>up</u> to a tested system



Note: there are many variations of the V model.

- Iterations might be needed
- Don't skip steps

Requirements vs Specifications

- Requirements: user or application point of view. What should the product be able to do?
  - Task, features, performance, constraints, …
- Specifications: designer point of view. How will the design meet the requirements?
  - Architecture
  - Component/circuit parameters

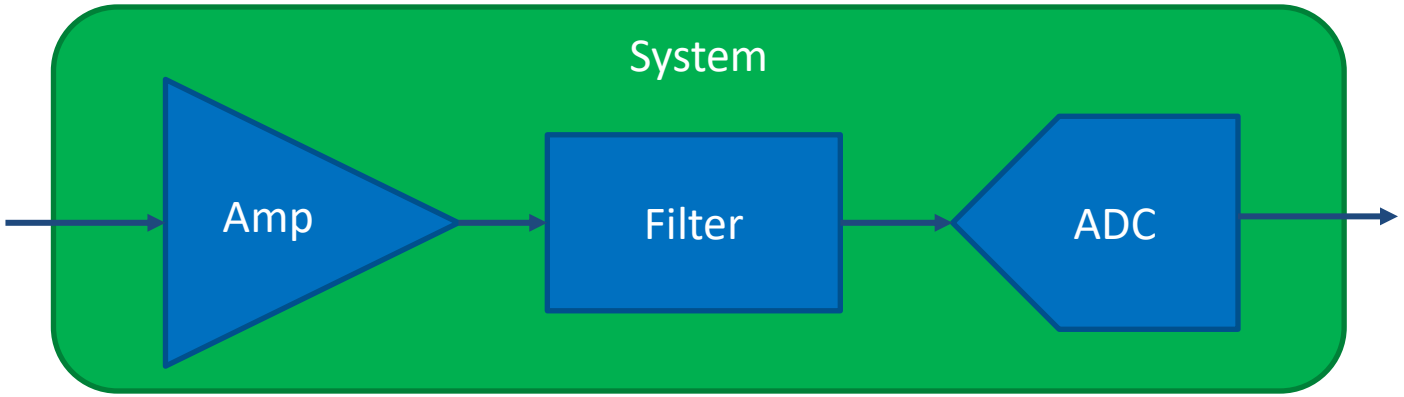
Example: smart watch

Requirements:
- It should display time and date
- It should count # daily steps
- It should have a GPS to track location
- It should be small enough to wear

Specifications:
- The display is 2cm x 2cm, has 150 x 150 pixels, and is B & W
- It has a counter with a range from 0 to $1 \cdot 10^6$ steps
- The overall size is xxx and weight xxx

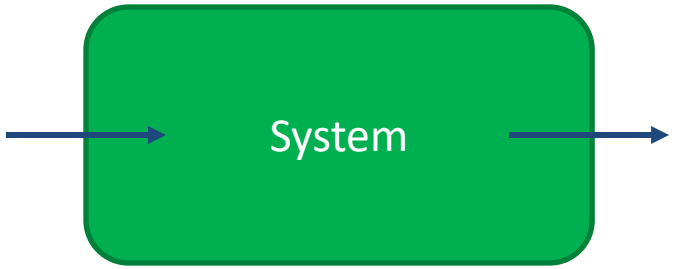
System vs Block Specifications

- Overall system is composed of building blocks
  - System specifications: treat entire system as a black box; specify overall performance (e.g. power consumption <1mW)
  - Block specifications: specify performance for each individual block (e.g. the amp should consume <0.5mW, filter <0.2mW, ADC <0.3mW)
  - System model helps to make this *translation* from system to block level
    - Trade-offs!



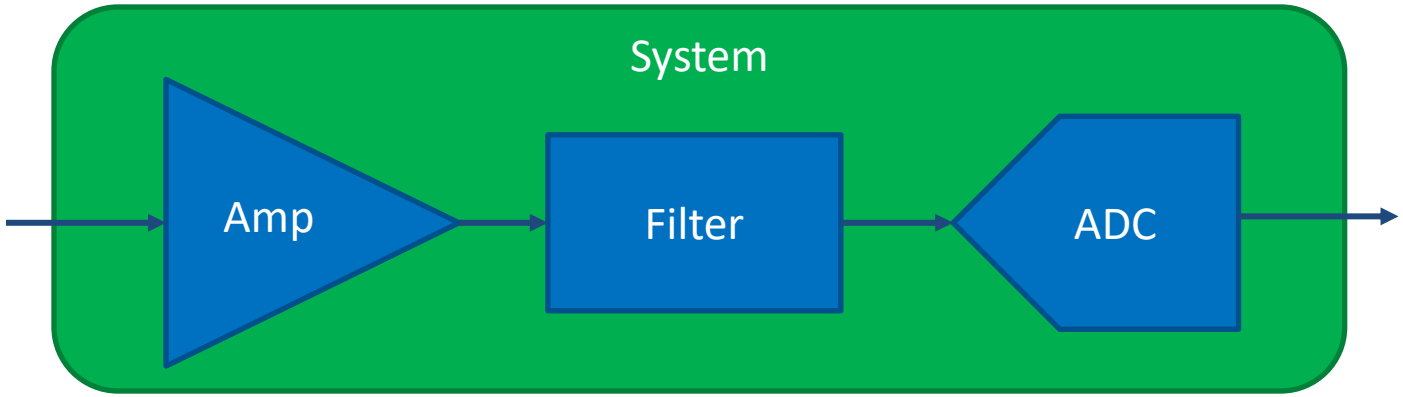
System Model (#1)

- Black box system model
  - Matlab/Simulink/Excel sheet/Circuit with ideal blocks
- Functionality of the system (input vs output)
- Define system-level specifications (fit to requirements)
- Verification (testing):
  - Compare simulation vs requirements
  - Compare calculation/estimation vs simulation
  - Check if system model makes sense



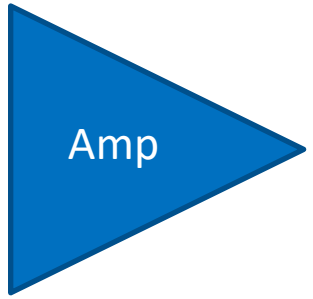
System Model (#2)

- Refine black box model towards block-level model
  - Architecture development
  - Blocks in the model preferably match to the circuit blocks
- Translate system-level specifications to block-level specifications
  - Trade-offs
- Outcome: architecture, block specifications
- Verification (testing):
  - See previous slide



Circuit Implementation (Individual Blocks)

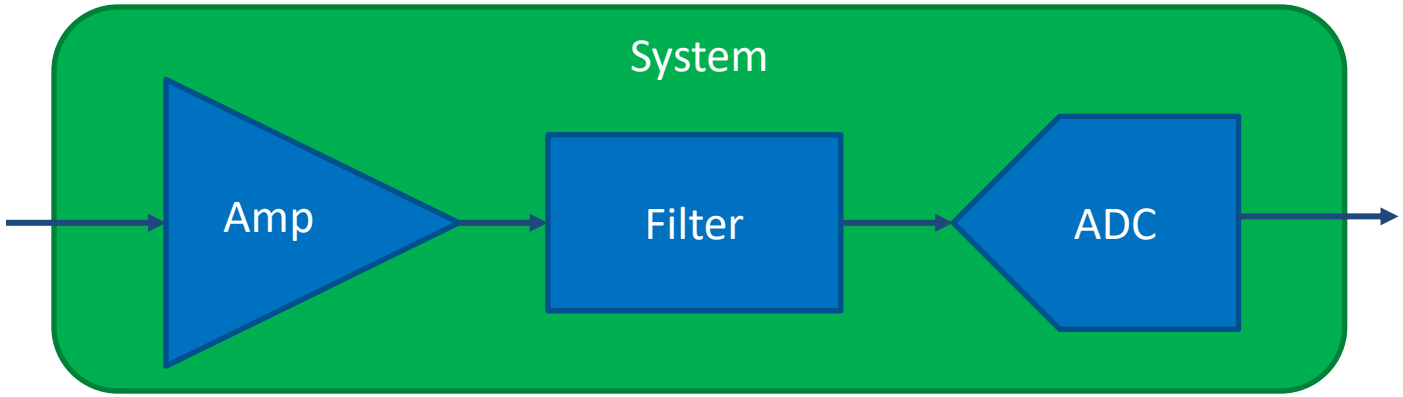
- Specifications known from system-level model #2
- Detailed (transistor-level) design
  - Decide exact topology, sizing of components
- Verification (testing):
  - Compare back-of-envelop calculation with simulations (circuit level)
  - Compare circuit simulations with system-model specifications



- Note:
  - If the circuit is large, it might be a ‘system’ in itself. E.g. an ADC

Circuit Integration (System)

- Put blocks together: full implementation of the entire system
- Verification (testing):
  - Check functionality
  - Check system-level specifications are met
  - Check requirements are met



Verification vs Validation

- Verification: evaluate whether the circuits, blocks, system meet the specifications and requirements.
- Validation: evaluate whether the overall solution meets the needs of the final user or the application. Can it be used for the intended goal in practice?

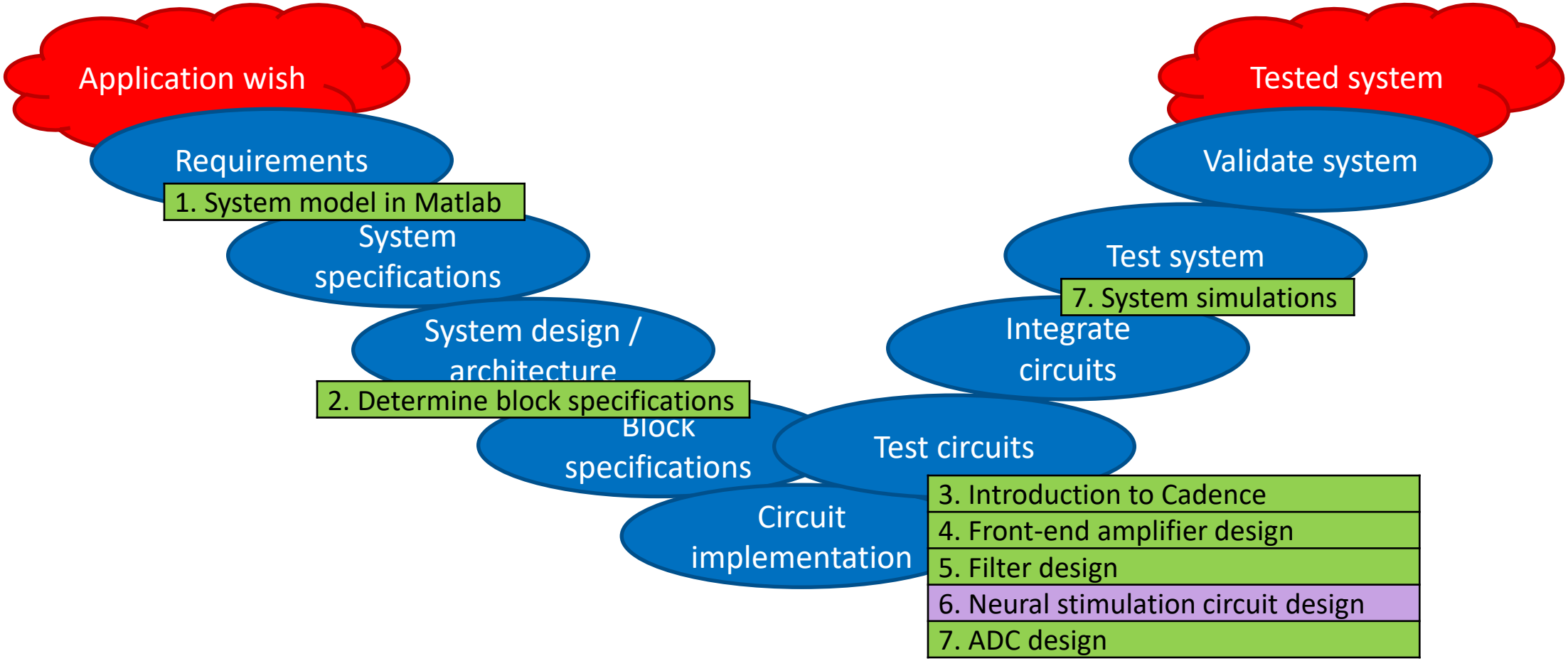
Example: smart watch

Verification (check reqs. & specs.):
- Is the display size correct?
- Can it display time and date?
- Can we count from 0 to $1 \cdot 10^6$ steps?
- Can it count steps & track location?
- Are overall size & weight OK?
- Is it small enough to be wearable?

Validation (use and evaluate):
- Issues: e.g. can not read display, battery is empty after 1hr, the software hangs at 5mln steps
- It may fail:
  - Missing requirement
  - Wrong req. → spec. translation
  - Design error

Design Assignment

- Design a neural recording interface for AP & LFP recording



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Risk Management

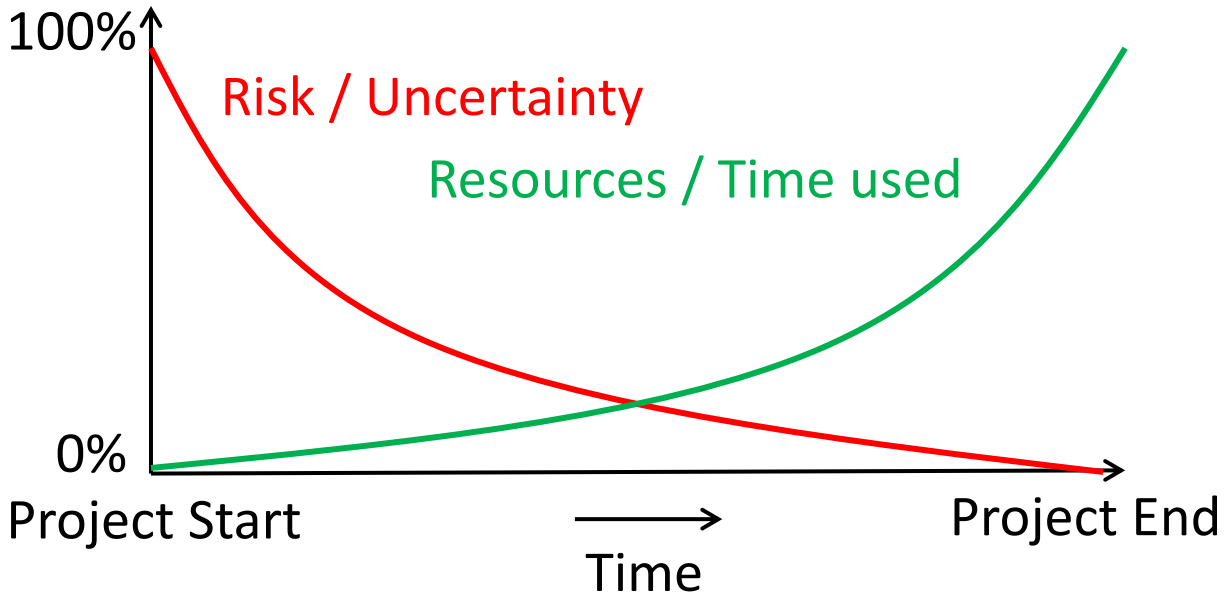
Technology

Power

A/D

Speed

Noise



- First aim: minimize the risk
  - Time $\propto$ 1 / Risk
  - Start with feasibility checks, literature study, back-of-envelope calculation, simple basic simulation → Simple and quick tasks aiming to reduce risk
  - Work top-down: first the big (rough) picture, then the details
  - Focus first on critical (uncertain!) blocks

Exercise 1: System Design

These questions relate to the design assignment of the AP/LFP neural recording interface.

Please note you have to make up some answers here, rather than extracting them from the actual assignment.

a) Can you mention 2 examples of requirements for this system?

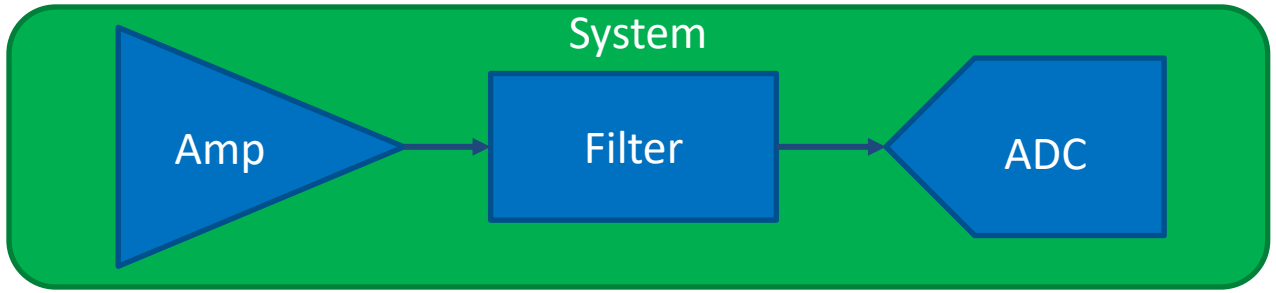
b) Can you mention 2 examples of system-level specifications for this system?

c) Can you mention 1 trade-off between the amplifier and the filter?

d) Can you mention 1 trade-off between the filter and the ADC?

e) Which risk(s) do you see when thinking of the system to be implemented?

f) What could you do to de-risk these risks at the start of the project?



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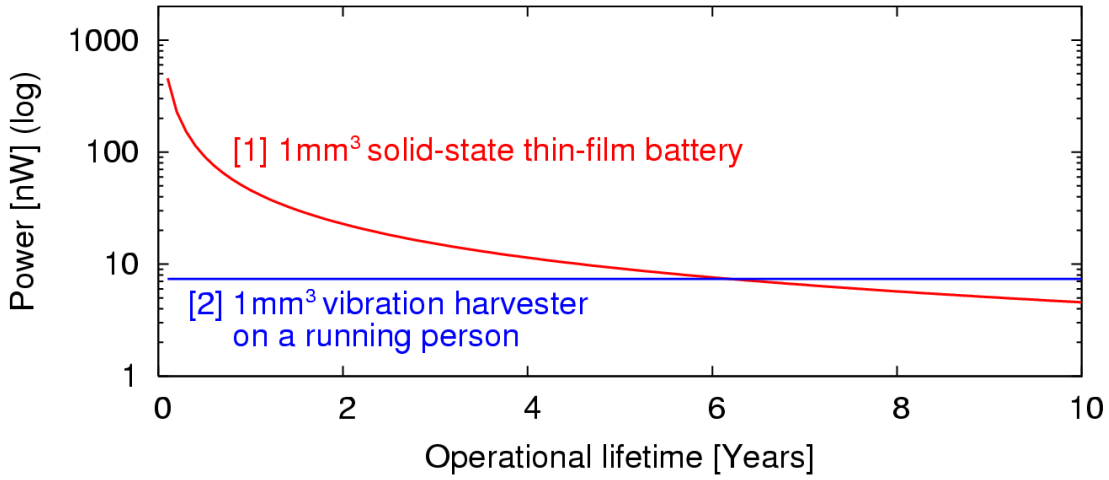
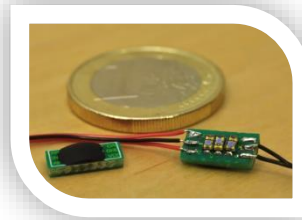
Need for Low Power

- Miniaturization enables new applications
  - Implants, wearables, mobiles

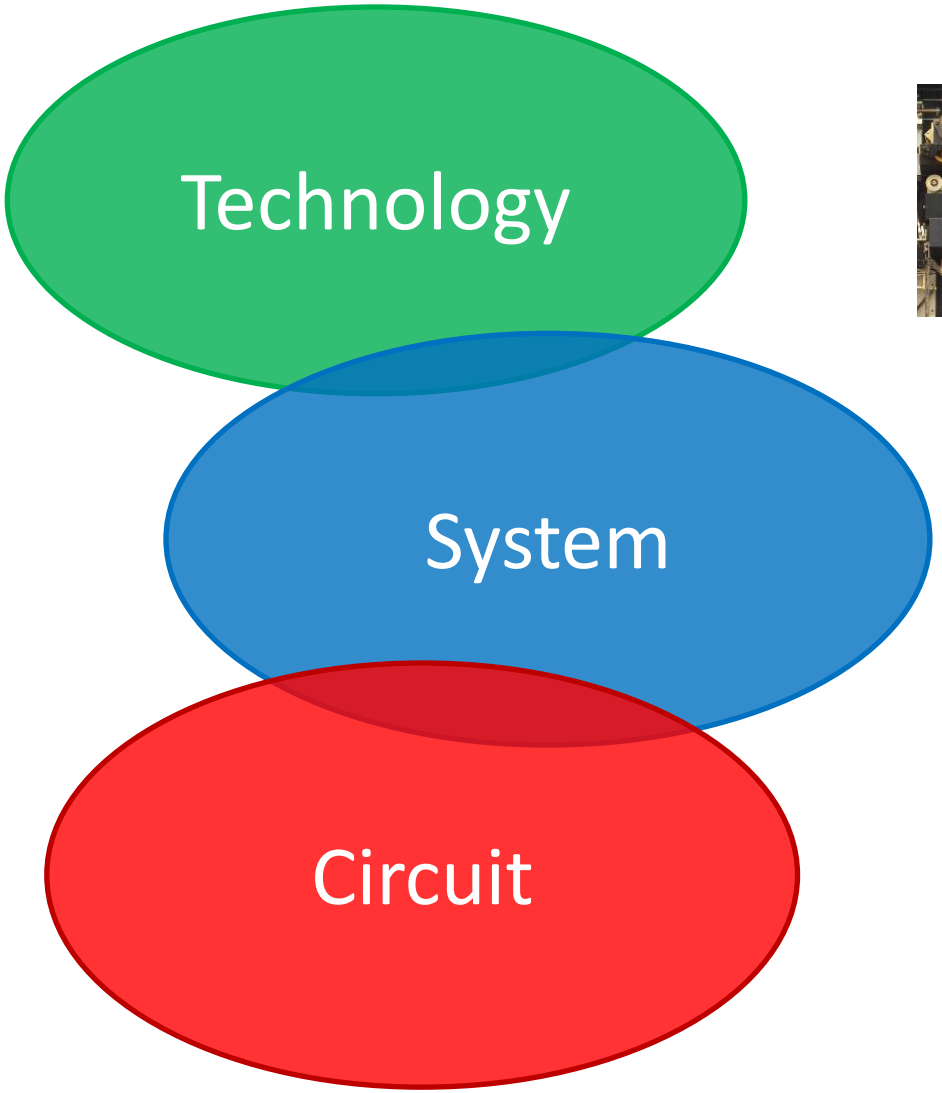




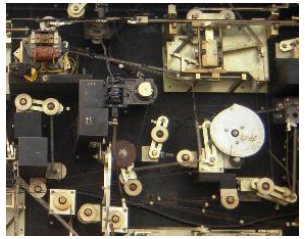
[Harpe, ISSCC 2015]

- Extremely low power electronics needed

Optimization at Different Levels

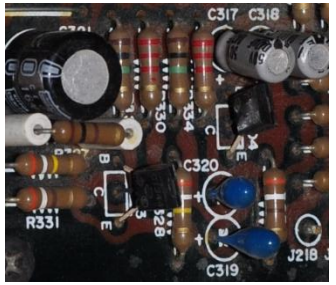


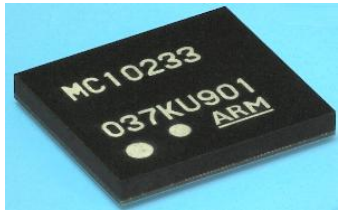
Change of technology, and scaling of technology (Moore's law)



[www.reddit.com]

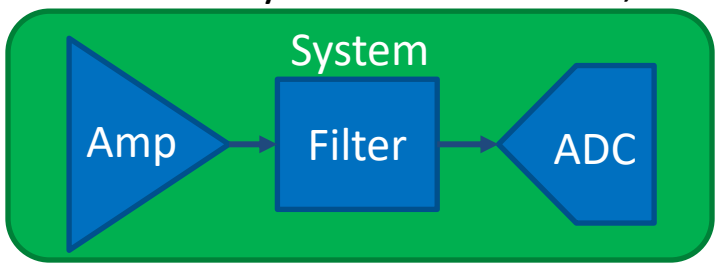
[www.wikipedia.org]

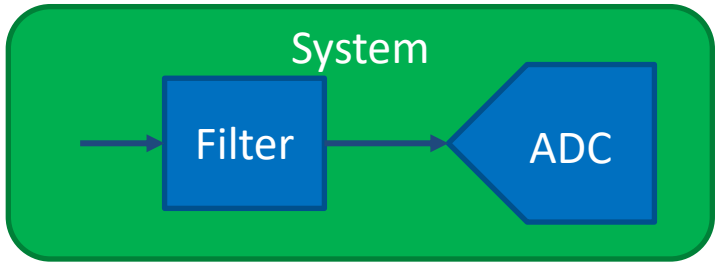




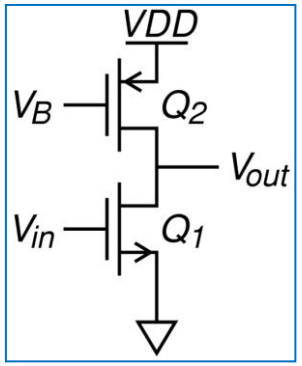
[www.renesas.eu]

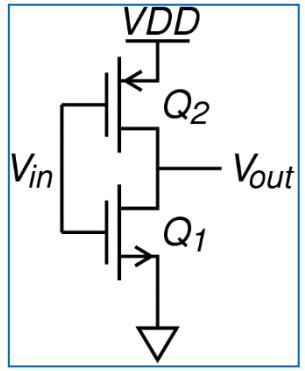
System architecture, and trade-offs between blocks





Circuit topology, and dimensioning of components





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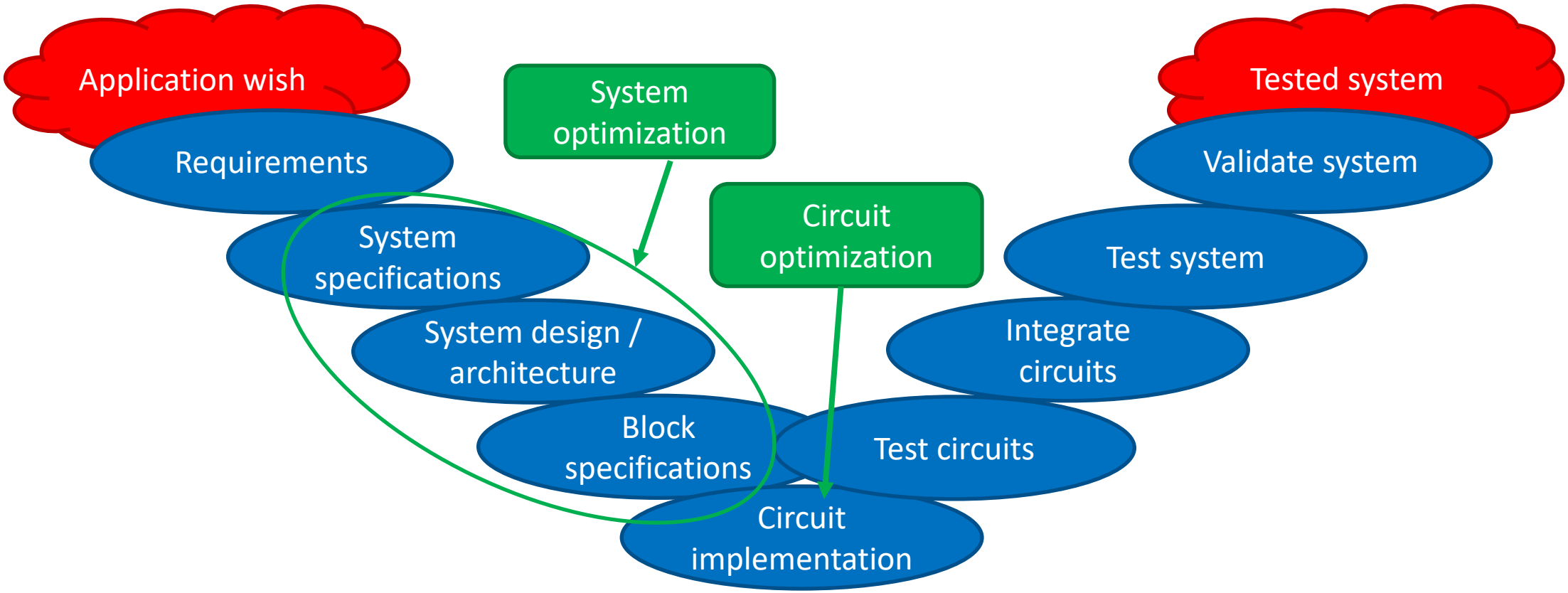
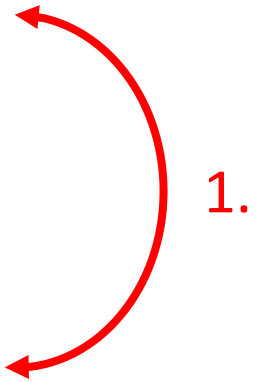
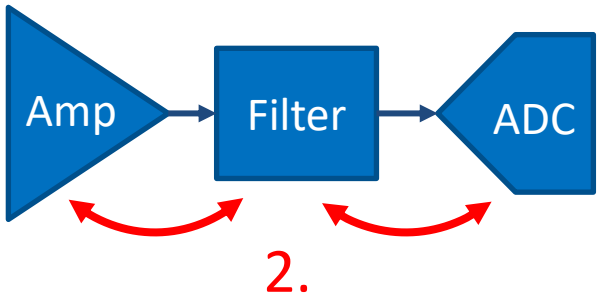
V Model


Application wish
Requirements
System specifications
System design / architecture
Block specifications
Circuit implementation
System optimization
Circuit optimization
Tested system
Validate system
Test system
Integrate circuits
Test circuits

What are the Main Trade-offs?

- "Performance" in processing signals
  - Amplitude (noise-level, maximum signal range, distortion)
  - Time/frequency (bandwidth, speed, clock frequency)
- "Costs"
  - Power consumption
  - (Chip area)
- Power-efficiency: ratio between performance and costs
- Trade-offs:
  1. Performance vs costs inside each block
  2. Between blocks





System Design Approach

- Step 1: Develop simple models/equations describing performance and costs for each block in the system

IRN = Input-referred noise level
BW = Bandwidth
P = Power consumption
→ Model: $P = Const \times BW / IRN^2$

- Step 2: Put these together in your system model
- Step 3: Vary parameters inside each block and between the blocks such that system-level specifications can be met
- Step 4: Optimize for minimum total power consumption
- Result: Block-level specifications for minimal power
  - Challenges: good yet simple models; optimization

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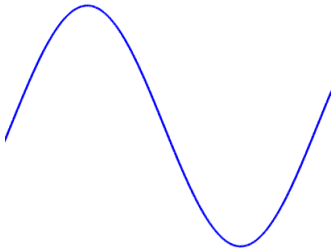
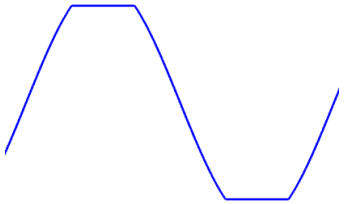
Signal, Noise, Distortion, Interference

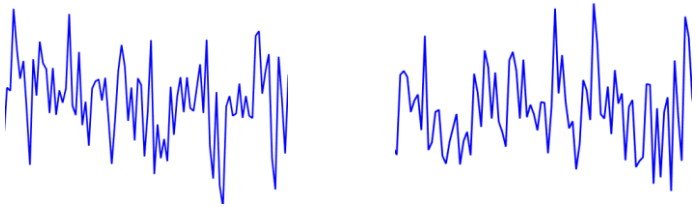
- Signal: Desired information to be processed
  - E.g. an ECG signal, a sine wave, etc.



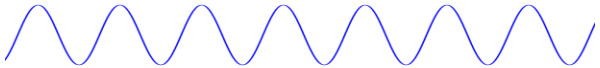
- Distortion: Deformation of the signal due to non-linearity of the circuit
  - E.g. saturation of an amplifier, non-linear transistor function (V_{gs}-I_d)



- Noise: *Random* disturbance
  - Generated by the circuit, or already contained in the input signal

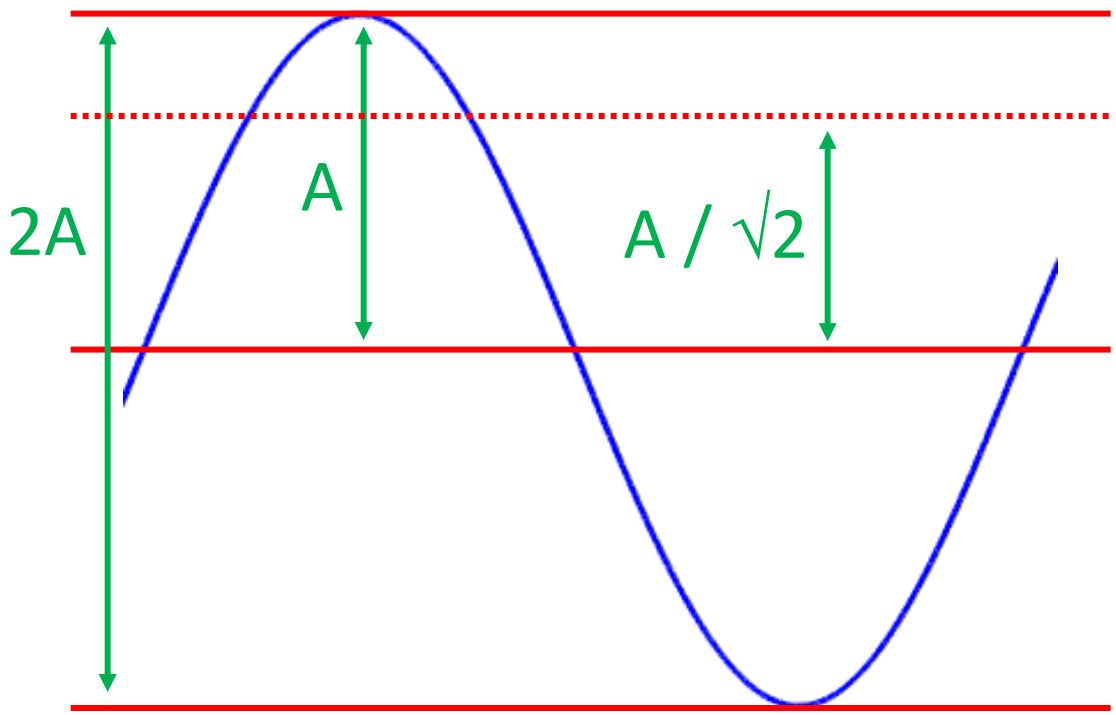


- Interference: Disturbance from an *unknown* signal from outside
  - E.g. power-line interference



Signal

- Sinewave $x(t) = A \sin(2\pi ft)$
- Amplitude: A [V]
- Peak-peak amplitude: 2A [V_{pp}]
- Rms amplitude: $A / \sqrt{2}$ [V_{rms}]
  https://en.wikipedia.org/wiki/Root_mean_square

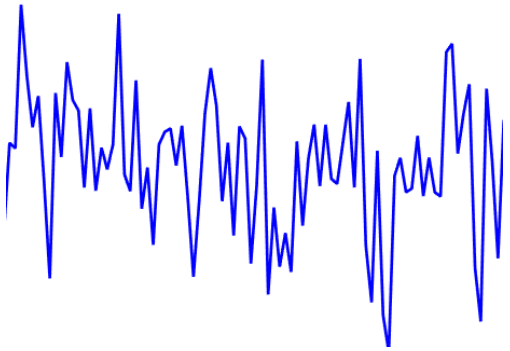


- Notes:
  - Be careful which amplitude definition is used
  - The input/output range of a circuit is often defined as peak-peak amplitude

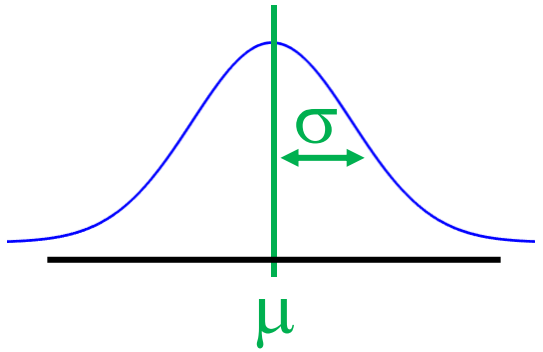
Noise

- Stochastic process
  - Not defined by a value, but by a distribution function
  - Often Gaussian distribution assumed: mean μ and variance σ^2

Noise vs time



Noise distribution



- For electrical noise: $\mu = 0$, σ is the rms value of the noise
  - E.g. a noise source with a value of $1mV_{rms}$ has a $\sigma = 1mV$.

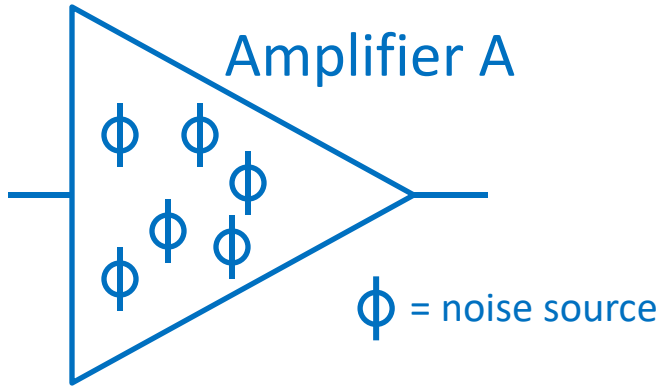
Adding Signal or Noise terms

- Addition of signal terms: amplitude domain
  - E.g.: 1V + 1V = 2V
- Addition of noise terms:
  σ or rms-value added in power (amplitude^2) domain
  - E.g: $1V_{rms} + 1V_{rms} \rightarrow 1.4V_{rms}$

Variable		X	Y	X + Y
Deterministic		X	Y	X + Y
Stochastic	Mean	μ_x	μ_y	$\mu_x + \mu_y$
	Standard deviation (rms value) or Variance (rms^2 value)	σ_x or σ_x^2	σ_y or σ_y^2	$\sqrt{(\sigma_x^2 + \sigma_y^2)}$ or $\sigma_x^2 + \sigma_y^2$

Input/Output-Referred Noise

- Circuit noise is generated by components inside the circuit:
  - An amplifier has many internal noise sources

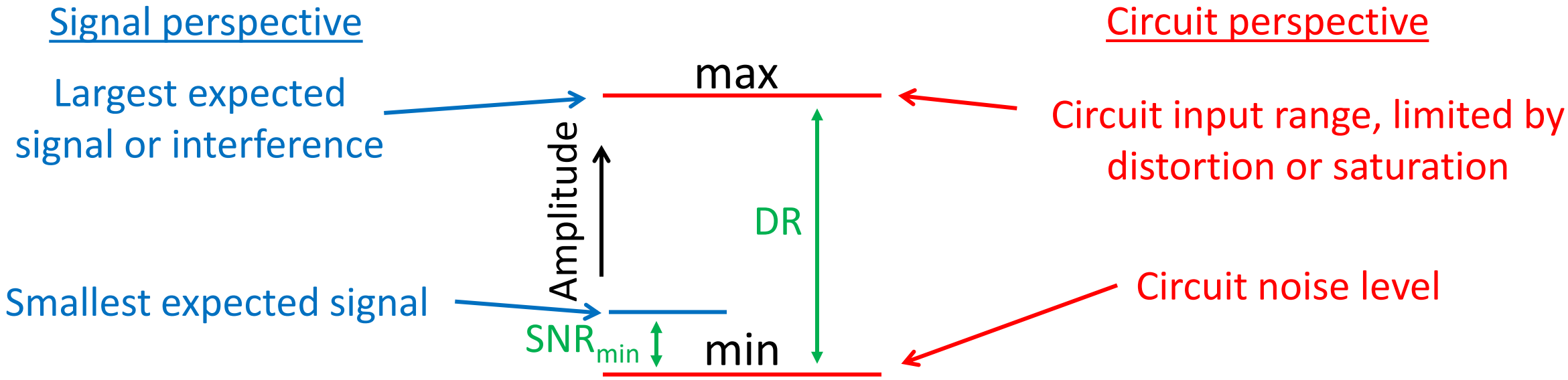


- Can be modeled by an *equivalent* noise source at the input/output of the circuit, representing the total noise of that circuit:
  - IRN (V_{irn}) = Input-referred noise
  - ORN (V_{orn})= Output-referred noise

Relation: $V_{orn} = A \cdot V_{irn}$

Dynamic Range (1)

- Dynamic Range (DR): Ratio between the largest signal vs the smallest signal that can be processed
  - Largest signal: bounded by the input range of a circuit, usually a sine
  - Smallest signal: bounded by the input-referred noise level of a circuit



Dynamic Range (2)

- Example, given an amplifier:
  - Input range is $1V_{pp}$
  - Input-referred noise is $10\mu V_{rms}$
  - SNR_{min} = 12dB
- Solve DR and minimum signal amplitude:
  - Input range is $1V_{pp}$ → 0.5V amplitude sine → $0.35V_{rms}$
  - Dynamic range is $0.35V_{rms}$ / $10\mu V_{rms}$ = $3.5 \cdot 10^4$
    In dB's, that becomes: $20 \log_{10} (3.5 \cdot 10^4)$ = 91dB
  - Smallest signal that satisfies SNR_{min}: 12dB higher than $10\mu V_{rms}$ → $40\mu V_{rms}$

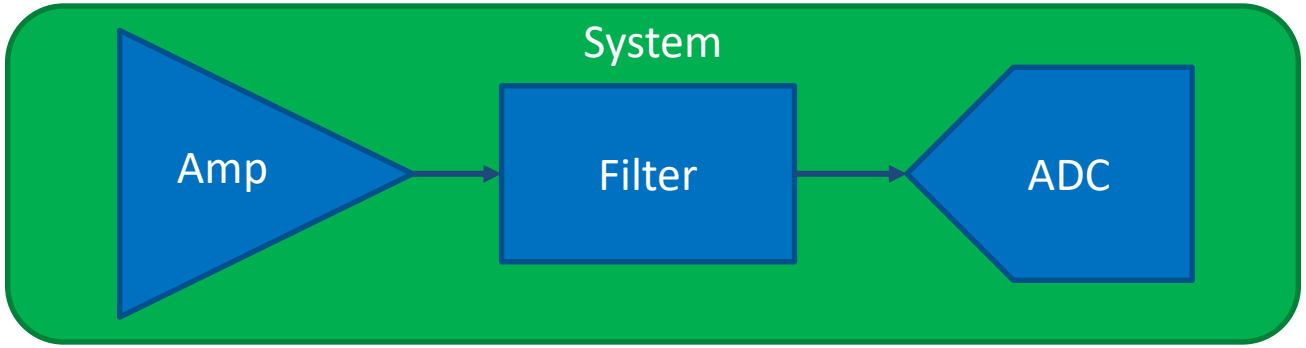
Exercise 2: System Noise, Input Range, and DR

Assume that the ADC has an input-referred noise of $1mV_{rms}$, the filter has an input-referred noise of $0.5mV_{rms}$, and the amplifier has an input-referred noise of $10\mu V_{rms}$. You may also assume that the amplifier has a gain of 100V/V, and the filter has unity gain. The input range of the amplifier is $20mV_{pp}$, the input range of the filter is $2.4V_{pp}$, and the input range of the ADC is $1.8V_{pp}$.

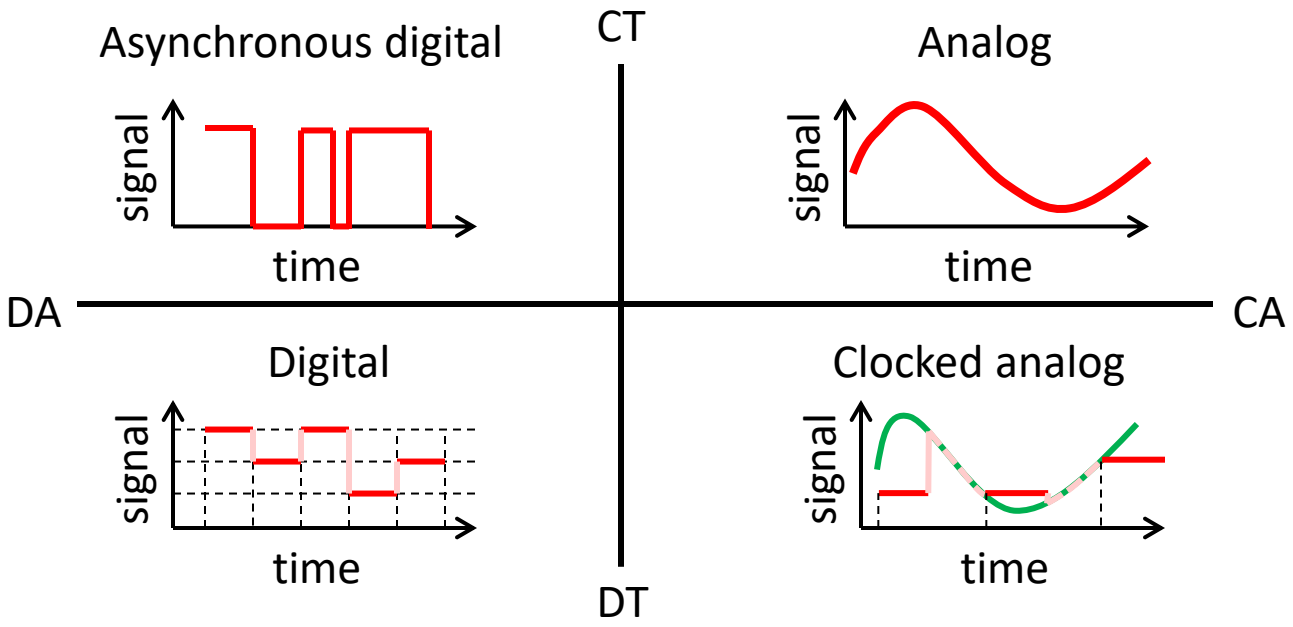
a) What is the total IRN of this system?

b) What is the input range of this system?

c) What is the dynamic range of the entire system?

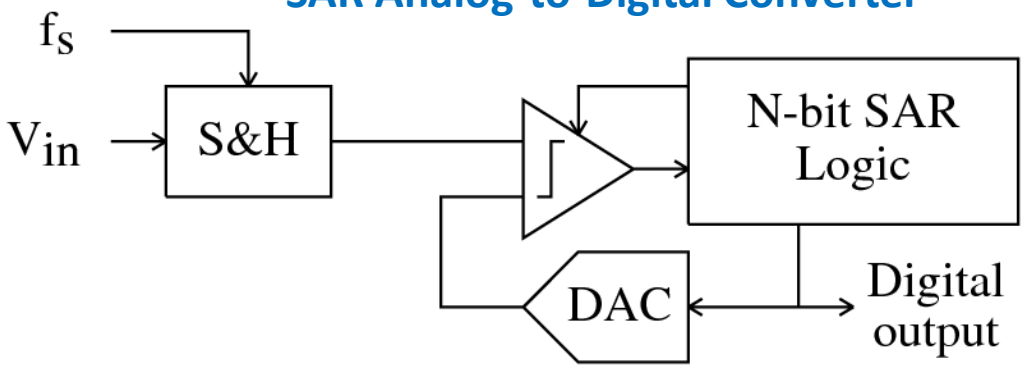


Analog, Mixed-Signal, Digital



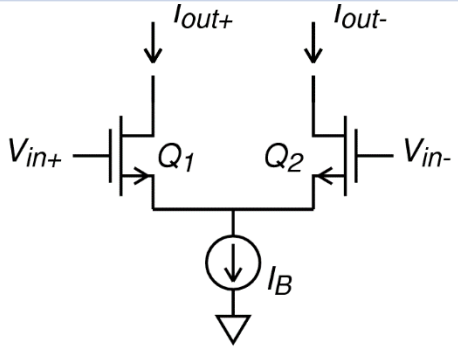
CT = Continuous Time
DT = Discrete Time
CA = Continuous Amplitude
DA = Discrete Amplitude

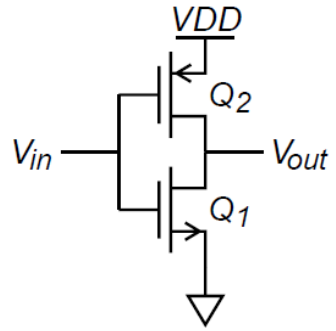
SAR Analog-to-Digital Converter



Analog versus Digital

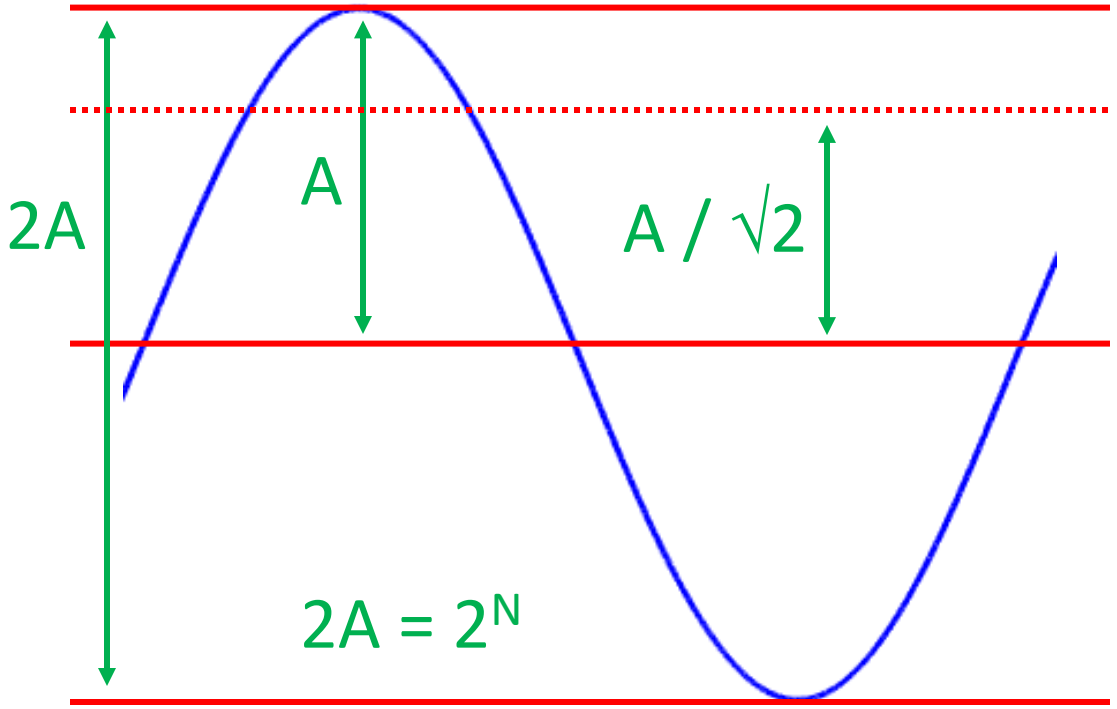
Analog	Digital
Compute on continuous signal [0 to VDD]	Compute on discrete set {0, VDD}
Basic functions based on physics (I-V, KCL)	Basic functions based on maths (AND, NOT)
Large amount of computation per device	Small amount of computation per device
One wire represents many bits of information	One wire represents one bit of information
Computation sensitive to physical parameters	Computation is insensitive to physical parameters
Noise due to physical devices	Noise due to quantization
Signal not restored but gradually degrading	Signal restored at each stage
Not easily programmable	Easily programmable
Efficient	**Robust**





DR (SQNR) of a Digital Signal

- Digital codes with N-bit resolution
  - Can represent 2^N levels
  - E.g. N = 4: 16 codes from 0000 to 1111
- Each (analog) signal has to be rounded off to a value in the finite set of 2^N levels
  - Introduces quantization noise



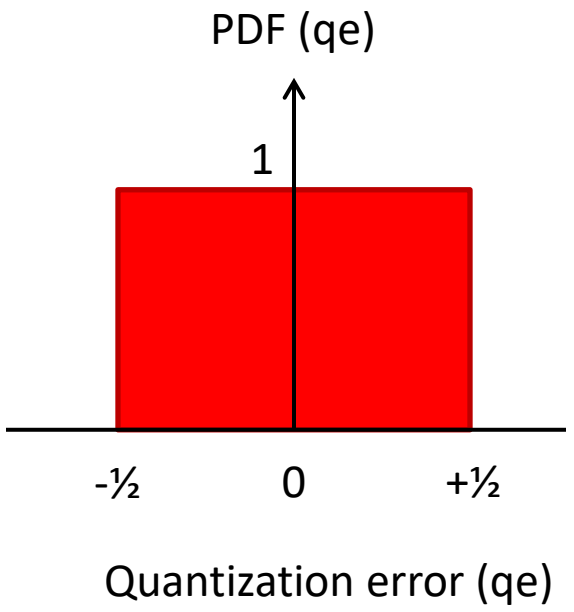
- RMS value signal: $2^N / 2\sqrt{2}$
- RMS value quantization noise: $1 / \sqrt{12}$ (σ for uniform distribution ± 0.5)
- $SQNR_{dB} = DR_{dB} = 20 \log_{10} \{(2^N / 2\sqrt{2}) / (1 / \sqrt{12})\} = 6.02N + 1.76$

Exercise 3: Quantization Noise

The previous slide mentions that the RMS value of the quantization noise is $1 / \sqrt{12}$. Why is that so? Can you prove this?

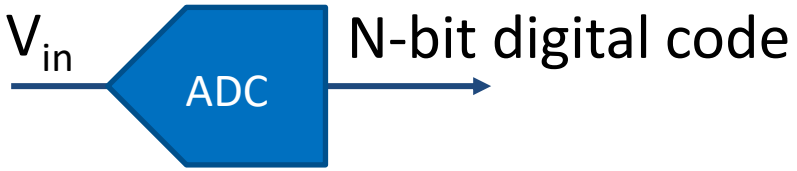
Hints:

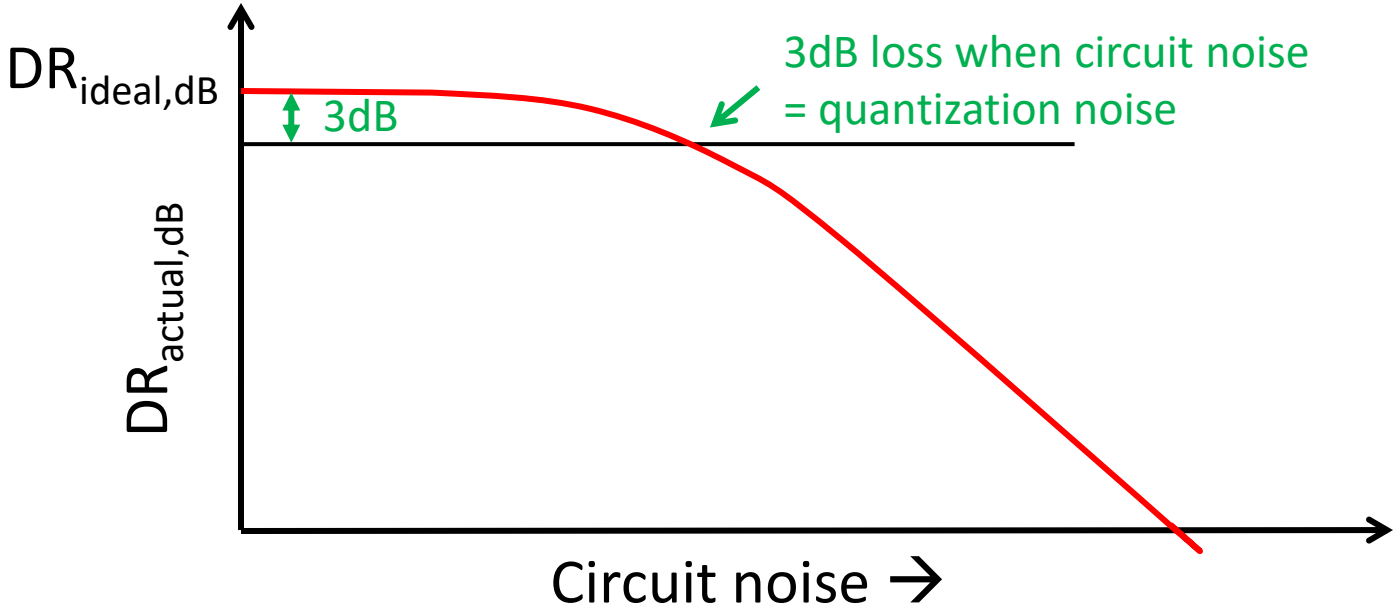
- The quantization error (qe) is bounded to ±½, because each value is rounded to the nearest integer value
- You may assume that each error within this range is equally likely, i.e.: the probability density function (PDF) of qe has a distribution as shown on the right
- The RMS value of the quantization noise is given by the standard deviation (σ) of qe



ADC Resolution and DR

- DR of the ADC is limited by both analog and digital DR
  - Digital side: limited by # bits N: $DR_{ideal,dB} = SQNR = 6.02N + 1.76$
  - Analog side: limited by circuit noise
- Overall: $DR_{actual,dB} = 6.02ENOB + 1.76$





ENOB is the effective number of bits (or effective resolution) including the effects of quantization noise and circuit noise

- Ideally equal to N
- In practice smaller than N

Exercise 4: ADC Resolution and DR

Given an ADC with N = 10bit resolution and an input-range of $2V_{pp}$. The input-referred circuit noise (excluding quantization noise) is $1.2mV_{rms}$.

a) What is the dynamic range of a 10bit resolution digital code?

b) How many levels can a 10bit code create (i.e.: what is the output range)?

c) What is thus the "gain" of this ADC: from input voltage to output code?

d) The output-referred quantization noise is equal to $1 / \sqrt{12}$ (codes or LSBs). What is the input-referred quantization noise of this ADC (in mV_{rms})?

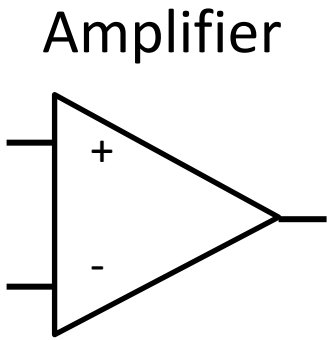
e) What is the total input-referred noise of this ADC?

f) What is the overall, actual dynamic range of this ADC?

g) What is the ENOB of this ADC?

Trade-offs Analog Block (Amplifier)

- Power as function of bandwidth and noise-level:
  - $P \propto I_{BIAS}$, in sub-threshold: $g_m \propto I_{BIAS}$
  - GBW $\propto g_m / C \propto P \rightarrow$ 100x power gives 100x bandwidth
  - $V_{irn}^2 \propto 1 / g_m \propto 1 / P \rightarrow$ 100x power gives 0.1x V_{irn}



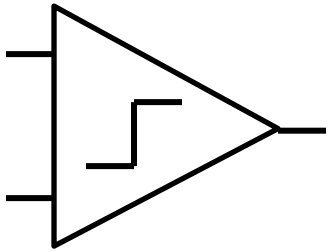
- Figure of Merit: NEF
  - $NEF = V_{irn}\sqrt{(2I_{BIAS} / (\pi \cdot V_t \cdot 4kT \cdot BW))}$
  - With constant NEF:
    - 100x more I_{BIAS} indeed implies 100x BW or 0.1x V_{irn}

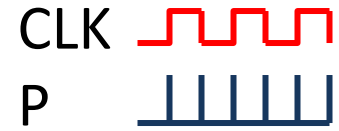
P = Power consumption
I_{BIAS} = Total bias current
g_m = Transconductance of input transistors
C = Capacitive load of amplifier
V_{irn} = Input-referred noise voltage
NEF = Noise Efficiency Factor
V_t = Thermal voltage (kT/q)
k = Boltzmann constant
T = Absolute temperature
q = Charge of one electron

Trade-offs Mixed-Signal Block (ADC)

- Power as function of bandwidth and noise-level:
  - Dynamic operation: $P \propto f_{sample}$, BW is max ½ f_{sample}
    → $P \propto BW$ → 100x power gives 100x BW
  - Dynamic range $\propto 1 / V_{irn} \propto P^{½}$ → $DR_{dB} \propto 10 \log_{10}(P)$
    → 100x power gives +20dB DR_{dB} or 0.1x V_{irn}

Dynamic comparator





- Figure of Merit: FOMS
  - FOMS = DR_{dB} + 10 $\log_{10}$ (BW / P) [dB]
  - With constant FOMS:
    - 100x more P indeed implies
      100x BW or 20dB better DR_{dB} (10x better in linear scale)

P = Power consumption
f_{sample} = Sample rate (clock)
DR = Dynamic Range
BW = bandwidth
V_{irn} = Input-referred noise
FOMS = Schreier FoM

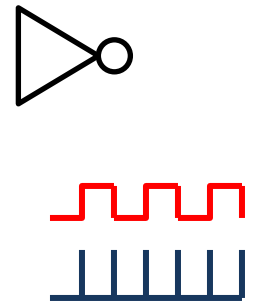
Note: Some definitions of FOMS use SNR or SNDR rather than DR

Trade-offs Digital Block (Logic)

- Power as function of bandwidth and noise-level:
  - Dynamic operation: $P \propto f_{clk}$
    → 100x power gives 100x speed
  - Dynamic range: not bounded by circuit noise but by quantization noise
    - DR (or SQNR) of a digital circuit is given by $DR_{dB} = SQNR_{dB} = 6.02N + 1.76$
    - Dependent on the digital function, P might be e.g. linear or quadratic in N
    - If assumed linear: DR_{dB} will be linear in P
    - Note: for analog/mixed-signal circuits, DR_{dB} will be logarithmic in P

→Digital is advantageous for high DR

Digital CMOS logic



P = Power consumption
f_{clk} = Clock frequency
DR = Dynamic Range
SQNR = Signal-to-quantization-noise-ratio
N = Number of bits in the digital codes

Exercise 5: NEF and FOMS Estimates

Suppose we want to make an amplifier with an input-referred noise level of $5\mu V_{rms}$, a bandwidth of 5kHz, a gain of 20X, and an output range of $1V_{pp}$. You may further assume that the power supply voltage is 1.2V and that an NEF between 2 and 3 is feasible. We want to minimize the power consumption.

a) In terms of efficiency, would you prefer to achieve an NEF of 2 or 3?

b) What is the minimal power consumption you expect for the amplifier?

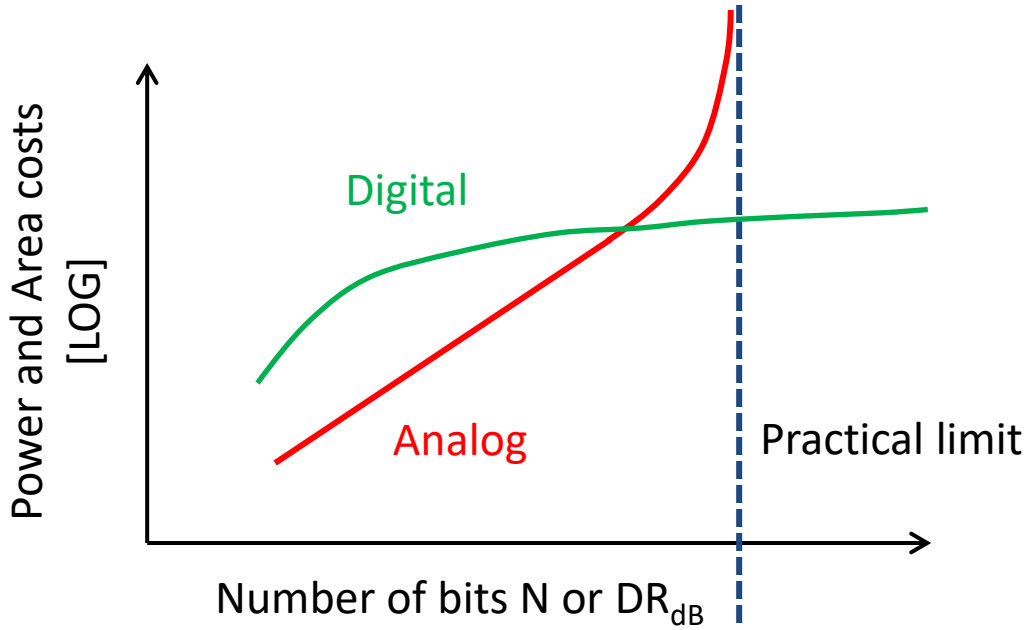
c) Assume that the amplifier is connected directly to an ADC. How many bits (N) should we have in the ADC so that it does not limit the dynamic range of the system?

d) What is the power consumption you expect for the ADC, assuming a FOMS of 170dB?

e) What do you think of the amplifier power consumption versus the ADC power consumption? Do you have an idea how you could balance this more?

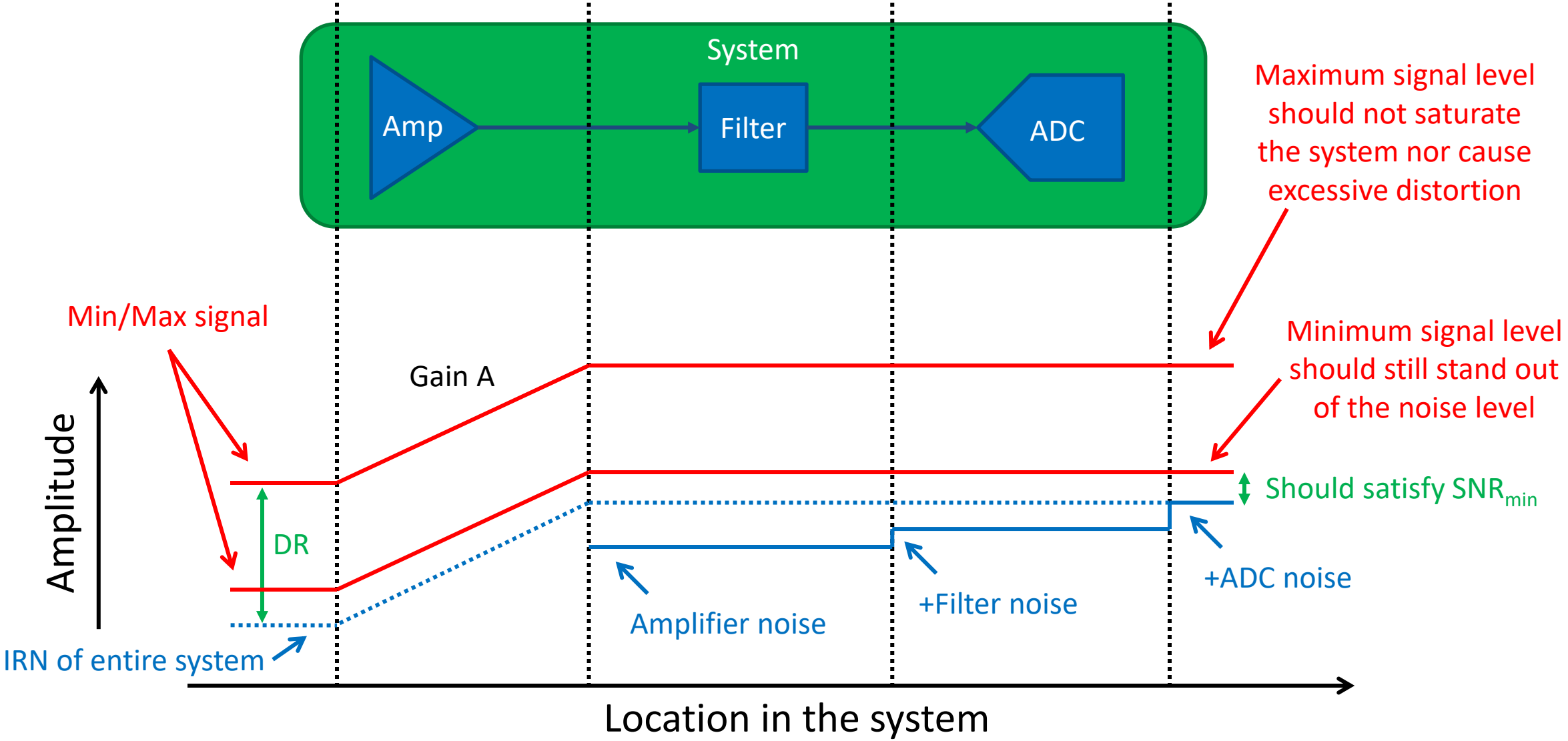
Analog versus Digital

- Power vs Clock rate / BW
  - Analog/Digital: linear grow
- Power (and area) vs DR_{dB}
  - Analog: exponential grow
    - Practical limits at some point
  - Digital: e.g. linear/quadratic grow
    - Not really a hard limit



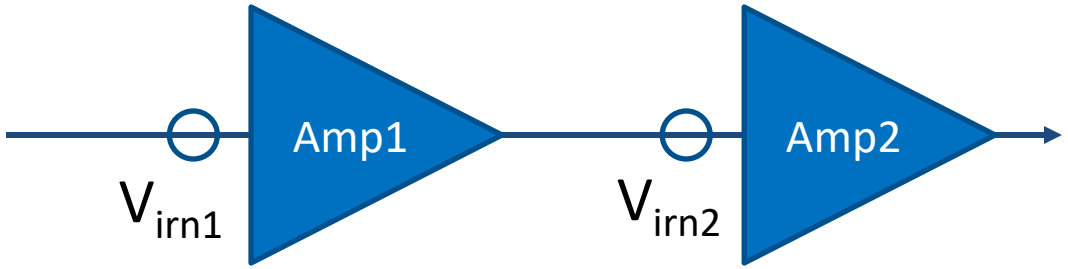
- Digital is favorable for high-DR systems in terms of power and area
- Analog is favorable for low-DR systems in terms of power and area
  → A lot of low power systems are relatively analog-intensive

System Budget Picture



Effect of Gain on Noise and Power Consumption

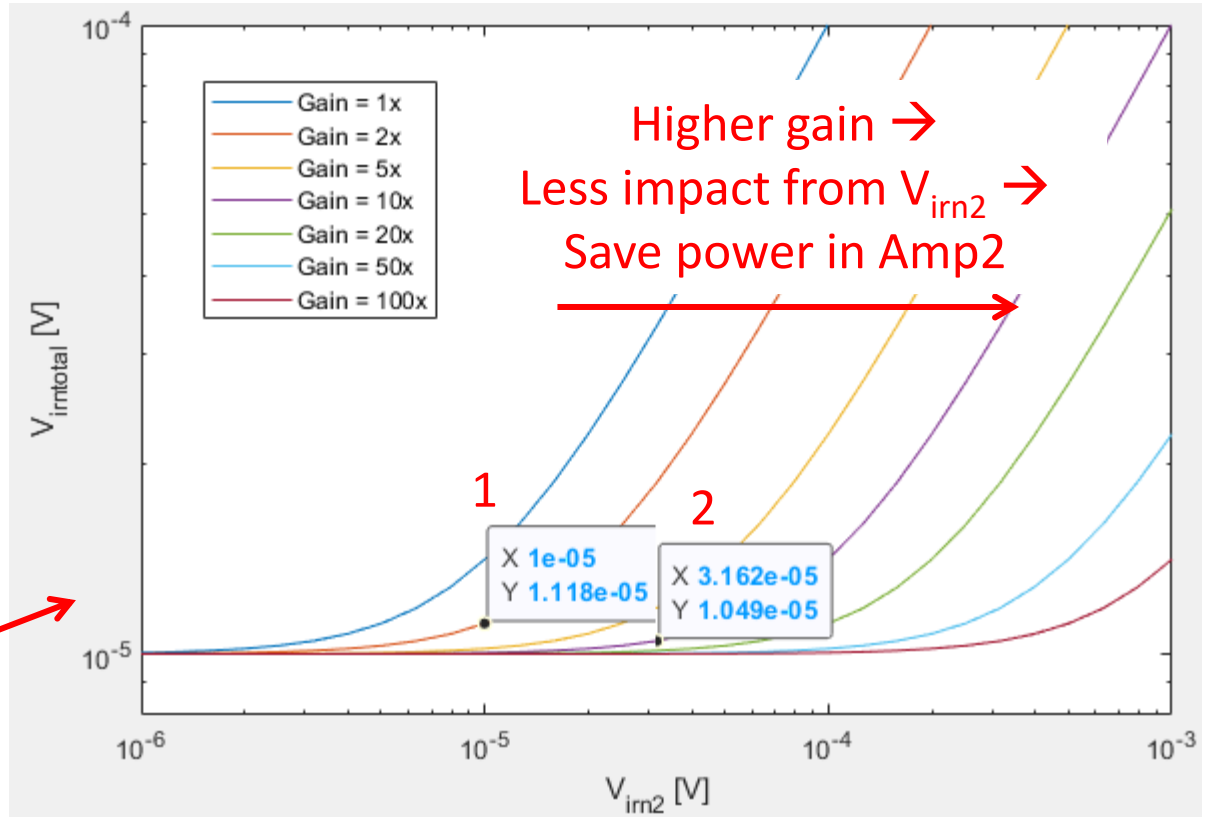
- Example: series connection of two amplifiers with gain A



- $V_{irntotal} = \sqrt{\{V_{irn1}^2 + (V_{irn2} / A)^2\}}$
- Assume $V_{irn1} = 10\mu V_{rms}$

Case	A	V_{irn2}	$V_{irntotal}$	P_2
1	2x	$10\mu V_{rms}$	$11\mu V_{rms}$	P_1
2	10x	$32\mu V_{rms}$	$10.5\mu V_{rms}$	$0.1P_1$

- Power is estimated from IRN using NEF trend



Case 1: Thanks to gain of Amp1, Amp2 contributes little noise, yet still consumes substantial power
Case 2: With higher gain of Amp1, Amp2 is relaxed: little noise contribution, little power overhead

Exercise 6: Gain, Noise and Power Consumption

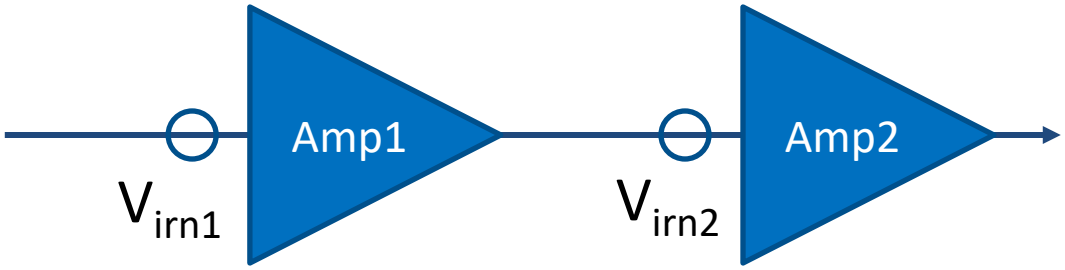
We design a series of amplifiers as shown below. We have the following requirements:

- The gain A of both amplifiers is identical and equal to 5 V/V.
- The total input-referred noise should be $2\mu V_{rms}$.
- We want to minimize the total power consumption of the system. You may assume (based on the NEF trend) that $P_1 V_{n1}^2 = P_2 V_{n2}^2 = \text{constant}$, where P_i is the power consumption of amplifier i and V_{ni} is the IRN of amplifier i.

a) What is the output-referred noise of the entire system?

b) How should we choose the input-referred noise of the first amplifier to achieve the above requirements? And of the second amplifier?

c) From the total power consumption, which percentage is from the first amplifier? And from the second?



Outline

- System design methodology: V model
- Risk management
- Optimization for low power at different levels
- System-level optimization and trade-offs
- Analog, mixed-signal, and digital circuits
  - Signal definitions, optimization strategies
- Summary

Summary

- V model & risk management
  - Go step-by-step, top-down to reach your implementation
  - Balance level of detail: not too detailed, not too simplified
  - Verify at every step!
  - Manage risks → Planning and priorities
- System optimization
  - Model building blocks (performance vs costs)
  - Optimize for power consumption & system specifications
- Models of power and performance in amplitude/frequency
  - Frequency: analog & digital scale similar
  - Amplitude: analog favorable for low DR, digital favorable for high DR

Solution 1: System Design

There are many possible answers. A couple of examples:

a) The device should be small enough to be implanted; it should be biocompatible.

b) The device volume should be <2cm^3; It should operate from 20°C up to 50°C.

c) If we add more gain to the amplifier, we can relax filter noise.

d) If the filter has a lower bandwidth (or a higher order) we can reduce the ADC's sampling rate based on the Nyquist sampling criterion: $f_s > 2$ BW.

e) We might not be able to make it small enough; It might consume too much power.

f) We could make a system overview with all components (high-level). Then we may identify which components are expected to be largest and spend a bit of time to check their expected size in a bit more detail. For power consumption we can do something similar: identify which blocks likely contribute most to the power consumption and do a back-of-the-envelope calculation or literature study to see if the required performance is realistic/feasible.

Solution 2: System Noise, Input Range, and DR

Assume that the ADC has an input-referred noise of $1mV_{rms}$, the filter has an input-referred noise of $0.5mV_{rms}$, and the amplifier has an input-referred noise of $10\mu V_{rms}$. You may also assume that the amplifier has a gain of 100V/V, and the filter has unity gain. The input range of the amplifier is $20mV_{pp}$, the input range of the filter is $2.4V_{pp}$, and the input range of the ADC is $1.8V_{pp}$.

a) $V_{IRN} = \sqrt{\{(10\mu V_{rms})^2 + [(0.5mV_{rms})^2 + (1mV_{rms})^2] / 100^2\}} = 15\mu V_{rms}$.

b) This is limited by the most severe limit. The amplifier limits the input range to $20mV_{pp}$, the filter limits it to $24mV_{pp}$, and the ADC limits it to $18mV_{pp}$. So overall: $18mV_{pp}$.

c) $20 \log_{10} (18mV_{pp} / (2\sqrt{2}) / 15\mu V_{rms}) = 52.6dB$.

Solution 3: Quantization Noise

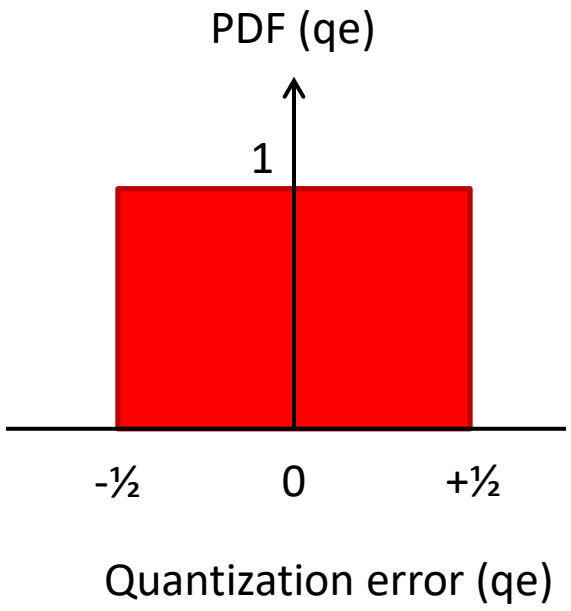
Mathematically, the variance (σ^2) is calculated by:

$\sigma^2 = \int_{-\infty}^{+\infty} \{x^2 \cdot PDF(x)\}dx$

If we solve this, we get:

$\sigma^2 = \int_{-\infty}^{+\infty} \{x^2 \cdot PDF(x)\}dx = \int_{-½}^{+½} \{x^2 \cdot 1\}dx = {}^1/_3\, x^3 |_{-½}^{+½} = 1/12.$

This results in $\sigma = 1 / \sqrt{12}$.



Solution 4: ADC Resolution and DR

Given an ADC with N = 10bit resolution and an input-range of $2V_{pp}$. The input-referred circuit noise (excluding quantization noise) is $1.2mV_{rms}$.

a) $DR_{digital} = 6.02 \cdot 10 + 1.76 = 62dB$.

b) $2^{10} = 1024$ levels, so the peak-peak range at the output is 1024 codes.

c) 1024 codes matches to $2V_{pp}$, so the "gain" is 1024/2 = 512 codes/V.

d) IRN = ORN / gain = $1 / \sqrt{12} / 512 = 0.56mV_{rms}$.

e) $\sqrt{(0.56mV_{rms}^2 + 1.2mV_{rms}^2)} = 1.33mV_{rms}$.

f) $DR_{actual} = 20 \log_{10} (2V_{pp} / (2\sqrt{2}) / 1.33mV_{rms}) = 54.5dB$.

g) $ENOB = (DR_{actual} - 1.76) / 6.02 = 8.8bit$.

Solution 5: NEF and FOMS Estimates

a) NEF = 2 is better as it has better efficiency.

b) Using the NEF formula: $2 = 5\mu V_{rms} \sqrt{(2I_{BIAS} / (\pi \cdot V_t \cdot 4kT \cdot 5kHz))}$, I_{BIAS} can be solved as 0.54µA. With a supply of 1.2V, that gives a power consumption of 0.65µW.

c) The input range of the amplifier is $1V_{pp} / 20 = 50mV_{pp}$, thus the DR is $20 \log_{10} (50mV_{pp} / (2\sqrt{2}) / 5\mu V_{rms}) = 71dB$. The ADC should at least be 12bit (DR of 74dB).

d) $170dB = 74dB + 10 \log_{10} (5kHz / P) \rightarrow P = 1.3\mu W$.

e) Reasonably balanced. To improve that, we need to reduce ADC power or increase amplifier power. We could try to look for an ADC with better FOMS, or sacrifice a bit of DR in the ADC.

Solution 6: Gain, Noise and Power Consumption

a) ORN = $2\mu V_{rms} \cdot 5 \cdot 5 = 50\mu V_{rms}$.

b) The following set of equations should be solved: $(2\mu V_{rms})^2 = V_{n1}^2 + V_{n2}^2 / 25$;
$P = P_1 + P_2$; $P_1 V_{n1}^2 = P_2 V_{n2}^2 = \text{constant}$; P should be minimized.
$(2\mu V_{rms})^2 = V_{n1}^2 + V_{n2}^2 / 25 \rightarrow V_{n2}^2 = 100p - 25V_{n1}^2$, where "p" stands for 10^{-12}.
$P = P_1 + P_2 = P_1 \{1 + V_{n1}^2 / V_{n2}^2\} = \text{constant} / V_{n1}^2 \cdot \{1 + V_{n1}^2 / (100p - 25V_{n1}^2)\} \rightarrow$
$P = \text{constant} \cdot \{1 / V_{n1}^2 + 1 / (100p - 25V_{n1}^2)\}$
Solving $\partial P / \partial V_{n1}^2 = 0$ to yield the minimum P yields:
$\partial P / \partial V_{n1}^2 = \text{constant} \cdot \{-2 / V_{n1}^3 + 50V_{n1} / (100p - 25V_{n1}^2)^2\} = 0$
$2 / V_{n1}^3 = 50V_{n1} / (100p - 25V_{n1}^2)^2 \rightarrow (100p - 25V_{n1}^2)^2 = 25\, V_{n1}^4 \rightarrow 100p - 25V_{n1}^2 = 5V_{n1}^2$
Solving this yields $V_{n1} = 1.83\mu V_{rms}$ and $V_{n2} = 4.08\mu V_{rms}$.

c) From the above set of equations, it also follows that the first amplifier consumes 83% and the second amplifier 17% of the total power consumption.