Process Development and Characterization of Thermal Compression Flip-Chip Bonding

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***Abstract*— Flip-Chip Technology offers a large number of connections and reduced signal propagation time compared to Wire Bonding. A process was developed to produce Flip-Chip Technology at TU/e, aiming to significantly reduce the time required for research involving this technology to obtain results. This process requires 4 steps: interposer design and production, bump placement, die alignment and placement and electrical testing. It was discovered that gold evaporation is the best metallization method for the interposer as it leads to more consistent bump placement and has the lowest interconnection resistance. Moreover, it was discovered that 25μm gold wire allows for more reliable bump placement, but require a pad pitch size larger than 90μm. In the die placement stage, a heat profile was found that resulted in confirmed electrical connections.** [1]

***Index Terms*—Flip-Chip, Process, Interposer, Die, Gold bumps, Testing, Electrical characterization**

I. Introduction

The concept of Flip-Chip Technology, first introduced by IBM in the 1960s, involves placing the die face down on a carrier material (substrate or interposer) using metal bumps instead of traditional bonding wires [2]. This technique allows for more connections per surface area and shorter connections which reduces resistance, inductance and capacitance, improving signal propagation time and thus chip performance [3], [8], [10], [11]. In order to make these connections reliable, 4 options for connecting the interposer and the die with metal bumps can be considered. These options are Thermal Compression bonding, Eutectic bonding, Ultrasonic bonding and Solder Bump bonding. Starting with Thermal Compression bonding, heat and force are applied to connect the bumps. Next is Eutectic bonding, which uses an intermediate solder alloy to form a continuous bond between two surfaces and is used often in die packaging for systems that are sensitive to outgassing of standard die attach materials [7]. Ultrasonic bonding uses high-frequency vibrations to bind the surfaces, which lowers the temperature budget required to make the bonding, thanks to additional energy generated by the localized friction (ultrasonic vibrations) at the surface contact between bumps and pads. Finally, Solder Bump bonding re-flows solder balls to connect the die.

These benefits, along with the selection of a suitable bonding techniques and the research into the characteristics of the metal bumps and the interposer tracks play a vital role in the integration of, for example, On-Chip Arrays such as LED arrays [1]. That is because the type of connection between two or more dies significantly impacts the practical use due to connection specific limitations such as a minimum required interconnection density. In the field of On-Chip Arrays, the amount of connections that must be made reliably can reach a few thousand connections. Flip-Chip Technology has the potential to increase die interconnection density compared to wire bonding, enabling a higher pin count in the same chip area. Therefore, understanding the limitations and requirements, as well as the impact of any substrate or interposer on signal transmission between dies, is of great interest. Due to this interest, the Integrated Circuits (IC) research group of the TU/e would benefit significantly from having a specified process for Flip-Chip Technology.

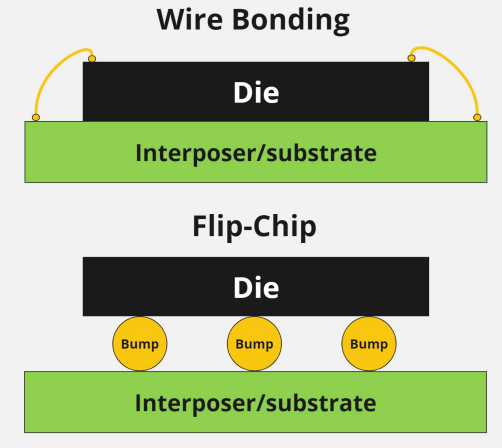

Fig. 1. Wire Bonding (top) and Flip-Chip Technology (bottom) visualized.

This paper describes the development of such a process, which can be used to speed up future research requiring Flip-Chip Technology. In section II the essential components and setup of the process are discussed. Section III describes the steps of the process, any obstacles that were faced and results that are obtained in each stage of the process. Finally, in Section IV conclusions are drawn and recommendations are given for any steps that still need to be investigated to complete the process.

II. Process Setup

The essential components required in the proposed Flip-Chip process are the bumps and interposer, which both employ gold as the metal for interconnection due to its high conductivity. The process utilizes university facilities, with the interposers produced in the clean-room on campus and the remaining development is carried out in the Electronics lab at Flux 8.070.

[1]This paper is written as part of a Bachelor End Project in the department of Electrical Engineering of the TU/e, in the period of 02-09-2024 → 17-01-2025 and was supervised by M. Fattori, G. Radulov and assisted by V. Vidojkovic.

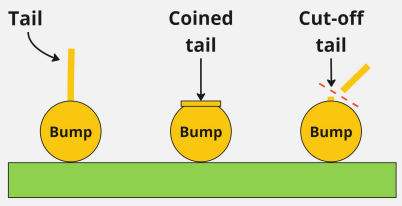

Fig. 2. The left bump in the image shows the tail present after placement, the middle shows the result of coining the bump in Ball Bump mode and the right bump shows the result of cutting the tail off in Ball Wedge mode.

Three setups are used in the Electronics lab for producing bumps, placing the die, and characterizing the interposer and bumps. Gold bumps are made with the TPT HB16 Wire Bonder: two gold wire diameters have been tested, 25μm and 17μm, respectively. There exists a trade-off between between the size of the bups and the diameter of the wire, with the latter being approximately three times the wire diameter [10]. Clearly, a smaller wire size yields a higher bump density.

The Wire Bonder has several parameters to optimize, varying by mode. Of the four modes available, only Ball Bump and Ball Wedge are of interest as the other modes are for Wire Bonding. Fig. 2 visualizes the difference between Ball Bump and Ball Wedge mode and Fig. 3 shows the setup of the Wire Bonder.

- Ball Bump Mode: Creates a bump with a tail that can potentially cause shorts during die placement. A coining tool can flatten the tails to reduce the risk of a short circuit being formed.
- Ball Wedge Mode: Cuts off the tail, leaving a well-rounded top, which is preferred to reduce short circuit risk.

In both modes, parameters like ultrasound (US) power, time, force, and stage heater temperature need to be optimized to successfully and reliably place the bumps on the interposer. For Ball Wedge mode, these parameters are split between Bond 1 and 2. A necessary addition to the Wire Bonder is a camera for inspection and capturing images. Moreover, the camera allows for a placement method that allows the operator to place bumps more accurately, which will be discussed in Section III.

After making the bumps, the die is placed using the Dr. Tresky T-5300, which offers high precision alignment with its beam-splitter, allowing to simultaneously view the die and interposer. In order to collect the die and position it, the Dr. Tresky machine makes use of a vacuum pick and place tool (pick mode). The workbench employs a vacuum to hold the interposer in place. Once aligned, the pick-and-place tool can be lowered to make contact with the bumps (touch-down recognition). Upon reaching the set force, the machine locks the tool for a set duration and then blowing off the die (release). The substrate heater is enabled during the place mode, allowing to apply a specific thermal profile to the assembly (interposer and die): optimizing the heating profile, placement time, and placement force is essential for reliable connections. The setup of the Dr. Tresky machine is shown in Fig. 3.

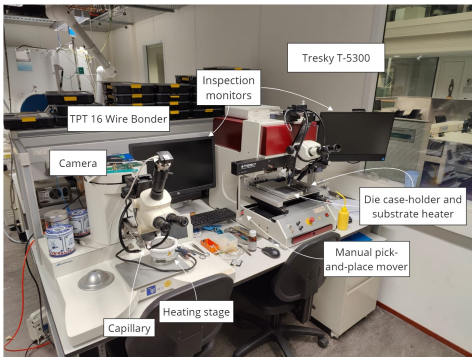

Fig. 3. TPT HB16 Wire Bonder (left) used to develop the bumps on the interposer and Dr. Tresky T-5300 (right) Flip-Chip machine employed for the alignment and placement of the die on the interposer.

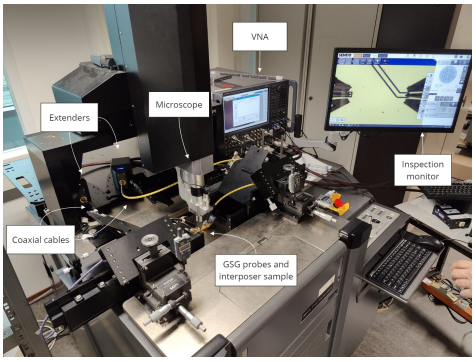

Fig. 4. Setup for the electrical characterization of the interposer and bump interconnections.

Finally, the proposed setup for testing the electrical characterization of the interposer uses a Keysight PNA-X N5247B Vector Network Analyser (VNA) covering a frequency range from 10 MHz to 110 GHz. Fig. 4 shows the setup of the VNA. For the scope of this project, the investigation has been limited to 10 GHz. The VNA connects to extenders with coaxial cables leading to 125μm pitch GSG probes. Calibration of the VNA and the probes is done using the ISS-101-190 substrate for OSLT (open-short-load-through) termination, moving the reference plane from the VNA to the probes. S-parameter measurements are performed on an open and a shorted test structure embedded in the interposer. The obtained S-parameters will be used to extract the S-parameters of the interconnections obtained via the bumps using the OS (open-short) de-embedding method once a die is successfully bonded to the interposer [9].

III. Process Developments

A. Interposer design and production

Fig. 5 shows the flowchart of the proposed Flip-Chip process in which each colour represents a different step. The first step is the design and production of the interposer. The interposers serve as a redistribution layer for the connections of the die and are designed such that the DC and AC characteristics of the interposer and interposer-to-die interconnection can be extracted, but also the trade-off between bump density, yield and reliability can be investigated. This results in the

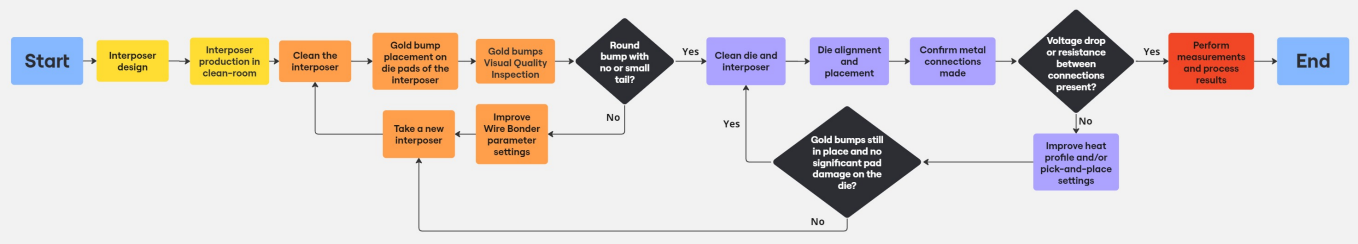

Fig. 5. Flowchart of the proposed Flip-Chip process showing the sequence of steps to follow for obtaining a desired result.

three designs shown in Fig. 6 and 7. The designs are made in Altium and the pad rings feature a 90μm pitch to match the pad organization of the 65nm Si-CMOS chips used for the assembly. Design 1 and 3 serve the same purpose i.e. to investigate the trade-off between the bump density, yield and reliability, however design 1 has a different pad-ring lay-out due to the first design being made for a different die than design 2 and 3 are. The pad-ring of design 1 feature a pad size of 70μm and 20μm spacing. For design 2 and 3 these are 60μm and 30μm respectively. Moreover, all designs have a trace width that matches the pad size. The purpose of design 2 is to investigate the interposer and interposer-to-die interconnection characteristics. This design contains 4 test structures, of which 2 are line structures and 2 are die structures. In both structure types, the top structures are terminated to ground, while the bottom structures are open circuit. The open line test structure is used to obtain the an equivalent RLC model of the transmission line. Furthermore, the top and bottom die structures are intended to be used as short and open termination of the transmission lines for the de-embedding process described in Section II. Ideally, the impedance of the transmission lines should, by design, exhibit a characteristic impedance of 50Ω. However, for the scope of this project the transmission line is not required to match the characteristic impedance due to the mathematical removal of the transmission lines from the complete structure in the de-embedding process. The reason for the transmission lines exhibiting the characteristic impedance is mainly to find the dimensions of the Coplanar Waveguide (CPWG). To achieve this, the program Qucs is used to find the width and spacing of the routing tracks. This resulted in a spacing 20μm for the CPWG in design 2, as can be seen from the results of the line-calculator in Fig. 8.

With the designs finished, samples are made in three batches in the TU/e clean-room. In the first batch Cr(15nm)/Au(100nm) electrodes were patterned on cleaned glass substrates by photolithography and followed by the lift-off process of the negative photoresist (AZ nLOF 2035). This batch contained 2 samples of each design and the gold metallization was obtained by means of sputtering. Unfortunately, the samples exhibited minor defects in the form of small random black spots. Moreover, the gold layer thickness of the first and second samples where 111 and 104nm, respectively. The metal tracks in the second batch were made of Ti(50nm)/Au(100nm) and contains 4 samples of each design: in 2 of these the metallization is obtained via sputtering, while the other 2 are

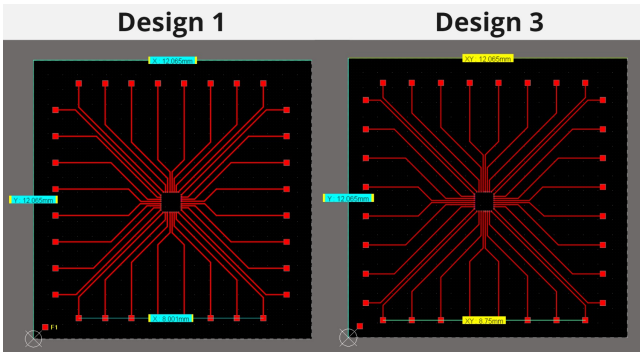

Fig. 6. Design 1 (left) for specific signal amplifier die and design 3 (right) for generic die including scale reference.

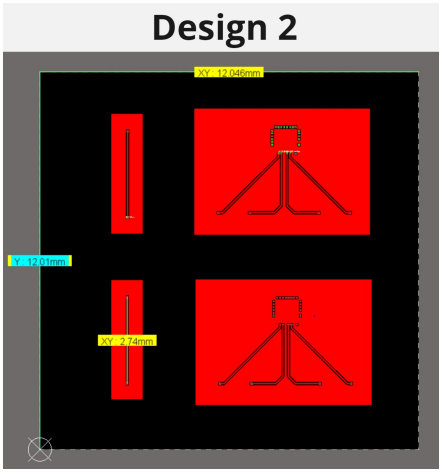

Fig. 7. Design 2 for generic die including scale reference.

obtained by evaporation. These sputtered samples contained fewer defects as production conditions where improved by using ultra-sonication and increasing the adhesion layer thickness. Finally, the tracks in the third batch are also made of Ti(50nm)/Au(100nm) and contains 2 samples in which the metallization is obtained by evaporation, which served as back-up samples. Fig. 9 shows what a sample looks like after production.

B. Bump placement

The second step of the proposed Flip-Chip process is the bump placement, shown in orange in Fig. 5. After many attempts of finding only inconsistent results with long tails, it was decided to discuss the consistency with Accelonix.

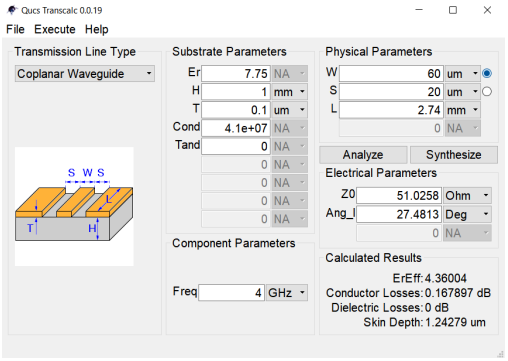

Fig. 8. Result for the spacing of the CPWG calculated in the line-calculator in Qucs.

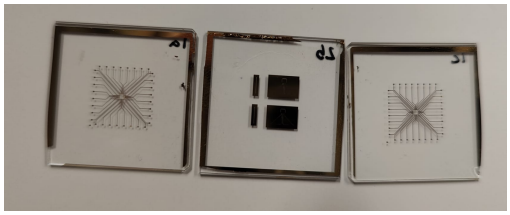

Fig. 9. Finished interposers ready for bump placement and testing.

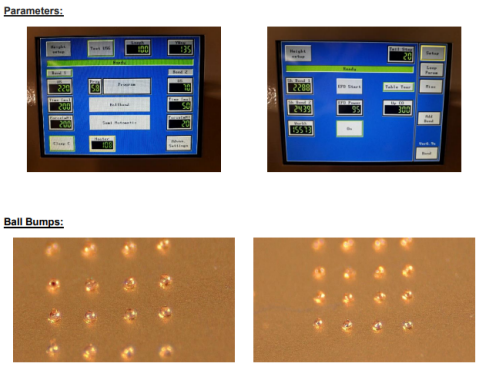

Fig. 10. Base settings and visual proof of high quality bumps on standard substrate of Accelonix.

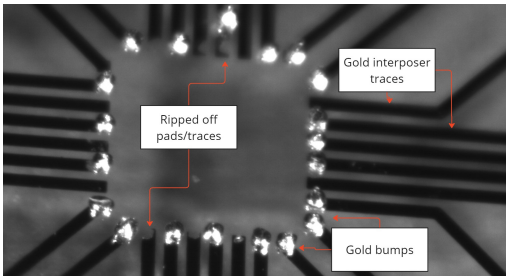

Fig. 11. Bump placement on gold evaporation sample of batch 2, yielding good bump quality but also containing ripped off traces.

Eventually, a base setting for the parameters was found. The bumps produced on their standard substrate yielded good visual results in terms of well-rounded bumps with no tail. These recommended base settings and visual proof are shown in Fig. 10.

Working with these settings for 25μm wire on design 1 of the first and second batch yielded good, but inconsistent results as the bumps often would not stick to the surface. However, when the same settings where applied to design 1 of an evaporation metallization sample of batch 2, it yielded more consistent and satisfactory results as can be seen in Fig. 11. Unfortunately, the excessive misalignment between the bump and the interposer pad, often lead to damages in the interposer pads as shown in Fig. 11. The Wire Bonder has no automatic way to ensure good alignment, making proper alignment highly susceptible to the skill of its operator. Although it was not possible to automate this, a workaround was found to improve alignment and make it less dependent on the operator's skill. When viewing the bumps through the camera of the setup in the Thorlabs application, a test area was used to place a bump. By placing a marker in the camera image, it is possible to use it as a target, enabling the operator to place the bumps in a more accurate way, and thus increasing the yield.

In terms of density, the wire diameter and EFO power determine the bump size and thus maximum die interconnection density. Bumps made with 25μm wire (Fig. 11) had a good reliability, but faced yield issues. When placing bumps on adjacent pads, the capillary might land on a neighbouring bump, coining it, or place the bump too far to the side, ripping off the pad. To address this, a 17μm gold wire was used, reducing bump size and thus preventing obstructions with neighbouring bumps due to the enlarged clearance. This change enabled bumps to be properly placed on a 90μm pitch size with a good quality of bumps. However, the capillary clogged more frequently and could only be unclogged by placing it upside-down and using USG to vibrate out the material through the large hole of the capillary, through which the wire is meant to be inserted. Several parameter adjustments, including reducing EFO and US power, were attempted but were unsuccessful in resolving the issue.

Although the bump quality is inspected visually, the size of the bump is very important in determining what the highest density could be. By writing a script in Matlab that applies circle detection to distinguish the bumps from the interposer and its traces, it not only automatically detects the bumps but also finds the diameter of the bumps (expressed in number of pixels). All that remains is to determine the conversion rate linking the edge size of a pixel to a metric value. This is done by taking a picture of a known length object and measuring the amount of pixels that spans the length of the object. This object was a 2x2 mm die and was measured in the Thorlabs camera software to be 1166 pixels in length. In (1) CR is the conversion rate in μm per pixel, W is the known width of the reference object and N_{px} is the number of pixels that span the known width. This resulted in a conversion rate of 1.715μm/px. Using this conversion rate, it was determined that for the 25μm gold wire, the bumps were in the range of 67-78μm diameter, which was expected as it is around 3 times the wire diameter [10].

$$CR = \frac{W}{N_{px}} = \frac{2000}{1166} \approx 1.715 \mu m/px \quad (1)$$

Assuming that the bumps are placed perfectly in the centre of the 70μm pads, in the worst case scenario of the bumps being 78μm it has 4μm overhang past the pad on any of its sides, leaving only 12μm spacing between adjacent bumps. In a practical sense, it was determined not to be enough space. As the 25μm wire yielded the best results, working with this wire size requires a larger pitch size. Increasing the spacing from 20 to 30μm or pad size from 70 to 80μm and thus increasing the pitch to 100μm would allow for a larger space to operate in and thus increase the yield. Depending on the requirements, it should be decided to either increase the spacing or pad size or even consider moving to 110μm pitch size to further increase the yield as this would increase the reliability of the process. As the pad pitch size was a fixed parameter in this project, it could not be adjusted for obtaining results at a different size.

After determining the need for a larger pitch size, the bumps were placed on design 2 of an evaporation metallization sample of batch 2. Unfortunately, the bumps where no longer well-rounded and instead had a cone-like shape due to an increased amount of gold surface area that is the large GND plane in the die test structures of design 2. The cone-like bumps are unlikely to make reliable interposer-to-die interconnections due to their shape. Although a significant amount of time was spent to find the right parameter settings for large gold surface area bump placement, the time constraints of the project were too narrow to obtain them.

C. Die placement

The third stage of the process is die placement. As discussed in the previous subsection, the 17μm wire had practical problems, but nonetheless it was possible to place bumps on all of the pads of design 1 of an evaporation sample. Thanks to the beam-splitter, it was possible to achieve a placement with a linear misalignment of less than 5μm in any direction. However, a critical step in the die placement is the choice of a suitable heat profile for the thermal compression bonding of the interposer (equipped with bumps) with the die. The heat profiles mentioned in [4] and [6] were attempted to be reproduced, but unfortunately due to a malfunction of the Dr. Tresky T-5300 workbench heater, it was not possible to achieve any temperature higher then 270 degrees. Despite this limitation, by using the heat profile reported in Fig. 12, a semi-successful bonding could still be achieved. If a metal connection is successfully made, a standard multimeter can be used confirm this, as the die will have protection diodes placed at each pad of the die. These diodes will exhibit a voltage drop between the probes and thus a significant amount of resistance. In case of a short this resistance will drop to values less than 1Ω. By using the aforementioned multimeter, a forward voltage drop of 107 mV was measured between IO and GND pins, measured by placing the handheld probes on the large pads. When measuring between two of the IO pins, a resistance of 69Ω was measured, thus confirming that metal connections are made with the die.

Unfortunately, the next day the die had broken off, indicating the interconnections were weak and thus not reliable. It is, however, worth noting that the die was a 2x2 mm, 65nm Si-CMOS chip containing 3 different designs (and thus pad-rings)

	Semi-successful attempt heat profile settings			**Heating profile settings recommended by Accelonix**	
	Stage 1	Stage 2	Stage 3	Stage 1	Stage 2
Segment type	Heat	Heat	Cooling	Heat	Cool
Start trigger	-	Wait for Touchdown	-	Wait for Touchdown	-
Start delay [ms]	0	0	0	0	0
Duration [ms]	40000	30000	40000	60000	0
Ramp/Slope [C/s]	10	10	-	30	-
Target temperature [C]	220	270	40	300	40
Wait for completion	Not selected	Not selected	Not selected	Not selected	Selected
Wait target	-	-	-	-	-
Logic	-	-	-	-	SKIP_EXEC
	Placement settings			**Placement settings**	
Place force [g]	600			500	
Place duration [ms]	40000			30000	

Fig. 12. The heat profile settings of a semi-successful die placement attempt and later discussed but untested recommendations from Accelonix.

of which only 1 was bonded to the interposer. Consequently, only about 1/4 of the surface area of the die had connection with the bumps, leaving the other 3/4 of the surface area as overhang. The mechanical stress induced by this asymmetry is likely to be one of the contributing factors to the delamination of the die.

D. Measurement results

After production, the primary focus is to evaluate the interposer's characteristics by determining the R (resistance), L (inductance), C (capacitance), and G (conductance) of the transmission line per unit length (μm). These values allow for modeling different interposer designs using the same process. Additionally, the sheet resistance (R_{sh}) and trace resistivity (ρ_{trace}) are assessed to compare production methods. After calibrating the VNA (see Section II), S-parameters are measured at four distances: 25, 100, 500, and 2740μm (the full length of the transmission line in design 2). This procedure is performed four times: twice for samples from batches 1 and 2 (sputtering technique) and twice for samples from batch 2 (evaporation technique). The S-parameters are processed in Matlab to obtain R_{sh} and ρ_{trace}. As the first S-parameter value of each measurement is at 10 MHz, (2) shows that this frequency is low enough to model the circuit with a lumped element rather than a transmission line, as the wavelength of the propagating signal (λ) is much larger than the length of the traces: in (2) where λ_{vacuum} is the wavelength of an electrical signal propagating in a vacuum, $\epsilon_{r,glass}$ the relative permittivity of the glass substrate, c the speed of light and f the frequency of the signal.

$$\lambda = \frac{\lambda_{vacuum}}{\sqrt{\epsilon_{r,glass}}} = \frac{c}{f\sqrt{\epsilon_{r,glass}}} = \frac{3 \cdot 10^8}{10^7\sqrt{7.75}} = 10.78[m] \quad (2)$$

By applying (3) to the first entry of each measurement (where Z_0 is the normalization impedance of 50Ω and $S_{1,1}$ is a specific entry in the measured S-parameters at 10 MHz), the line impedance is determined. A linear fit of the real part of the line impedance (the line resistance) is performed to estimate the contact resistance and sheet resistance (R_{sh}) with minimal error. Fig. 13 shows the plot of measured line resistances and its linear fit for normalized length, demonstrating that the linear fit accurately reproduces R_{sh}. The trace resistivity (ρ_{trace}) is calculated using (4), with Z_{line} as the line impedance, T_{trace} as the gold layer thickness, W_{trace} as the trace width, and l_{trace} as the line length.

	$R_{sh}[\Omega/square]$	$\rho_{trace}[S/m]$
Evaporation (batch 2)	0.3797	$3.9858 \cdot 10^{-8}$
Evaporation (batch 2)	0.3491	$3.6363 \cdot 10^{-8}$
Sputtering (batch 1)	0.4796	$5.0230 \cdot 10^{-8}$
Sputtering (batch 2)	0.4812	$5.0071 \cdot 10^{-8}$

TABLE I

RESULTS TABLE FOR INTERPOSER CHARACTERISTICS OF R_{sh} AND ρ_{trace} OF 2 EVAPORATION AND SPUTTERING METALLIZATION SAMPLES.

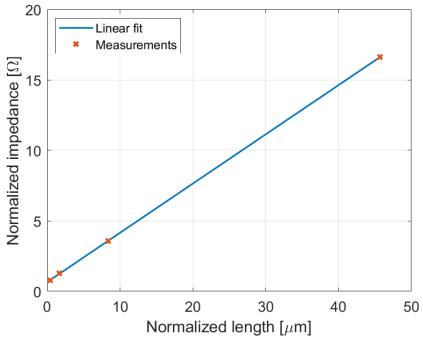

Fig. 13. Plot of the measured resistances normalized to the trace width against the normalized length of the measurement

$$Z_{line} = Z_0 \frac{1 + S_{1,1}}{1 - S_{1,1}} - Z_0 \tag{3}$$

$$\rho_{trace} = \frac{Z_{line} \cdot T_{trace} \cdot W_{trace}}{l_{trace}} \tag{4}$$

The resistivity of pure gold (ρ_g) is $2.041 \cdot 10^{-8}$ S/m. The evaporation metallization samples have resistivity factors of 1.953 and 1.782, while sputtering metallization samples have factors of 2.461 and 2.454. Higher resistivity results in higher resistance, making evaporation metallization preferable for both resistivity and bump placement. It is concluded that the increased resistivity in sputtering metallization is due to less densely packed gold with more impurities, such as air pockets.

Finally, a Matlab script based on the method in [5] processes the S-parameter measurements into RLCG values per μm over the measured frequency range. Fig. 14 shows these values plotted from 10 MHz to 10 GHz at 1 GHz intervals for an evaporation metallization sample. The plots of other samples exhibit similar behaviour within the same range of values.

IV. CONCLUSION

Despite not successfully completing the process due to time constraints, a sequence of steps has been established for the Flip-Chip process. The evaporation production method for the metallization of the interposer is preferred over sputtering because it leads to a more consistent bump placement and reduced resistivity. During bump placement, the obtained base parameter settings yielded high-quality bumps on small gold surface areas but poor quality on larger areas. The process with the 25μm gold wire was more reliable than the process with the 17μm wire, which had clogging issues. A pitch size of 90μm was impractical for the 25μm gold wire and increasing it to 100μm or even 110μm would greatly improve yield. Moreover, a semi-successful heat profile was found

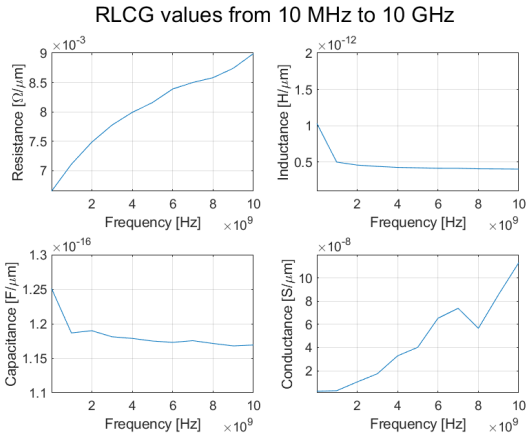

Fig. 14. Resistance, inductance, capacitance and conductivity of an evaporation metallization sample per μ m of the open line test structure of design 2.

for die placement, requiring further improvement for greater consistency and reliability.

Setting up the process required a significant amount of time, leaving some issues unfinished within the time frame set for the project. The issues that still require investigation in future research are: 1) optimizing parameter settings for consistent, well-rounded bumps on large gold surface areas 2) improving the heat profile and die placement settings 3) investigating the AC characteristics of design 2 and 4) exploring the DC and AC characteristics of the bumps. The improvements and issues of the production steps are recommended to be worked out in collaboration with Accelonix.

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