Microsyst Technol (2016) 22:337–347
DOI 10.1007/s00542-014-2390-6

TECHNICAL PAPER

High frequency characterization and analysis of through silicon vias and coplanar waveguides for silicon interposer

Huijuan Wang · Xiaoli Ren · Jing Zhou · Cheng Pang · Chongsheng Song · Fengwei Dai · Kai Xue · Feng Jiang · Daquan Yu · Lixi Wan

Received: 18 November 2014 / Accepted: 3 December 2014 / Published online: 28 December 2014

Abstract A silicon interposer test vehicle with through silicon vias (TSVs) is evaluated under radio frequency (RF) application from DC to 10 GHz. TSVs with 30 μm diameter and 150 μm height were fabricated with one layer RDL of 20 μm line width. A group of coplanar waveguides (CPW) are designed and tested to analyze the electrical performance of the interposer under high frequency in both the time and frequency domains. Results show that the interposer cannot be used above 1 GHz because of excessive losses and high reflections. Based on the analysis of the test results and simulation results for different CPW (coplanar waveguides) structures, it is concluded that the poor performance was mainly caused by accumulated space-charge at the SiO_2–Si interface and impedance mismatch of transmission lines. Solutions that were implemented included enhancing the thickness of the SiO_2 insulation layer between the metal and silicon substrate and improving the design of the transmission line. Implementation of these changes led acceptable interposer performance up to 10 GHz.

H. Wang (✉) · J. Zhou · C. Song · F. Dai · D. Yu · L. Wan
Institute of Microelectronics of Chinese Academy of Sciences, No. 3, Beitucheng West Road, Chaoyang District, Beijing 100029, China
e-mail: wanghuijuan@ime.ac.cn

D. Yu
e-mail: yudaquan@ime.ac.cn

H. Wang · X. Ren · C. Pang · C. Song · F. Dai · K. Xue · F. Jiang
National Center for Advanced Packaging (NCAP China), Building D1, 200 Linghu Boulevard, Wuxi 214135, Jiangsu, China

1 Introduction

Rapidly evolving electronic and computing systems strive to achieve higher functionality at higher bandwidth in a denser, higher performance, integrated package. To address these drivers, various forms of three-dimensional integration have emerged. System-in-package (SiP) based on a silicon carrier or interposer is a fast emerging technology that offers system design flexibility and integration of heterogeneous technologies (Zhou et al. 2012). The 2.5D/3D silicon interposer with TSVs vertical connectivity and wiring layers has been proposed and is being applied to a growing number of electronic packaging products because of its unique processing capabilities and demonstrably improved electrical performance (Hui 2009; Chen et al. 2011; Li et al. 2012) such as lower parasitic effects at higher frequencies, denser circuits, reduced form factor and power consumption, and heterogeneous systems and die integration such as environmental and optical sensors, GPS, operating system, wireless access, flash memory, and entertainment system.

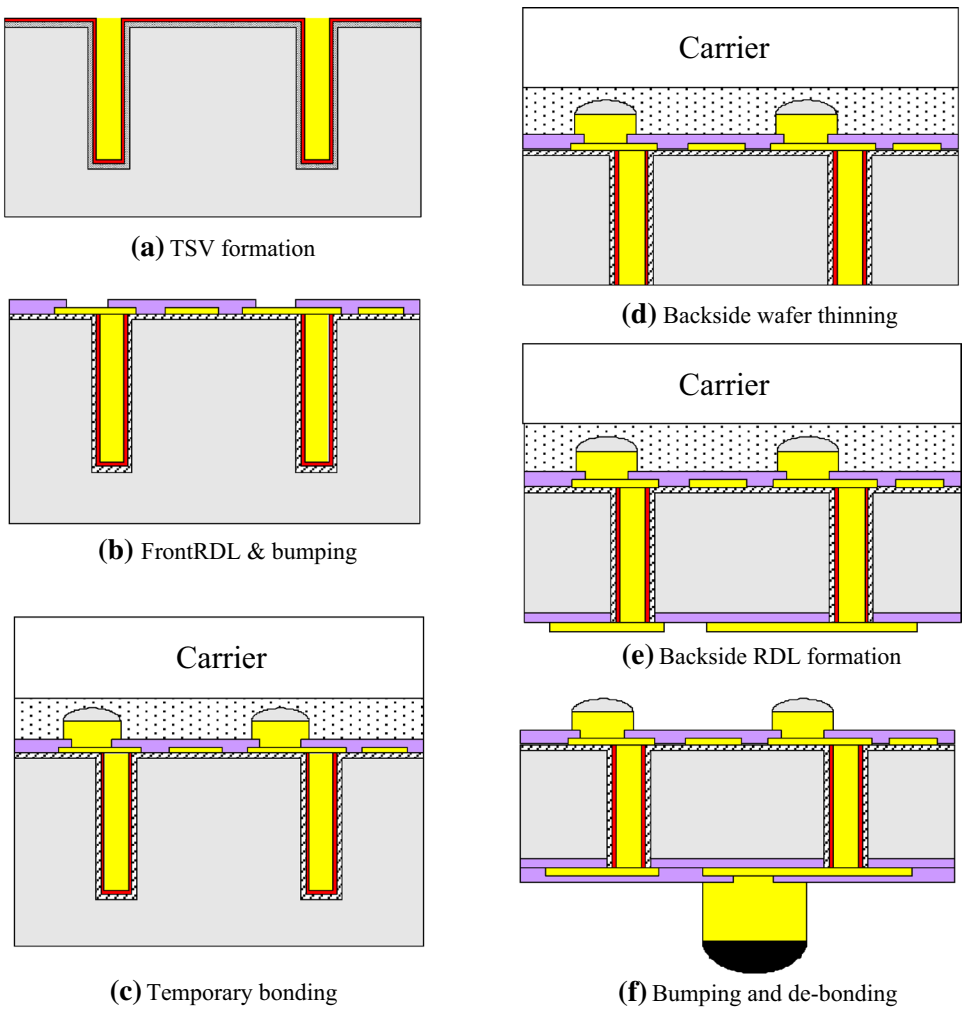
However, silicon might not be the most ideal platform for high speed and high frequency applications since interconnections on the silicon substrate suffer from substrate losses caused the interaction of the electric and magnetic fields with mobile charge in the silicon substrate. In an environment in which thousands of interconnections are compactly packed with fine pitch on a lossy silicon substrate may cause crosstalk (Chen et al. 2011). In particular, since the operating frequency of RF devices is increasing, it is necessary to pay more attention to the high frequency performance of the signal transmission path both on and through the silicon interposer (Li et al. 2012). According to these requirements, it is necessary to evaluate the system's electrical behavior as a function of frequency.

However, only a few papers have described the electrical behavior of TSVs at RF frequencies (Kim et al. 2009; Kato et al. 2009).

Specifically designed structures, their analysis and experimental verification are effective ways to guide product integration on a TSV interposer platform, especially at RF frequencies. In this paper, a TSV interposer test platform with TSVs, RDL (redistribution layers) transmission lines and coplanar waveguides. The platform is designed to test the eye diagram in the time domain, from which it is learned that the transmission line model tends to overestimate the Bit Error Rate (BER). The platform is also designed to tests the CPW structures of different lengths as a function of frequency, where it is found that the CPW performance is unsatisfactory for frequencies greater than 1 GHz. Modeling and simulations using 3D EM software tools spotlighted two main causes for the unacceptable high frequency performance of the silicon interposer test structures. Substrate loss and impedance mismatch between CPW and TSV and capture pad. Test structures with improved designs were fabricated and tested. Measured S-parameter results suggest that the transmission lines, pads and TSVs on the silicon interposer platform perform adequately at frequencies up to 10 GHz.

2 TSV interposer fabrication and structure

The TSV interposer was fabricated on 8-inch silicon wafers by a back-end of the line semiconductor process. Figure 1 sketches the typical process which contains the following main steps: Etch silicon to form 30 μm diameter and 150 μm deep TSVs; apply insulation and barrier layers to the TSV wall; filled the vias by plating cooper. After TSV formation, front side RDL & bump fabrication, the wafer is bonded to a carrier or handler wafer which supports the wafer during the thinning and backside TSV reveal process. This is followed by the formation of RDL and bumps on the backside. Finally the interposer wafer will be de-bonded from the carrier wafer and diced for 2.5D system assembly. The fabrication of a TSV interposer can be divided into four process modules: TSV formation, RDL and bumping, TSV revealing,



(a) TSV formation

(b) FrontRDL & bumping

(c) Temporary bonding

(d) Backside wafer thinning

(e) Backside RDL formation

(f) Bumping and de-bonding

Fig. 1 Typical fabrication steps for a 2.5D TSV interposer

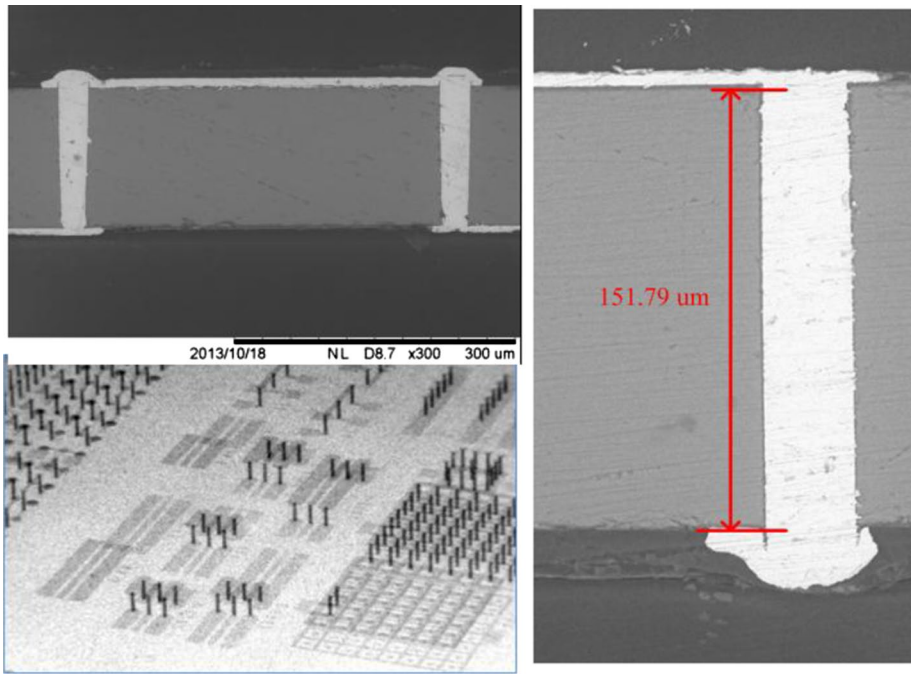


Fig. 2 The cross sections and X-ray micrographs of the TSV interposer. *Left top* interposer cross section showing *top*/*bottom* RDL between two TSVs; *left bottom* microfocus X-ray transmission image of the electrical test area; *right* cross section of a single TSV

Table 1 Summary of interposer design parameters

Parameters	Value
TSV diameter (D)	30 μm
TSV height (H)	150 μm
RDL metal and thickness	Cu, 4 μm
Insulation layer and thickness	TEOS SiO_2, 1 μm
RDL spacing/min	10 μm/10 μm
Back RDL spacing	20 μm
Back side insulator	PBO polymer

and bonding/de-bonding, respectively. The TSV interposer includes RDLs, TSVs, micro-bumps, and copper pillars.

The manufacturing processes for TSVs and two redistribution layers (one front layer and one back layer) were developed based on silicon BEOL processes. The structure of the fabricated interposer is shown in Fig. 2, while the geometrical parameters are summarized in Table 1. We focus on the electrical test area of the interposer, on which there are a series of CPW structures dedicated to high frequency testing.

3 CPW structure design and test

CPW transmission lines on different layers with different structures and transmission paths to TSVs were designed and their electrical properties were investigated using 3D EM simulation tools and later verified by S-parameter measurements. The S-parameters of the signal transmission paths were extracted by a Vector Network Analyzer (VNA) and 200 μm pitch micro-probes. In Fig. 3 are shown a sketch of the CPW structures under test. The width of signal line "S" is 100 μm, the width of ground line "G" is 180 μm, the distance between signal and ground is 60 μm, the silicon substrate thickness "H" is 150 μm. The thickness "h" of the SiO_2 isolation layer on silicon is 1 μm. If losses are ignored the CPW characteristic impedances of the transmission lines is about 50 Ω.

3.1 Characterization of the CPW–TSV link

The behavior of interposer channel links, consisting of CPWs and TSVs, at high frequency is evaluated by examining the eye diagram characteristics. Structures similar to those shown in Fig. 3 were probed with 200 μm pith GSG probes and a TEK error analyzer. The length of the CPW line was 1,200 μm. Figure 3a, d showed images of a typical test structures. The front and back RDL line lengths are both 400 μm are connected by two TSVs. Figure 4 shows the eye diagram for the electrical link consisting of one 1,200 μm CPW with two TSVs measured at 1 Gb/s, 3 Gb/s, 5 Gb/s and 7.5 Gb/s. In Fig. 4 (a), at 1 Gb/s the eye diagram is symmetrical and open. However the open area diminishes progressively with increasing data rate and the eye is essentially closed by 5 Gb/s. There are generally two reasons for eye diagram degradation: one is impedance mismatch caused by excessive reflections; the other is propagation loss. Impedance mismatch can cause signal dithering, which is not observed here. In Fig. 4 there is no clear jitter ripple as would be caused by an impedance mismatch.

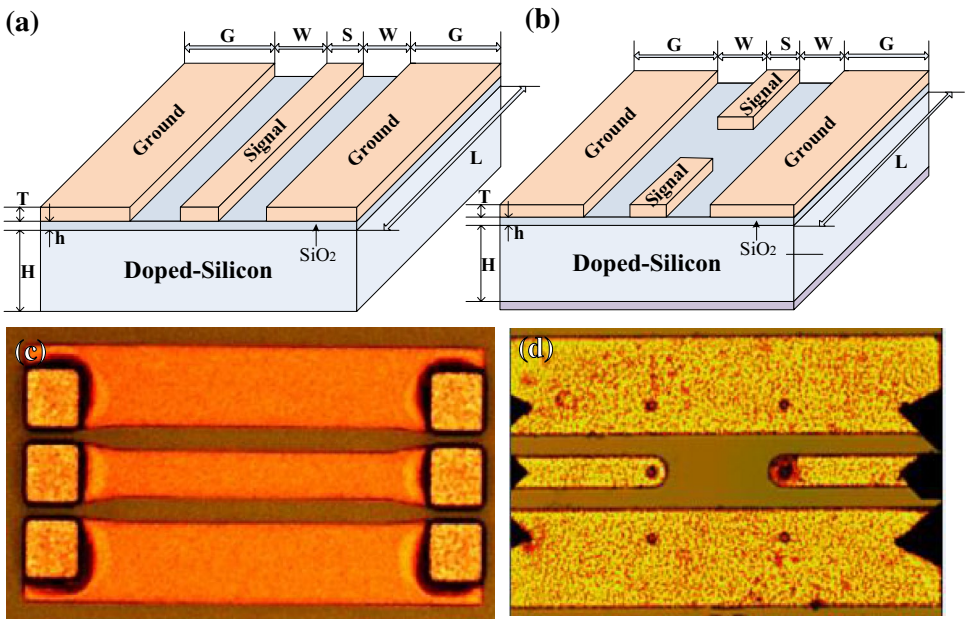


Fig. 3 Sketches of the cross section and pictures of the CPW structure under test. **a**, **c** The CPW structure on the front of interposer. **b**, **d** The CPW structure with TSVs

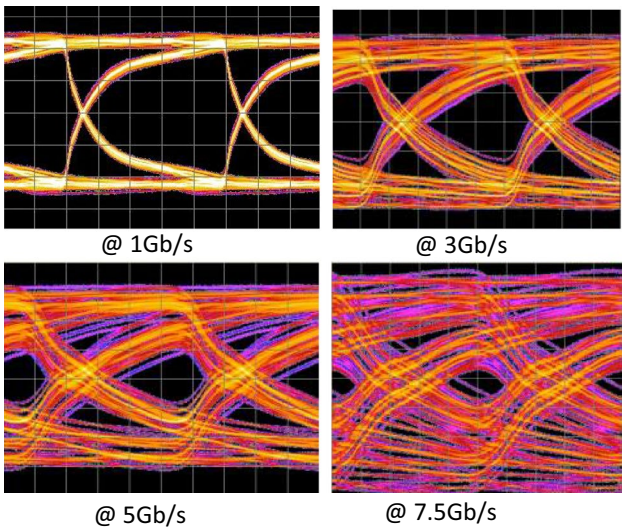


Fig. 4 Eye diagram for a 1,200 μm CPW electrical link with two TSVs as a function of data rate. **a** Insertion loss from 0 to 40 GHz, **b** return loss from 0 to 40 GHz, **c** S12 from 0 to 3 GHz

3.2 CPW without TSV in frequency domain

To extract the S-parameters of the electrical link in the frequency domain, we used a 40 GHz Vector Network Analyzer (VNA) with 200 μm pitch micro probes. The electrical link with TSVs is more complex and requires de-embedding algorithms to extract the S-parameters for each structure. We first test the CPW structure without TSV to obtain propagation loss. Figure 5 summarizes S-parameter test results for various CPW lengths. Figure 5a summarizes the measured S21 for CPW lengths of 800, 1,000, 1,200, 1,600 and 1,800 μm. The propagation loss (S21) of the CPW is seen to be substantial with a large reflection (S11) contribution. The insertion loss (S21) is less than −3 dB for frequencies less than 2 GHz, however from 0.2 to 40 GHz, the return loss (S11) is above than −15 dB. These results indicate that this silicon substrate is not suitable for RF applications.

In Fig. 5b, we can observe a each curve displays a local minimum, indicated by the dark point on the curve. This depth of the local minimum decreased as the length of the signal line increases. The behavior is similar to that of the resonance frequency of microstrip line, which is attributed to reflections due to impedance mismatch. From the expression for the impedance or a transmission line, shown as expressions (1–3) where R is the resistance, G is the conductance, L the inductance, C the capacitance and Ω is the angular frequency (Bogatin 2005). In Eq. (3) S is the area of the transmission line in contact with the insulator and L is the insulator thickness. The loss tangent is denoted by tan(δ). We can see that: the larger the relative dielectric permittivity of the insulator (in this case, the SiO_2 layer) and the thinner its thickness, the greater the capacitance C and the greater the conductance G, which leads to a smaller impedance, Z. It is therefore possible that process variations may contribute, in part, to an out-of-design transmission line impedance. However, other factors such as out-of-spec substrate bulk resistivity may also contribute.

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{1}$$

$$G = \omega \cdot \tan(\delta) \cdot C \tag{2}$$

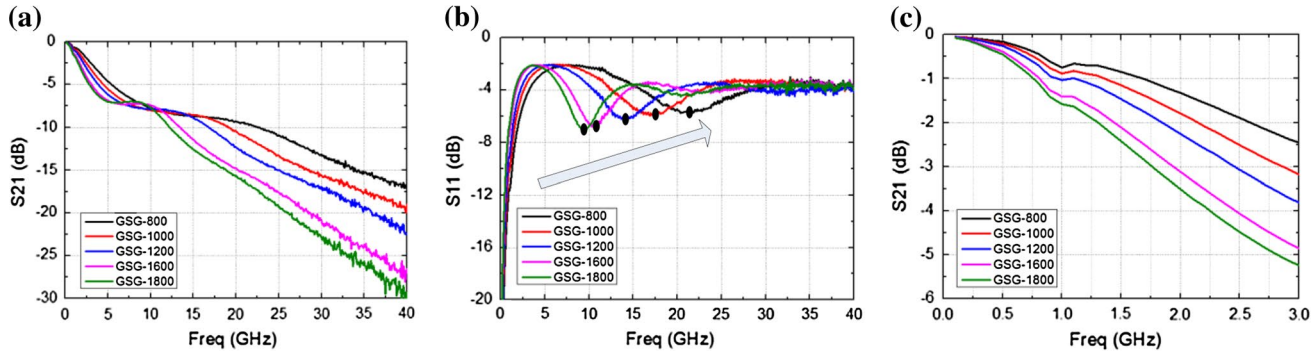


Fig. 5 Measured S parameters for various CPW lengths in the absence of TSVs. **a** Insertion loss from 0 to 40 GHz; **b** return loss from 0 to 40 GHz; **c** S12 from 0 to 3 GHz

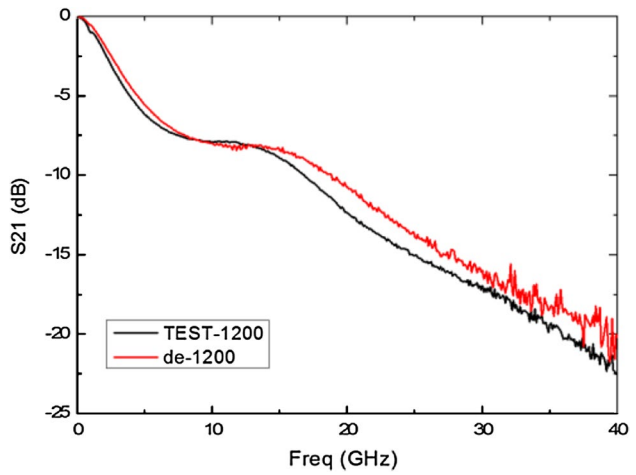


Fig. 6 Comparison of measured and de-embedded scattering coefficient

$$C = \varepsilon_0 \varepsilon_r \cdot \frac{S}{L} \tag{3}$$

3.3 De-embedding the test results

In order to investigate the effects of the GSG probe on the measurements we apply a de-embedding procedure using ADS software. It first make accurate simulation based models under test with only remaining test part, then the ADS can subtract the pad effects. Figure 6 shows the measured insertion loss S21 (black trace) for a 1,200 μm long CPW transmission line and the de-embedded (red trace) S21. The two curves are nearly the same over the entire frequency range 0–40 GHz. These results indicate that the observed large propagation loss is not caused by the test methodology.

According to the formation of a strong interfacial polarization at the Si–SiO_2 interface, referred to as the Wagner effect, a thin space-charge layer is firmed at the SiO_2–Si interface at lower frequencies (Asegawa et al. 1971; Hasegawa et al. 1971; Prodromakis et al. 2010). Influenced by this effect, the transmission line and TSVs are influenced by the onset of a slow-wave mode, which is characterized by very slow signal phase velocity. These accumulated space-charges act like a lossy ground plane that, at low frequencies, looks like an insulator with a larger relative permittivity. The frequency range over which the slow wave propagation mode is active, depends on the resistivity of the silicon substrate and the structure of transmission line. In our interposer structures, fabricated on a silicon substrate with resistivity between 1 and 10 Ω-cm, the slow mode is expected to be active between about 1 and 10 GHz (Ndip et al. 2011). The thin dielectric layer also increase the capacitance C which eventually lead to the smaller Z. That's another possible reason for the test results. We will investigate this second scenario leading to high insertion loss further in the next paragraph.

4 3D model analysis for interposer design

In order to analyze the test results in section III and to guide interposer design for achieving high frequency operation, we set up a 3D model for analysis using HFSS high frequency EM simulation, as shown in Fig. 7. The model structure is shown in Fig. 3 with design parameters summarized in Table 1. The red lines in Fig. 7 represent the signal lines of GSG CPW structures (refer to Fig. 6). We will compare the simulated S parameters with de-embedded measurements.

4.1 The influence by silicon substrate

The resistivity of the starting silicon has a strong influence on the characteristics of the CPW structure in interposer. The black curve labeled "TEST" in Fig. 7 represents the measured S parameters for our sample whose bulk resistivity and type is unknown other than it is within the customary range for CMOS substrates. In the HFSS

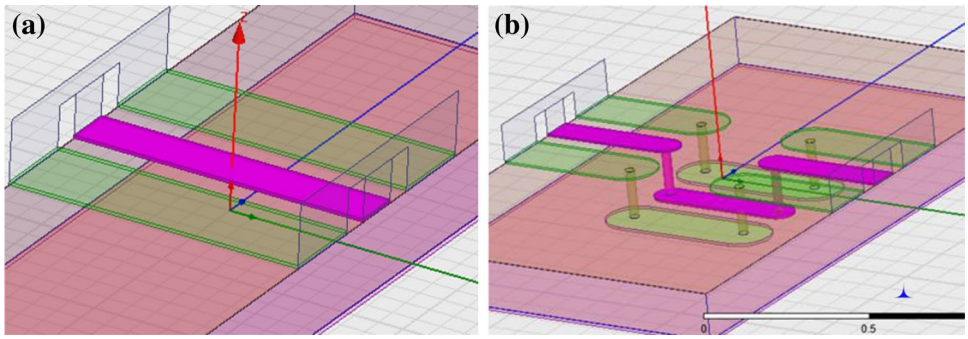


Fig. 7 The 3D HFSS model for the CPW structure (**b**) with and (**a**) without TSVs. **a** Straight CPW; **b** CPW with TSVs

Table 2 Silicon substrate properties used in the HFSS simulation

Silicon-type	Dielectric constant of silicon	Loss tangent of silicon substrate	Silicon conductivity (s/m)	The thickness of dielectric layer (μm)
Silicon1	11.9	0.02	3	1.5
Silicon2	12.3	1.4	8.3	1.5
Silicon3	12.3	2.2	13.5	1.5

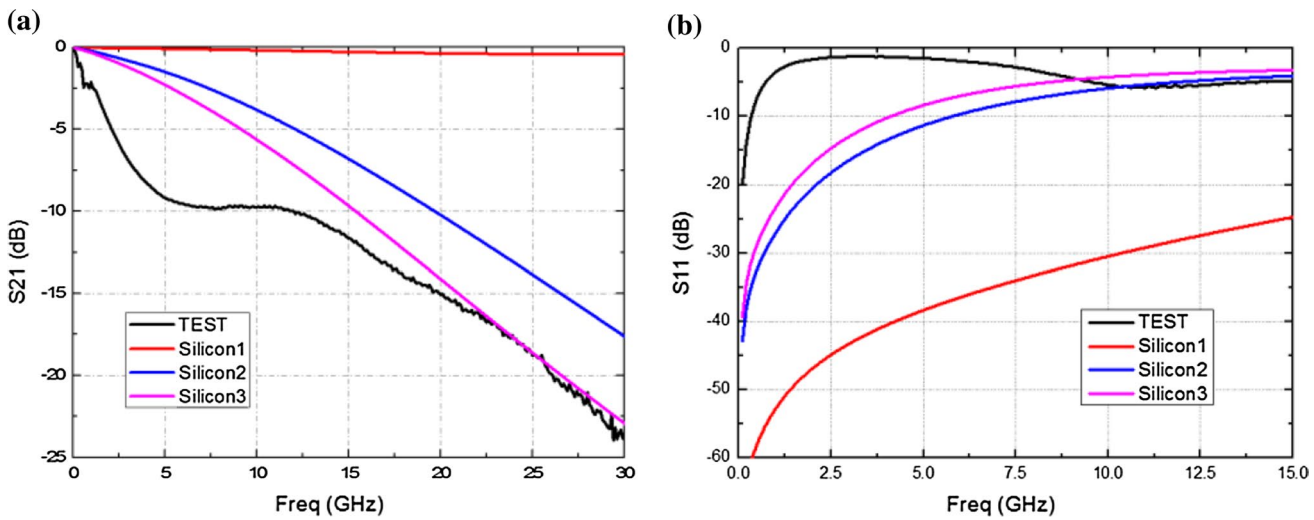


Fig. 8 Comparison of measured and HFSS simulated S parameters for the CPW structure (no TSVs) on different silicon substrates. **a** Insertion loss, **b** return loss

model, the length of the GSG CPW is 1,000 μm and the insulating SiO_2 layer is 1 μm thick. It also simulated the same test structure with the simulation was done for three different silicon conductivities, summarized in Table 2, along with other relevant substrate parameters. Simulated S-parameter results are comparison with the measured and de-embedded values for our sample and are shown in Fig. 8. Clearly, substrates with the lower resistivity show the greater propagation loss. For frequencies greater than 20 GHz, the model insertion loss fits with the simulation curve for a silicon conductivity of 13.5 S/m. The return loss also fits well with data above 10 GHz. The large insertion loss up to 20 GHz is consistent with the slow-wave model based on the Wagner effect (Ndip et al. 2011). Figure 8 suggests that a transmission line on a substrate, having conductivity typical of CMOS Si, undergoes a slow-wave transition when signal frequencies fall below about 10 GHz. On the other hand, the range 10–20 GHz is representative of a transition from slow-wave propagation modes to the dielectric, quasi-TEM propagation mode which results in insertion losses that are more consistent with HFSS model predictions. From Fig. 8 we can also infer that the conductivity of our tested sample is about 13.5 S/m (7.4 Ω-cm) with a loss tangent of 2.2.

The resistivity of silicon has a significant influence on the characteristic of the CPW structure. The black curve

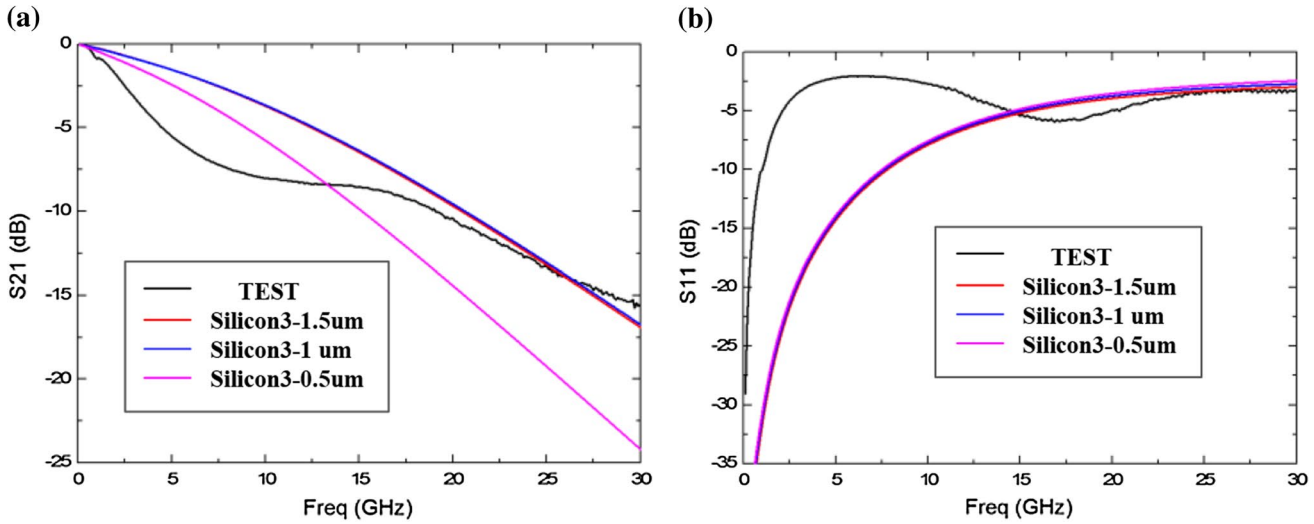


Fig. 9 Measured and simulated S parameters of the CPW structure with different thickness of oxidation. **a** Insertion loss, **b** return loss

marked "TEST" in Fig. 8 are the measured and de-embedded S parameters for the sample with unknown conductivity. A 1,000 μm long CPW signal line was measured. The same CPW structure was simulated on a silicon substrate with three different conductivities. Table 2 shows the material properties for the three substrates and Fig. 8 compares the results of the simulation and test (Ismail et al. 2006). It is found that the smaller the resistivity, the greater the CPW loss. When the frequency is above 20 GHz, the simulated insertion loss fits the data reasonably well for a silicon conductivity of 13.5 S/m. The return loss also matches closely the higher conductivity substrate, Silicon3 and Silicon2, above 10 GHz. Large insertion losses up to 20 GHz are consistent with the Wagner effect. Within the context of the Wagner effect it can be said that the transmission line undergoes a transition to the slow-wave propagation modes for frequencies less than 10 GHz, while between 10 and 20 GHz CPW propagation modes transition from slow-wave modes to dielectric quasi-TEM propagation modes with essentially linear insertion loss (Asegawa et al. 1971; Hasegawa et al. 1971; Prodromakis et al. 2010). From Fig. 8 we also can infer that the conductivity of the measured substrate is about 13.5S/m; a value which is used for subsequent simulations in the sections below.

4.2 The influence by silicon oxide

We also simulated the same test structure on a Silicon3 substrate (see Table 2) but with three different thicknesses of the oxidation layer between the conductor and the silicon substrate. The CPW line under test and simulated is 1000 μm long. A comparison between measured and simulated S parameters is shown in Fig. 9. Clearly, if the SiO_2 thickness is less than 1 μm, the insertion loss increases dramatically. In the simulation model the oxidation layer is treated as an ideal insulator with no interface charges. However, CPW magnetic and electric fields still interact with mobile charges in the Si substrate and an MOS capacitance is still present at the SiO_2–Si interface and is frequency dependent. Based on Fig. 9, the fabrication process will use a layer of silicon dioxide of thickness 1 μm or greater. However, the SiO_2 thickness along the wall depth, in some places, will be unavoidably thinner than 1 μm as a as a result of the of the deposition process.

4.3 The influence by Wagner effect

In order to compare the performance of the transmission line on the surface of the interposer with and without TSVs, the GSG CPW structures are designed to have the same 1,200 μm total length for the signal line. The S11 and S21 parameters are simulated and measured up to 40 GHz with results shown in Fig. 10.

In Fig. 10, TEST-1200 represents the test result for a CPW without TSV of length 1,200 μm, while SIM-1200 shows the corresponding simulation results. TEST-1444 represents the test result for a CPW with TSV but retaining a total length of 1,200 μm (400 μm front line, 400 μm back line and 400 μm front line), while SIM-1444 shows the corresponding simulation results. The green inserts in Fig. 10 show the layouts of these two structures. As can be seen, the structure with TSVs suffer a drastic loss (−16 dB) at 5 GHz. This loss may be caused by the Si–SiO_2 interface and an enhanced Wagner effect. Above 10 GHz, the difference between the two structures remains almost constant, and we can extract the actual TSV loss. We find that

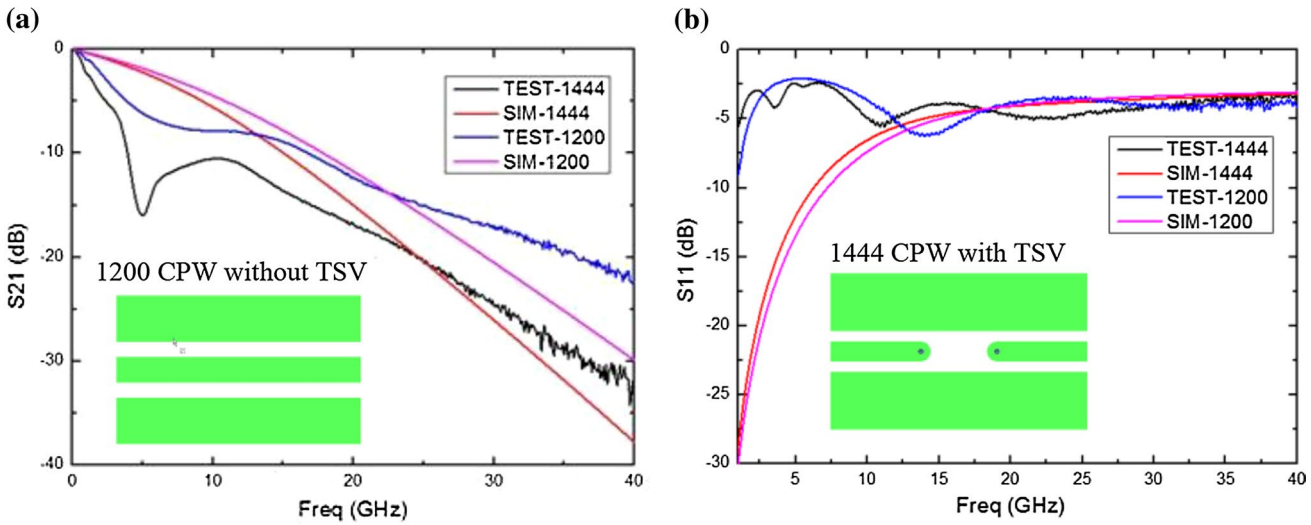


Fig. 10 Measured and simulated S parameters of the same length GSG-CPW structure with and without TSVs. **a** Insertion loss, **b** return loss

between 10 and 15 GHz the added propagation loss of two TSVs between −3 and −5 dB. From Fig. 10b, reflection loss is seen to trend toward −5 dB above 10 GHz. It should be noted that the HFSS simulator is not designed to take the Wagner effect into account.

4.4 The detail parasitical model for test structure

To investigate the characteristics of the CPW structure at lower frequencies up to 5 GHz, a circuit model for 1,000 μm long CPW structure is proposed, as shown in Fig. 11a, in which the oxide capacitance is denoted as "C1". The "R2" and "C2" represent substrate resistance and capacitance, respectively. "R1" and "L1" represent metal resistance and inductance, and coupling capacitance "C3" is between signal and ground. By tuning the value of the elements in the circuit, we can match the measured S parameters. Figure 11b, c compare the circuit model results to the measured results, thus demonstrating that the circuit model can make a good to the physical model. From the circuit model, it is clear that the parasitic capacitance of the CPW is large at lower frequencies. It extracted characteristic impedances of the 1,000 μm CPW line is about 105 Ω, which is much bigger than was calculated in the original design. These results further illustrate the problem of impedance mismatch.

In light of the above analysis we can venture certain conclusions: (1) at lower frequencies, the Wagner effect leads to a larger parasitic capacitance; (2) wafer with high conductivity cause excessive propagation loss. (3) The design of test structure is not reasonable for impedance match; (4) dielectric insulator may be too thin in places, especially on sidewalls near the bottom of the TSVs. The minimum insulator thickness on the sidewall should be greater than 1 μm and the Si substrate resistivity should be greater than 30 Ω-cm. Better results should be obtained by decreasing the parasitic capacitance between transmission lines and the substrate by increasing the insulator thickness. In general, a 1–2 μm thick SiO_2 layer or a thicker polymer insulator should substantially decrease the parasitic capacitance. Increasing the thickness of the transmission line to about 8 μm helps a little to reduce resistance line width and line separation should be used to bring the line impedance close to 50 Ω.

5 Testing and verification

The remedies and design improvements suggested above were implemented in a new fabrication. Figure 12a shows the cross-section of the redesigned interposer with 20 μm diameter, 200 μm deep via. The two metal layers forming the front side RDL are clearly visible. In this new structure, a polymer passivation layer is coated as an insulator and patterned. The substrate conductivity is 10 S/m. The new CPW test structures are shown in Fig. 12b, c. The line width and spacing are both 20 μm, and the length is 1,000 μm. The top copper line thickness is 5 μm and the bottom line thickness is 3 μm. The two ground ports are shorted to one another to avoid the coupling capacitance labeled "C3" in the circuit model.

To obtain the S-parameters of the transmission lines, measurements were also carried out using the VNA with 200 μm pitch micro probes. Figure 13 gives the measured S-parameters of the structure shown in Fig. 12c. The insertion loss (S21) at 10 GHz is −0.65 dB, while the return loss (S11) at 10 GHz is −17 dB. Figure 14 shows the

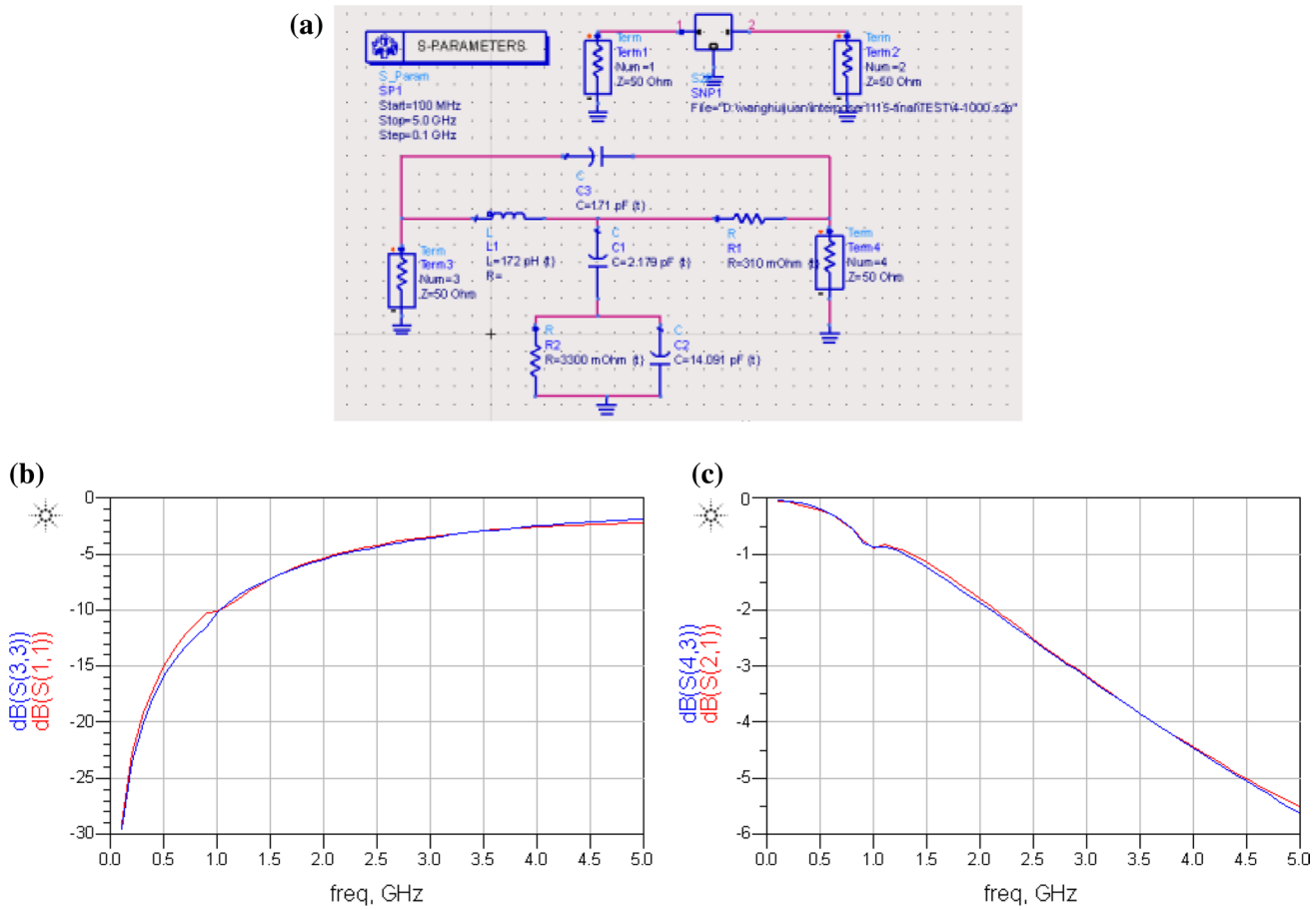


Fig. 11 Tuning circuit elements and comparison of circuit S parameters with measurements. **a** The circuit model of CPW structure, **b** insertion loss, **c** return loss

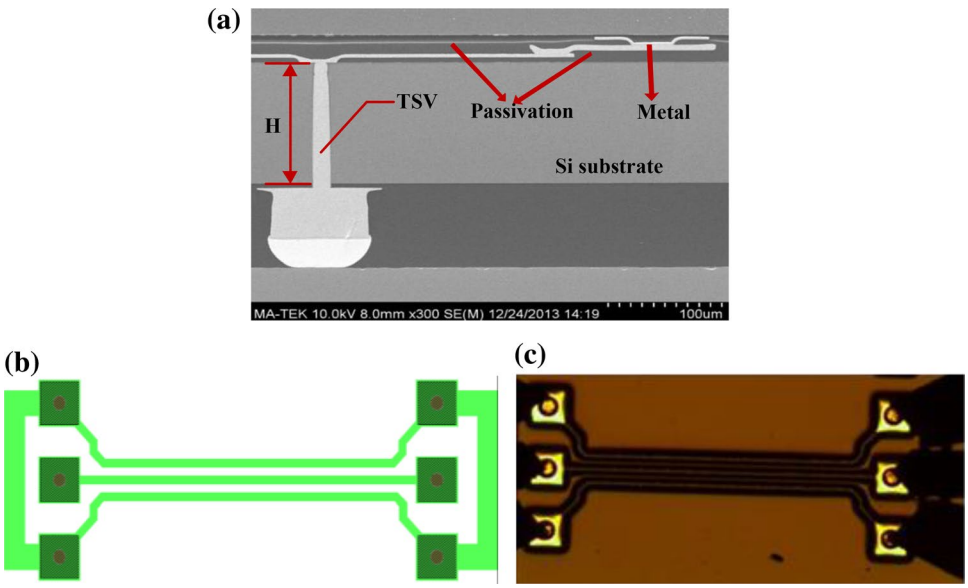


Fig. 12 The cross section of the new TSV interposer and GSG structure of the top metal layer. **a** The SEM of the new interposer design, **b** CPW layout, **c** image of the test structure

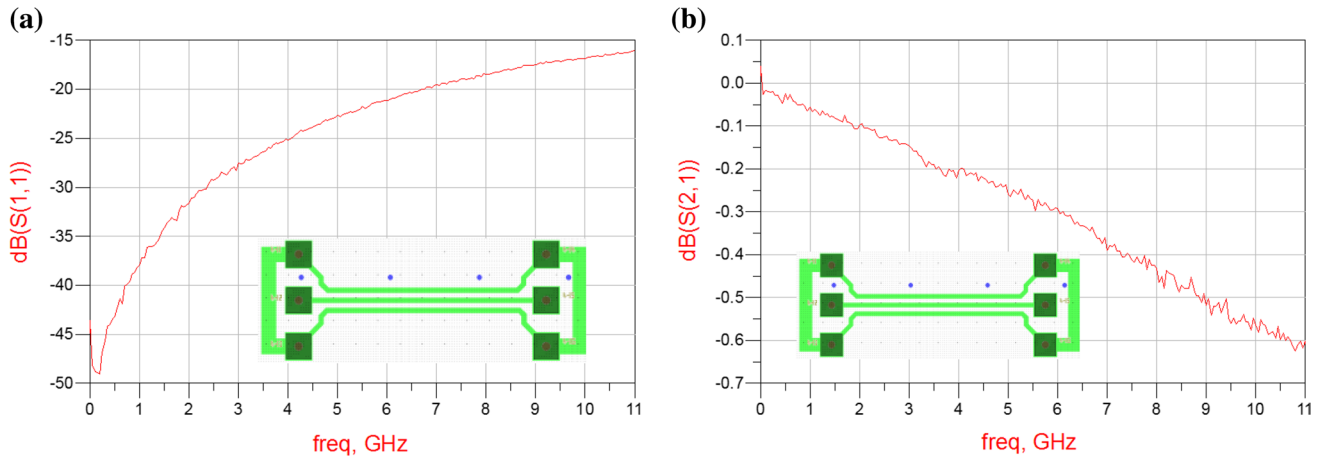


Fig. 13 S-parameters of the new RDL GSG CPW structure. **a** Return loss (S11) of the new CPW structure, **b** insertion loss (S21) of the new CPW structure

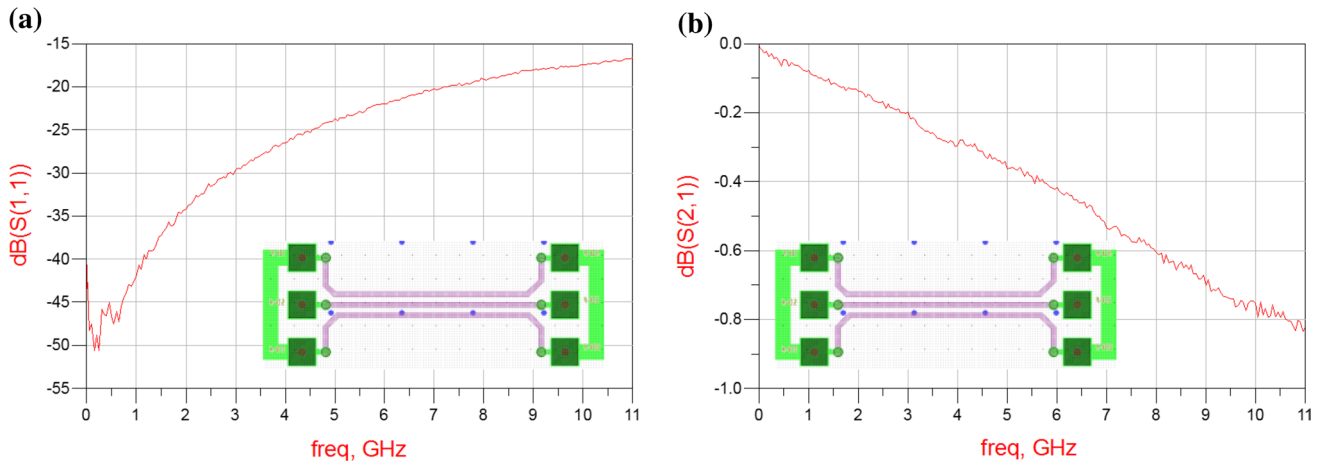


Fig. 14 S-parameters of the new bottom RDL GSG CPW structure. **a** Return loss (S11) of the new CPW structure, **b** insertion loss (S21) of the new CPW structure

measured responses of the CPW structure on the bottom RDL. The return loss (S11) at 10 GHz is −17.5 dB and the insertion loss (S21) at 10 GHz is −0.8 dB. The new structures are acceptable for use at high frequency. These results clearly show that a double isolation layer between the metal lines and silicon substrate can produce acceptable signals with low losses. The thicker insulation also reduces the parasitic coupling. These results are significant in that they enable the realization of a viable 3D interposer for RF application.

6 Conclusion

We have proposed and fabricated a TSV interposer test vehicle with test CPW structures to investigate the electrical performance at RF frequencies. The eye diagram and S parameters were tested and analyzed. In a first test vehicle the performance was unacceptable above 1 GHz. Simulations of different structures on substrates having various conductivities, but still within the CMOS range and different RDL insulator thickness and composition. A circuit model was developed to better understand the parasitic sources of the structure up to 5 GHz. Some guidelines are given to improve interposer performance. Based on the preliminary performance of an improved test vehicle we can project good behavior at least up to 10 GHz.

Acknowledgments Daquan Yu also appreciates the support of National Natural Science Foundation of China (61176098). The authors would also like to thank the help of their workmates.

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