A Comparison of Electrical Performance between a Wire Bonded and a Flip Chip CSP Package

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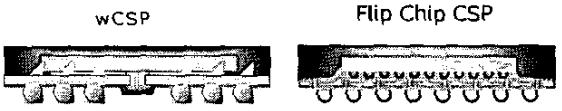
Abstract

In this paper, electrical simulations are performed to characterize a wire-bonded window CSP (wCSP™) package and a flip chip CSP (fcCSP) package designed for the same die. Results indicate that fcCSP has a slightly wider bandwidth than window CSP. Although, window CSP has a larger parasitic resistance and inductance for the target nets, it has a lower crosstalk in terms of peak-peak voltage due to shorter parallel traces. An optimized flip chip design is proposed and the results show a vast improvement over the wire bonded CSP package. Parametric studies are also performed to investigate the effects of bond wires with different diameter and horizontal distance, and variations in signal traces. These results provide useful insights on design and process selection for high-performance semiconductor packages.

Introduction

Semiconductor packages are increasingly moving towards miniaturization due to widespread trend in mobility of electronic devices and products. Window CSP is a high performance cost effective chip scale BGA package developed by UTAC for high-speed memory applications. Its advanced packaging design enables effective package miniaturization compared to a conventional leadframe based TSOP. The window CSP package design accommodates die shrinks without affecting package outline. This allows the customer a seamless transition when migrating to next generation of memory products. With flip chip technology deemed as the superior interconnect technology for packaging, it is expected to grow in demand and adoption not only in the high performance IC segments (MPU, DSPs), but also into the mainstream applications such as consumer electronic ICs and PCs. The primary driver for flip chip packaging in the memory applications is its superior electrical performance as compared to its wire-bonded counterparts.

In this paper, electrical simulation was performed to characterize a 60-ball window CSP and a 60-ball flip chip CSP (fcCSP) package. The cross-sectional views of the two packages are shown in Fig. 1.



a. Window CSP b. Flip Chip CSP (fcCSP)

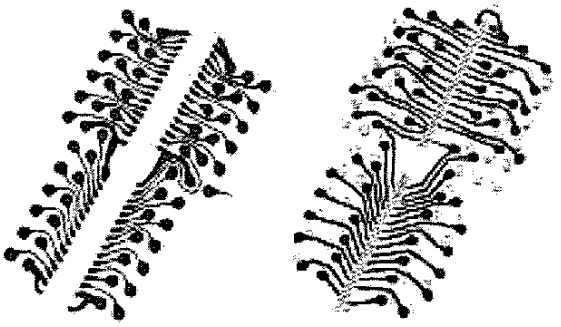
Fig. 1: Cross-sectional view of a). window CSP and b). fcCSP

These two packages were designed for the same die. The simulations were done both in frequency domain and time domain. Electrical performances were compared in terms of insertion loss, return loss, cross talk noise and propagation delay. To look at the performance heterogeneity as a result of manufacturing process, parametric studies are also performed to investigate the effects of bond wires with different diameters and horizontal distances, and variations in signal traces. These results provide useful insights on design and process selection for high-performance semiconductor packages. Section II presents the package information, RLC extraction, frequency and time domain simulation. Section III is the parametric study on bond wires and signal traces. Section IV is the summary and conclusion of this paper.

Package Information and Simulation

Package information

Shown in Fig. 2 is the 3D model of window CSP and fcCSP.



a. window CSP *b. fcCSP*

Fig 2: 3D model of a). window CSP and b). fcCSP

Both packages are CSP type with 60 solder balls. To facilitate study, two signal traces of the same pin name from each package are chosen as target nets for simulation. The top view of target signal nets was shown in Fig.3.

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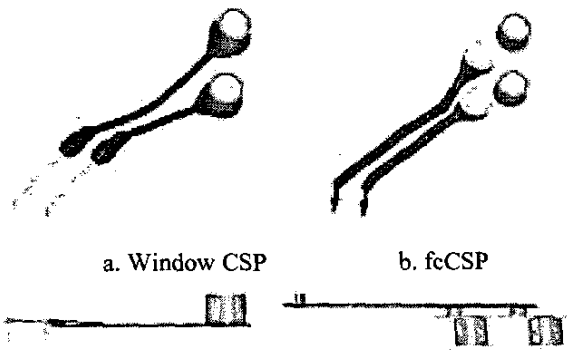

a. Window CSP b. fcCSP

c. Cross-section of a d. Cross-section of b

Fig. 3: 3D view of target nets

The general information of the two packages are tabulated in Table 1.

Table 1. Package Information for window CSP and fcCSP

Item	window CSP	fcCSP
Package size	15.2mm x 15.2mm	15.5mm x 15.5mm
Die size	14.24mm x 14.24mm	14.24mm x 14.24mm
Trace thickness	27 um	20um
Trace material	Cu	Cu
Trace length	1.16mm/1.86mm	1.15mm/2.38mm
Wire/bump diameter	25.4um	100um
Wire length/ bump height	0.5mm/0.55mm	80um
Dielectric thickness	100um	100um
Dielectric material	BT	BT

RLC extraction

Ansoft Q3D 5.0 is used to extract the RLCs of the longest and shortest nets as well as the target nets in window CSP and fcCSP, respectively. Simplified 4-point profile recommended by [1] is adopted for bond wire simulation. The package is simulated with a copper ground reference plane 0.152 mm away from the bottom of the solder ball [2]. Between the package and the reference ground plane is FR4 epoxy. The simulation results are listed in Table 2.

Table 2. RLCs Extracted Using Ansoft Q3D 5.0

Net Name / Package Type		R (ohm)	Ls (nH)	Lm (nH)	Cs (pF)	Cm (pF)
Longest	wCSP	1.113	4.476	-	0.308	-
	fcCSP	0.047	2.350	-	0.300	-
Shortest	wCSP	0.029	0.925	-	0.147	-
	fcCSP	0.022	0.598	-	0.265	-
Net1	wCSP	0.073	2.350	0.740	0.329	0.114
	fcCSP	0.039	2.010	0.810	0.333	0.140
Net2	wCSP	0.058	1.720	0.740	0.290	0.114
	fcCSP	0.030	1.470	0.810	0.296	0.140

From Table 2, it is obvious that window CSP package has a much larger RL values for the longest nets than fcCSP. The RL values of the shortest nets are comparable. Concerning the target nets, window CSP has a larger resistance and self-inductance value than fcCSP. This is mainly due to different interconnections. For window CSP, the interconnection is achieved by wire bonding, while for fcCSP, the interconnection is achieved through small solder bumps between chip and substrate and via holes between top and bottom of the substrate. Compared with solder bump plus via hole, the thinner bond wire has a larger resistance and inductance. However, the load capacitance of fcCSP is slightly larger than that of window CSP because of longer trace and via which is capacitive in behavior. From Fig. 3(a) and Fig. 3(b), It is obvious that the parallel portion of the two signal traces in fcCSP is longer than that of in window CSP, resulting in a higher inductive and capacitive coupling. This, in turn, will cause a larger crosstalk as will be shown in section 2.4.

High frequency simulation

To investigate the high frequency characteristics of the two packages, the target signal nets are simulated for S-parameters using Ansoft HFSS 8.5 in the frequency range of 0.1GHz to 10 GHz. The two signal nets are set up as a four-port system. The same assumptions on the bond wire profile and system ground reference plane that used to extract RLCs in Q3D are made in setting up high frequency models. All the four ports are lumped gap ports with an impedance value of 50 Ω. At the ball side, the ports extend from the bottom of the solder ball directly to the PCB ground reference plane. At the wire/bump side, the ports are shorted to the PCB ground reference plane by two perfect conductors which represent local chip ground. As an example, the 3D model of fcCSP in HFSS is shown in Fig. 4.

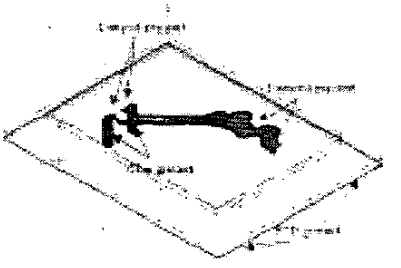

Fig. 4: 3D model of fcCSP target nets in HFSS 8.5

The return loss and insertion loss of net1 is shown in Fig. 5 and Fig. 6, respectively. Both figures indicate that fcCSP has a slightly better electrical performance in terms of return loss and insertion loss. This is what we expected as the thinner bond wire in window CSP causes more impedance mismatch due to the excessive inductance. From Fig. 5, we can see that for a specified return loss, say, -20dB, window CSP has a bandwidth of about 1.1GHz while fcCSP has a bandwidth of around 1.3GHz. If we look at the insertion loss shown in Fig. 6, both packages have an insertion loss better than 0.5dB for a frequency range up to 3GHz. However, fcCSP has a slightly lower insertion loss than window CSP for a specified operating frequency in the simulated frequency range.

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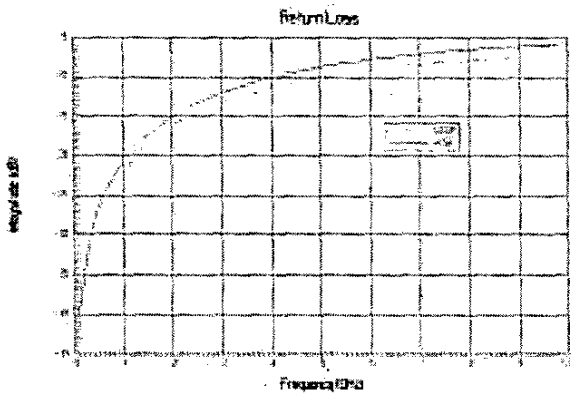

Fig. 5: Magnitude of return loss of net1

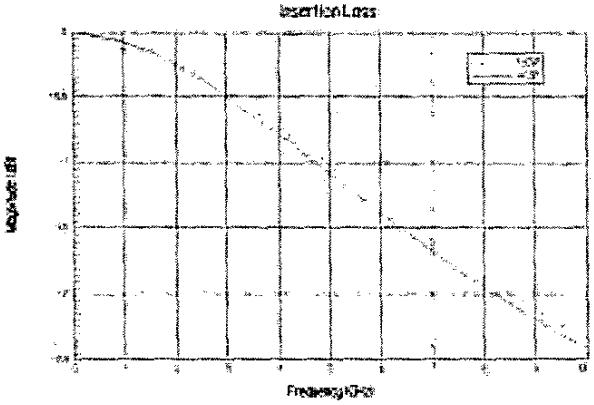

Fig. 6: Magnitude of insertion loss of net1

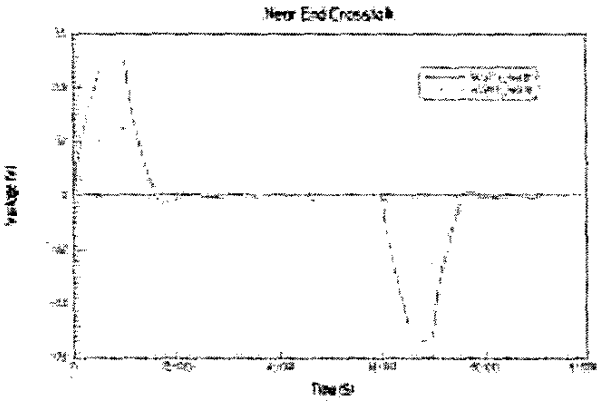

Fig. 8: Near-end crosstalk in terms of peak-peak voltage

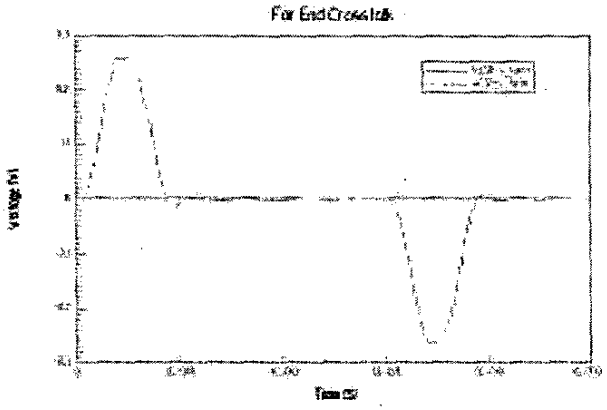

Fig. 9: Far-end crosstalk in terms of peak-peak voltage

SI analysis

Time domain simulation is carried out using Ansoft schematic capture 5.0 to investigate the signal integrity. A voltage pulse with a magnitude of 5V and a rise time of 100ps is used as excitation. This rise time corresponds to a bandwidth of 3.5GHz in the frequency domain according to $F_{3dB} = \frac{0.35}{T_r}$ [3]. $50\,\Omega$ resistors were used as the input and output impedance for both active and victim signal nets. The simulation results are shown in Fig. 7-9.

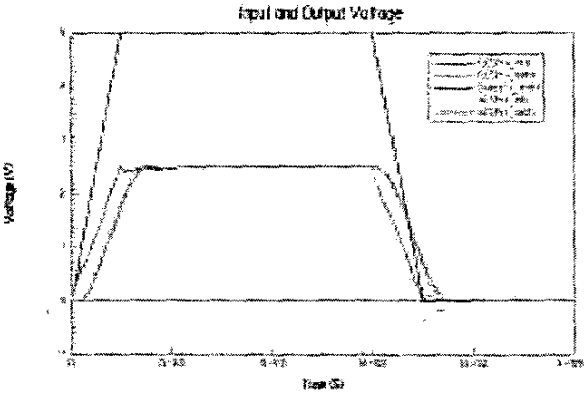

Fig. 7: Input and output signal

Fig. 7 is the plot of input and output voltage waveform. The steady-state output voltage has half the magnitude of the source voltage. This is because the $50\,\Omega$ input impedance and the $50\,\Omega$ output impedance work together as a voltage divider. The near-end and far-end crosstalk was shown in Fig. 8 and Fig. 9, respectively. It is clearly seen that fcCSP has a much larger crosstalk at both near-end and far-end than window CSP. On a general scenario, one would expect a lower crosstalk for a flip chip interconnection than a wire-bonded interconnection. However, it is only true for packages with the same routings. As was discussed in section 2.2, the two traces under study routed differently in window CSP and fcCSP. The coupling length in fcCSP is much longer which results in a higher crosstalk.

A closer examination of Fig. 9 reveals an interesting phenomenon: far-end crosstalk of window CSP is a negative pulse while fcCSP, a positive one. For far-end crosstalk, it is the overall effect of inductive coupling and capacitive coupling. For a step-up voltage pulse, the far-end crosstalk induced by inductive coupling is a negative pulse while the far-end crosstalk caused by the capacitive coupling is of positive polarity. Generally speaking, inductive coupling is dominant for two parallel signal traces in high-speed digital systems [3]. That is why in most cases, the far-end crosstalk induced by a step-up voltage pulse is a negative one. The positive far-end crosstalk of fcCSP in Fig. 9 is most likely

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caused by the dominance of capacitive coupling in this particular design.

Optimized fcCSP design

From the above-mentioned discussion, we see a comparable electrical performance for the two packages. This is because both the bump pads and the bond pads on the die side are center-positioned. Thus, very short bond wires are needed to achieve chip-to-substrate interconnections. As a consequence, the advantage of the flip chip interconnection method is not obvious. However, one of the advantages of the flip chip design lies in its design flexibility. Bond pads can be designed in a way to minimize the distance between the substrate vias and flip chip interconnection. This optimized design will have a superior electrical performance. Shown in Fig. 10 is the cross-section of the optimized design.

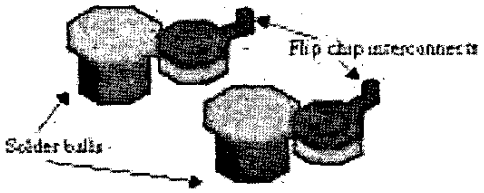

Fig. 10: Cross-section of an optimized flip-chip design.

Frequency domain and time domain simulation results of this optimized flip chip design are plotted in Fig. 11-13.

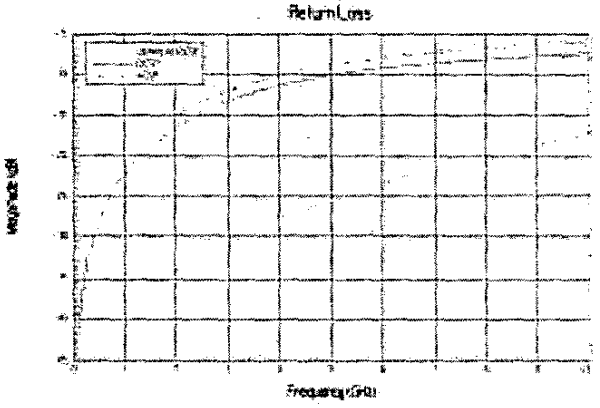

Fig. 11: Magnitude of return loss vs. frequency

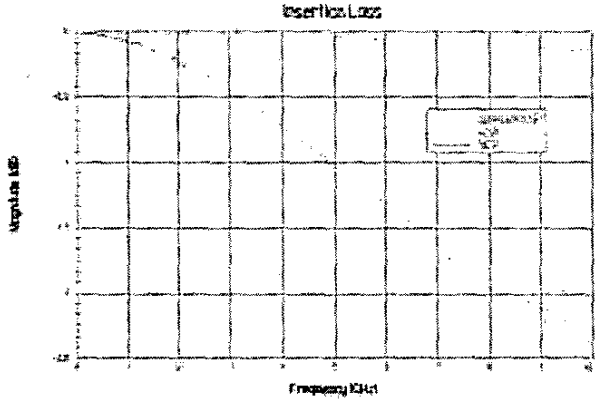

Fig. 12: Magnitude of insertion loss vs. frequency

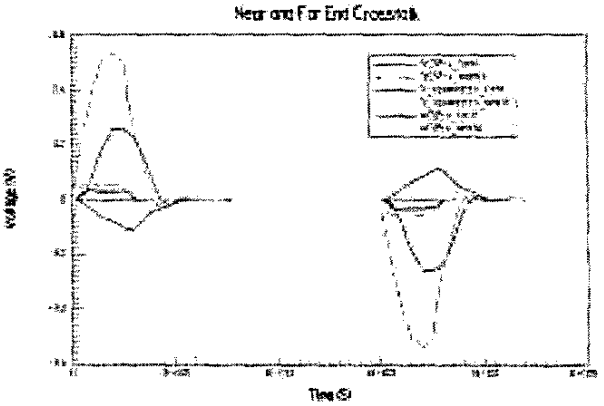

Fig. 13: Near and far end crosstalk in terms of peak-peak voltage

Fig. 11 demonstrates that the optimized fcCSP has a bandwidth up to 8GHz for a return loss of 20dB. Within the simulated frequency range, its insertion loss is less than 0.2dB. From the crosstalk plot shown in Fig. 13, we found a 75% reduction in far-end crosstalk and an 89% reduction in near-end crosstalk for the optimized fcCSP compared with the standard fcCSP design.

Parametric Study on Bond Wires and Signal Traces

Bond wires

Wire bonding is a widely used interconnection technology in semiconductor industry. As both the clock speed in digital systems and operating frequency in RF and Microwave circuits are becoming higher and higher, bond wires become a critical element that limits the system electrical performance. Therefore, parasitic parameters of bond wires must be taken into account in a wire bonded package simulation. According to [1], the bond wire can be described by five parameters. Consequently, the modeling of bond wires can be standardized. Using 4-point simplified profile recommended by [1], parasitic parameters for bond wires with different length and diameter can be extracted. These parasitic parameters can further be curve-fitted to get the simple analytical formula which enable designers a quick yet accurate estimation of bond wire parasitic parameters.

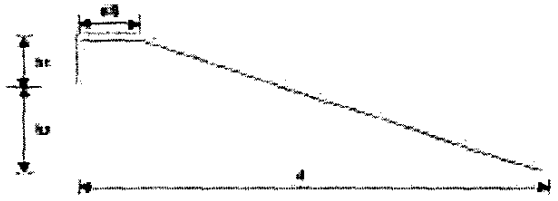

Fig. 14: 4-point simplified bond wire profile [1] (d : total distance the wire covers in the horizontal plane. h_1 : height between the bond pad and the top of the loop. h_2 : height between the bond pad and the bond finger).

Assuming $h_1 = 150\mu m$ and $h_2 = 300\mu m$, parasitic resistance, inductance and capacitance as a function of d with a diameter of $24.5\mu m$ and $25.4\mu m$ (two typical values used in industry) are extracted and depicted in Fig. 15-17. The capacitance values are extracted with the bond wire

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surrounded by mold compound with a dielectric constant of 3.9.

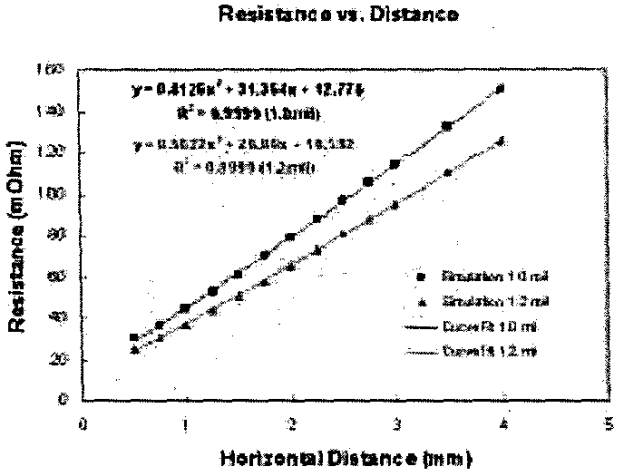


Fig. 15: Parasitic resistance of bond wires vs. horizontal distance

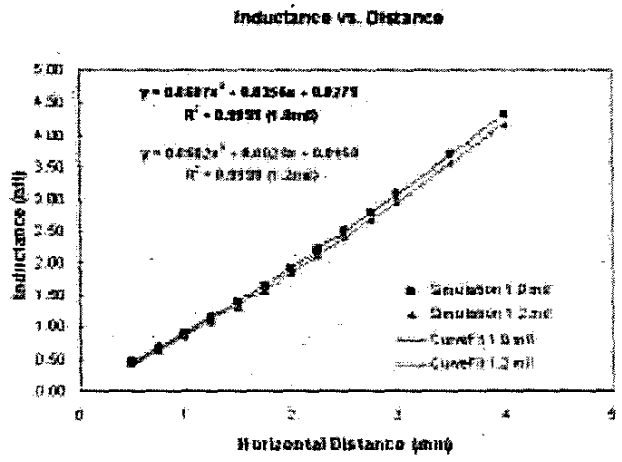


Fig. 16: Parasitic inductance of bond wires vs. horizontal distance

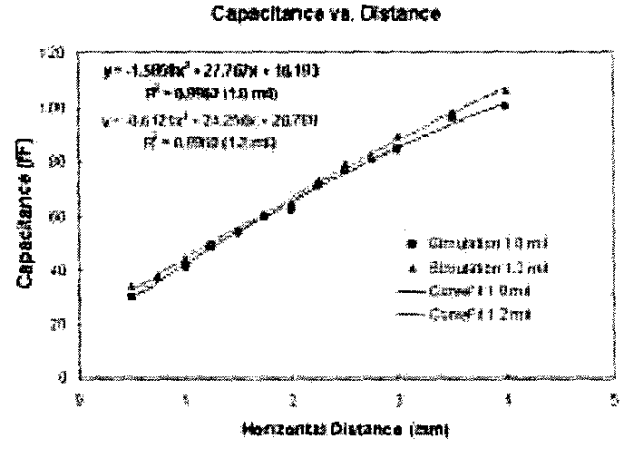
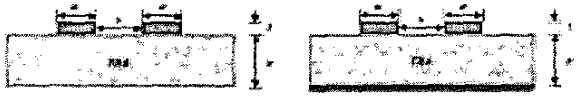


Fig. 17: Parasitic capacitance of bond wires vs. horizontal distance

Common trace vs. controlled impedance trace

When there is a solid ground plane presenting in close proximity to common signal traces, these traces are said to have controlled impedance. To investigate the effect of the solid ground plane, crosstalk simulations were carried out to two 0.5 inch long parallel traces with cross-sections shown in Fig. 18.



a. Common b. Controlled impedance

Fig. 18: Cross-section of two parallel signal traces

In the simulation, $w = s = 75\mu m$ and $t = 27\mu m$. For the common trace configuration, $h = 100\mu m$. For the controlled impedance trace configuration, $h = 100\mu m$ and $200\mu m$, respectively. The simulation results are depicted in Fig. 19-20.

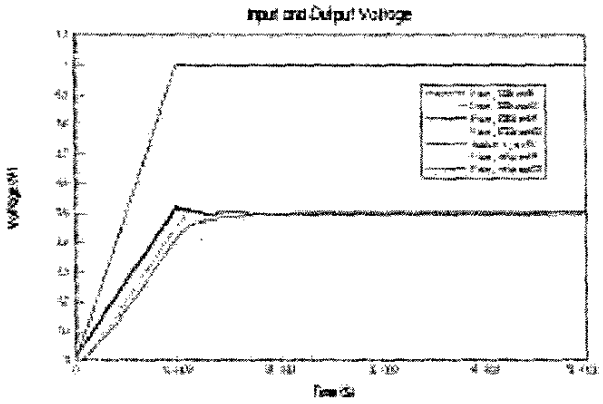


Fig. 19: Input and output signal in time domain simulation

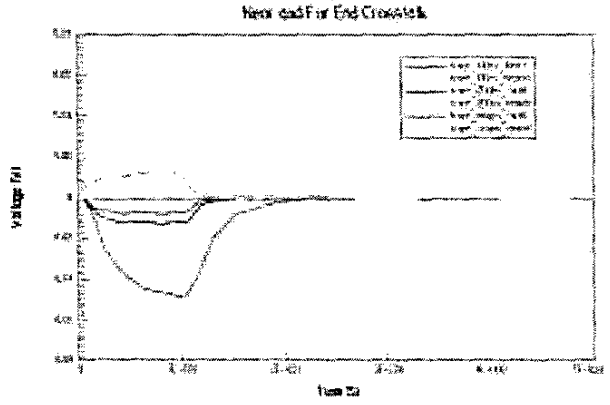


Fig. 20: Crosstalk in terms of peak-peak voltage

It is very clear that the common trace configuration has both largest time delay and crosstalk as was shown in Fig. 19 and Fig. 20, respectively. For the controlled impedance trace configuration, decreasing the thickness of the dielectric degrades the input signal rise time while decreases the crosstalk.

Conclusions

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Simulations of a window CSP package and an fcCSP package were carried out both in frequency domain and time domain. The results show that for a center bond pad layout, window CSP and fcCSP has comparable electrical performances. Thus, window CSP is a cost effective solution for high speed memory applications. However, taking advantage of the flexibility of fcCSP design, optimized fcCSP can be implemented by designing the bond pads as close as possible to the vias in order to minimize the electrical parasitics and crosstalk. This optimized design will have a vast improvement over the window CSP package. Finally, controlled impedance design has a great advantage in suppressing crosstalk noise. To minimize crosstalk, the solid ground reference plane should be as close as possible to the signal traces. The window CSP package can very easily implement this design since it only uses one metal plane for the signal trace and solder ball routing.

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