5XCC0 Biopotential and Neural Interface Circuits

Electronics Fundamentals

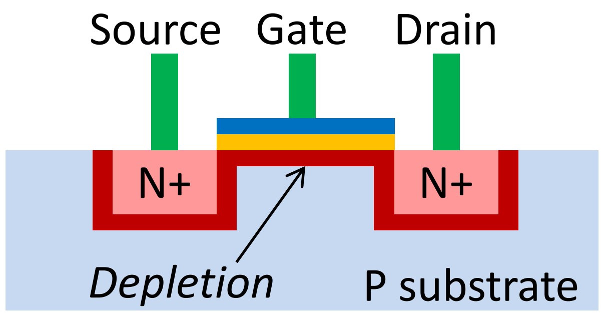
Pieter Harpe

Outline

- Devices: MOS transistors
  - Diffusion & Drift
  - Above threshold & Sub-threshold operation
- Noise
  - Shot noise, 1/f noise
  - Noise in devices
  - Noise in circuits

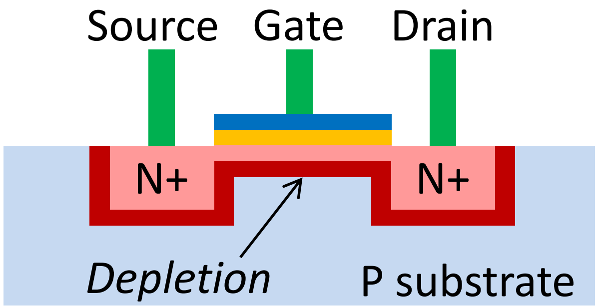
Basic N-channel MOSFET Behavior

$V_{GS} < V_{th}$: Sub threshold: $I_{ds} = 0$



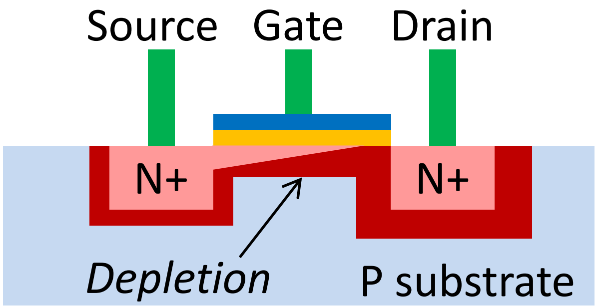
$V_{GS} > V_{th}$ & $V_{DS} < V_{GS} - V_{th}$: Above threshold, linear mode

$$I_{ds} = \mu_n C_{ox} {}^{W}/_{L}\{(V_{gs} - V_{th})V_{ds} - ½V_{ds}{}^2\}$$



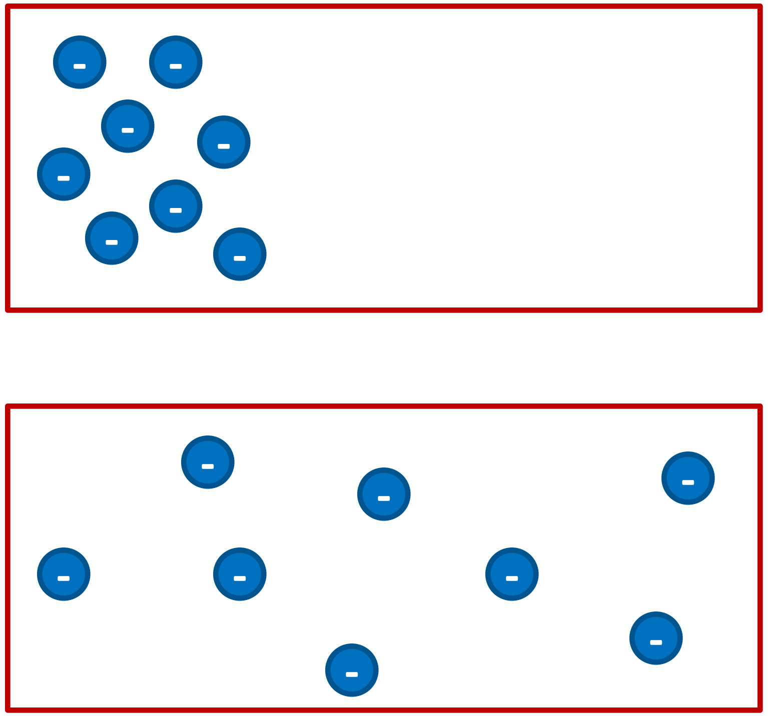
$V_{GS} > V_{th}$ & $V_{DS} > V_{GS} - V_{th}$: Above threshold, saturation mode

$$I_{ds} = ½\mu_n C_{ox} {}^{W}/_{L}(V_{gs} - V_{th})^2$$

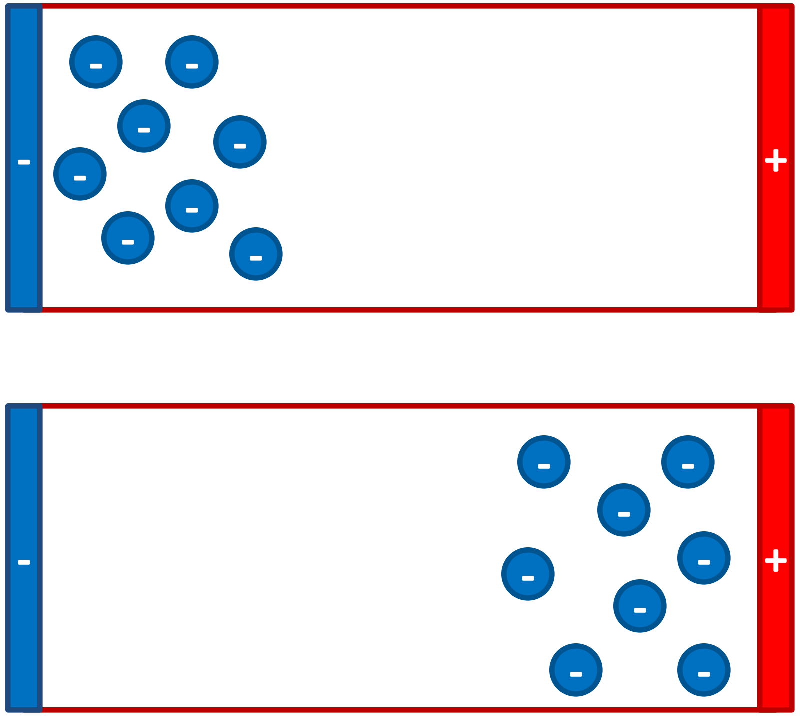


Diffusion & Drift Current

Diffusion:
Difference in concentration
➔ Current flow

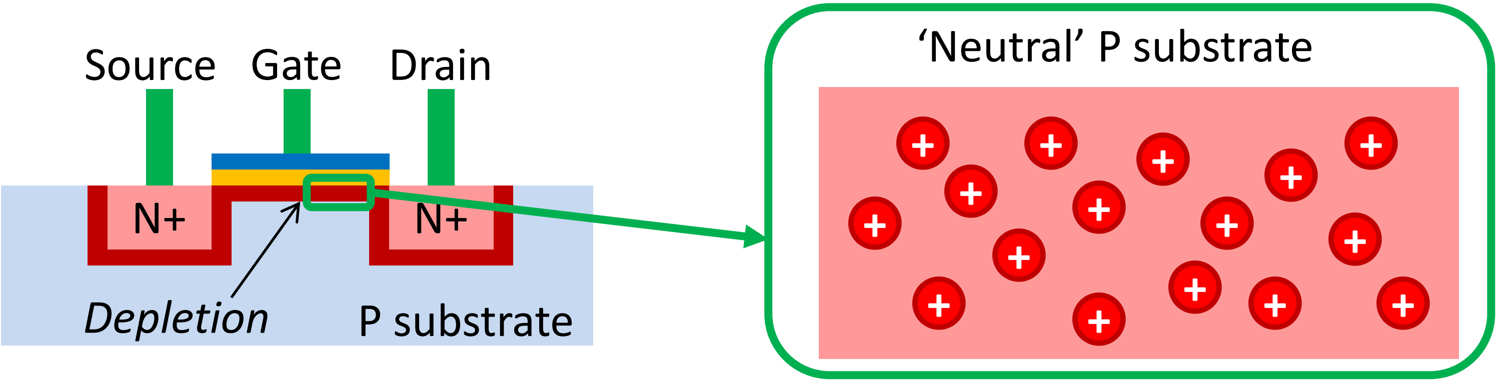


Drift:
Difference in surface potential
➔ Current flow



 = Electron

Sub/Above-Threshold Behavior

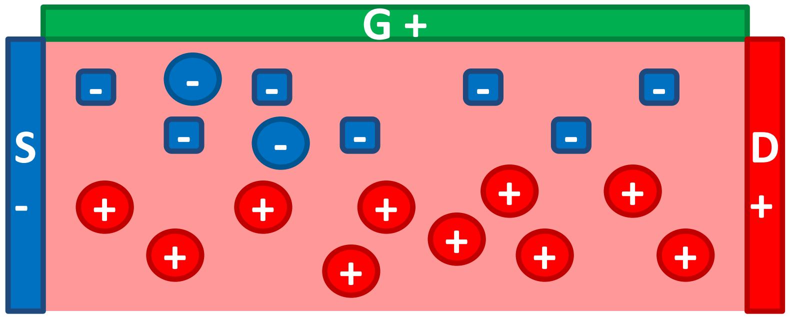


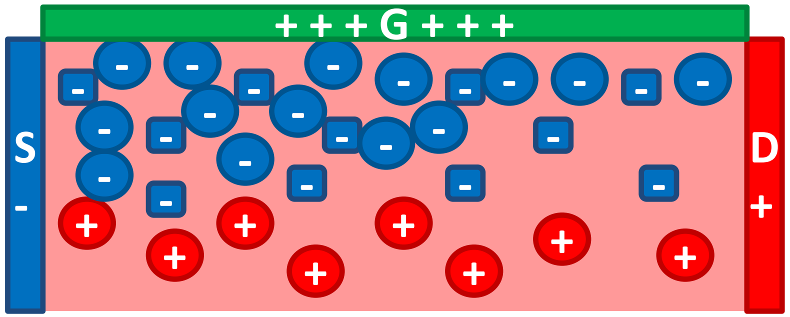
<u>Sub</u>-Threshold: Small V_{gs}

- Depletion; few electrons in channel
- V_{ds} causes concentration difference
- Diffusion current: $I_{ds} = I_0 \exp(K_s V_{gs}/\Phi_t)$

<u>Above</u>-Threshold: Large V_{gs}

- Depletion; many electrons in channel
- V_{ds} causes electric field
- Drift current: $I_{ds} = \frac{1}{2}\mu_n C_{ox} {}^{W}/_{L}(V_{gs} - V_{th})^2$

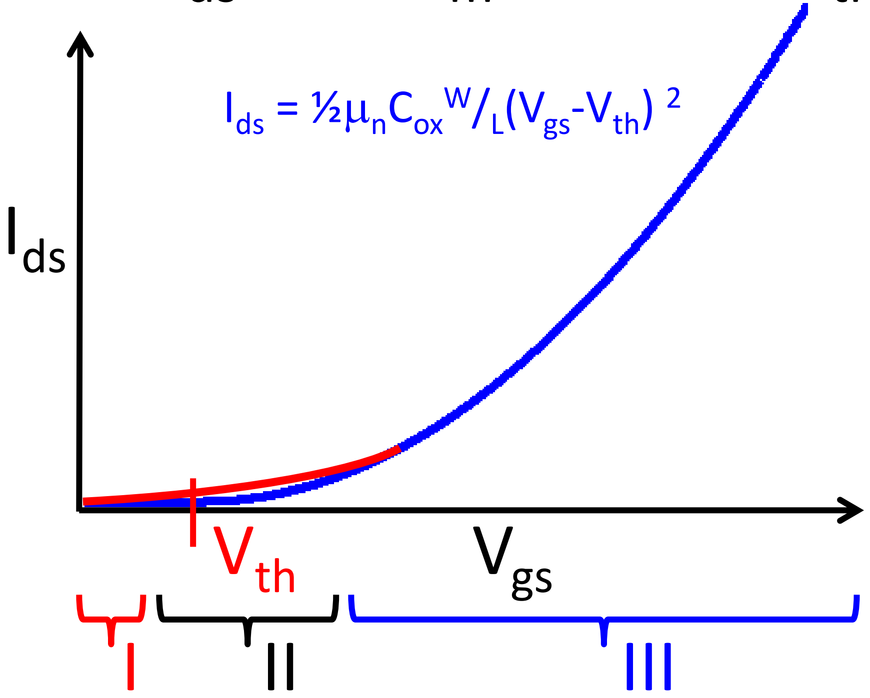


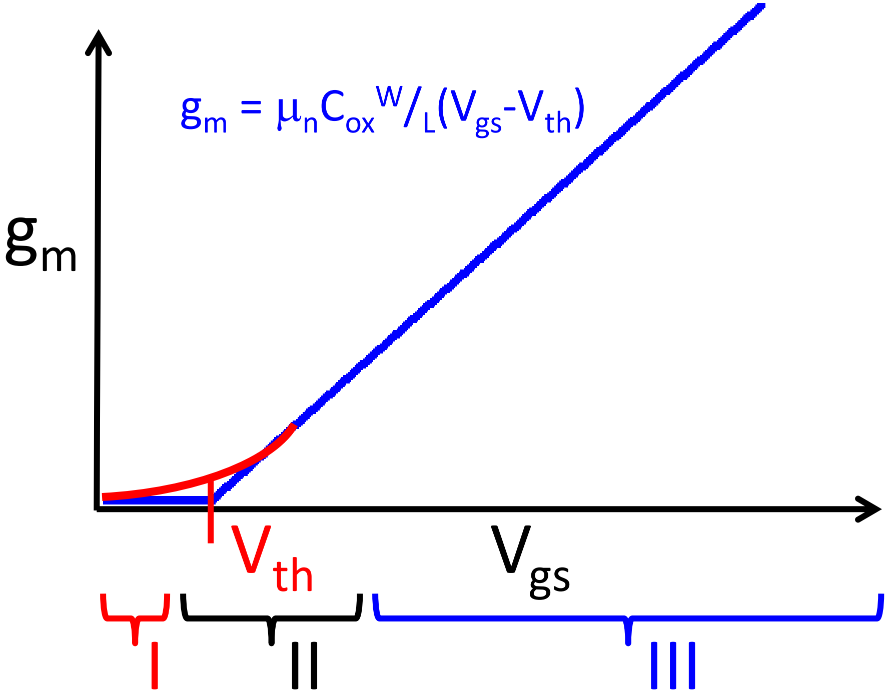


= Electron = Hole = Fixed negative charge

Extended Behavior in Saturation

- Change in I_{ds} and g_m around V_{th} because of *diffusion*





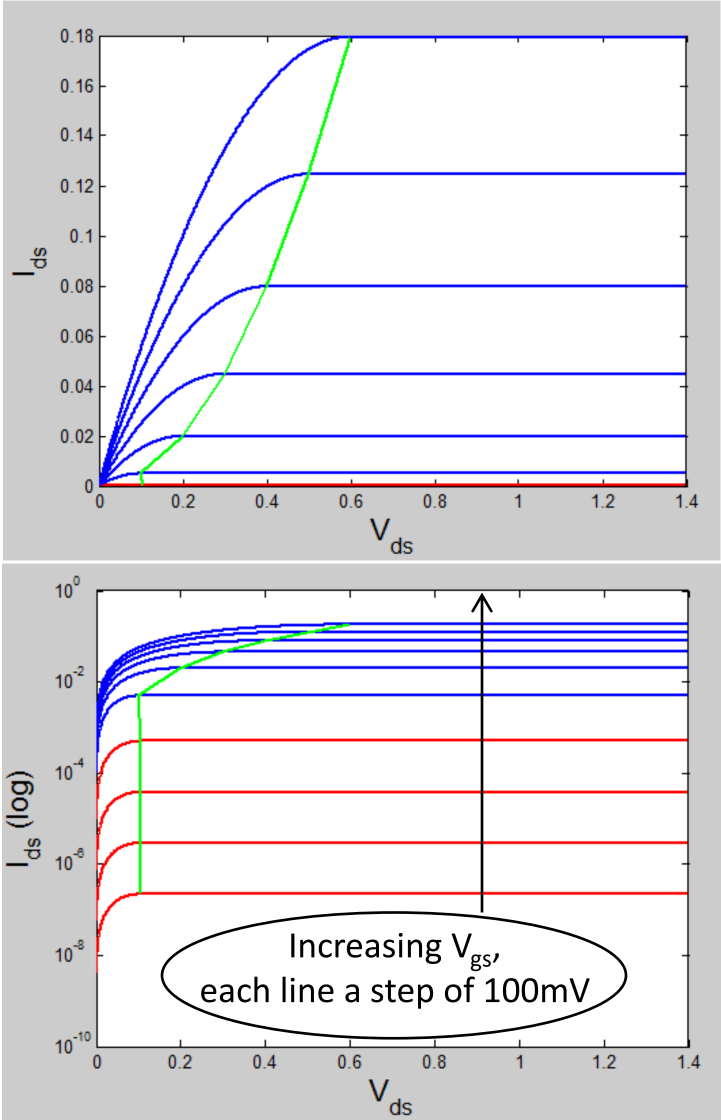
I = weak inversion: diffusion current

II = moderate inversion: transition area

III = strong inversion: drift current

Note: the typical saturation model is ONLY valid in strong inversion

I_{ds}-V_{gs}-V_{ds} Behavior



Two times the same picture, but Y-axis changed from linear to logarithmic.

- Difference between each red/blue line is a V_{gs} step of 100mV
- Green line is the border between linear and saturation region

- Blue lines: $V_{gs} > V_{th}$
  - Strong inversion mode
  - I_{ds} quadratic to V_{gs}
  - Saturation if $V_{ds} > V_{gs} - V_{th}$

- Red lines: $V_{gs} < V_{th}$
  - Weak inversion mode
  - I_{ds} exponential to V_{gs}
  - Saturation if $V_{ds} > 4\Phi_t$
    (Φ_t = kT/q, $4\Phi_t \approx$ 100mV)

Overview of Modes

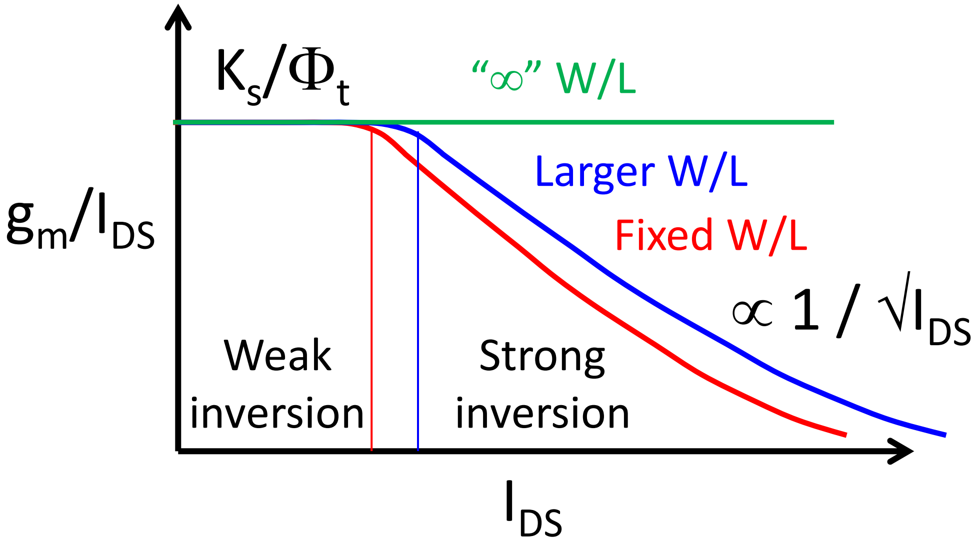
- Linear & saturation modes can occur with sub & above threshold

	Linear Region	Saturation Region
Sub-Threshold = Weak Inversion	$V_{gs} < V_{th}$ $V_{ds} < 4\Phi_t$ ($\approx$ 100mV)	$V_{gs} < V_{th}$ $V_{ds} > 4\Phi_t$ ($\approx$ 100mV)
Above-Threshold = Strong Inversion	$V_{gs} > V_{th}$ $V_{ds} < V_{gs} - V_{th}$	$V_{gs} > V_{th}$ $V_{ds} > V_{gs} - V_{th}$

$\Phi_t = kT/q$

$$g_m = \partial I_{ds}/\partial V_{gs}$$

Sub-Threshold, Saturation	**Above-Threshold, Saturation**
$I_{ds} = I_0 \exp(K_s V_{gs}/\Phi_t)$	$I_{ds} = ½\mu_n C_{ox} {}^W/_L (V_{gs}-V_{th})^{2}$
$g_m = K_s/\Phi_t \cdot I_{DS} \approx 27\ I_{DS}$ K_s is constant (around $^2/_3$), $\Phi_t = kT/q$	$g_m = \mu_n C_{ox} {}^W/_L (V_{GS}-V_{th})$ $= \sqrt{\{2\mu_n C_{ox} {}^W/_L I_{DS}\}}$
$g_m/I_{DS} = K_s/\Phi_t \approx 27$ *	$g_m/I_{DS} = \sqrt{\{2\mu_n C_{ox} {}^W/_L / I_{DS}\}}$



Sub-threshold is more *power efficient*

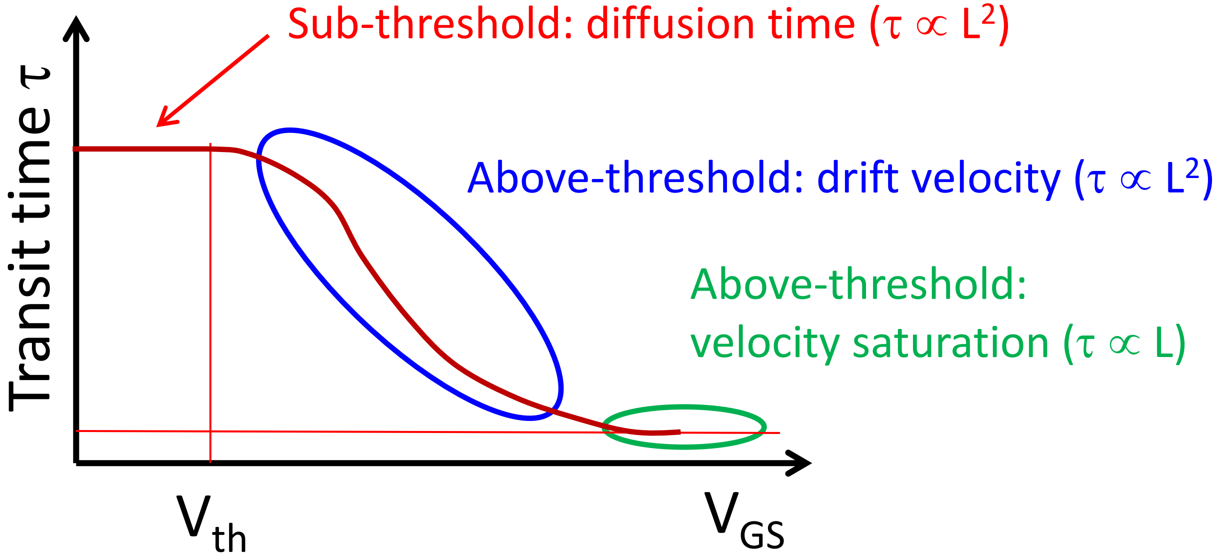
Note: bipolar transistors (NPN, PNP) behave similar to sub-threshold MOSFETs:

- $I_{ce} = I_0 \exp(V_{be}/\Phi_t)$
- $g_m = 1/\Phi_t \cdot I_{CE} \approx 40\ I_{CE}$

* Note: the value 27 is an example or approximation. The actual value my vary.

Transit Time

- Transit time: average time of an electron to travel the length of the channel



Sub-threshold is slower but scales down with L^2,
above-threshold scales ultimately with L

Sub/Above-Threshold Comparison

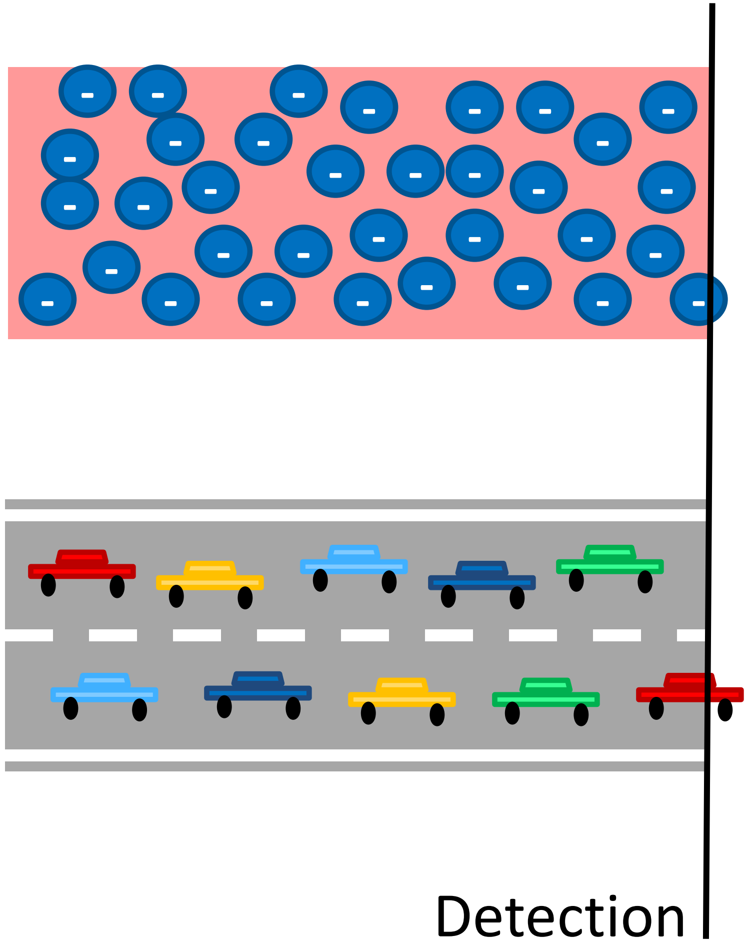
Sub-Threshold	**Above-Threshold**
Saturation current is exponential in V_{gs}	Saturation current is square law in V_{gs}
V_{dsat} is constant, approx. 100mV	V_{dsat} is variable with V_{gs}: $V_{gs} - V_{th}$
Current flows by diffusion	Current flows mainly by drift
Charge concentrations are small	Charge concentrations are large
Currents are small	Currents are large
Good for ultra-low-power operation	Good for high-power operation
Power efficiency is constant with current	Power efficiency is lower and degrades with larger currents
Higher noise and offset (absolute values)	Lower noise and offset
Can work on low power supply voltages	Needs higher power supply voltages
Reduced speed of operation	Higher speed of operation
Becoming increasingly important	Traditional use in the past

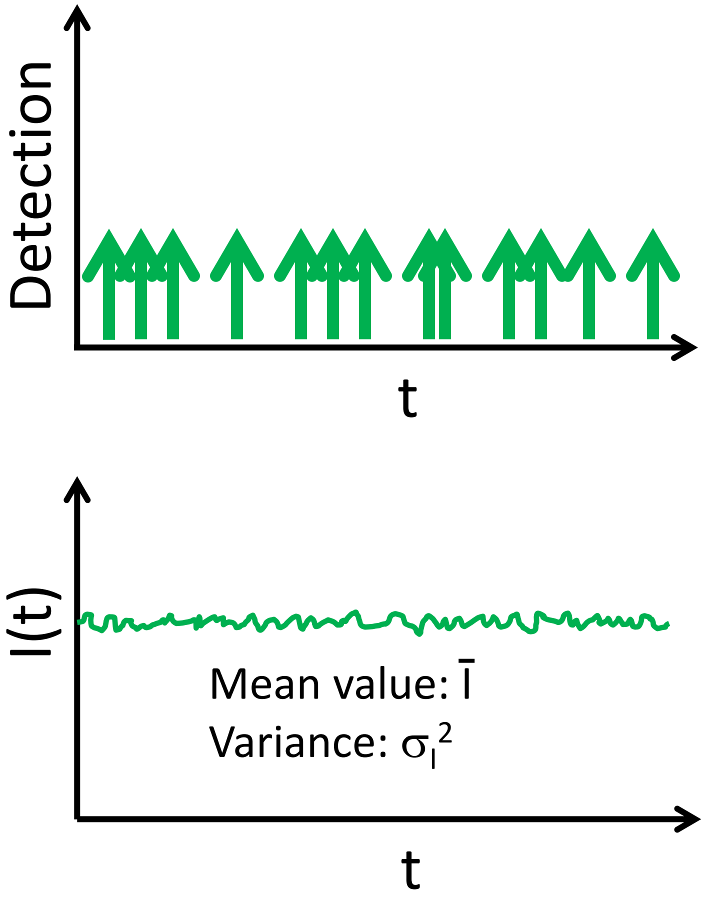
Outline

- Devices: MOS transistors
  - Diffusion & Drift
  - Above threshold & Sub-threshold operation
- Noise
  - Shot noise, 1/f noise
  - Noise in devices
  - Noise in circuits

Shot Noise (1)

- Current: flow of charge (electrons/holes) → <u>Discrete</u>

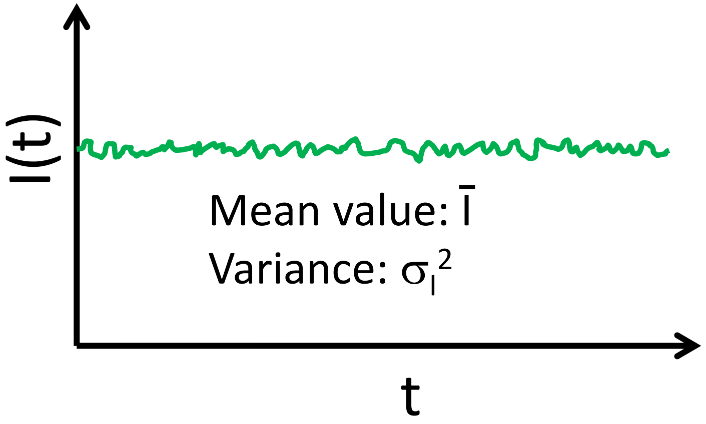




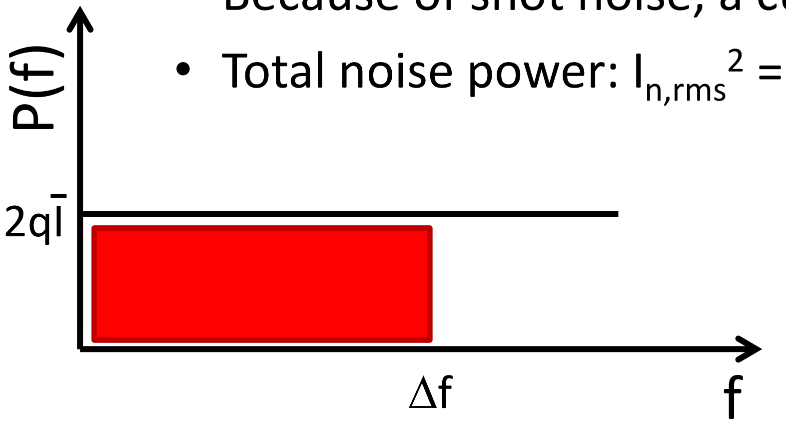
Shot Noise (2)

- Time domain

Mean value: $\bar{I}$
Variance: σ_I^2



- Frequency domain
  - Power Spectral Density (PSD): P(f) or $S_I^2(f)$ [A^2/Hz]
  - Because of shot noise, a current with average value $\bar{I}$ will have a noise P(f) of $2q\bar{I}$
  - Total noise power: $I_{n,rms}^2 = \sigma_I^2$: $2q\bar{I}\Delta f$, where Δf is the bandwidth of interest



Summary Noise Terminology

Time domain	Current	Voltage
Amplitude	$I_{n,rms}$ [A]	$V_{n,rms}$ [V]
Power	$I_{n,rms}^2$ [A^2]	$V_{n,rms}^2$ [V^2]
Frequency domain (spectral density)		
Amplitude spectral density	$S_I(f)$ [$A/\sqrt{Hz}$]	$S_V(f)$ [$V/\sqrt{Hz}$]
Power spectral density	$S_I^2(f)$ [A^2/Hz]	$S_V^2(f)$ [V^2/Hz]
Frequency domain (integrated noise), and relation to time domain		
Amplitude of integrated noise (in a bandwidth Δf)	$I_{n,rms} = \sqrt{\Delta f} \cdot S_I(f)$ [A]	$V_{n,rms} = \sqrt{\Delta f} \cdot S_V(f)$ [V]
Power of integrated noise (in a bandwidth Δf)	$I_{n,rms}^2 = \Delta f \cdot S_I^2(f)$ [A^2]	$V_{n,rms}^2 = \Delta f \cdot S_V^2(f)$ [V^2]

Note: the term “power” used in noise terminology refers to squared amplitudes, like V^2 or I^2, but it is not a power in “Watt”!

Exercise 1: SNR

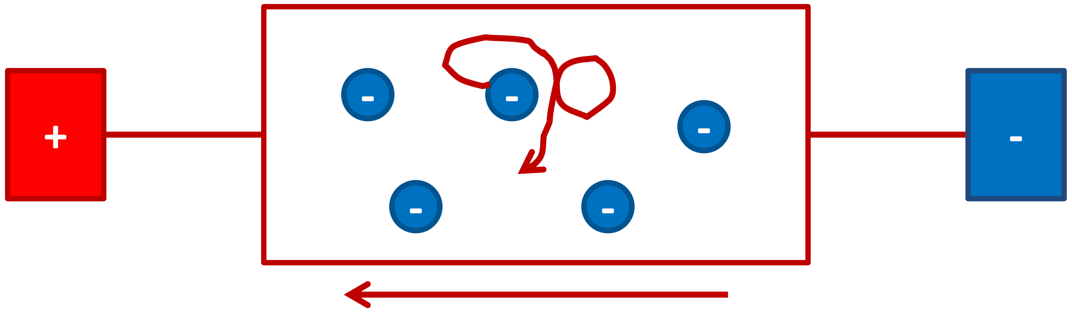
Consider at some point in our system, we have a signal and we have thermal noise.

The signal is a sinusoid with an amplitude of 1mV.

The thermal noise has a spectral density of $3\mu V/\sqrt{Hz}$ and a bandwidth of 100Hz.

a) Calculate the signal power
b) Calculate the integrated noise power
c) Calculate the rms value of the noise
d) Calculate the SNR in this system (in dB)

Resistor Noise (1)



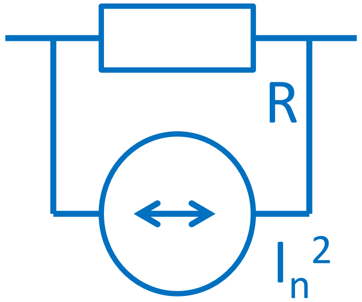
$R = 1 / G$

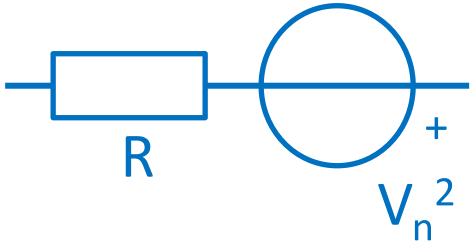
$V = I \cdot R$

- Current flows:
  - Drift (due to externally applied voltage)
  - Random thermal movement
- Signal current determined by drift ($I = V/R$)
- Noise dominated by thermal movement (I_t):

  $P(f) = 2q\bar{I}_t$, which ends up in:
  - Current PSD: $S_I^2(f) = 4kTG = 4kT/R$

Resistor Noise (2)



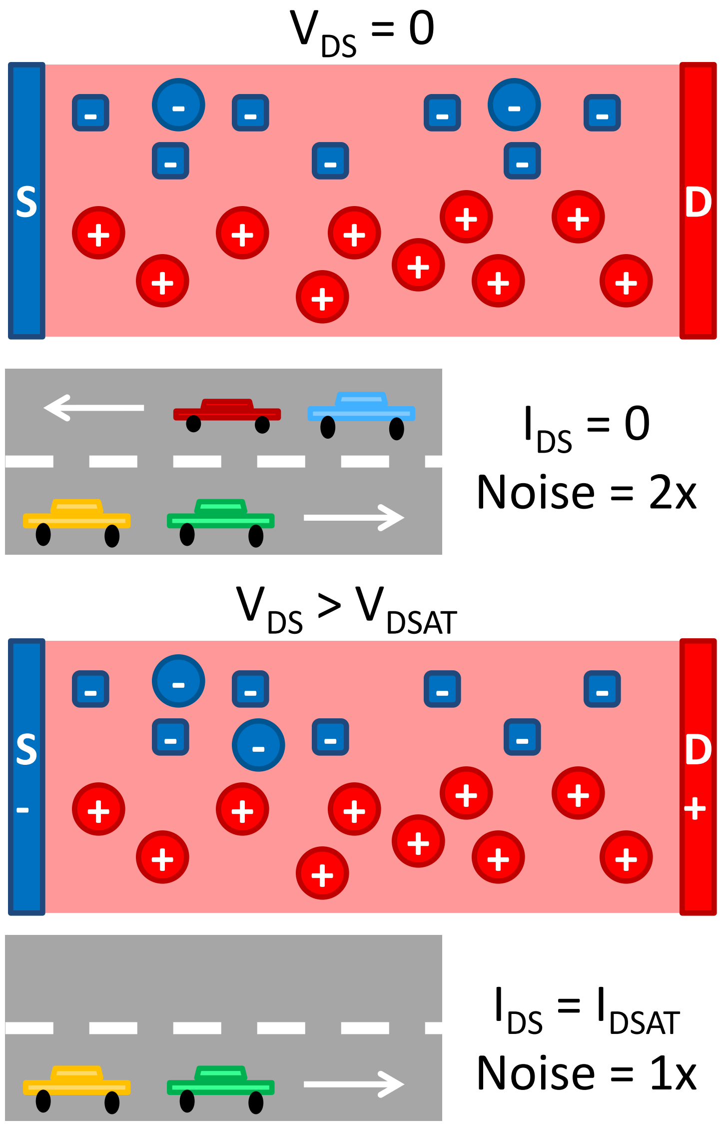


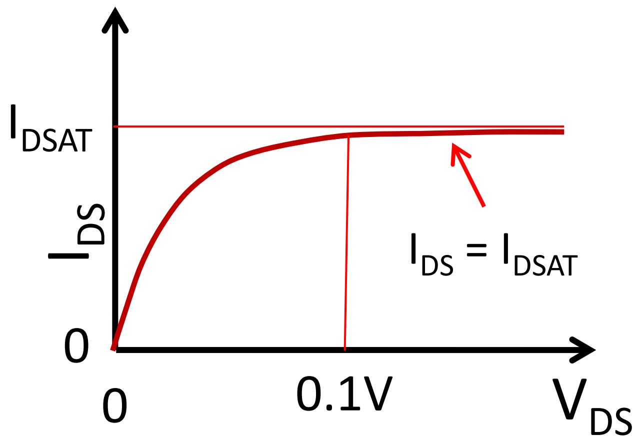
- Current PSD: $S_I^2(f) = 4kTG$
- Voltage PSD: $S_V^2(f) = 4kTR$

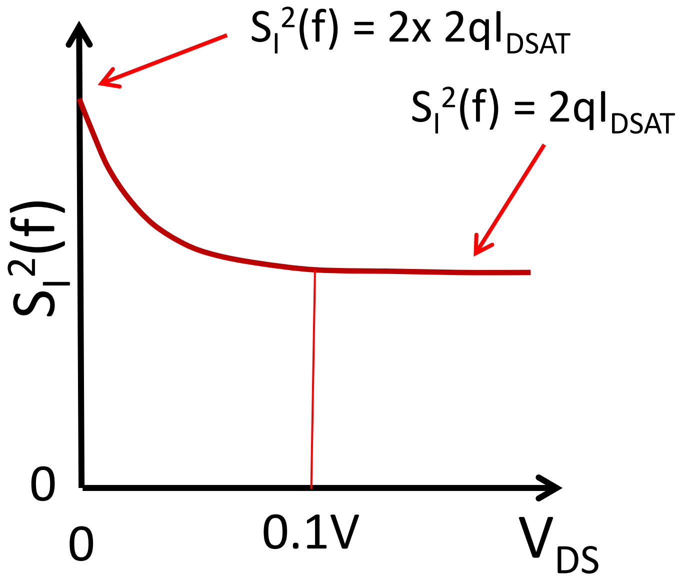
- $S_V^2(f) = S_I^2(f) \cdot R^2$

- The direction of a noise source doesn't matter, as they are random sources with average 0.

Sub-Threshold MOSFET Noise

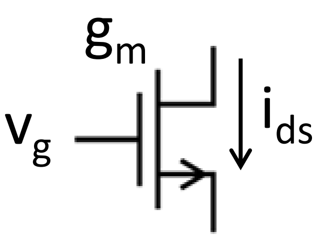


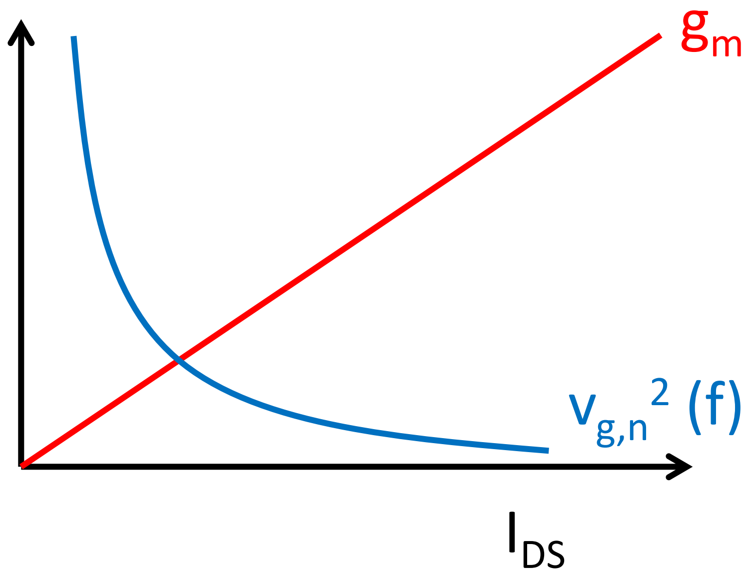




Sub-Threshold Noise, Gain and Power

- In saturation:
  - $g_m = K_s/\Phi_t \cdot I_{DSAT}$ ($\Phi_t \approx 25mV$, $K_s/\Phi_t \approx 27$)
  - $S_I^2(f) = 2qI_{DSAT}$
  - $v_{g,n}^2(f) = S_I^2(f) / g_m^2 \approx kT / 9I_{DSAT} \approx (4kT \cdot {}^2/_3) / g_m$





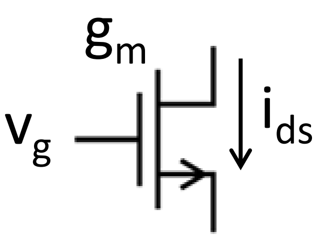
More power (I_{DS}):

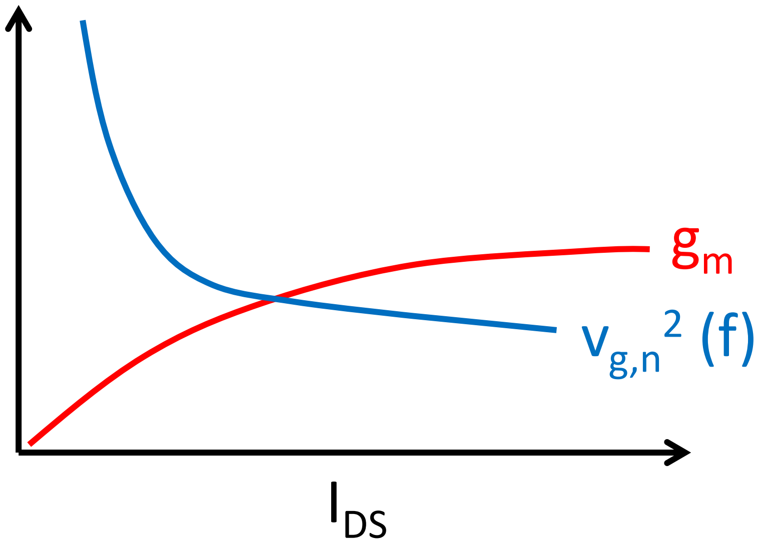
- Proportionally higher g_m
- Lower input-referred noise

$v_{g,n}^2(f) \propto 1 / I_{DSAT} \propto 1 / g_m$

Above-Threshold Noise, Gain and Power

- In saturation:
  - $g_m \propto \sqrt{I_{DSAT}}$
  - $S_I^2(f) = (4kT \cdot {}^2/_3) \cdot g_m$
  - $v_{g,n}^2(f) = S_I^2(f) / g_m^2 \approx (4kT \cdot {}^2/_3) / g_m \propto 1 / \sqrt{I_{DSAT}}$



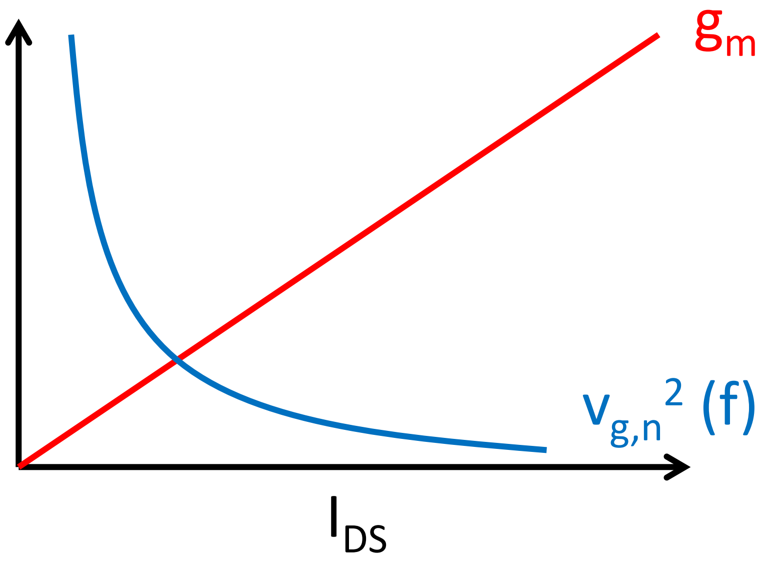


More power (I_{DS}):
- Higher g_m, but only with $\sqrt{}$
- Lower input-referred noise, but only as:

$v_{g,n}^2(f) \propto 1 / \sqrt{I_{DSAT}} \propto 1 / g_m$

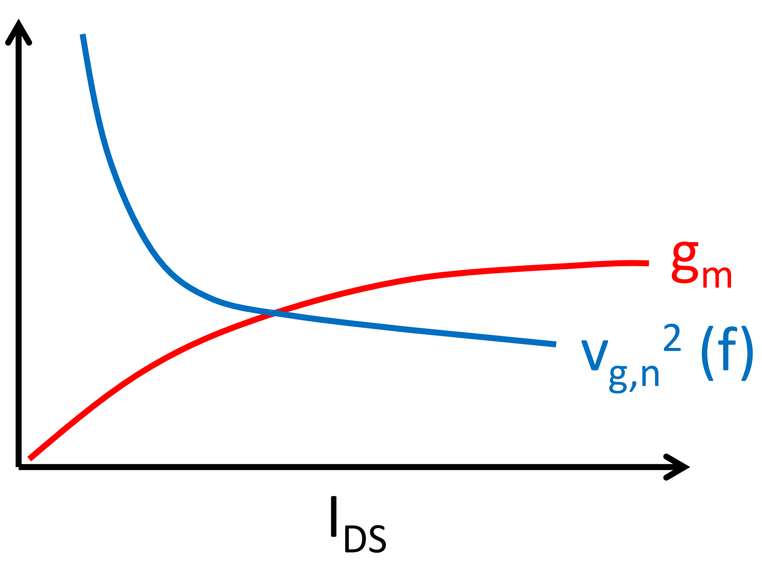
Sub/Above-Threshold Comparison

Sub-Threshold



- $g_m \propto I_{DSAT}$
- $v_{g,n}{}^2(f) \approx (4kT \cdot 2/3) / g_m$
- $v_{g,n}{}^2(f) \propto 1 / I_{DSAT}$

Above-Threshold

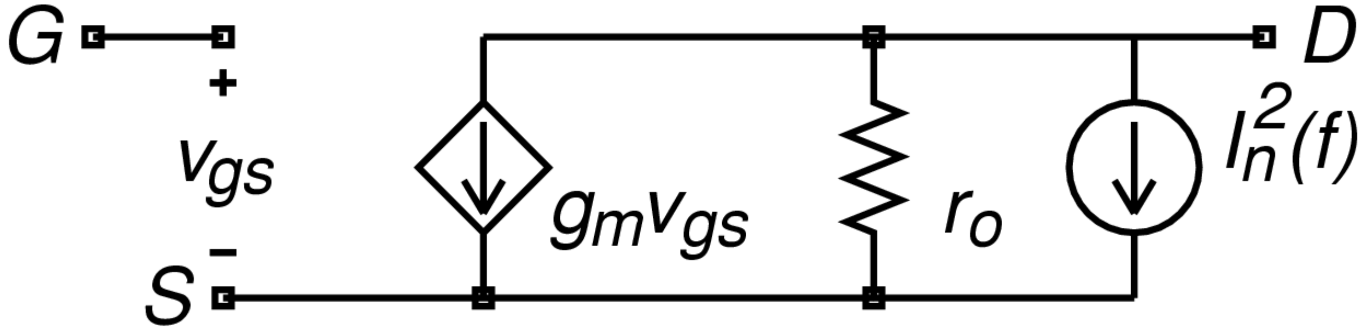


- $g_m \propto \sqrt{I_{DSAT}}$
- $v_{g,n}{}^2(f) \approx (4kT \cdot 2/3) / g_m$
- $v_{g,n}{}^2(f) \propto 1 / \sqrt{I_{DSAT}}$

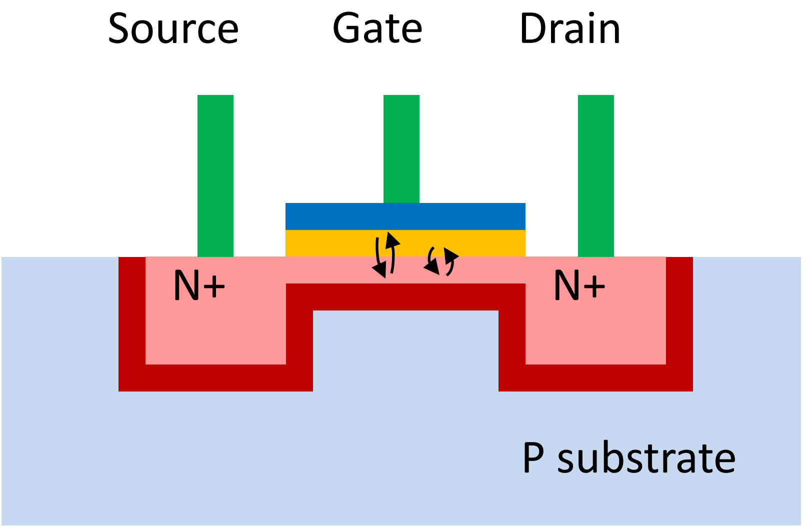
Sub-Threshold more power efficient: higher g_m and lower $v_{g,n}{}^2(f)$ for the same I_{DS}

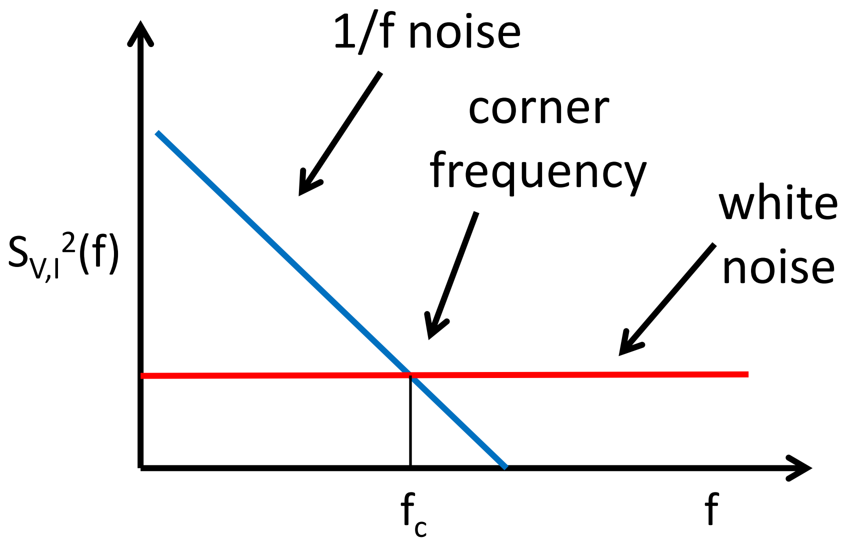
NMOS Small-Signal Model (in Saturation)

- $g_m \cdot v_{gs}$ represents the transconductance
- r_o represents the finite output resistance
- $I_n^2(f)$ represents the transistor's noise



1/f or Flicker Noise





- Not as fundamental as shot noise
  - Depends on a.o. technology, purity, PMOS or NMOS, area (WL)
- Still largely empirical; limited understanding
  - Charges get trapped in the isolation layer, released after delay
  - Deeper trap has a higher energy level but takes longer → 1/f nature

1/f in Transistors

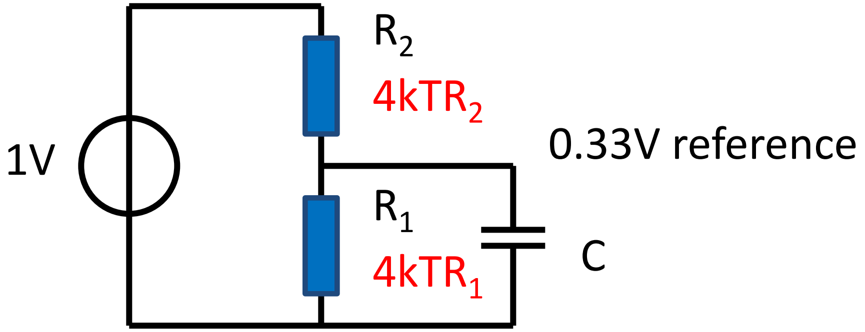
$S_I^2(f) =$

$K\, I_{DS}^2 / f$	in sub-threshold
$K\, I_{DS} / f$	in above-threshold
$\propto g_m^2 / f$	in both cases

- Improve 1/f noise performance by:
  - – Increase area WL
  - – Use PMOS instead of NMOS
  - – Use bipolar transistors
  - – Use special circuit techniques, e.g. chopping

Noise in Circuits

- Resistive divider with capacitor



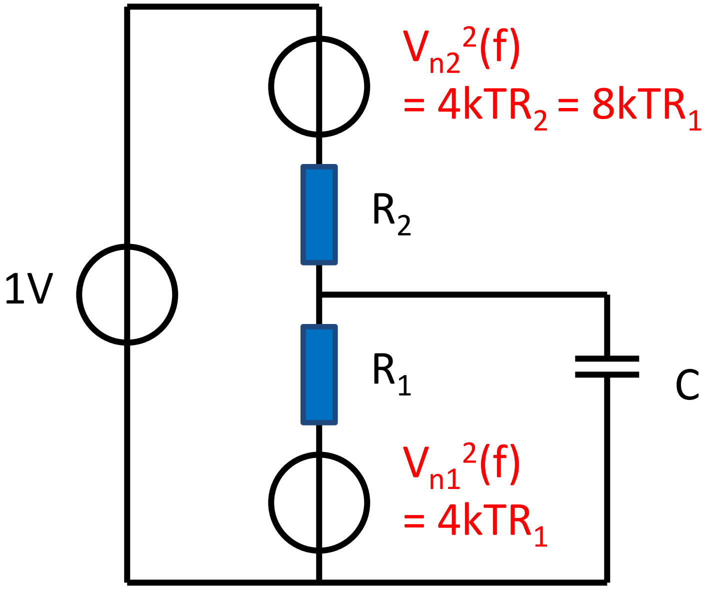
$V_{out} / V_{in} = R_1 / (R_1 + R_2)$

$R_2 = 2\ R_1$

- How to choose R_1 and R_2?
  – $R_1 = 1\Omega$, $R_2 = 2\Omega$?
  – $R_1 = 1G\Omega$, $R_2 = 2G\Omega$?

Adding Noises

- Superposition: noise contributions can be added together, but in the power domain!



$H_{n1}(s) = R_2 / (R_1 + R_2)$
$H_{n2}(s) = R_1 / (R_1 + R_2)$

For $R_2 = 2R_1$: $H_{n1}(s) = {}^2/_3$; $H_{n2}(s) = {}^1/_3$

$V_{nout}^2(f) = V_{n1}^2(f)\ |H_{n1}(f)|^2 + V_{n2}^2(f)\ |H_{n2}(f)|^2$

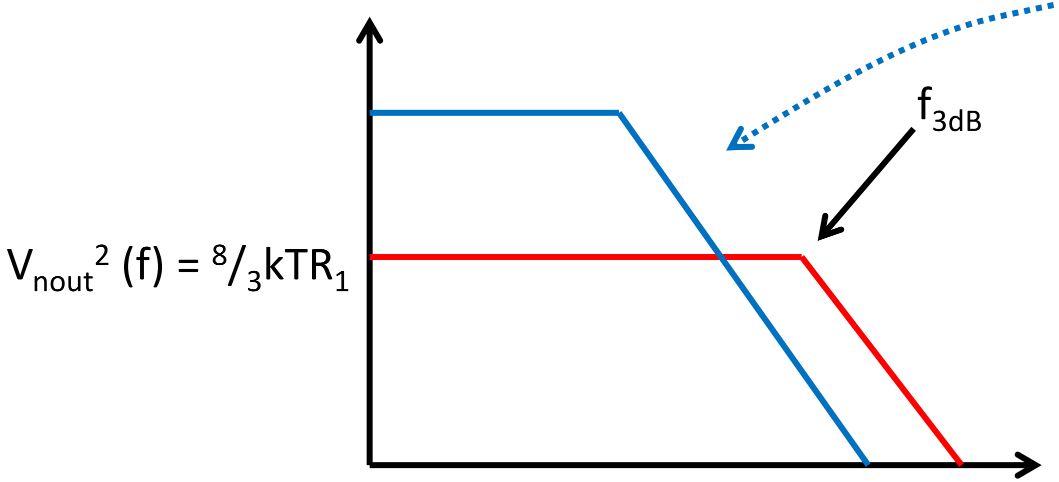
For given values:

$V_{nout}^2(f) = 4kTR_1\ ({}^2/_3)^2 + 8kTR_1\ ({}^1/_3)^2 = {}^8/_3 kTR_1$

- C was ignored until now: what is its influence?

Influence of Capacitor

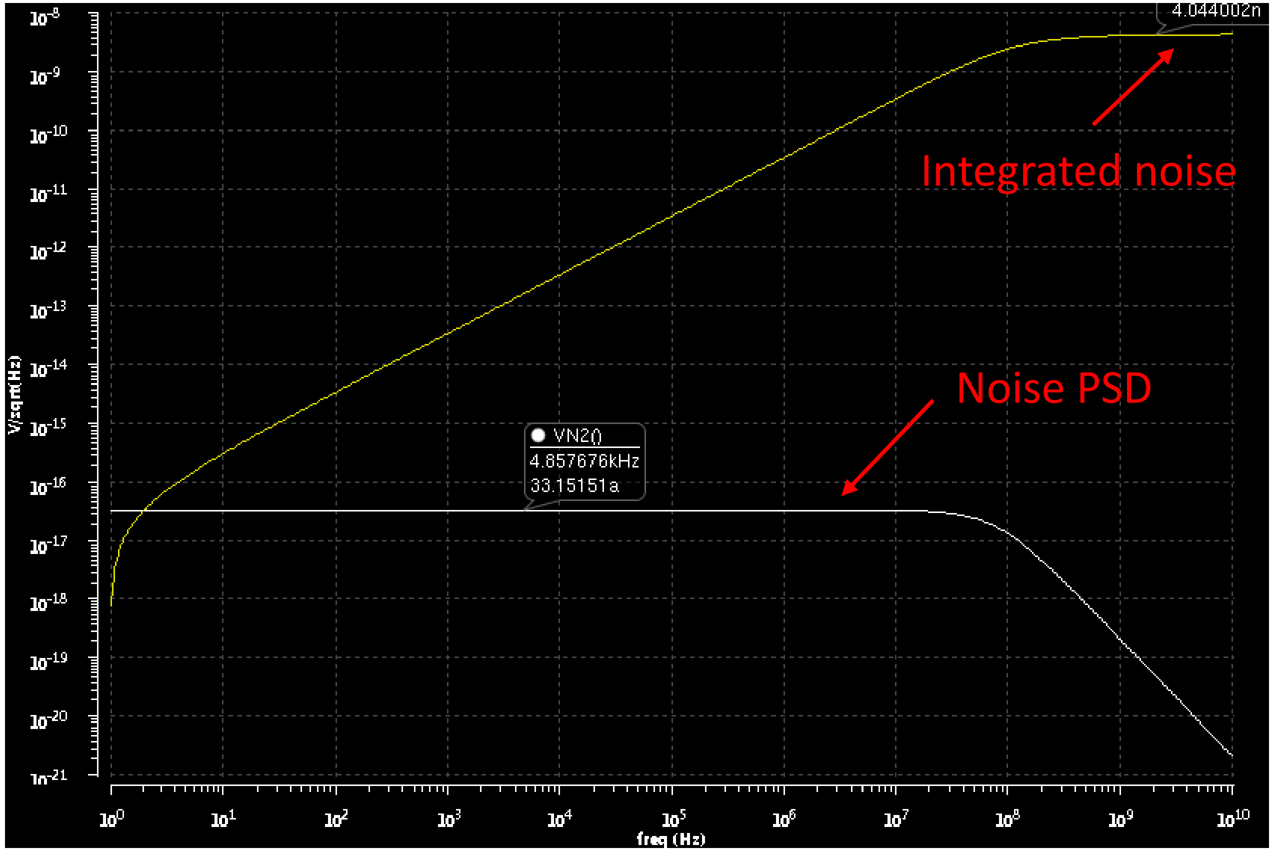
- Low-pass filter with cut-off:
  $f_{3dB} = 1 / 2\pi R_{eff}C$, $R_{eff} = R_1R_2 / (R_1 + R_2)$



- $P_{nout} = \int V_{nout}^2 (f) = kT/C$, independent on R_1 and R_2!
- Higher R_1 and R_2 increases noise PSD at low frequencies, but reduces bandwidth, resulting in the same total noise power

Cadence AC Noise Simulation

- $R_1 = 3k\Omega$, $R_2 = 6k\Omega$, $C = 1pF$
- $^8/_3 kTR_1 = 33aV^2/Hz$, $kT/C = 4.1nV^2$



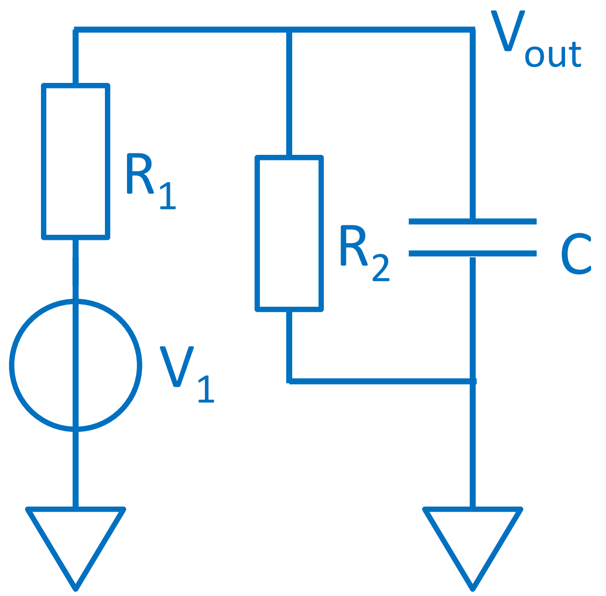
Exercise 2: Noise in an RC Network

Consider the circuit composed of a DC voltage source V_1 = 1V, two resistors R_1 = 1MΩ, R_2 = 2MΩ, and a capacitor C = 10pF. Both R_1 and R_2 generate thermal noise.

a) Calculate the DC output voltage V_{out}.

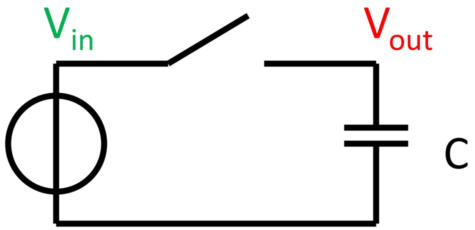
b) Calculate the noise power spectral density at the output V_{out} for very low frequencies. (so you can ignore C)

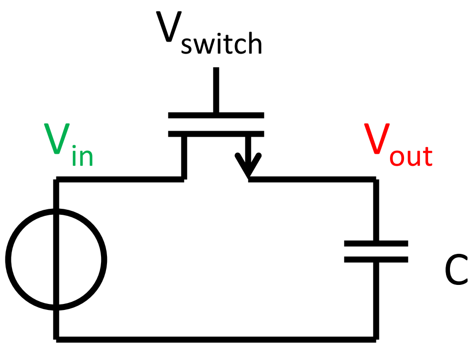
c) What is the total integrated noise power at output V_{out}?

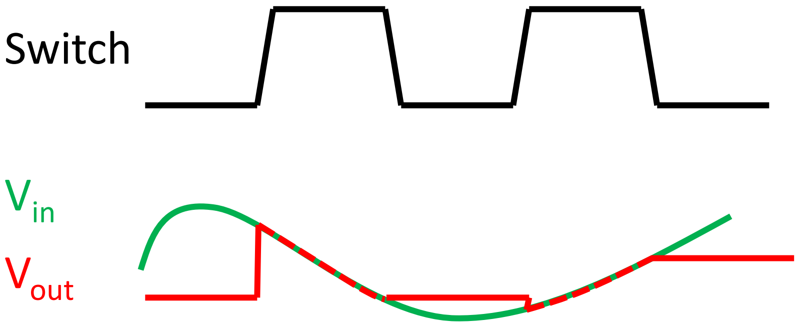


Sampled Noise

- Switched Capacitor networks; Sample&Hold (S&H) for ADCs







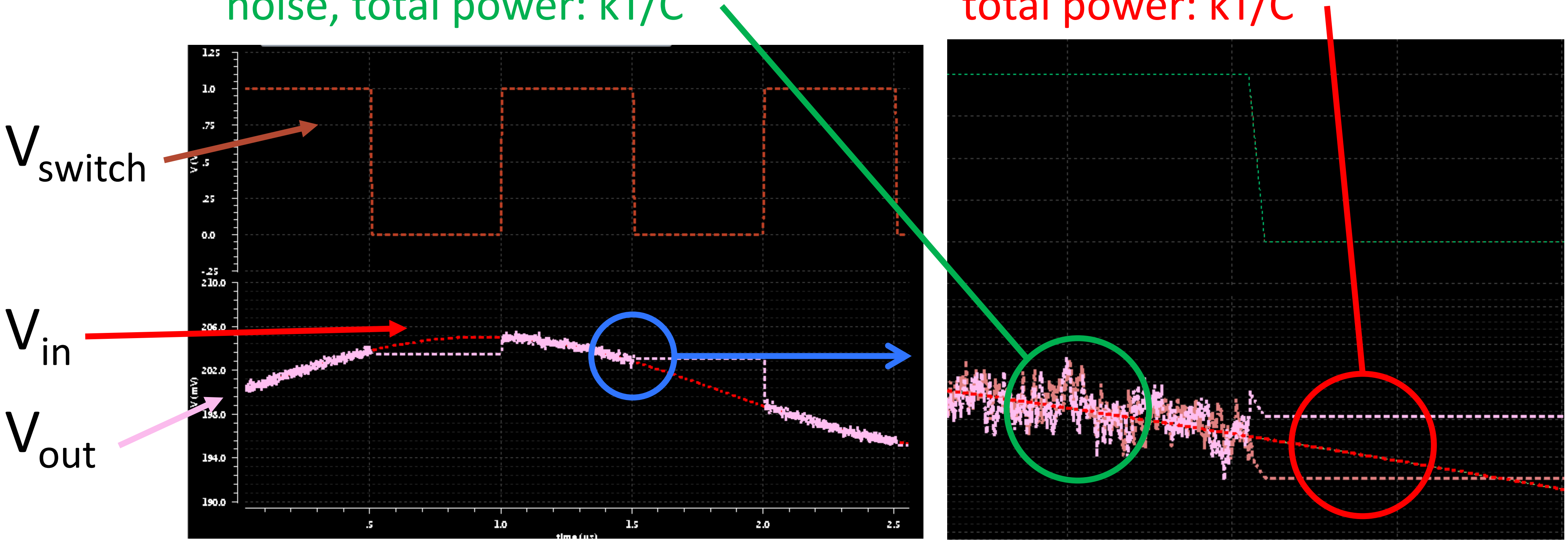
- Transistor in linear mode or saturation?
  - Linear mode, it is a switch with $V_{ds} \approx 0V$
- How is the transistor modeled in this mode?
  - As a resistor: r_{on}
- What is the noise model?
  - $S_V^2(f) = 4kTr_{on}$, just like a resistor!
- What is the total noise power at the output?
  - $P_{nout} = kT / C$
- What does the noise look like in the time-domain?
  - 2 phases; continuous noise and sampled noise

Cadence Transient Noise Simulation

- At the sampling moment, the S&H takes a sample of:
  (1) the input signal PLUS (2) the instantaneous noise

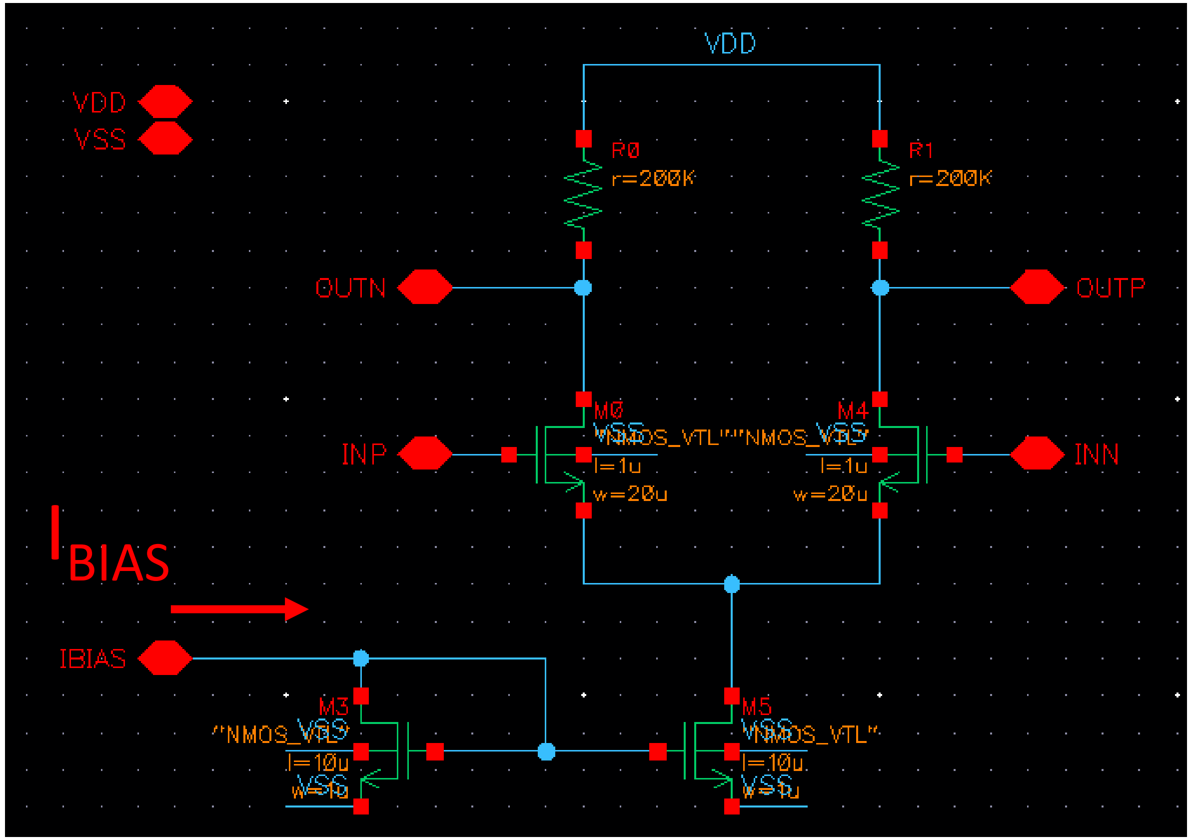
Switch closed: continuous noise, total power: kT/C

Switch open: sampled noise, total power: kT/C



Basic Differential Pair Amplifier

- VDD = 1V, I_{BIAS} = 2μA, R = 200kΩ, sub-threshold, current mirror 1:1
- I_{DS} = 1μA
- g_m = 25μA/V
- $A_0 = g_m r_{out} = 5$
- $v_{nout}^2(f) = 2 \cdot 2qI_{DS}\,[r_{out}]^2 = 26\text{fV}^2/\text{Hz}$
- $v_{nin}^2(f) = v_{nout}^2(f) / A_0^2 = 1\text{fV}^2/\text{Hz}$



Cadence Simulation Results

- I_{DS} = 0.9µA (1µA)
- g_m = 22µA/V (25µA/V)
- A_0 = 4.4 (5)
- $v_{nout}^2(f)$ = 40fV²/Hz (26fV²/Hz)
- $v_{nin}^2(f)$ = 2fV²/Hz (1fV²/Hz)

DC simulation

gm	22.12u
gmbs	4.359u
gmoverid	24.57
ibulk	-48.78p
id	900.1n

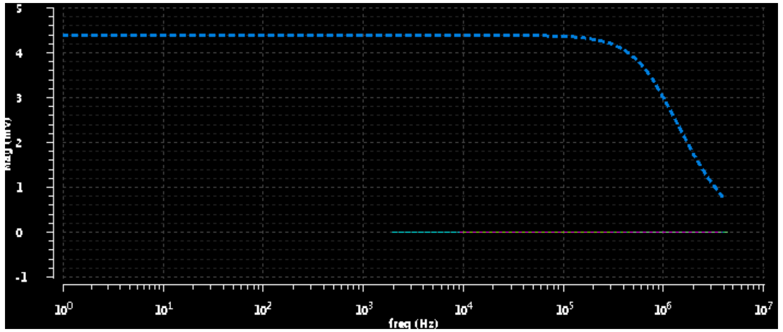
Noise simulation

Device	Param	Noise Contribution	% Of Total
/I5/M0	id	1.64082e-14	40.55
/I5/M4	id	1.64082e-14	40.55
/I5/R1	rn	3.24862e-15	8.03
/I5/R0	rn	3.24862e-15	8.03
/I5/M0	fn	5.72244e-16	1.41
/I5/M4	fn	5.72244e-16	1.41
/I5/M4	igd	1.27403e-18	0.00
/I5/M0	igd	1.27403e-18	0.00
/I5/M0	rgbi	8.46603e-19	0.00
/I5/M4	rgbi	8.46603e-19	0.00

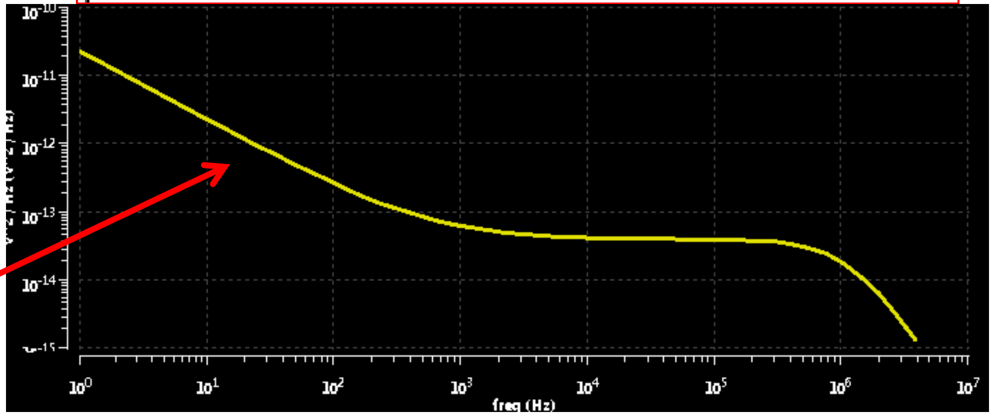
Spot Noise Summary (in V^2/Hz) at 20K Hz Sorted By Noise Contributors
Total Summarized Noise = 4.04625e-14
Total Input Referred Noise = 2.11258e-15
The above noise summary info is for pnoise data

Noise from resistors (4kTR)

AC simulation: gain



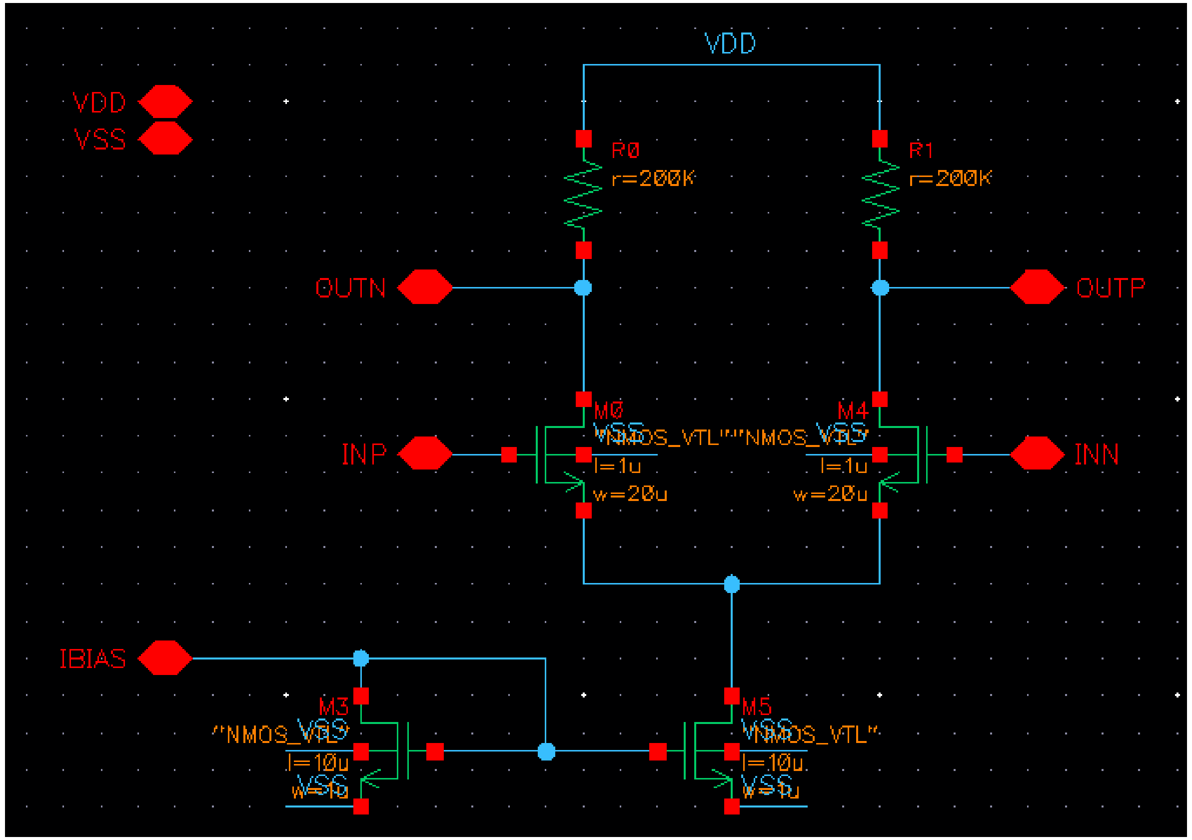
Lot of 1/f noise



Exercise 3: Amplifier Noise

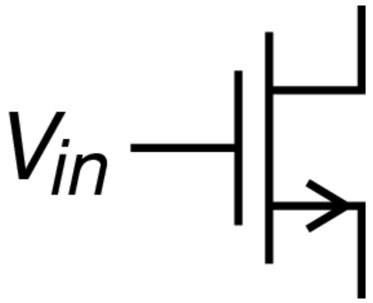
Given: VDD = 1V, I_{BIAS} = 2μA, R = 200kΩ, sub-threshold, current mirror 1:1

a) Calculate the input-referred noise power spectral density (as on the previous slides), but now account for the 4kTR noise of the two load resistors.



Exercise 4: Design for Noise

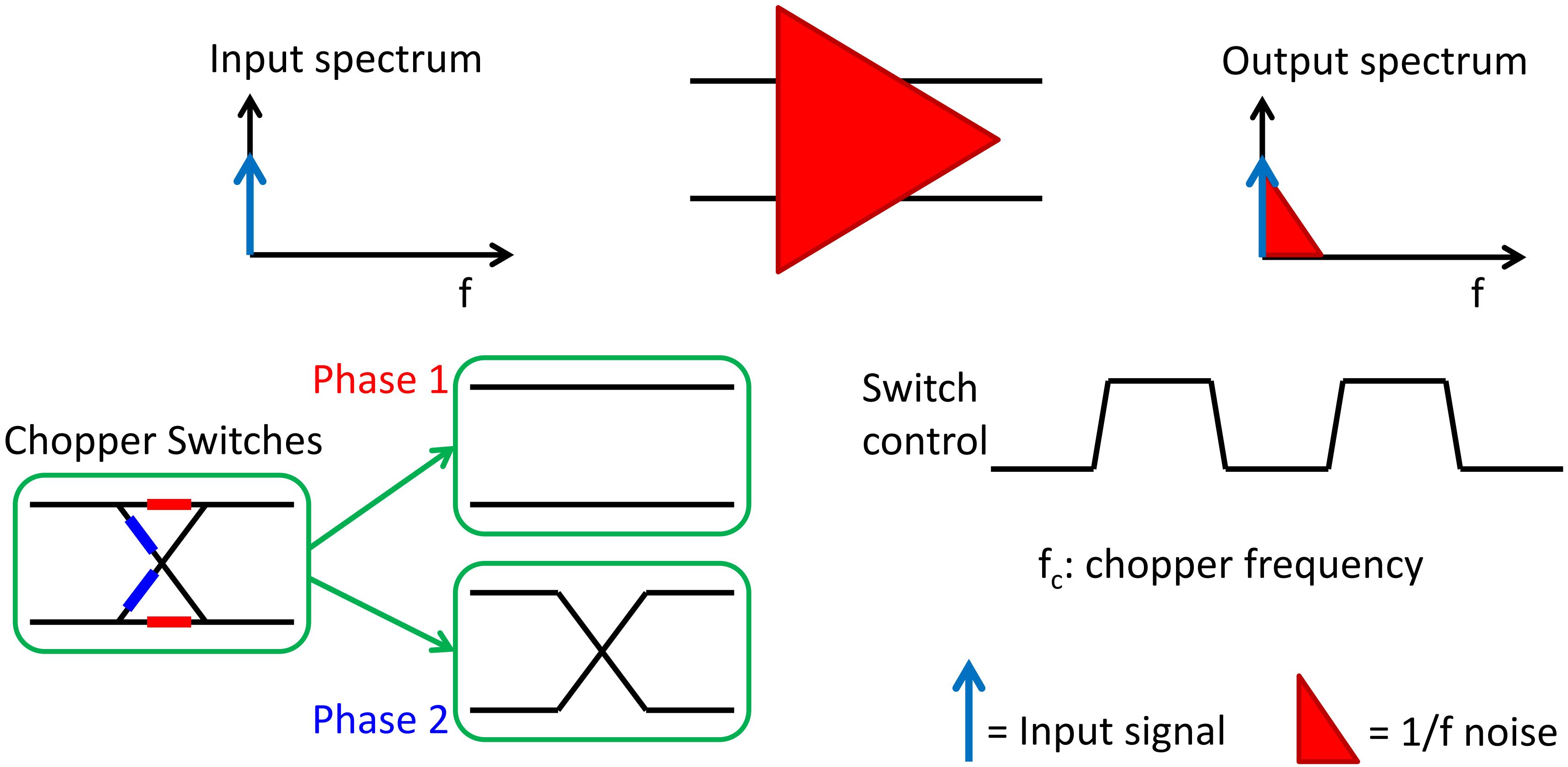
- Considering just a single transistor
- Assume it is biased in weak inversion and saturation
- Our goal is to have an input referred noise of $0.4\mu V_{rms}$ in a bandwidth from 0 to 400Hz



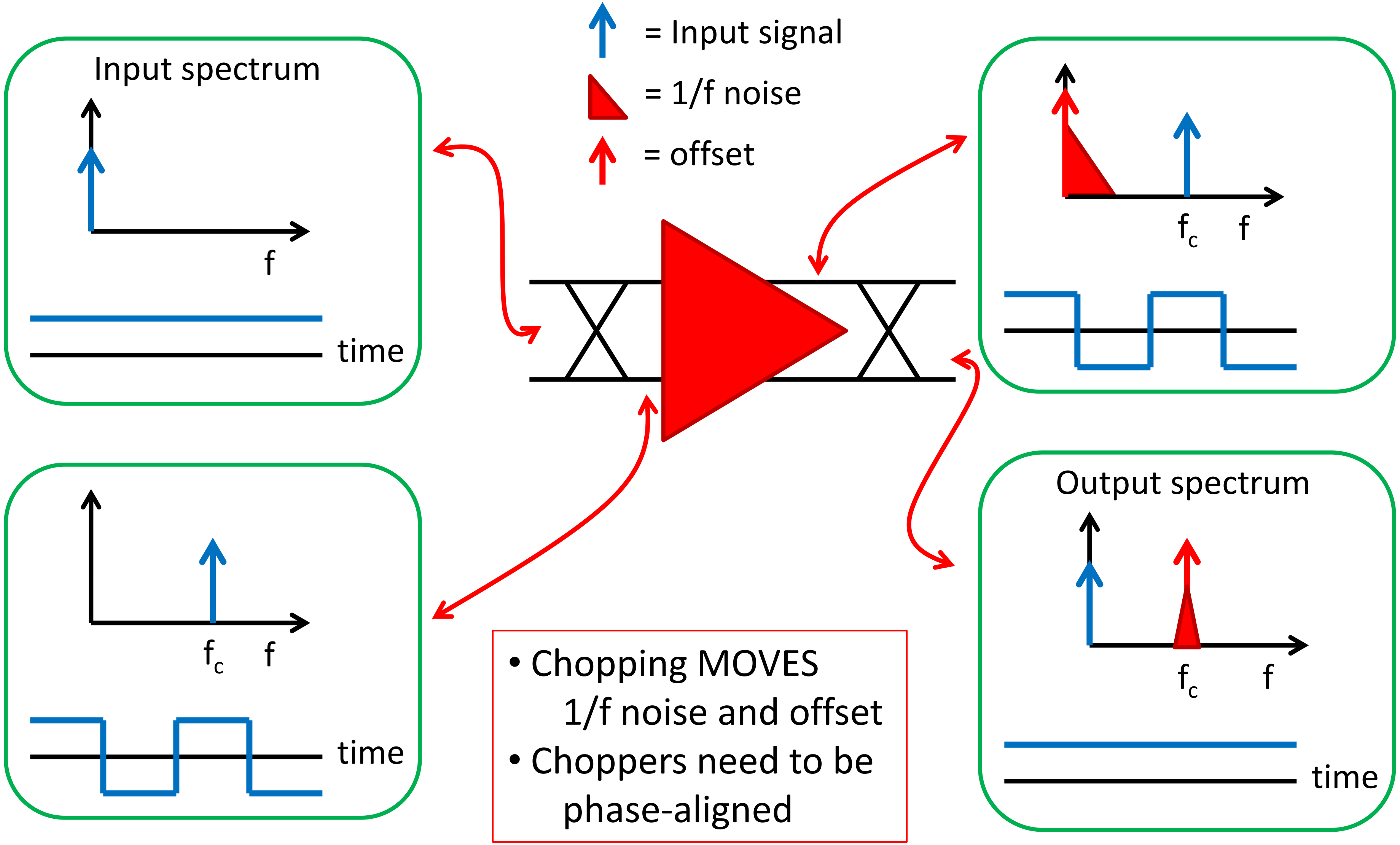
a) Calculate the noise power spectral density
b) Calculate the required g_m for this transistor
c) Calculate the required bias current I_{DS} for this transistor

Chopping Amplifier (1)

- Amplifier with 1/f noise (and/or offset)
- Input signal is a DC level

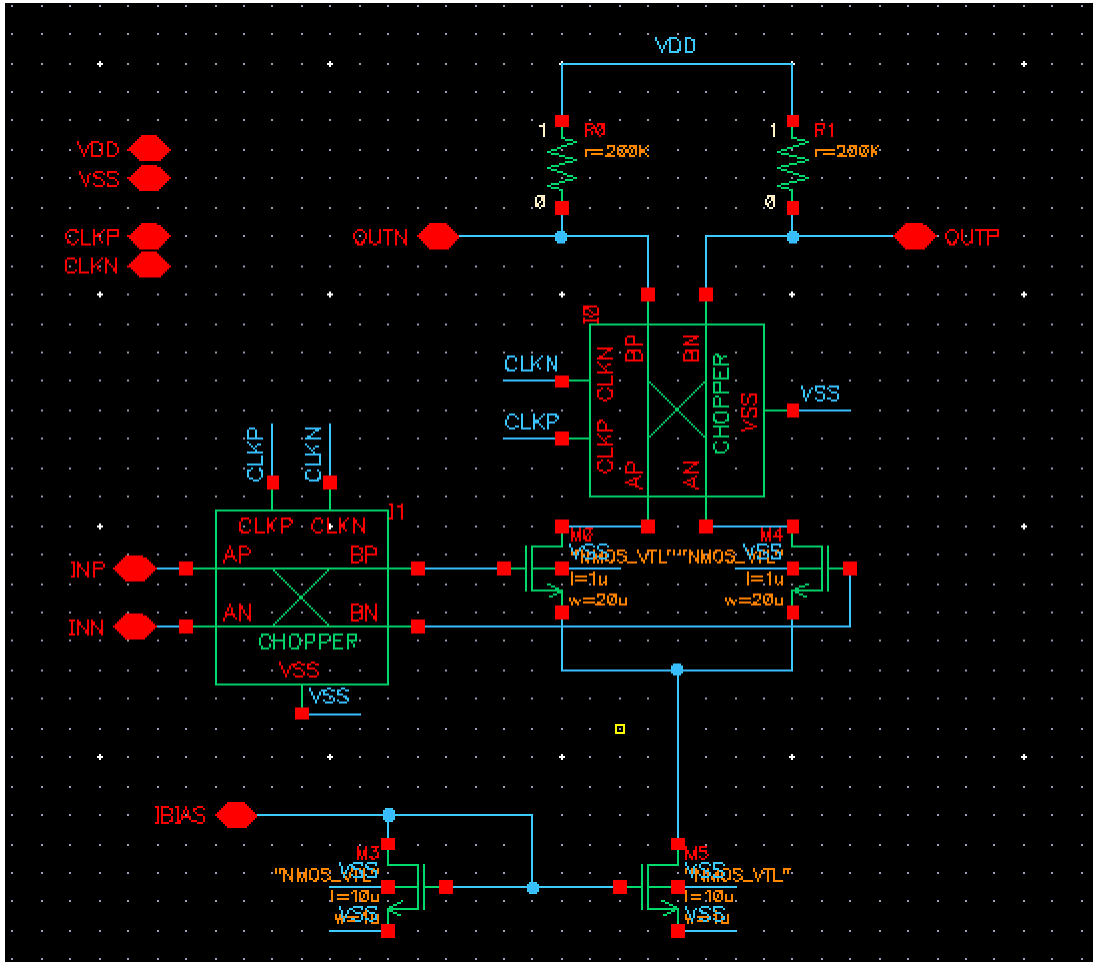


Chopping Amplifier (2)



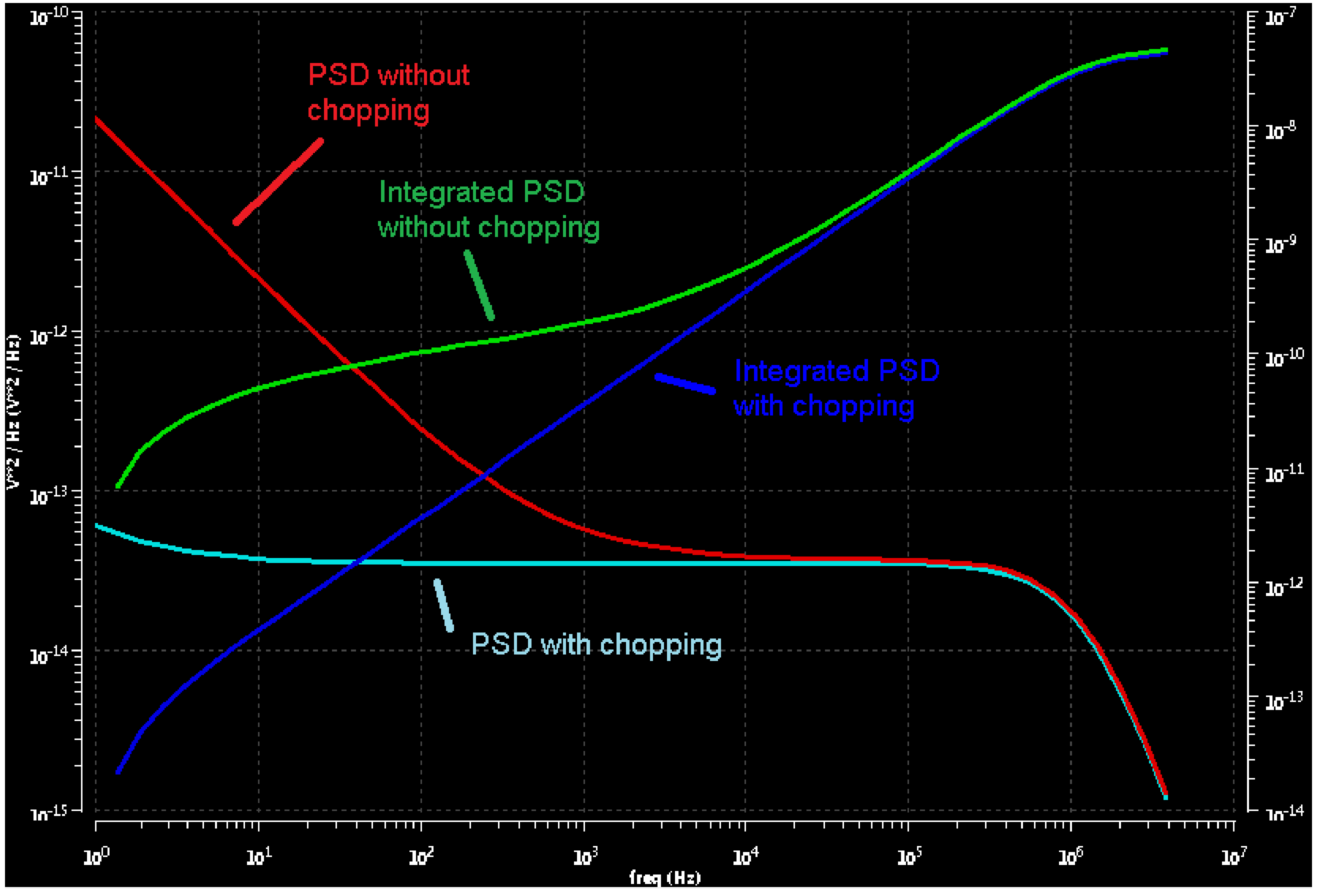
- Chopping MOVES 1/f noise and offset
- Choppers need to be phase-aligned

Differential Pair with Chopping



Cadence Simulation Results

- Chopping reduces 1/f noise



Noise Simulations

- Noise: AC (small signal) noise simulation
  - Only possible for circuits with a DC point → Circuits with static bias
  - Not valid for time-variant systems (e.g. circuits with dynamic operation)
- Periodic noise or transient noise simulation
  - Can be used for time-variant systems
    (e.g. chopping amplifiers, switched-capacitor circuits, comparators)

Summary

- Devices: MOS transistors
  - Diffusion & Drift
  - Above-threshold & Sub-threshold operation
  - Power-efficiency
- Noise
  - Shot noise, 1/f noise
  - Noise in devices
  - Noise in circuits
  - Simulation in Cadence

Solution 1: SNR

a) $\frac{1}{2}A^2 = 0.5\mu V^2$

b) $V_n(f) = 3\mu V/\sqrt{Hz} \rightarrow V_n^2(f) = 9pV^2/Hz \rightarrow P_{noise} = V_n^2(f) \cdot BW = 900pV^2$

c) $V_{n,rms} = \sqrt{(900p)} = 30\mu V$

d) $SNR = 10 \log_{10} (P_{signal} / P_{noise}) = 27.4dB$

Solution 2: Noise in an RC Network

a) $V_{OUT} = 0.667V$

b) $V_{n,out}^2(f) = 4kTR_p$, where $R_p = R_1R_2 / (R_1 + R_2) = 11fV^2/Hz$

c) $V_{n,out,rms}^2 = kT / C = 0.4nV^2$

Solution 3: Amplifier Noise

a)

- $I_{DS} = 1\mu A$
- $g_m = 25\mu A/V$
- $A_0 = g_m r_{out} = 5$
- $v_{nout}^2(f) = \{2 \cdot 2qI_{DS} + 2 \cdot 4kT/r_{out}\}[r_{out}]^2 = 32fV^2/Hz$
- $v_{nin}^2(f) = v_{nout}^2(f) \;/\; A_0^2 = 1.3fV^2/Hz$

Solution 4: Design for Noise

a) $V_{n,rms}^2 = 0.16pV^2 \rightarrow V_n^2(f) = 0.4fV^2/Hz$

b) Assuming $V_n^2(f) = (4kT \cdot {}^2/_3) / g_m \rightarrow g_m = 27.6\mu A/V$

c) Assuming $g_m = 27I_{DS} \rightarrow I_{DS} = 1\mu A$