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Displacement-controlled coining of large arrays of gold stud bumps

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Abstract

A novel, simple, and low-cost displacement-controlled coining (DCC) process is developed for the coining of gold stud bumps. A bottom mold made of aluminum, which contains an array of geometrically well-defined cavities (nests) with known and pre-defined depth values in each nest, is designed and manufactured to adjust areas of coined surfaces and heights of coined stud bumps during the sequential DCC processes. A double-side-polished and thick borosilicate glass substrate is used as a flat surface to be in direct contact with the tails of the stud bumps to be coined. Above the glass substrate, another thick and rigid mold is positioned to uniformly apply the displacement-controlled deformation force to the stud bumps via the polished surface of the glass substrate. With the proposed DCC process, the height and bonding surface area of the stud bumps can be tailored for flip-chip bonding (FCB) processes, especially when the maximum applicable force configuration of the FCB tool is limited (maximum of 20 N) during thermo-sonic flip-chip bonding (TSFCB) processing. The proposed technique can be used to simultaneously coin arrays of stud bumps with high precision, providing an alternative, cost-effective, precise, and time-efficient processing of stud bumps prior to TSFCB applications.

Supplementary material for this article is available online

Keywords: stud bump, coining, flip-chip bonding, displacement control, stopper, wire bonding, limited force

List of all acronyms used in the research article:

ASIC	application-specific integrated circuit
CNC	computer numerical control
CRC	coining rate controlled
DCC	displacement-controlled coining
FAB	free air ball
FCC	force-controlled coining
FCB	flip-chip bonding
GSB	gold stud bump
HAZ	heat-affected zone
MEMS	micro-electro-mechanical systems
SAC	stopper-adjusted coining
SEM	scanning electron microscope
SCS	semiconductor characterization system
SCC	stopper-controlled coining
SLC	stopper-limited coining
TAB	tape automated bonding
TSFCB	thermo-sonic flip-chip bonding

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1. Introduction

Depending on the required connection applications between pairing chips, stud bumps may require flat connection surfaces, adjusted stud bump heights, or adjusted surface areas for good connections between the paired chips. Coining is a type

of controlled deformation process that is used to satisfy these requirements for good electrical and mechanical connections between chips that need to be connected by flip-chip bonding (FCB) techniques. Having appropriate coining is one of the most critical processing steps for successful FCB applications.

According to the literature, the coining process is applied for gold stud bumps (GSBs) [1–10], copper stud bumps [11], and bumps of various solders [12–17]. Depending on the application, after the coining process, coined surfaces of the stud bumps are connected to Au pads [1], conductive adhesives [2, 11, 18–20], solder jetted spheres [2], solder bumps [12, 13], tape automated bonding (TAB), solder, or conductive adhesives [3, 4], or aluminum on PCB pads [5].

Materials can be coined by compressing the top of the stud bumps with a tool [1, 7], a polished and flat plate with uniform thickness, made of glass, silicon, or ceramic [21–24], flip-chip bonder equipment [2, 9, 15, 25, 26], a modified advanced tension/compression tester capable of adjusting the height, coining rate, and coining temperature [12–14], a wire bonder with a blunt flat tip [3, 4, 6], a low-cost in-house developed chemical mechanical polishing process [27], nanoimprinting (a.k.a microforging) [28], or a wafer bonder that is capable of applying a very large compressive force (i.e. 3.2 kN) on wafer-scale substrates [8].

While the majority of the published research emphasizes the importance of a flat surface, co-planarity, and bump height in the performed coining studies, the importance of the *surface area* that is formed after the coining process is rarely mentioned [2, 10, 29]. Furthermore, among the studies that mention the surface area after the coining process [2, 10, 29], very few emphasize the importance of the applied pressure in the coming process step (i.e. the FCB process after the coining process) [10]. However, none of these articles needed to explain the process parameter details of the types of coining processes. Hence, in the publicly available scientific literature, it is not obvious how the coining process can obtain stud bumps with such adjusted surface areas. From this perspective, the studies conducted herein give very detailed coining process information about a novel method that can be used to obtain adjusted and known surface area values for specific pressure values that may be needed during thermo-sonic flip-chip bonding (TSFCB) processes with limited force application configurations of the FCB tools.

The 'coining' process in FCB applications refers to a mechanical flattening step applied to the top of the stud bumps (or solder bumps) before the actual FCB process is performed. The primary goal of the coining process is to improve the uniformity, planarity, and co-planarity of the bumps to ensure better contact between the chip and the substrate, or between the chips, during the bonding process.

For FCB applications, the coining processes in the research literature can be widely classified under force-controlled coining (FCC), with very few exceptions that may be classified as coining rate-controlled (CRC) coining [12].

During FCC, a certain amount of force is applied to the uncoined surfaces of the stud bumps (i.e. force/bump) in order to flatten the top surface of the stud bumps. The FCC process continues until a force balance is reached between the forces applied by the force actuator (i.e. the FCB tool) and the reaction force from the stud bump under FCC. In such FCC approach, the applied force is the main definer of the final geometry of the coined stud bump. During CRC coining, the speed (μm s^{-1}) of the flat coining tool is controlled, and the coining force is usually measured as an output of the CRC coining.

Another coining approach, which has not been explored so far, is the displacement-controlled coining (DCC) (or, stopper-controlled coining (SCC), stopper-adjusted coining (SAC), or stopper-limited coining (SLC)) process, where the stud bump under the coining deformation process is required to deform only for a certain deformation distance, and not more (or less) than that distance. In DCC (or SCC, SAC, or SLC), the applied force is still important and required to deform the uncoined stud bump. However, in DCC, the main controlled parameter is the amount of displacement that the uncoined tip of the stud bump is required to deform by a stiff and flat coining surface. Hence, the stiff and flat coining surface is allowed to progress only for a certain distance by some type of stiff mechanical 'stopper surface' to prevent further displacement (further progress) of the stiff and flat coining plate that is applying the displacement for the coining of the stud bumps. Unlike FCC and CRC coining, as demonstrated in the next sections of the manuscript, the DCC process does not require complicated or expensive equipment because there is no force control or CRC in the DCC process. In fact, in the DCC process, there are stoppers (stopper surfaces) or nests (cavities) with known depths that allow only the planned amount of displacement for the flattening of the uncoined surfaces of stud bumps (i.e. part of the variable tail height of a stud bump) that are initially protruding upward from the reference stopper surface of the nest (see figure 1). The reason for the variable tail height is explained in the coming paragraphs of this section.

From another point of view, readers may find a significant analogy between how comb-actuator or electro-static micro-electro-mechanical systems (MEMS) devices are prevented from the pull-in (snap-in, snap-down) instability [30–33], and how a stud bump is coined under displacement control. For example, comb actuators or electro-static MEMS devices are manufactured with stoppers, where these stoppers do not allow further movement of the mobile fingers of the comb actuators even if the needed force is available, but this available force is balanced by fixed-position stoppers to prevent further displacement of the mobile part of the comb actuator. Similar to the stoppers in MEMS devices, the top surface of the mold containing the nest (see figure 1), where the chip with uncoined stud bumps is positioned, can be considered as the stopper surface to prevent further progress of the flat surface that is used

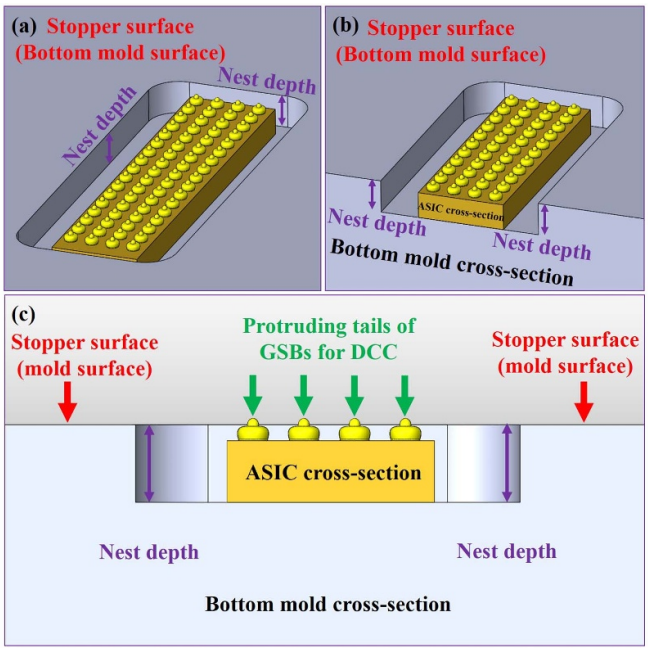


Figure 1. DCC process. (a) A chip is placed inside a nest (cavity) with known depth that is formed inside a rigid bottom mold. The top surface of the mold is the stopper surface during the DCC process. The depth of the nest defines how much displacement deformation will be applicable on the uncoined stud bumps. (b) Cross-section of the nest where the chip with uncoined stud bumps is positioned. (c) Cross-sectional view showing the uncoined or protruding tails of GSBs that need to be coined to adjust the needed surface area/bump and pressure/bump that is needed in the coming TSFCB process step under limited maximum applicable force configuration of the FCB tool.

to apply the displacement to deform only the needed part (protruding part) of the top surface of the uncoined tail part of the stud bumps.

According to the published literature, none of the studies needed to be studied under limited TSFCB force configuration during the TSFCB process. In other words, studies in the published literature so far always had a sufficient amount of compressive force per bump (i.e. force/bump) during TSFCB processes; hence, researchers have rarely needed to carefully adjust the surface areas of the coined surfaces of the GSBs for specific pressure/bump requirements during the TSFCB process. Furthermore, while the importance of preventing potential substrate or PCB damage due to excessive force during coining is emphasized with suitable solutions [12], none of the publicly available literature emphasized the importance of having stopper features or nests (cavities) to limit the excessive force that may be applied on the GSBs or connection pads below the GSBs, and to limit and adjust the surface area of GSBs for pressure/bump adjustments during the subsequent TSFCB process (see figures 1 and 5). From this perspective, the novel studies conducted in this research paper reveal all the details about how to work under limited TSFCB force conditions and inside a nest (cavity) where the top surface of a nest is deliberately used to stop the deformation due to excessive force that may originate from the coining process.

To have better control over the surface area adjustment during the DCC process, the process is repeated (with reduced nest depth in each repetition) until the required surface area of the coined stud bumps is reached. For the first 'coined surface area' adjustment and tail surface planarization study during the DCC process, the 'displacement' is the amount of displacement that the tails of the uncoined stud bumps are deformed or shortened due to compression by the polished surface of the borosilicate glass workpiece that presses on top of the initially uncoined tails of the GSBs. The stopper for the controlled-displacement is the flat top surface of the bottom mold that has nest (or cavity) geometries with known depth values. Hence, initially, when a chip with uncoined GSBs is positioned into a nest, the uncoined tails of the GSBs should have tails that protrude from the flat top surface level of the bottom mold that has the nest. Right after the first displacement-controlled coining process, the uncoined tails that were protruding from the top surface of the bottom mold that has the nest are coined only until the borosilicate glass workpiece with polished surface is in full contact with the flat top surface of the bottom mold that has the nest. After the first coining process, explained above, the same chip with the same GSB array is positioned in a shallower nest in the same bottom mold for the second coining process. Now, the compression by the polished surface of the borosilicate glass workpiece is repeated. Because there are again protruding tails (due to the shallower depth of the nest), these protruding tails are again coined only for the amount that is protruding from the flat top surface of the bottom mold. Hence, the second coining process is performed only for the amount of displacement that is protruding from the flat top surface level of the bottom mold. After the first DCC process, as well as after the second DCC process, the total coined surface area as well as the surface areas of individually coined GSBs can be calculated to understand if sufficient DCC is achieved to adjust the pressure that can be applied at the coined surface with the limited force (a maximum of 19 N force for 143 coined stud bumps in our case) that is available during a TSFCB process, which may not be sufficient to perform the FCB process for large arrays of GSBs. Here, it is important to emphasize that as the depth of the nest becomes shallower, the surface areas of the GSBs become wider. Hence, widening the surface areas of GSBs more than needed works against the limited force capability of the FCB tool that is needed during the TSFCB process. To prevent this, the DCC process must be done such that the surface areas of the GSBs are not deformed more than the needed surface area/bump or more than the needed pressure/bump during the TSFCB process.

Stud bump fabrication via a wire bonder offers an economical and reliable method for FCB applications. In addition, it is very suitable for research and development studies because researchers may need to change the design of substrates and stud bump dimensions at any time [34]. GSBs are widely used in applications of thermo-sonic FCB [21, 35–44],

thermo-compression FCB [45, 46], and conductive adhesive FCB [26, 47].

GSBs are fabricated by a modified wire bonding process called stud bump bonding. Fabrication starts in the same way as ball bonding. A ceramic capillary tool is attached to the horn of a wire bonder and wire is threaded inside the capillary tool. The electronic-flame-off capability of the wire bonder tool is used to create a free air ball (FAB). A capillary tool with an FAB at the tip of the capillary tool is pressed against a bonding pad on a chip to bond the FAB to the bonding pad. During the bonding step, a known amount of ultrasonic energy is applied to locally soften the contact sides of the FAB and bonding pad for the bonding between FAB and bonding pad, while the chip containing the bonding pads is kept preheated at a predefined temperature to help the interface bonding between the contact sides of the FAB and the bonding pad. Once the ball bonding is completed, the capillary tool moves upward and breaks the connection of the bonded FAB from the rest of the gold wire. Thus, a GSB is formed with a mushroom-like shape with a sharp tail. This entire process is repeated as many times as necessary to form the needed amount of GSBs [48].

A heat-affected zone (HAZ) occurs in the wire in regions of the wire that are close to the FAB, after the formation of the FAB. After the ultrasonic welding of the FAB, upward motion of the capillary tool breaks the wire randomly from a region within the HAZ. Therefore, GSBs have variable tail lengths after the stud bumping process. Variable tail lengths with large standard deviation are not suitable for FCB and TAB applications because large height differences between tails of GSBs can lead to unsuccessful bonding due to the uneven distribution of pressure in each stud bump, which causes misalignment during the FCB and TAB processes. To reduce the deviation in the variable tail length, the upward motion of the capillary tool when breaking the wire and ball connection may be performed in a specified upward motion trajectory. Furthermore, a flat surface on top of the GSB is preferred for reliable bonding. As mentioned before, a process called 'coining' is used for leveling the heights and flattening the top surfaces of the GSBs. According to the literature, height-level variations of ± 5 μm or less may be required for reliable FCB and TAB applications [10]. Considering that more than two decades have passed since the publication of the information in [10], and that there are significant technological advancements in the FCB processing requirements, the FCB and coining requirements , including the requirements for minimal height-level variations, need to become stricter.

In this study, different from what has been proposed and carried out in the literature so far, a DCC process is developed for stud bump arrays. Furthermore, for TSFCB applications, using the tail height regions of the GSB for compressive pressure adjustments by DCC is also implemented. An aluminum rigid mold containing an array of chip nests (or cavities) with controlled depth values is designed and manufactured to control the displacement of deformation during the DCC process. Moreover, double-side-polished, relatively thick (3.3 mm) borosilicate glass is used as a flat surface that transfers the applied displacement and force to the stud bumps.

2. Method

2.1. GSB and pseudo ASIC chip fabrication

In this study, using microfabrication approaches, pseudo application-specific integrated circuit (ASIC) chips and pseudo MEMS chips, which are cheaper geometrical replicas of the real ASIC and MEMS chips, are designed and microfabricated for the development of the DCC and FCB processes to reduce the process development costs and to confirm the validity of the developed processes before performing studies on real ASIC and MEMS chips. Pseudo ASIC chips are made of Pyrex (7740) material substrate with 500 μm $\pm$ 25 μm thickness. The pseudo ASIC chip has 143 bonding pads (figure 2(a)). The dimensions of the pseudo ASIC chip are 6.17 mm x 1.43 mm x 0.5 mm (thickness). The pseudo MEMS chip is designed as a substrate for the FCB process with dimensions of 16.75 mm x 16.75 mm x 0.5 mm (thickness) . The pseudo MEMS chips are made of Pyrex (7740) with 500 μm $\pm$ 25 μm thickness (figure 2(b)). The design view of a bonded pseudo ASIC chip on the pseudo MEMS chip after the TSFCB process is shown in figure 2(c).

A semiconductor characterization system (Keithley 4200-SCS) is used to measure the conductivity of the bonded regions after the TSFCB processes, using the two-probe resistance measurement method. To measure the electrical conductivity (hence, identify mechanical connectivity) of the bonded regions, specific connections are designed between the bonding pads of the pseudo ASIC chip (figure 2(a)) and those of the pseudo MEMS chip (figure 2(b)). Two probes of the semiconductor characterization system are in contact with the corresponding circular features on the pseudo MEMS chip as shown in figure 2(d). The electrical resistances of the TSFCB bonded regions are measured after TSFCB trials with the DCC-coined GSBs. Since the two-probe measurement method is used in our studies, in addition to the electrical resistances of the two bonded GSBs, the probe resistances and wire resistances that are connecting the two bonded GSBs are also included in the resistance measurement results. It is important to emphasize that there are higher precision 'joint resistance' measurement techniques to measure the resistance of only the region where a coined stud bump is connected to the corresponding bonding pad of the corresponding chip [17]. Because the focus of our research is to demonstrate the DCC process, we were only interested in demonstrating the electrical connectivity and mechanical connectivity of the connections that were connected with DCC-coined GSBs. Hence, in our current study, the two-probe resistance measurements were assumed to be sufficient to demonstrate the electrical connectivity and mechanical connectivity between the DCC-processed GSBs and bonding pads. In our future studies, where the emphasis of our studies will be on the quality of the electrical resistance of the TSFCB connections, specific connections that are proposed in [17] and [29] will be designed and manufactured to remove the effect of wiring resistances. Furthermore, four-point resistance measurement techniques will be used rather than two-point techniques.

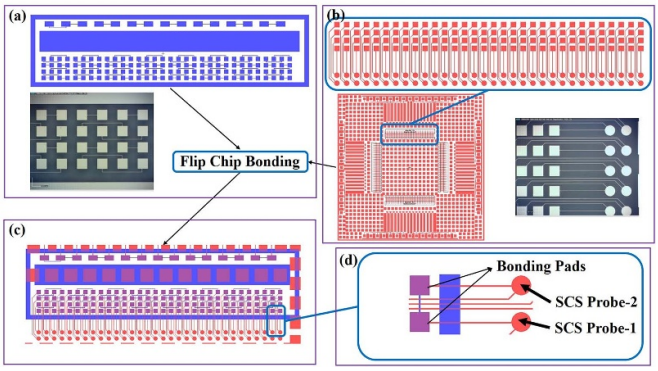


Figure 2. Design of the pseudo ASIC chip and the pseudo MEMS chip and two-probe measurement technique that is used for this study. (a) Design of the pseudo ASIC chip and partial view from the array of bonding pads of the pseudo ASIC chip (in the optical microscope image, each square feature is 95 μm x 95 μm). (b) Design of the pseudo MEMS chip, design of the bonding pads of the pseudo MEMS chip, and partial view from the array of bonding pads of the pseudo MEMS chip. (c) Aligned pseudo ASIC chip on the pseudo MEMS chip after the TSFCB process. (d) Two-probe resistance measurement method is used to measure the electrical resistances of the wires and two connected GSBs to confirm the electrical and mechanical connectivity between the pseudo ASIC and pseudo MEMS chips via the DCC-coined GSBs.

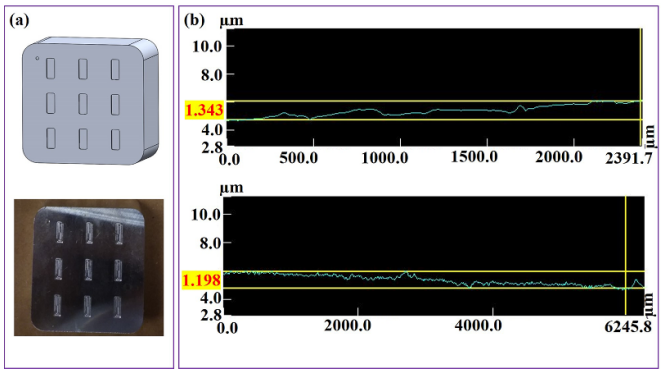


Figure 3. The aluminum mold. (a) Design of the aluminum mold and fabricated aluminum mold; (b) lateral (top image) and longitudinal (bottom image) parallelism measurements between bottom surface of a nest and aluminum rigid mold.

In this study, the main objective is to reveal the details of the DCC process. Furthermore, for the sake of completeness of the study, in section 2.4.2, the process parameter ranges of a representative TSFCB process, the measured total electrical resistances (i.e. including the wire resistances) of connections passing through the interfaces of the two flip-chip-bonded GSBs, and the bonding of some of the GSBs after the TSFCB process are shown to experimentally demonstrate the capability of the DCC process. The ultrasonic and TSFCB-related detailed resistance and bonding quality results will be published in a separate research paper (in preparation).

GSBs are fabricated via a stud bump bonding process, which was explained in detail in the introduction section of this paper. A TPT HB16 semi-automated wire bonder is used *manually (in semi-automated mode)* for the formation and positioning (placement) of GSBs on the bonding pads, and 25 μm gold wire (Au-HA 3) from Heraeus is used for GSB fabrication. A UTS-35FE capillary tool from Small Precision Tools is used as a capillary tool for the stud bump bonding process for this study. A total of 143 GSBs with 75 μm–83 μm diameters and 50 μm–60 μm ball heights are fabricated for each pseudo ASIC chip.

To form bonds between the pseudo ASIC chips and pseudo MEMS chips, the TSFCB process is used. The coining process is required before the FCB processes to flatten the contact surface and nominally equalize the heights of the GSBs. As aforementioned, around 1 N/stud bump has been recommended for the coining process in the published literature. This recommendation suggests that 143 N of force is needed for coining the GSBs on the pseudo ASIC chips. However, the FCB tool used in this study (Fineplacer Matrix Ma from Finetech GmbH) was configured to apply force values up to 20 N only. Thus, another novel solution was needed for coining the GSBs before the TSFCB process.

2.2. *Aluminum mold design and fabrication*

An aluminum mold with a 3 × 3 array of nine nests (or cavities) is designed and manufactured as shown in figure 3(a). By design, each cavity in the array has a defined depth value. The cavities in the aluminum mold with known depths are used as nests for the pseudo ASIC chips and also for the displacement-controlled deformation of GSBs on the pseudo ASIC chips during the coining process. The dimensions of the rigid aluminum molds are 40 mm × 40 mm × 20 mm, where 20 mm is the thickness of the mold. The width and length dimensions of the rigid cavities are 6.80 mm × 2.65 mm with 0.5 mm radius curves at the corners. The dimensions (width, length, depth) of the nest geometries need to be adjusted based on the dimensions (width, length, depth) of the chips that have uncoined stud bumps that need to be coined for appropriate coined surface area and stud bump height. It is required to have the nest width and length at least 0.5 mm larger than the width and length dimensions of the chip that needs to be placed inside the nest. The larger dimensions of the nest geometry are to make sure that the chips can be easily inserted and positioned inside the nest, and can be easily removed from the nest once the first part of the DCC process is completed (details and procedures of the DCC process are given in section 2.4.1). The aluminum mold is fabricated by a computer numerical control (CNC) milling process.

The designed depth values of the nine nests in the rigid mold are 515 μm, 520 μm, 525 μm, 530 μm, 535 μm, 540 μm, 545 μm, 550 μm, and 560 μm, respectively. Furthermore, after CNC milling, a confocal microscope (Keyence VKX-100) measured the depth values of the nine nests as 515 μm, 516 μm, 525 μm, 528 μm, 534 μm, 545 μm, 547 μm, 550 μm, and 558 μm, respectively. Here, it is very important to emphasize that 5 μm depth movement is a more sensitive value than the movement resolution limits of the CNC milling machine

that is used for the fabrication of the nests in the aluminum mold. Therefore, due to the CNC movement resolution limits, some of the cavities have different measured depth values than the designed depth values.

After determining the actual depth of each nest in the rigid mold with a confocal microscope (Keyence VKX-100) or a surface profilometer, one can use any nest that is known to have an appropriate depth value for the coining process. The parallelism between the bottom surface of a nest and the top surface (i.e. stopper surface) of the rigid mold is also measured. The parallelism measurement is performed by accepting the profile of the mold top surface as a flat reference. The deviation is then measured on the bottom surface of a nest with a confocal microscope (Keyence VKX-100). The average deviation between the parallelism of the bottom surface of a nest and the mold top surface, as measured longitudinally and laterally, is 1.198 μm and 1.343 μm, respectively (figure 3(b)). Furthermore, CNC milling machines with higher movement resolution and higher precision may be employed for studies that need higher precision for height values of the coined stud bumps.

Since pseudo ASIC chips have approximately 500 μm thickness, the expected GSB heights after the DCC process are approximately 15 μm, 16 μm, 25 μm, 28 μm, 34 μm, 45 μm, 47 μm, 50 μm, or 58 μm, depending on which nest is used for the DCC process. Furthermore, usually, 4 inch diameter wafers are produced with a $\pm$ 25 μm thickness variation. This is the usual thickness variation value given by the wafer manufacturers or wafer suppliers when wafers are purchased. However, based on our personal experience, the actual measured wafer thickness variations are usually less than $\pm$ 5 μm across the same Si wafer. Hence, chips fabricated from the same wafer may have different thickness values within $\pm$ 5 μm variation. On the other side, different wafers can have different thickness values within $\pm$ 25 μm variation. One should measure the actual thickness of the chip before performing the coining process and select a suitable mold cavity (nest) according to the measured thickness value. In this way, even with different chip thicknesses, the same bump height and desired average surface area per bump can be achieved using the DCC process. Here, it is important to emphasize that especially under limited force (i.e. the TSFCB tool is configured to apply a maximum of 19 N) conditions during the TSFCB process, having the capability to obtain the desired average surface area per bump for the desired average surface pressure per bump is an *enabling* capability that may not be achieved if the standard 1 N/bump convention is used for a large array of 143 GSBs.

2.3. Borosilicate glass

Double-side-polished borosilicate glass is used as a flat surface to flatten the coined surfaces of the GSBs by applying limited displacement to the protruding tips of the stud bumps that are inside the nests in the rigid mold. An image of the piece of borosilicate glass is shown in figure 4. The thickness of the borosilicate glass is 3.30 mm. The thickness of the borosilicate glass is important to have a high bending stiffness value to prevent undesired bending of the glass. A high bending stiffness ensures that there will be limited or no bending of the glass during the coining process, depending on the magnitude of the applied uniformly distributed force.

Figure 4. Borosilicate glass with thickness of 3.3 mm.

2.4. Coining process

2.4.1. DCC process steps. First, a summary of the DCC processing steps is given. Then, the details of the DCC process are given.

1. Formation of FABs and placement of these FABs as uncoined GSBs on the gold connection pads of a pseudo ASIC chip is done by manual positioning using the semi-automated mode of the wire bonder.
2. A pseudo ASIC chip with uncoined GSBs is placed inside a nest in the aluminum mold.
3. The known depth of the nest inside the aluminum mold is selected based on the desired coined surface areas and coined height values for the GSBs.
4. A thick borosilicate glass piece is then placed on the top surface (i.e. stopper surface) of the aluminum mold where the pseudo ASIC chip with uncoined (protruding) GSBs was placed inside the nest with the known depth. The borosilicate glass is used as a flat surface to ensure (a) uniform deformation on the surfaces of the GSBs, and (b) co-planarity between borosilicate glass surface, aluminum mold top surface (i.e. stopper surface), and coined surfaces of GSBs.
5. Another aluminum piece with the same dimensions and thickness as the first (bottom) aluminum mold, but without the nest arrays, is placed on top of the thick borosilicate glass.
6. A compressive force is applied to the top of the top aluminum piece to perform the first part of the coining process. In this step, the borosilicate glass partially flattens the tails of the GSBs. Also, the top surface of the bottom aluminum mold is used as a mechanical stopper (see figures 1 and 5) to prevent excessive flattening of the tails above the GSBs.

   In order to minimize the coined stud bump height variations caused by the inclination of the mold cavity (see

7.

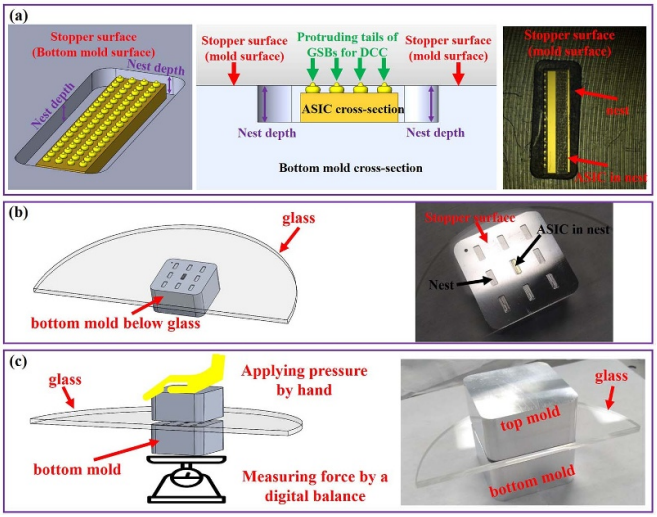


Figure 5. Steps of the DCC process. (a) Placing the pseudo ASIC chip inside the selected nest of the rigid mold, (b) placing the borosilicate glass on top of the aluminum mold, (c) placing another aluminum piece on top of the borosilicate glass and application of compressive force to coin the GSBs.

figure 3 and section 2.2), the same pseudo ASIC chip is removed from the nest, rotated 180° (without being flipped upside down) with respect to its initial position, and replaced into the same nest for the second part of the coining process. Then, the same amount of compression force is applied to the top of the top aluminum piece to complete the second (which is also the last) part of the coining process. Again, the top surface of the bottom aluminum mold is used as a mechanical stopper to prevent excessive flattening of the tails above the GSBs.

8. Scanning electron microscopy (SEM) images for geometrical measurements of the GSBs are taken both before and after the coining process.
9. Optical microscope images of the DDC-processed surfaces of the GSBs are taken for surface area calculations.
10. ImageJ software and image processing techniques are used to measure the surface areas, heights, tail heights, and diameters of all 143 GSBs in order to quantitatively evaluate the performance of the DCC process.

A pseudo ASIC chip with uncoined GSBs is placed inside a nest in the aluminum mold (figure 5(a)). The depth of the nest is selected based on the desired DCC-coined surface area (hence, the compressive pressure that is applied during the TSFCB process), and the height value for the GSBs. The polished flat surface of borosilicate glass is then placed on top of the aluminum mold that has the nest (figure 5(b)). Another aluminum piece with the same dimensions and thickness as the first aluminum mold is placed on top of the glass. A cleanroom wiping tissue can be placed on top of the borosilicate glass before placing the top aluminum piece to protect the glass from scratches. A compression force, the magnitude of which can be measured with a digital balance, is applied by human hand (further explanations of how the compressive force may be applied are in section 3) to the top of the top aluminum piece to perform the first part of the coining process. Here, it is important to emphasize that, in order to minimize the coined stud bump height variations caused by the inclination of the mold nest shown in figure 3(b), the same pseudo ASIC chip is removed from the mold nest, rotated 180° (without being flipped upside down) with respect to its initial position, and replaced into the same aluminum mold nest for the second part of the coining process. Then, the same compression force, the magnitude of which is again measured with the digital balance, is applied by human hand to the top of the top aluminum piece to complete the second (which is also the last) part of the DCC coining process (figure 5(c)).

In this approach, the top surface of the aluminum mold with known nest depth is used as a displacement-controlled barrier (this may also be called a displacement-controlled stopper, or stopper, or displacement limiter) during the coining of the uneven tail heights of GSBs. The nest inside the aluminum mold is used to prevent excessive deformation of the coined stud bumps and pseudo ASIC chip. Borosilicate glass is used as a flat surface to ensure uniform deformation of the stud bumps, and co-planarity between the glass surface, stopper surface, and coined surfaces of the GSBs. Since the displacement of the borosilicate glass is controlled (i.e. limited), GSBs are deformed to a defined height *all together at the same time*. Assuming that all the structures (i.e. aluminum molds, borosilicate glass, pseudo ASIC chip) are rigid except the GSBs, after the coining process, the final height of the GSBs is expected to be defined by the height of the nest depth in the rigid mold.

Although we did not need to measure with very high precision the compressive force that deforms the GSBs, we approximately applied at least 1 N/bump force for GSBs made from 25 μm diameter wires. The bottom mold, the borosilicate glass, and the top aluminum piece are placed on a digital balance to track the applied compressive force during the DCC process (figure 5(c)).

ImageJ software and image processing techniques are used to measure the height, tail height, diameter, and surface area of all 143 stud bumps in order to quantitatively evaluate the performance of the DCC process.

To obtain SEM images for geometrical measurements of the coined stud bumps, both before and after the coining process, individual pseudo ASIC chips with GSBs were placed on specific types of SEM stubs to eliminate measurement difficulties that may arise due to angle inclinations. Extra effort is paid to ensure that angle inclinations due to SEM stubs are eliminated to measure accurate dimensions. To use SEM images for geometrical measurements, ImageJ is employed to manually measure the height, tail height, and diameter of the GSBs (figure 6(a)). After the DCC processes, optical microscope images of the coined surfaces of the GSBs were also taken. The images were converted to 8-bit format. Using ImageJ's threshold function, images were separated into pixels representing the foreground and the background. The top surface areas of the GSBs

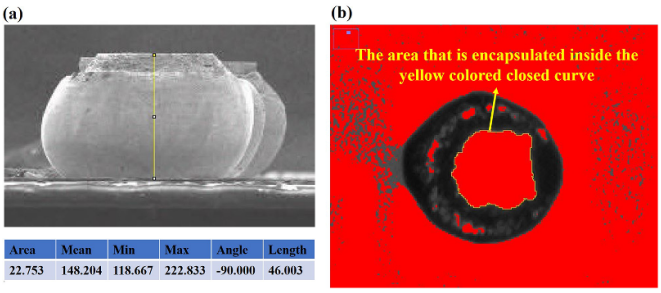
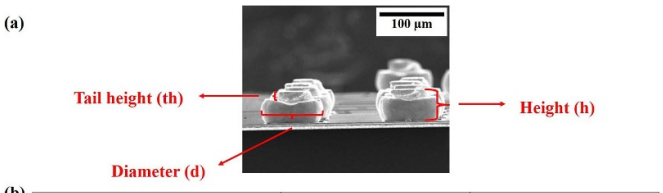


Figure 6. ImageJ measurements. (a) Measuring height of a GSB; (b) measuring the surface area of a GSB by selecting the foreground pixel area encapsulated inside the yellow-colored closed curve.

were calculated by selecting the foreground pixel regions (figure 6(b)).

2.4.2. DCC process trials. The initial GSB properties before the DCC process are given below in figure 7(b). Initially, there are large variations in the stud bump heights and tail heights of the GSBs due to the nature of the wire bonding process, because the wire is separated from the bonded ball randomly in the HAZ region after ball bump bonding (left side image in figure 8(c)). The mean standard deviation of the GSB heights is 11.5 μm, which is more than the maximum allowable variance of 5 μm for FCB processes according to the literature [10]. Therefore, for our TSFCB application with 25 μm diameter gold wires, the coining process must be done on the stud bumps before the FCB process. A total of 14 coining processes are performed with the pseudo ASIC chips. Among them, two of the processes are carried out with the 545 μm deep nest in the mold, three are carried out with the 547 μm deep nest, and nine are carried out with the 550 μm deep nest. The nest depths are selected with respect to the initial GSB properties and desired GSB properties after the coining process. A total of 143 N (1 N/bump) of compressive force is manually applied (figure 5(c)) for each DCC process trial.

Before the DCC process, the tail heights of the GSBs vary significantly due to the random breakage of the gold wire within the HAZ. Sharp tails are observed after the wire bonding process in SEM imaging (left image in figure 8 (c)). Standard deviations of the tail heights also vary significantly again due to the random breakage of the gold wire within the HAZ. The tail parts of the GSBs seem to have a darker color before the coining process during optical microscope imaging because of the scattering of light iin different directions. The DCC process flattens the tops of the tails. The coined tails of the GSBs appear to have a yellowish color during the optical microscope imaging (figure 8(b)) because of the flattened gold surface after the coining process. Although the heights and standard deviations of the tails still vary, the values are limited to a narrower range. Furthermore, in this application, instead of the tail height values, the total height values of the GSBs are critical for FCB processes. Therefore, the mean height values



(b)

ASIC Chip	Mean Height Value (µm)	Mean Standard Deviation of Height (µm)
Pseudo ASIC	50 to 60	11.5

(c)

Trial	ASIC chip	Depth of MC (µm)	Mean h (µm)	SD h (µm)
1	Pseudo ASIC 1	545	46.6	0.814
2	Pseudo ASIC 2	547	48.8	0.909
3	Pseudo ASIC 3	547	47.1	2.28
4	Pseudo ASIC 4	550	52.4	0.986
5	Pseudo ASIC 5	550	51.9	0.656
6	Pseudo ASIC 6	550	52.1	0.737
7	Pseudo ASIC 7	550	50.0	1.008
8	Pseudo ASIC 8	550	50.2	1.135
9	Pseudo ASIC 9	550	49.8	1.018
10	Pseudo ASIC 10	550	50.8	0.809
11	Pseudo ASIC 11	547	47.6	1.096
12	Pseudo ASIC 12	545	46.1	0.797
13	Pseudo ASIC 13	550	49.7	1.382
14	Pseudo ASIC 14	550	49.8	1.733

Figure 7. GSB properties before and after the DCC process. (a) Anatomy of a coined GSB, (b) mean values of the GSBs before the coining process, (c) mean values of the GSBs after DCC process trials. **h**: height, **MC**: mold cavity (nest), **SD**: Standard deviation. Details of figure are given in supplementary document.

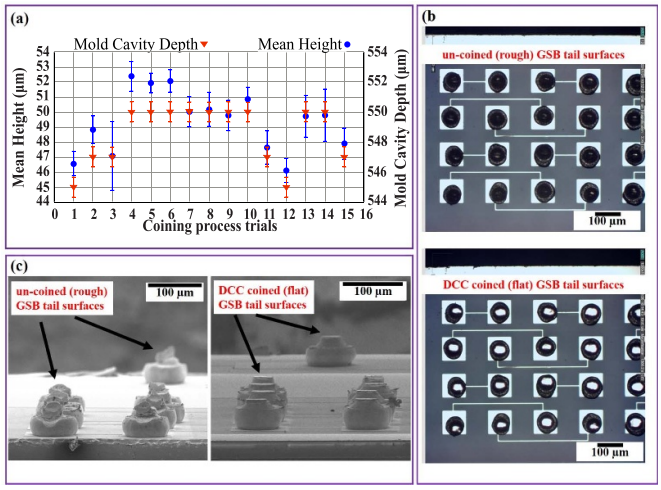


Figure 8. Results of the DCC process. (a) Mean height values of the GSBs and standard deviation of the height values of the GSBs after the DCC process (the *y*-axis on the right indicates the depth of the mold cavities with orange triangle markers). (b) Optical microscope images of the pseudo ASIC chip before (top) and after (bottom) the DCC process. (c) SEM images of the pseudo ASIC chip before (uncoined (rough) GSB tail surfaces; left image), and after (DCC-coined (flat) GSB tail surfaces; right image) the DCC process.

of the GSBs are measured after each trial as shown in figure 7(c) and plotted in figure 8(a).

After the coining process is initiated, once the stopper surface of the aluminum mold is in contact with the borosilicate glass, the movement of the borosilicate glass stops. Thus, the displacement of the borosilicate glass is controlled and the GSBs are deformed to the same height as the top stopper surface level of the mold. Moreover, standard deviations of the

height of the GSBs are important to examine the suitability of the GSBs for the FCB processes after the coining process. The standard deviation values are low enough to be suitable for the FCB process used in this application.

Another very important detail (probably the most important detail of this manuscript) is that the surface areas of the DCC-coined tails of the GSBs are narrower than the DCC-coined surface areas in the 'body' part of the GSBs if the DCC process is completed in the tail height part of the GSBs.

Due to the relation between pressure, force, and surface area ($P = F/A$), when the surface area, A, of the DCC-coined surface is narrower, the total pressure value, P, at the DCC-coined surface area increases for the same amount of applied force, F, during the TSFCB process.

Furthermore, the pressure per bump value increases even for the same force per bump value during the TSFCB process by utilizing smaller surface areas for the DCC-coined surfaces (i.e. in the tail region of the GSB).

The *pressure per bump* value is a more descriptive process parameter for FCB processes, compared to the *force per bump* value, since the total pressure value, P_T, that is applied to the coined total bonding interface area, A_T, can significantly change for the same total force value, F_T, depending on the available total surface area (i.e. the DCC surface area or bonding interface area) value, A_T.

Since the total amount of coined surface area can be controlled by the DCC process, the total surface area of the GSBs (especially at the tail part of the GSBs) can also be manipulated to increase or decrease the total pressure value needed for successful FCB processes.

For example, one can use a deeper nest in the mold to deform the GSB surface areas less to have smaller surface areas at the tail regions after the DCC process. Thus, the pressure-per-bump value during the FCB process will be higher for the same amount of applied force.

To demonstrate our capability of manipulating the coined surface areas starting from the tail region to the body region of the stud bumps, a test chip is DCC-coined within 550 μm, 540 μm, and 530 μm deep nests in the mold, as shown in figure 9(b). The pressure-per-bump values that are applied at the TSFCB interface, and the average surface area-per-bump values that are used at the bonding interface during the TSFCB processes are calculated after each coining process with respect to a fixed 19 N force value for 143 bumps that may be applied during the TSFCB process. As can be seen in figure 9(a), the pressure-per-bump value that can be applied during the TSFCB process significantly decreases (from left to right in the graph) when larger DCC-coined surface area values are obtained by working with shallower mold cavities.

TSFCB processes have been used to integrate pseudo ASIC chips to pseudo MEMS chips after the DCC process. A 1 W to 3 W ultrasonic power range, 0.9 s to 1.2 s ultrasonic time range, 24 °C to 375 °C temperature range, and 19 N fixed force processing parameters are used for the TSFCB trials. The electrical connectivity and mechanical connectivity of the bumps were investigated via the two-probe resistance measurement method described in section 2.1, and are shown in figures 2(b)

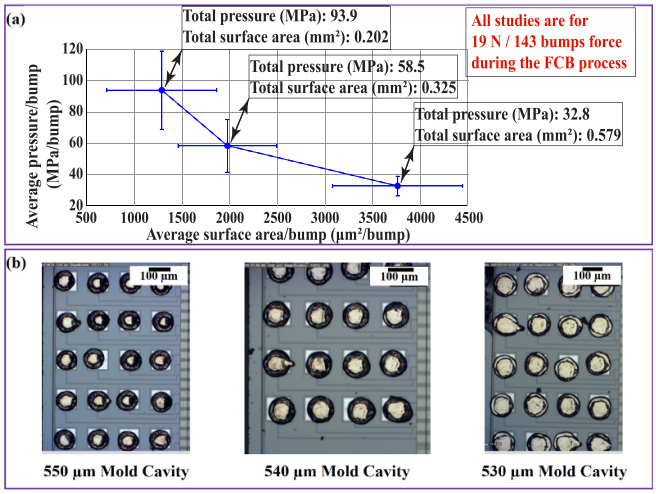


Figure 9. Surface area of the GSBs after the DCC process. (a) Average pressure/bump (MPa) vs average surface area/bump (μm^2/bump) after the DCC process. (b) Optical microscope images of the surface areas of the GSBs after coining with 550 μm, 540 μm, and 530 μm deep mold cavities, respectively.

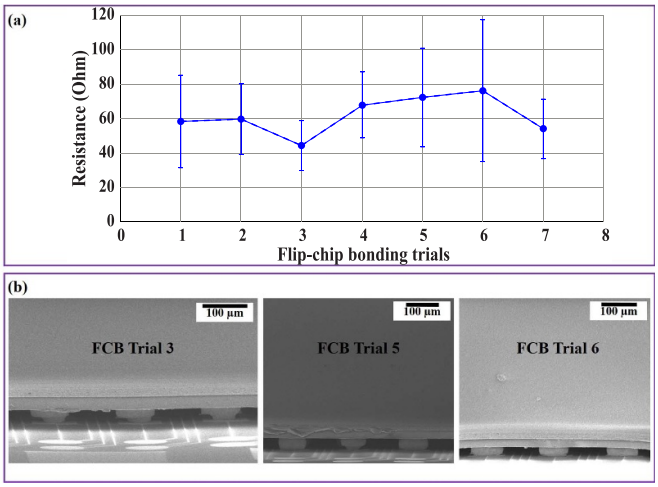


Figure 10. Two-probe total resistance measurements for the demonstration of electrical and mechanical connectivity of the GSBs after the TSFCB processes. (a) Total resistances of two GSB pairs (including the wiring resistances) of connections passing through the interfaces of the two flip-chip-bonded GSBs after the TSFCB process; (b) FCB structures after the FCB processes (resistance values of figure are given in supplementary document).

and (d). One hundred percent successful electrical connectivity (hence, mechanical connectivity) results were obtained for multiple TSFCB process trials (figure 10(a)). As described in detail in section 2.1, the two-probe resistance measurement method used in our measurements results in relatively large standard deviations for the measured resistance values. Based on our literature research, we conclude that there are four main reasons for these large standard deviations in the measured resistance results. The first reason is due to the use of a two-probe resistance measurement method rather than a four-probe method that is specifically designed and optimized for

measuring the connection resistance (i.e. joint resistance) of interest between the bonding pad and the DCC-coined GSBs [17]. The second part of the electrical resistance variation is due to the different wire lengths (hence, resistances) for different electrical measurement paths that are used for connecting the two flip-chip-bonded GSBs and four bonding interfaces (i.e. two of the bonding interfaces are between DCC-coined sides of the two GSBs and the corresponding bonding pads on the corresponding chip, while the other two interfaces are formed one by one while connecting an FAB to a bonding pad to form a GSB on the chip that is hosting all of the 143 GSBs) [49]. The third reason for the variation between the resistances is due to the variation in the coined surface areas of the DCC-coined individual surfaces (i.e. variation from GSB to GSB due to initial tail length variations) before the FCB process is actually done [6, 11]. The fourth reason for the variations between the resistances may be due to the post-coining surface quality and/or the pre-FCB cleanliness of the bonding pad surfaces [50]. SEM images of the FCB bonded structures after TSFCB are shown in figure 10(b). As emphasized before, in our future studies where our studies will be more focused on the quality of the electrical resistance of the TSFCB connections, the specific connections that are proposed in [17] and [29] will be designed and manufactured. Furthermore, a four-point resistance measurement technique will be used.

3. Results and discussion

The DCC technique described in this study allows for a bump height variation of 1.09 μm on average, with the bump geometries and 25 μm wire diameter we used in this study. After the TSFCB experiments using pseudo ASIC chips coined by this technique, completely conductive TSFCB connections are obtained.

The surface area and height values of the GSBs can be tailored according to the FCB process requirements by adjusting the height of the mold cavity (nest) (figure 9).

The height of the mold cavity, the co-planarity between the relevant planes, the applied compressive force, and the high bending stiffness of the polished flat surface that is used for DCC coining (in our case, borosilicate glass) are the most important parameters for the DCC process. The bending stiffness of the flat coining surface material must be high enough to have a high-precision coining process.

To investigate whether the polished surface of a standard and approximately 500 μm thick, 4 inch diameter, silicon wafer (instead of a 3.3 mm thick borosilicate wafer) may be used as the coining surface, a DCC process (Trial-15) is performed using a 526.4 $\pm$ 1.9 μm thick silicon wafer as the polished flat surface between the aluminum mold pieces. A bottom mold cavity with a depth of 547 $\pm$ 0.66 μm is used for the experiment. During the DCC process, a force/bump of 1 N/bump (i.e. a total of 143 N for 143 bumps) is applied. The DCC process results in an average height value of 47.9 μm and a standard deviation of 1.04 μm for the coined

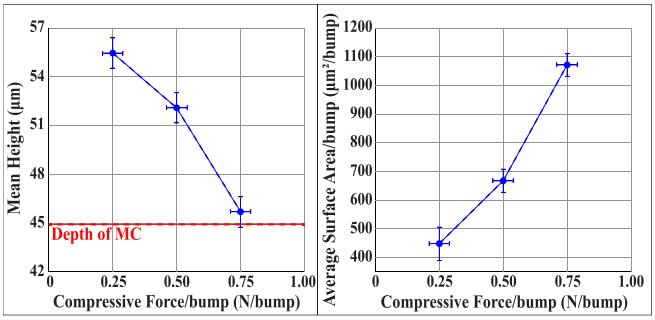


Figure 11. Comparison of 0.25 N/bump, 0.5 N/bump, and 0.75 N/bump DCC processes. Mean height value vs. compressive force/bump plot (on the left) shows that height of the GSBs decreases with increasing compressive force/bump. Average surface area/bump vs. compressive force/bump plot (on the right) shows that average surface area increases with increasing compressive force/bump value (details of 0.25 N/bump, 0.5 N/bump, and 0.75 N/bump trials are given in supplementary document).

GSBs (figure 8 (a). This experiment indicates that the polished surface of a 526.4 $\pm$ 1.9 μm thick silicon wafer (i.e. standard, 4 inch diameter, Si wafer) can serve as a coining surface when supported by an aluminum block as shown in figure 5(c).

The applied compressive force value is systematically varied and studied in order to understand the effects of the applied compressive force on the DCC process. A pseudo ASIC chip (named 'Pseudo ASIC32') is DCC-coined with 0.25 N/bump, 0.5 N/bump, and 0.75 N/bump, respectively, to study low compressive force values. Because of the initial height variations in the tail length or body length of the stud bumps (i.e. due to variations in the GSB process), and because the contact between the flat surface of the borosilicate glass and the top surface of the aluminum mold may be poorer at low compressive force values, 13 GSBs could not be coined after the 0.25 N/bump trial, and four GSBs could not be coined after the 0.5 N/bump trial. All GSBs were coined after the 0.75 N/bump trial (details of the 0.25 N/bump, 0.5 N/bump, and 0.75 N/bump trials are given in the supplementary document). Changes in the average height value and average surface area/bump value are shown in figure 11. The average height value decreases, and the average surface area/bump value increases with the increasing compressive force/bump value.

For each DCC experiment, the mean height values, total surface area values, and total pressure values of the stud bumps are measured after each coining process. SEM images are used to show the change in the height of the stud bumps, and optical microscope images are used to show the change in the coined surface areas of the stud bumps, shown in figures 12 (a) and (b), respectively.

Also, using the displacement-controlled approach, a pseudo ASIC chip (named 'pseudo ASIC31') is coined with 1 N/bump and 2 N/bump, respectively, to study compressive forces that are higher than the recommended value ($\sim$1 N/bump) as shown in figure 13 (details of the 1 N/bump and 2 N/bump trials are given in the supplementary document).

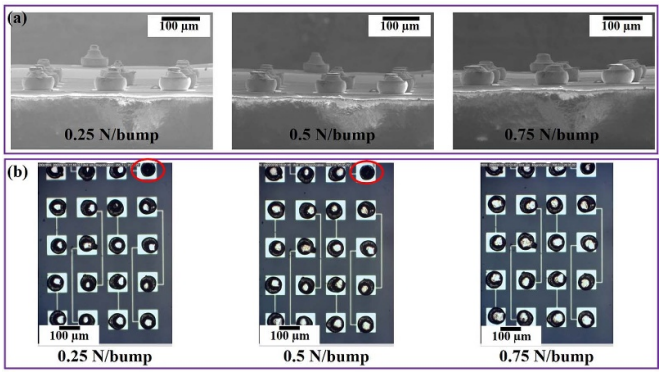


Figure 12. SEM (a), and optical microscope (b), images of the GSBs after 0.25 N/bump (b-left), 0.5 N/bump (b-middle), 0.75 N/bump (b-right) coining processes, respectively. In b-left and b-middle, a red circle highlights an uncoined GSB. The GSBs are all coined in b-right.

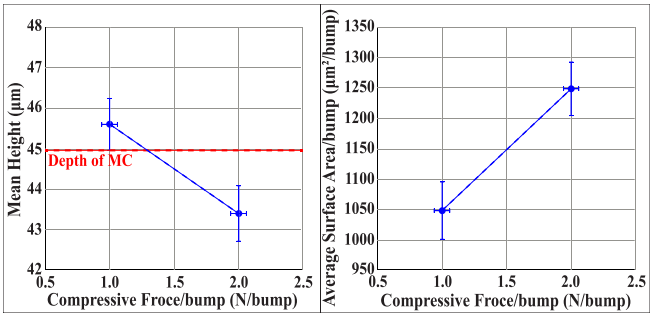


Figure 13. Pseudo ASIC31 is coined with 1 N/bump and 2 N/bump to study effects of the high compressive forces. Height value decreases when increasing the compressive force/bump as shown in the plot on the left. Also, average surface area/bump value increases when increasing the compressive force/bump as shown in the plot on the right (details of 1 N/bump and 2 N/bump trials are given in supplementary document).

First, pseudo ASIC31 is coined with 1 N/bump. All of the GSBs are coined (i.e. formed flat surfaces). The final height of the GSBs is very close to the depth of the mold cavity, which means that the displacement is controlled during the DCC process. In addition, the total surface area of the pseudo ASIC31 after 1 N/bump is almost the same as the total surface area of the 0.75 N/bump coined pseudo ASIC32.

Again, using pseudo ASIC31, 2 N/bump compressive force is applied for the second coining process. After 2 N/bump compressive force is applied, the final average height of the GSBs is approximately 2 μm below the top surface (i.e. stopper surface) of the mold cavity. Insufficient (i.e. low, or compliant) local bending stiffness and a relatively low Young's modulus value of the borosilicate glass or the aluminum mold may be the reasons for the final average height value of the stud bumps that is approximately 2 μm below the top surface of the bottom mold cavity.

For pseudo ASIC31, although the compressive force is increased by 100% (i.e. from 1 N/bump to 2 N/bump) for the second DCC process, the mean GSB height only decreases by

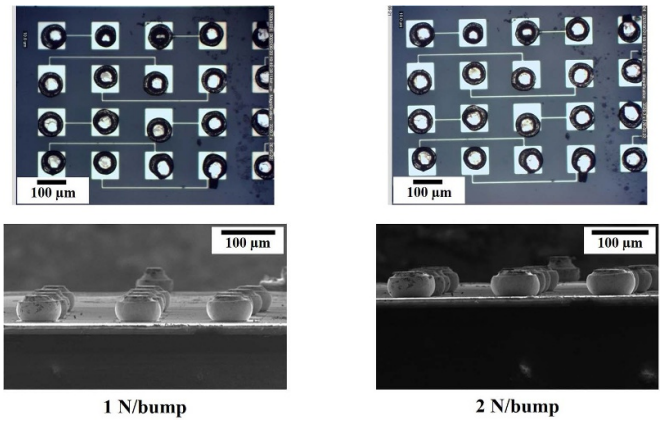


Figure 14. Pseudo ASIC31 is coined with 1 N/bump and 2 N/bump to study effects of the high compressive forces. Optical microscope and SEM images are shown after the coining processes.

5% and the total DCC-coined surface area only increases by 19% compared to the 1 N/bump coining process. This suggests that the displacement of the borosilicate glass plate is still controlled, but the local bending stiffness of the plate is not stiff enough to maintain a flat borosilicate surface in the mold cavity region for a 2 N/bump compressive force value.

Optical microscope images show the amount of change in the surface area after the coining processes (figure 14). SEM images show the change in the height of the GSBs after the coining processes (figure 14). As a result of DCC rather than FCC, the surface area increased less and the height decreased less than predicted with the 2 N/bump applied compressive force. The deformation was still within the needed standard deviation for a successful coining process. If a coining flat plate with a higher bending stiffness value is used, the 2 N/bump trial might have given higher mean height values compared to the depth of the mold cavities. Due to the higher Young's modulus values compared to borosilicate or aluminum, flat plates with polished and flat coining surfaces made from titanium or steel materials can be used as flat surfaces and molds to increase the precision capability of the DCC process.

Low and high compressive force coining process trials in this specific experimental setup of this study suggest that 0.75 N/bump to 1 N/bump should be used for the DCC process of stud bumps obtained from 25 μm diameter gold wires, in order to have a strong enough contact between the flat surface of the borosilicate glass and the top surface (i.e. stopper surface) of the aluminum mold that is in contact with the glass. Furthermore, we should always keep in mind that if we have smaller diameter wires (i.e. 17 μms, or 12 μms, or even smaller) for GSB formation, these 0.75 N/bump to 1 N/bump force values that are needed for 25 μm diameter wires will be more than needed because the surface areas that can be flattened become smaller and smaller for smaller diameter wires.

In DCC, the tail heights and DCC-coined surface areas of the tails of the GSBs may be tailored by the depth of the nest

in the mold without using an excessive amount of compressive force in order to obtain properly coined ASIC chips.

It is reasonable to think that using a human hand to apply the compressive force during the DCC process may cause concerns about uncontrollable vibration of the human hand. We want to emphasize that we did not observe a measurable effect that could have been due to possible hand vibrations on the flattened surface areas of DCC-coined surfaces. Furthermore, it is important to emphasize that instead of using a human hand (i.e. due to concerns such as uncontrollable vibration of the hand) to apply the needed compressive force that is measured with the help of the digital balance, an alternative approach to apply the needed amount of compressive force would be to use a well-defined piece of mass (m) to apply the needed amount of compressive force (F) (i.e. $F = m^*g$, where g is the acceleration due to gravity) to perform the DCC process.

If a DCC process is of interest for industrial applications, the work can be converted to apply the pressure or force with higher-precision equipment, rather than manually by human hand, to very precisely control the force needed for the DCC process. In the case of our study, there was no other available, affordable, and fast way to apply the needed measurable compressive force values other than using a digital scale to measure the force while the force was applied by pressing by hand (see figure 5(c)).

The DCC process is very suitable for R&D studies, and may be very suitable for mass manufacturing due to the array-type designed aluminum mold, especially when expensive FCB tools with larger compressive force needs are not available.

One can design nests with different depth values to optimize the DCC processes for R&D purposes, and one can design nests with the same depth values in all the nests to perform the DCC process for multiple chips simultaneously. Also, with this approach, an expensive and high-tech FCB tool with high force output may not be needed for DCC processing. Thus, the FCB tool would not be busy performing DCC processes, which saves significant processing time. Furthermore, if the FCB tool is used for the coining process, co-planarity between the die collet and the surface of the FCB tool that is holding the chip to be coined may become a very critical parameter that may affect the success of the coining process. One can avoid co-planarity problems by having the DCC process performed in a nest of the mold, assuming that the manufactured nest satisfies the co-planarity requirements for the specific coining process. Local and global co-planarity of the coined GSBs are satisfied by the manufacturing capabilities of the CNC tool. If very high precision local co-planarity and very high precision global co-planarity are needed, ultra-precision state-of-the-art CNC machines or electrical discharge machines may be used for the preparation of the coining nests in molds.

Below are two possible FCB manufacturing line scenarios that may benefit from the DCC process:

Scenario #1: Multiple (preferably hundreds of) chips, that already have arrays of uncoined stud bumps positioned on these hundreds of chips may be placed into an array of nests, where all the nests in this array are CNC manufactured in the mold. As described in the manuscript, the surface of this nest array mold is the stopper surface that defines the average surface area of the coined GSBs and the average height of the GSBs. Furthermore, the co-planarity between the bottom surfaces of the array of nests and the top surface of the same array of nests mold defines the co-planarity between the borosilicate glass flat surface and features that will be coined at the tail sides of the GSBs. Borosilicate glass is used for coining the stud bumps because of its very smooth surface. Instead of borosilicate glass, other materials (for example, Ti) that have higher stiffness compared to borosilicate glass may be manufactured and used as well. This alternative stiffer material (i.e. titanium) should be large enough to be able to cover all the hundreds of chips simultaneously. This way, the top workpiece would be able to coin all these chips simultaneously.

Scenario #2: A full-scale wafer that has undiced chips, that already have arrays of uncoined stud bumps positioned on these hundreds of chips [8], may be placed into a large nest that must have the capability to keep the wafer flat on the bottom surface of the nest. For example, there may be vacuum holes at the bottom surface of the nest to keep the wafer coplanar with the bottom surface of the nest. As described in the manuscript, the top surface of this nest mold is the stopper surface that defines the average surface area of the coined GSBs and the average height of the GSBs.

There are fabricated coining tools designed for wire bonders for coining individual stud bumps [48]. Stud bumps can be coined individually using these coining tools. Although these tools are very effective for coining, they can be time-consuming, particularly for large arrays. Time-wise, simultaneous DCC of multiple chips may be more efficient compared to using coining tools that are designed for individual stud bump coining.

Another advantage of DCC processing is that, if there are capabilities to conduct the stud bumping and coining processes in inert environmental conditions, without being exposed to oxidizing environmental conditions, materials that are oxidized in ambient environmental conditions (i.e. aluminum and copper) can also be coined by this approach. Oxidation of the materials must be prevented for electrical conductivity.

It is important to emphasize that it may be necessary to consider the interfacial reactions between the flat coining surface (i.e. the borosilicate glass) and the stud bumps (i.e. GSB) before the coining process. At room temperature, there is no interfacial reaction between gold, borosilicate glass, and aluminum. However, for cases where such interfacial reactions between the materials that are in mechanical contact may happen, surface functionalization steps may be carried out to prevent the reactions, or a suitable combination of materials may need to be selected to prevent adhesion or reaction possibilities between contact surfaces before coining on the flat surface.

In this study, although we demonstrated high-precision DCC using GSBs made from 25 μm diameter gold wires, DCC can be extended to smaller diameter wires (for more compressive pressure values with the same compressive force values) as well as larger diameter wires that can be used for stud bump formation.

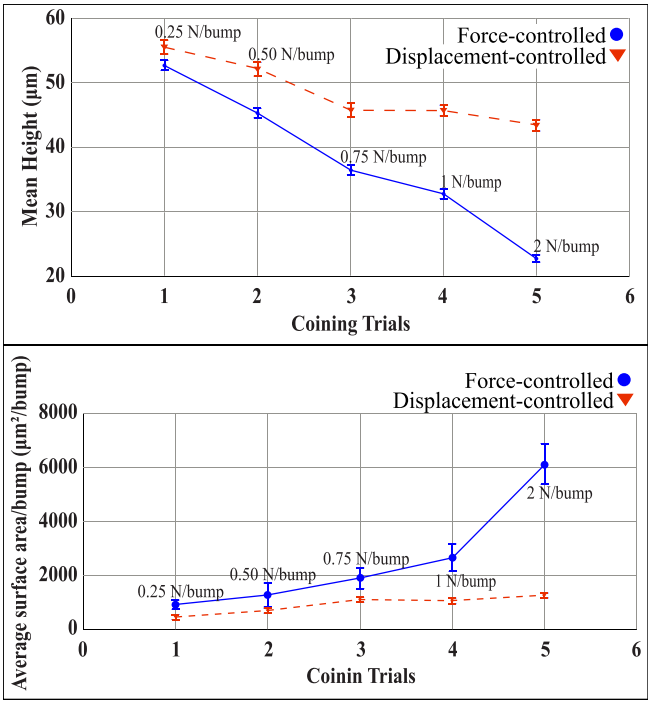


Figure 15. Comparison of the coining processes performed by the DCC process and the FCC capability of an FCB tool (details of comparison of DCC and FCC are given in supplementary document).

If the coining processes had not been performed inside mold cavities of known depth, and had not been performed under DCC experimental setup, 627.2 MPa (for 0.25 N/bump), 785.7 MPa (for 0.50 N/bump), and 719.2 MPa (for 0.75 N/bump) total pressure values would have been instantaneously applied to the deformed surface areas of the coined stud bumps during these coining process trials. Because these high pressure values are larger than the compressive yield stress of GSBs (compressive yield stress of the GSB is 127.7 MPa according to the publication of Wang *et al* [35]), the stud bumps would be plastically deformed under compression, until a force balance is obtained as the surface area of the coined stud bumps becomes large, if there were no displacement-controlled (i.e. stopper surface-controlled) nest depths in the molds. In other words, even if compressive pressure values that are greater than the compressive yield strength of gold are used for these DCC trials, the displacement of the flat coining surface of the borosilicate glass is stopped at the top surface of the mold cavities and the deformation is displacement-controlled (i.e. stopper-controlled) successfully. A set of experiments that support the information explained in this paragraph (comparison of FCC processes using a flip-chip bonder tool and DCC process) is also shown in figure 15.

In figure 15, the FCC process using a FCB tool and DCC process is compared. For the force-controlled case, five different chips, where each chip has eight bumps, are used for the coining experiments. For the force-controlled case, eight bumps/chip is selected because of the 20 N maximum force limitation of the available FCB tool. For the displacement-controlled case, chips with 143 bumps are used, the results of which are already presented in figures 11 and 13. Coining forces ranging from 0.25 N/bump to 2 N/bump are applied in five different trials for each coining technique. It is concluded that the surface areas of the GSBs increase more, and the heights of the GSBs decrease more when coining is performed by the FCC with the FCB tool, even when the same amount of force/bump is applied for both coining techniques. This mechanical deformation bias in the FCC case must be related to the fact that there is no 'displacement-controlled stopper surface' during the FCC case. Figure 15 depicts the greater decrease in the height values and the greater increase in the surface area values for the FCC process using an FCB tool. Both methods provide an accurate coining process, but the DCC approach is preferred when the maximum force value of an FCB tool is insufficient to coin large arrays of stud bumps.

Finally, pseudo ASIC chips made of silicon material are used for the DCC process. There is no significant difference between Pyrex pseudo ASIC chips and silicon pseudo ASIC chips after the DCC process, which suggests that silicon chips can be coined by the method presented in this study.

4. Conclusion

In this study, a DCC process for GSBs has been developed, which does not exist in the available technical literature so far to the best of our knowledge. The DCC approach successfully controls the the displacement of the coined flat surface so that the height and surface area of the stud bumps can be controlled by selecting the desired mold cavity (nest) depth value. With the bump geometries and wire diameter we used in this study, the method produces $\pm$ 1.09 μm bump height variation and helps to achieve successful TSFCB results. The method is suitable for coining large and small arrays for R&D studies and may be suitable for mass manufacturing because there is no need to use advanced level FCB equipment for the coining process. However, it is important to emphasize that as the stud bump sizes become smaller, the bump height tolerances become tighter. This means that higher precision CNC machining of the molds (nests) would be needed for higher precision DCC. Furthermore, the height and surface area of the stud bumps can be adjusted by defining the desired mold cavity depth value.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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