Bond-on-Lead: A Novel Flip Chip Interconnection Technology for Fine Effective Pitch and High I/O Density

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Abstract

A new flip chip interconnection structure termed BOL (Bond on Lead) comprising attachment of bumps to narrow pads or traces as opposed to conventional circular capture pads has been developed. The motivation for such a structure is to free up real estate for escape routing of signal lines between bumps on the topmost layer of the substrate leading to either complete elimination of layer pairs or relaxation of design rules for routing on the top layer. The reliability of the asymmetric solder joint structure so formed is investigated using hi Pb (97% Lead & 3% Tin) bumps and ABF (Ajinomoto Build-up Film, or other widely used film based high density substrates) Build-up and Laminate substrates by means of a test vehicle device and through Finite Element Analysis. It is shown that the solder joints are at least as reliable as conventional solder joints; furthermore, it is found that the maximum plastic strain in the solder joint is in fact reduced by virtue of the asymmetric BOL structure which in turn increases the fatigue resistance of the solder joint as well as reduces the stress on the silicon induced by CTE (Coefficient of Thermal Expansion) mismatch. Extended reliability studies and formal qualification results are presented. The implications of the higher routing density enabled by BOL interconnection on substrates for common device families such as GPU's, ASIC's, DSP's and FPGA's are examined – it is found that an I/O (Input/Output) density parameter termed "effective signal escape pitch" for most devices falls in the range of 50 um to 110 um and greater than 50 % of these devices can be routed in 4 layers using BOL methodology and a microstrip transmission line architecture, while the rest can be designed so as to relax the design rules for signal escapes on the top layer of the substrate.

1. Introduction: The BOL Interconnection Concept

As flip chip packaging becomes mainstream, much effort is being directed at improvements in design, manufacturing and overall cost of ownership. The ability to efficiently fan out the high I/O density of the device enabled by flip chip's area array I/O architecture continues to be a dominant challenge which is manifested in the high complexity and cost of flip chip substrates. Substrates typically make up 50 – 70 % of the total cost of a flip chip package. Substrate suppliers have made strides in improving density in the form of finer lines and spaces, via diameters, smaller capture pads, blind /buried and stacked vias and via-in-pad structures[1, 2]. However, in addition to such developments, we believe in the coming years, new paradigms are likely to emerge that would fundamentally re-visit the a priori conventional wisdom regarding the flip chip package structure in order to realize more substantial gains in efficiency, productivity and cost. BOL interconnection is one such development pioneered by the R&D groups at STATSChipPAC. We have re-looked at the conventional paradigm that the ideal solder joint structure is one in which the diameter of the support pad on the substrate side is approximately equal to the diameter of the bump UBM (Under Bump Metallization) on the die side[3].

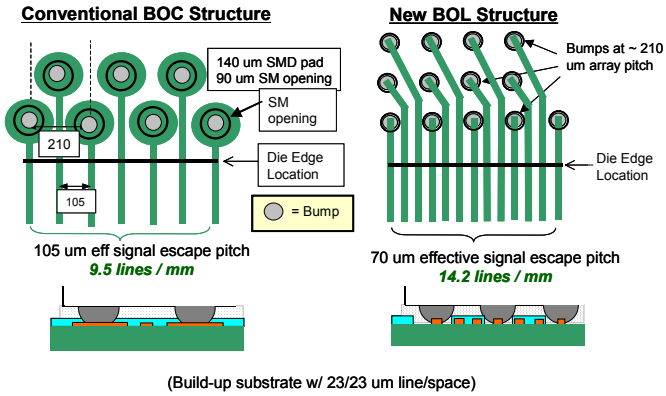


Fig. 1.1: Illustration of Conventional Bond-on-Capture pad (BOC) and new Bond-on-Lead (BOL) substrate designs

The BOL interconnection concept is depicted in the diagram in fig. 1.1. A conventional substrate layout in the die region of the flip chip device is shown on the left side; it represents flip chip pads on a 210 um area array pitch in an SMD (Solder Mask Defined) configuration with one signal escape between bump pads resulting in an effective escape pitch of 105 um (110um?); dimensions shown are typical of standard design rules for ABF Build-up substrates. It is apparent that efficiency of signal escapes on the top layer is severely limited by the conventional structure of a capture pad with a solder mask opening and associated tolerances in the size and alignment of the latter. The diagram on the right shows the corresponding layout using BOL methodology; here, the landing pad on the substrate is merely the trace itself, or a slightly widened version of the trace which results in freeing up of enough routing space to allow routing an additional trace between bumps thereby resulting in an effective escape pitch of 70 um without changing the design rules (trace width & space) of the substrate. As will be appreciated later (section 3), the effective escape pitch of ~ 70 um is adequate to route > 70 % of IC designs that commonly employ flip chip interconnection (e.g. ASIC, GPU, Chipset, DSP, FPGA) on a single layer based on the inherent I/O density of the device architectures. BOL technology also further opens the prospect of routing a considerable proportion of flip chip designs in conventional through-hole laminate substrates, since laminate substrates are now capable

of line / space capabilities of ~ 40 / 40 um, which would result in substantial cost reductions and potential re-use of the manufacturing base and infrastructure for wire bond substrates.

2. Evaluations & Results

2.1 Test Vehicle Description

The test die was a daisy-chain design comprising 97Pb3Sn solder bumps with polyimide re-passivation, 180um pitch of peripheral bumps and 250um pitch of center bumps for a total of 4751 bumps and a die size of 17x17 mm. There were two versions of the substrate, namely, a 1-2-1 high density ABF Build-Up (the terminology 1-2-1 refers to the layer stack-up comprising # Bottom Build-up Layers - # Core layers - #top build-up layers) version and a 4-lyr Laminate version. For reference, 2-2-2 ABF Build-Up substrate for the conventional BOC was used as a control case. For more detail, the specification of test die and substrates are listed in Table 2.1. The designed test vehicle had serial daisy chain electrical interconnections for full electrical continuity coverage of the outer 5-6 rows of the area array and partial coverage of the inner rows.

Specification		ABF Build-Up (BU) BOL	Laminate BOL	Reference: Conventional BOC
Die	Size	17.0 x 17.0 mm		
	Bump Pitch/Qty	Total 4751bumps; Outer 5-6 rows @ 180 um and inner array @ 250 um pitch		
	Bump Composition	97Pb3Sn		
	Passivation	Polyimide re-passivation		
Substrate	Core	HL830	HL832	HL830
	Pre-preg	ABF	-	ABF
	Layer	1/2/1	4 Layer	2/2/2
	Thickness	1.00mm	0.6mm	1.10mm
	Bump Pad	SOP on Cu	SOP on Cu	SOP on Cu
	Bump Pattern	BOL for outer rows, BOC for center	All BOL	All BOC
Package	Size	31x31	31x31	45x45
	LD Count	683	683	1936

Table 2.1 Specification of test die and substrate

2.2 Test vehicle assembly and solder joint comparison

Test samples were assembled on the 3 types of substrate as described above. The attachment was performed with the jet flux method for the robust and stable solder joint and the typical solder reflow condition was applied with peak temperature of 235'C for solder joining of Hi Pb bumps with eutectic SOP (Solder-on-Pad). And the flux cleaning process was followed to remove the flux residue around bumps because water-soluble flux was used. Package characterization was carried out with next 2 steps of evaluations; (1) as-attached package without underfill for the accelerated fatigue testing to assess the fatigue resistance of the solder joints with 3 types of substrate, (2) full packages with 4 kinds of underfills to verify the reliability performance and the underfill compatibility with the used flux. Based on the characterization results of the (1) and (2) steps of evaluation, the internal qualification was performed with the large sample size using the optimum underfill material to meet the internal reliability requirement. Cross section, electrical test and C-SAM analysis were done to assess the solder joints of the as-attached samples and inspect the failed samples during step (1) and to check the solder joint integrity during step (2).

The typical solder joint structure after chip attach for the 3 types of substrates is depicted in Fig. 2.2.1. These bumps were divided into the two areas of solder joint, hi Pb area and hyper-eutectic solder joining area. But due to the different pad width of 3 kinds of substrates, they had the different shape of solder joint at the solder joining area on substrate side. ABF BU BOL, 30um pad width, had the most sharply tapering shape of solder joint, and BT laminate BOL, having 40um pad width and broad etching factor, had a relatively wider shape. The formation of the sharp solder joint on BOL substrates resulted from the upward wicking of solder material, from the SOP pads of the BOL substrate. BOC substrate had the conventional solder joint, as known generally.

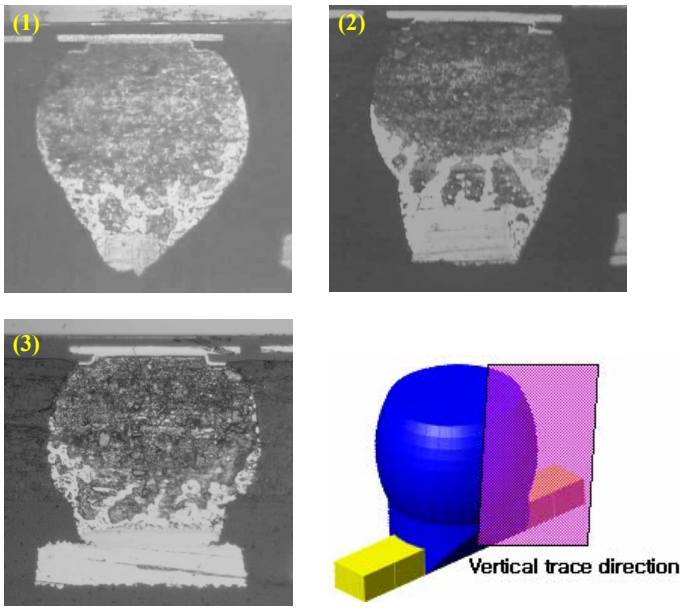


Fig 2.2.1 The as-attached solder joint shape of 3 kinds of substrate along the "vertical" direction (as shown); (1) ABF BU BOL substrate, (2) BT Laminate BOL substrate and (3) conventional BOC substrate

2.3 Accelerated Fatigue Testing

"Accelerated Fatigue Testing" was performed to evaluate and compare the fatigue resistance of BOL solder joints against BOC solder joints. In this test, the die is attached to the substrate but no underfilling is performed in order to accelerate the cracking of the solder joints by the fatigue mechanism. This test is useful on two counts (a) a comparison of relative solder joint fatigue behavior between a known case and a desired new configuration can be obtained in a very short time (b) the simplicity of the structure lends itself to validation by Finite Element Modeling (see later). The cycling conditions used were –55 to 125 deg C (also known as TC "B") and electrical tests were done to check continuity

every 5 cycles. And this testing was continued until all samples in the 3 kinds of substrate experienced 100% failure of all daisy chains.

The test results are depicted in Fig. 2.3.1. As seen in Fig. 2.3.1, BT laminate BOL and BOC started to fail early during the accelerated fatigue testing; ABF BU BOL, on the other hand, had good electrical continuity with number of cycles to 1st failure of 15 cycles. Furthermore, the solder joints of BT laminate BOL completely failed all test pins at TC "B" 15 cycles, but ABF BU BOL and BOC failed almost all test pins at TC "B" 30 cycles. These accelerated fatigue testing results showed that the solder joints of ABF BU BOL were at least as reliable as the conventional solder joints of BOC. This was somewhat counterintuitive because the highly asymmetric BOL solder joint in case of the ABF BU BOL was expected to be the weakest solder joint among the three substrate configurations.

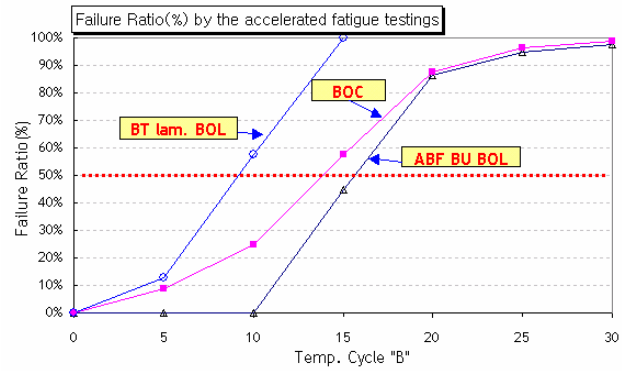


Fig. 2.3.1: Results of Accelerated Fatigue Testing showing the superior resistance of ABF BU BOL package among the 3 types of substrate configurations evaluated.

The failed samples i.e. BT laminate BOL after TC "B" 15 cycles and ABF BU BOL and BOC after TC "B" 30 cycles were analyzed by x sectioning. The results are depicted in Fig. 2.3.2. It was found that all BOL parts had bulk solder cracks at the lower bump area and a more distorted bump shape, compared to the as-attached bump shape (refer to Fig 2.2.1), on the other hand, BOC had the solder cracks between UBM and bulk solder at the upper bump area. It is thought that these different locations of bump cracks are due to the difference in the stress states induced by the cyclic thermal stressing. As will be appreciated in the next section, the tapered configuration of the BOL solder joint with a narrow interconnect region at the substrate interface and no solder mask constraint, results in a sort of "relief structure" that allows free deformation of solder at the substrate interface, thereby dissipating the concentration of plastic strain that normally occurs at the die-solder interface in the more conventional BOC structure. This free deformation at the solder-substrate interface is evident in the distorted joint shape in fig. 2.3.2; it eventually leads to failure at the substrate interface, however, notably, the failure occurs much later than in case of the conventional BOC solder joint with the concentration of strain at the die interface. It is also evident from fig. 2.3.1 that BT laminate BOL had the least fatigue resistance in accelerated fatigue testing. This behavior is not fully understood and it is thought that it could be related with the laminate structure and its lesser overall thickness of 0.61mm compared to 1.0 mm for ABF BU. The ABF BU BOL structure was selected for subsequent testing and qualifications, the BT laminate BOL version will be presented later in a subsequent paper.

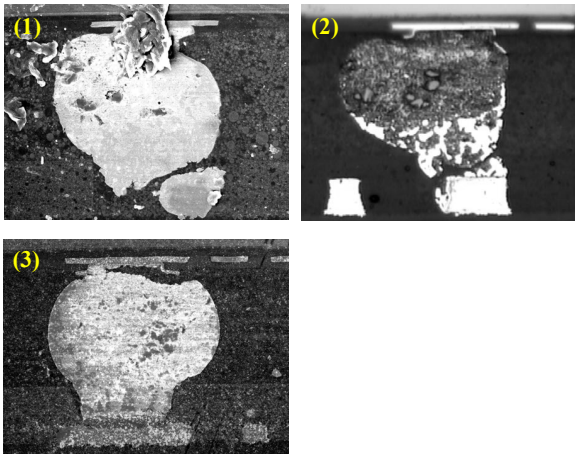


Fig 2.3.2: The failure mode of solder joints in the 3 kinds of interconnect configurations (1) ABF BU BOL (2) BT Laminate BOL and, (3) conventional BOC

2.4 FEA Modeling of the Solder Joint Structures

The improvement in fatigue behavior of BOL solder joints over conventional BOC joints in the ABF BU substrates was somewhat counterintuitive given the highly asymmetric interconnect structure of the joint, since such a structure deviates from the conventional wisdom that the shape and support area of the base of the solder joint on the die side should be approximately equal to that on the substrate side for optimal results. Based on the observations in section 2.3 above, the following hypothesis seemed most plausible: in the conventional BOC structure, although the average strain is determined by the CTE mismatch between the Si and the substrate, there is a high strain concentration that occurs at the solder/silicon interface, since at this location, there is an abrupt change in the CTE; hence, fatigue failure is driven by the concentrated plastic strain at this location, not by the average strain. With BOL, a high compliancy region or "relief structure" is created at the narrow trace-bump interface on the substrate side, which has the effect of diffusing the strain concentration at the die-solder interface, thereby reducing the magnitude of the max plastic strain, hence prolonging the fatigue life. The FEM analysis was aimed at testing this hypothesis. Various cases of BOL interconnection structure were analyzed along with the BOC structure as a control case and the maximum plastic strain in the solder joint was examined as a response variable (since fatigue life is governed by the magnitude of plastic deformation in each cycle). Fig. 2.4.1 shows the geometry and mesh for the BOL interconnect structure and Fig 2.4.2 shows the dimensions used for modeling the solder joints. These dimensions are representative of the actual structure of BOL solder joints in the test vehicle.

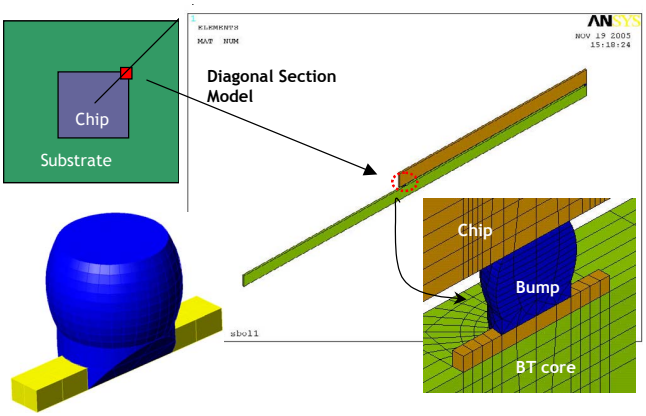
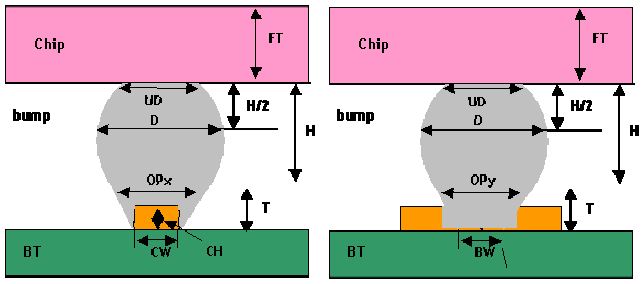


Fig 2.4.1 FEA model of solder joint with BOL interconnection



	UBM_Dia	Bump dia	Solder Height	SM open	SM ThK	Cu width	Cu ThK
	UD	D	I+T	OPx	T	CW	CH
BOC	0.090	0.110	0.075	0.095	0.040	0.115	0.020
BOL	0.090	0.110	0.075	N/a	0.040	0.030	0.020

Fig. 2.4.2: Dimensions used in the FEM analysis

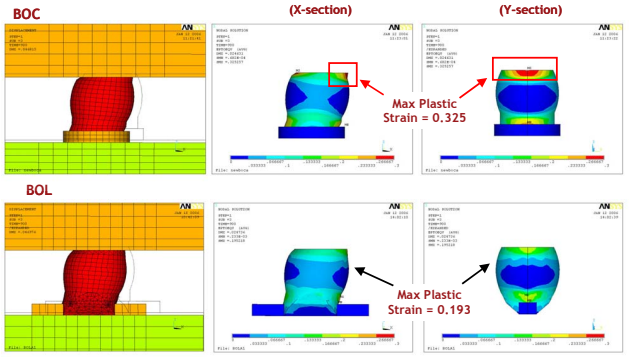


Fig. 2.4.3: Results of FEM analysis of the solder joints for BOC and BOL configurations

The emphasis in the analysis was to look at the maximum plastic strain in the corner-most solder joint, which would represent the location with the highest Distance from Neutral Point (DNP ~ 11.9 mm). Fig. 2.4.3 shows the modeling results for the BOC and BOL cases based on typical dimensional parameters in Fig. 2.4.2. The plastic strain contours viewed along the diagonal direction (X-section) and perpendicular to the diagonal direction (Y-section) are shown separately. It is evident from the contours that there is a considerable strain concentration at the solder-silicon interface which is the location of the max plastic strain in the BOC structure, whereas, in the BOL structure, the strain concentration seems to have been alleviated and the position of the max strain has moved closer to the solder-substrate interface in proximity to the narrow trace to which the bump is mated; furthermore, the magnitude of the max plastic strain in the BOL structure has dropped by approximately 35 %. These key results corroborate well with the empirical data from the Accelerated Fatigue Tests (section 2.2-2.3) in that the # of cycles to first failure for the BOL structure has increased and the cracking in the open solder joints is seen to occur at the solder-die interface in BOC versus at the solder-substrate interface in case of BOL.

As a further exercise, we have used the FEM models to study the variation of the max plastic strain as a function of the trace orientation and the trace width. Such analysis is valuable in defining the optimal BOL configuration in real substrate designs through the use of validated FEM models. It is important to note that, since the BOL land is rectangular (versus circular for BOC) the mechanics of solder deformation will depend on how the land is oriented with respect to the radial direction as referenced to the neutral point (center of the die); this is because thermal displacements occur along radial lines emanating from the neutral point. The results presented thus far were for a "parallel" orientation i.e. the orientation of the long dimension of the land is radially pointing towards the geometric center of the die. An alternate orientation would be the "perpendicular" orientation, wherein the land is running perpendicular to the radial direction. All lands in a real deign would have to fall within the limits of these parallel and perpendicular orientations. Also, the width of the BOL trace is critical, because, the narrower the trace, the more dense is the escape routing that can be achieved, however, other considerations such as substrate yield or substrate cost may require widening the trace, hence, it would be of interest to know how the max plastic strain changes with progressive widening of the trace. The analysis of trace orientation and trace width is summarized in Table 2.3.1. It is evident that there is a moderate dependence of strain on orientation and lead width, the perpendicular orientation giving approximately 15 % higher strain than the parallel orientation and the 50 um trace width giving approximately 20 % increase in strain, yet both of these cases result in strain values significantly lower than in the BOC configuration.

Design Type	Max Plastic Strain	Comment
BOC	**0.32526**	Control
BOL (30 um trace; parallel)	**0.19521**	Preferred Design
BOL (30 um trace; perpendicular)	**0.22785**	Effect of Orientation
BOL (40 um trace; parallel)	**0.21193**	Effect of BOL Land Width
BOL (50 um trace; parallel)	**0.23198**	

Table 2.3.1: Summary of max plastic strain data for different BOL cases configurations

The reduction of strain concentration at the bump-die interface has another significant consequence: it will result in lower stresses in the die especially in the sub-surface regions of the die, which is a blessing for new generations of Cu-low

K (commonly used Cu metallization and low dielectric constant insulation structure on Silicon) devices that are becoming increasingly sensitive to failure induced by CTE mismatch stresses.

2.5 Margin Testing (Wear out Modes)

The margin study was performed with 4 different underfill materials to check the underfill compatibility and the reliability performance of the ABF BU and BT laminate BOL FCBGA. The specification and properties of underfills are listed in Table 2.5.1. These underfills were selected with internal pre-evaluation to get the lowest package warpage and good compatibility with the flux used.

Table 2.5.2 shows the evaluation matrix and the results of the margin study up to unbiased HAST (Highly Accelerated Stress Test) 168hrs and TC "B" 2000x. There were 4 different underfills applied to ABF BU substrate and 2 different underfills applied to BT laminate substrate. Fig. 2.5.1 and Fig. 2.5.2 show the C-SAM (C-mode Scanning Acoustic Microscopy) analysis after assembly indicating normal void-free underfilling using standard assembly parameters (same as in case of BOC).

Underfill		Underfill A	Underfill B	Underfill C	Underfill D
Base Resin + Hardner		Epoxy/ Phenol	Epoxy/ Amine	Epoxy/ Amine	Aromatic Amine
Particle Size (Average)	um	2	2	2	2
Brookfield Viscosity @25℃	Pa.s	60	10	13	45
Tg (TMA)	C	70	80	122	120
CTE α 1(TMA*)	ppm/C	32	32	25	27
CTE α 2 (TMA)	ppm/C	110	116	79	97
Bending modulus	G Pa	9	8	12	10

* Thermo Mechanical Analyzer

Table 2.5.1: Comparison of pertinent mechanical properties of selected underfill materials.

Bill of Material			Reliability Test					
Substrate	Underfill	S/Size	EOL	MSL L3, 260°C	Unb-HAST "A"	TC "B"		
					168hrs	1000x	1500x	2000x
ABF BU BOL	A	20	0/20	0/20	0/10	0/10	0/10	0/10
	B	20	0/20	0/20	0/10	0/10	0/10	0/10
	C	20	0/20	0/20	0/10	2/10	0/8	0/8
	D	20	0/20	0/20	0/10	0/10	0/10	0/10
BT Lam. BOL	A	20	0/20	0/20	0/10	0/10	0/10	0/10
	B	20	0/20	0/20	0/10	0/10	0/10	0/10

Table 2.5.2: The margin study matrix and extended reliability test results.

The margin study results, depicted in table 2.5.2, showed all underfills had good reliability performance with BOL substrates, except for underfill C with ABF BU BOL substrate. C-SAM analysis after TC "B" 1000x, depicted in Fig. 2.5.3 (C), showed ABF BU BOL package with underfill C had the delamination at the corner of die after TC "B" 1000x. It is established that this delamination originated from the inside crack in the Si die, as seen in Fig. 2.5.5. It is not

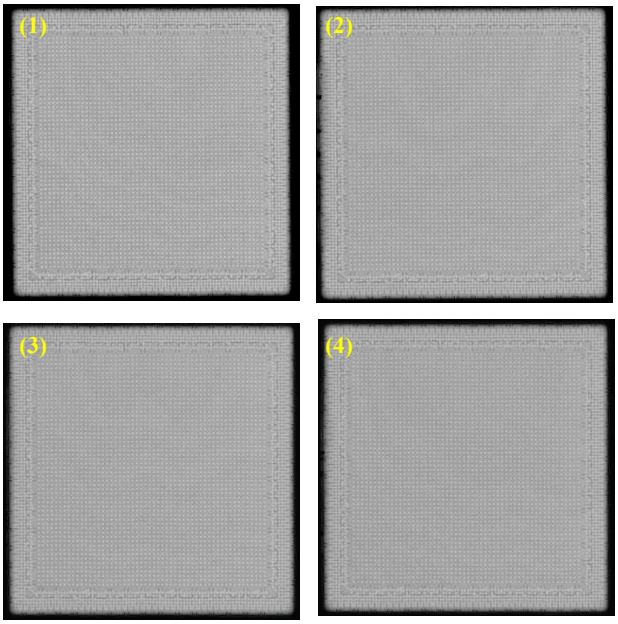


Fig. 2.5.1: C-SAM analysis result of ABF BU BOL package using (1) underfill A, (2) underfill B, (3) underfill C and (4) underfill D at EOL

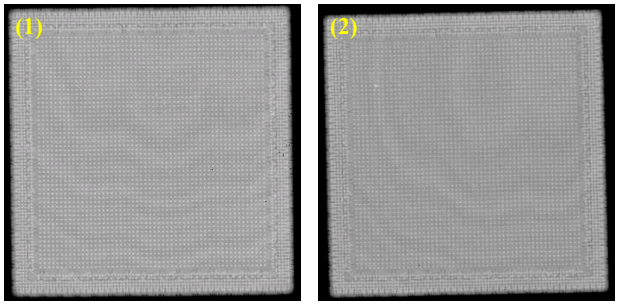


Fig. 2.5.2 C-SAM analysis result of BT laminate BOL package using (1) underfill A and (2) underfill B at EOL

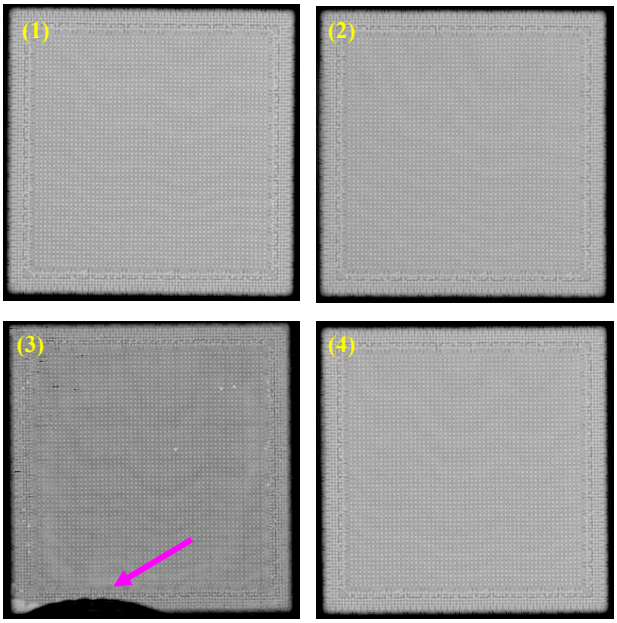


Fig. 2.5.3: C-SAM analysis result of ABF BU BOL package using (1) underfill A, (2) underfill B, (3) underfill C and (4) underfill D after TC "B" 1000x; (3) Underfill C showing the delamination at the die-corner area.

clear what caused this crack, for the failures did not get progressively worse with cycling up to 2000 cycles.

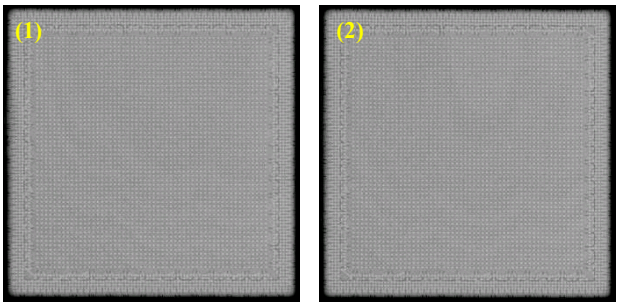


Fig. 2.5.4: C-SAM analysis result of BT laminate BOL package using (1) underfill A and (2) underfill B after TC "B" 1000x.

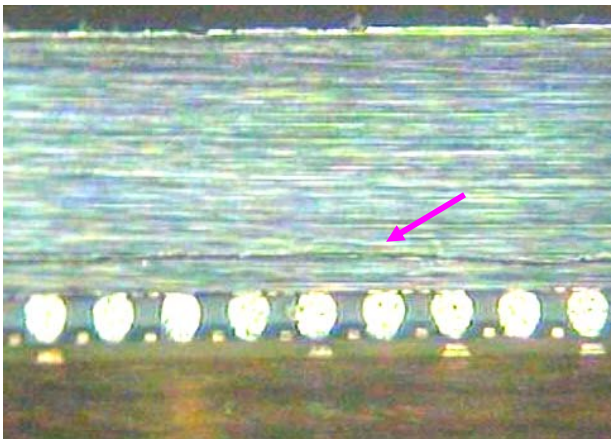


Fig. 2.5.5: Cross sectional analysis of ABF BU BOL package with underfill C, showing the die crack area after TC "B" 1000x.

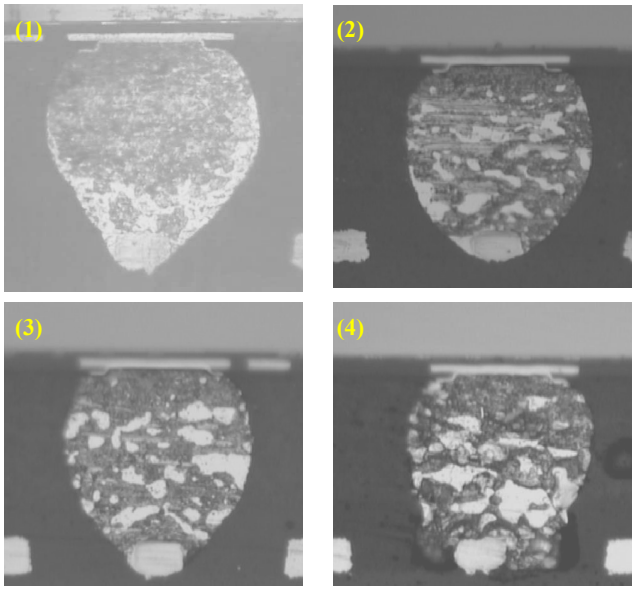


Fig. 2.5.6: Cross sectional analyses of ABF BU BOL with underfill A during Temp. Cycle, showing the robust solder joint up to 2000x; while some microstructure changes in the form of grain growth are apparent, there is no evidence of damage in the form of fatigue cracks; at (1) EOL, (2) 1000x, (3) 1500x and (4) 2000x.

While no open failures were detected up to 2000 cycles, cross sectional analyses was performed to gauge the onset of incipient damage in the solder joint structure with progressive cycling. As seen in Fig. 2.5.6, the solder joints of ABF BU BOL package had no evidence of damage in the form of fatigue cracking even though the microstructure showed coarsening of the grains in the hypereutectic phase as would be expected from the prolonged temperature exposure.

2.6 Package Qualification

Based on the accelerated fatigue testing and the margin study reliability performance, ABF BU BOL substrate and underfill A were selected for formal qualification. The package assembly and reliability testing were performed to assess the process repeatability and fulfillment of the internal reliability specifications i.e. unb-HAST "A" 168hrs, TC "B"1000X w/Precon and HTST 1000hrs. The internal qualification results are depicted in Table 2.6.1.

As seen in Table 2.6.1, all qualification legs were made with larger sample size of 66 units / 3lots to verify the reliability performance and to check the process repeatability of ABF-BU BOL package. The reliability results confirmed that the FC BGA with ABF BU BOL interconnection had acceptable reliability based on standard JEDEC specification of unb-HAST "A" 168hrs, TC "B" 1000x with precon. L3/260'C and HTST 1000hrs w/o precon, and was at least as reliable as the conventional FC BGA with BOC interconnection.

Matrix	Bill of Material			Reliability Test						
	Substrate	Underfill	S/Size	EOL	MSL L3, 260'C (30'c/85%RH 192hrs)	Unb-HAST "A"	TC "B" (-55'c ~ 125'c)		HTST(150'c) w/o Precon	
						168hrs	500x	1000x	500 hrs	1000 hrs
Leg 1	ABF BU BOL	A	66	0/66	0/44	0/22	0/22	0/22	0/22	0/22
Leg 2			66	0/66	0/44	0/22	0/22	0/22	0/22	0/22
Leg 3			66	0/66	0/44	0/22	0/22	0/22	0/22	0/22

Table 2.6.1 Internal qualification matrix and reliability results for unb-HAST "A", TC "B" and HTST (Hi Temp Storage Test) 1000hrs.

3. Significance of BOL Technology

3.1 Impact on Various Device Families

The escape routing of the I/O nets of a device places a significant burden on the density of flip chip substrates. In most cases, this means the use of more than one wiring layer for signals, and usually an additional wiring layer for a Ground return sandwiched between the two signal layers to maintain low parasitics. Hence, flip chip substrates in predominant use for flip chip packaging of Graphics, ASIC's and Chipsets tend to be 2-2-2 or 3-2-3 ABF Build-up substrates. BOL technology presents the highly desirable prospect of achieving all signal escapes on a single layer, which means the substrate layer structure can be reduced to a 1-2-1, or, in some cases, to a 4-lyr conventional through-hole laminate substrate. In order to assess the feasibility of escaping all signal nets of a device on a single layer, it useful to define a figure of merit which we will call the "effective

signal escape pitch" of a device, or ESEP for short. The ESEP of a device or die can be defined as the value of the perimeter of the die (expressed in some suitable units, such as microns) divided by the number of signal nets in the device. In can be appreciated that the ESEP effectively represents the I/O density of the device expressed in 1- dimensional form. It can be further appreciated that a fair assessment of the routability of a design on a single substrate layer can be made by comparing the value of ESEP with the minimum routable effective pitch that can be realized by a certain substrate technology. The reason why only signal nets are counted in calculating ESEP but not Pwr/Gnd nets, is that the Pwr/Gnd nets usually can be made to "drop" directly to planes by means of vias and do not require routing channels.

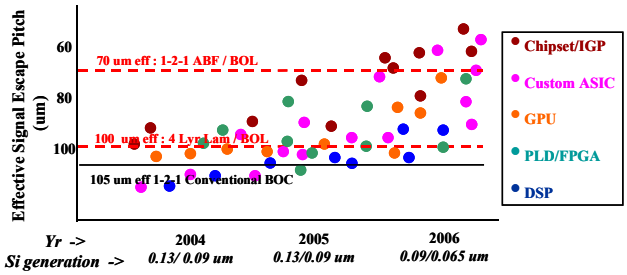
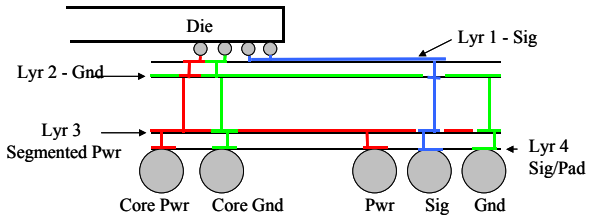


Fig. 3.1.1: Illustration of ESEP (Effective Signal Escape Pitch) of various device families; the lines represent the min effective pitch that can be realized by the use of BOL and BOC interconnection.

Fig. 3.1.1 is a diagram representing the ESEP for several device architectures covering past, present and future Si technology nodes. On the same plot are overlaid the minimum effective pitch that can be realized by 1-2-1 ABF and 4-Lyr through-hole laminate substrates using either BOL or BOC interconnection. As an example, referring to fig. 3.1.1, for a 1-2-1 ABF Build-up substrate, conventional BOC interconnection would realize an effective pitch of 105 um, whereas, BOL would realize a pitch of 70 um. Based on the ESEP for common devices, it is evident that a negligible percentage of devices could be routed on a single layer of a ABF Build-up substrate using BOC, but approximately 75 % of the designs would be routable using BOL interconnection. Furthermore, it is seen that almost 30 % of the designs would have been routable using conventional laminate through-hole substrates with BOL interconnection.



- Lyr 1 - signal escape routing
- Lyr 2 - Gnd Plane; provides micro-strip controlled impedance
- Lyr 3- Pwr plane (segmented if necessary)
- Gnd and Pwr pads routed under the die with large vias (could be thru hole)

Fig. 3.1.2: Typical layer stack-up for a 4-layer substrate based on BOL design methodology.

Fig. 3.1.2 represents a typical 4-ly substrate stack up and the partitioning of signal and ground nets among individual layers. The electrical environment for the signal nets is one of microstrip controlled impedance transmission lines. Furthermore, since there is no routing of signals on inner layers, there are no jogs or vias in the signal path in the region under the die, resulting in a cleaner parasitic environment than conventional BOC configurations that necessitate inner layer routing of signal nets.

3.2 Challenges and Next Steps

The focus of the present work has been to demonstrate the signal routing benefits of BOL interconnection and to prove the assembly feasibility and long term reliability of the asymmetric solder joint so formed. However a few challenges still remain (a) The conventional process of applying SOP (solder-on-pad) finish on the flip chip landing pads of the substrate results in lower yields due to the relatively small wettable surface area of the narrow leads exposed within the solder mask opening; this will require further optimization of the shape and size of both the exposed portion of the lead and the solder mask opening; such work is currently under way (b) Despite the improved escape pitch achievable by BOL interconnection, the pitch is still currently limited by the design rules of the solder mask (both minimum opening size and registration tolerance); a significant further reduction of effective pitch is achievable (from 70 um currently to approximately 55 um) by eliminating the solder mask as a solder confinement means; this will also require concomitantly shrinking the bump size to prevent adjacent trace shorting which is in fact feasible using plated bumping technology (c) To capitalize fully on the benefits of BOL interconnection, it is necessary to take BOL design methodology into account during the design of the bump array on the chip; for example, it is preferable to minimize the placement of Pwr/Gnd pads in the outer rows of the array, since these pads typically are "via'd down" to inner layers, thus requiring large capture pads which consume routing real estate.

Conclusions

A new kind of flip chip interconnection structure termed BOL (Bond-on-Lead) is demonstrated which enables more efficient routing of signal nets of a device on a single substrate layer. It is shown that the finer effective pitch achievable by BOL interconnection will allow greater than 70 % of flip chip designs for common device architectures like ASIC, GPU, FPGA, Chipset and DSP to be routed in 1-2-1 ABF Build-up or 4-lyr through hole laminate substrates. The long-term reliability of the asymmetric solder joint formed by BOL interconnection is demonstrated through successful margin testing and formal qualification. Using a combination of empirical testing and FEM analysis, it is shown that, contrary to intuition, the asymmetric BOL solder joint structure in fact results in the reduction of the maximum plastic strain in the solder, thereby prolonging the # of cycles to first failure as well as reducing the stress on the silicon induced by the mismatch in CTE between Si and the substrate. A few challenges and next steps are described that would simplify the broader adoption of BOL technology.

Refrences

1. Takami S. et al, "High Density Organic Laminate for High Pin-count Flip Chip Packages" *Proc 52nd Electronic Components & Technology Conference*, San Diego, CA, May 2002, pp 119-123.
2. Lai, C. S. et al, "Innovative Solutions to Enable Smaller Substrate Bump Pad Size for Flip Chip Technology" *Proc 54th Electronic Components and Technology Conference*, Las Vegas, NV, pp. 1471 – 1474.
3. IBM C4 Product Design Manual, Vol. 1: Chip and Wafer Design, Issue A, 1994.