5XCC0 Biopotential and Neural Interface Circuits

Digital Design

Analog-to-Digital Converters

Layout Techniques

Pieter Harpe

Outline

- Digital design
  - Power consumption & Low-power techniques
  - Technology scaling
- Analog-to-Digital Converters (ADCs)
  - Basics
  - Low-power architectures, circuits, and techniques
- Layout techniques
  - Floorplanning, parasitics, matching
  - Impact on power consumption, accuracy, speed

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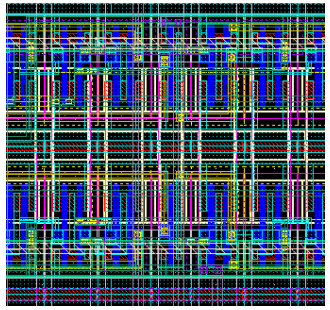
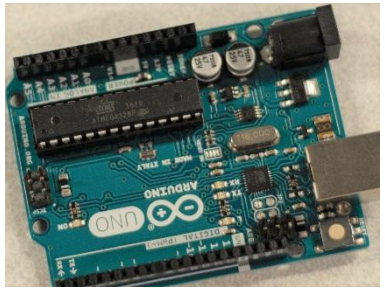
Low-Power Digital Design

System level

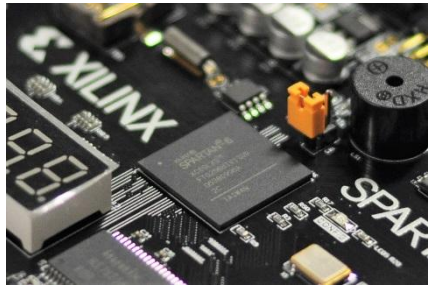
Application Specific Hardwired Logic



Microprocessor

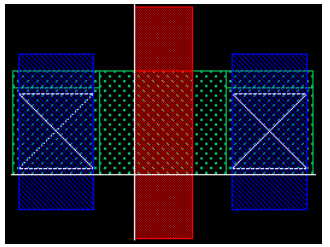


FPGA



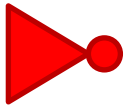
Technology level

0.18um



45nm

Circuit level

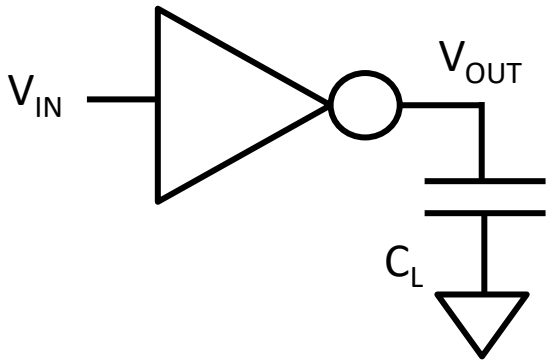


Logic

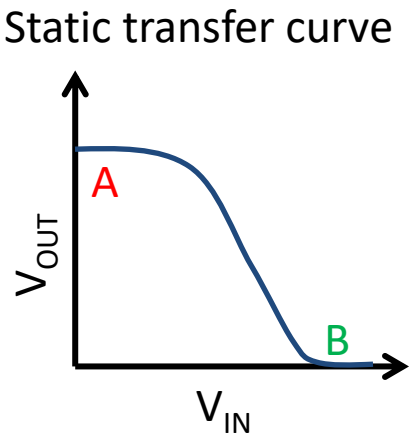
Memory

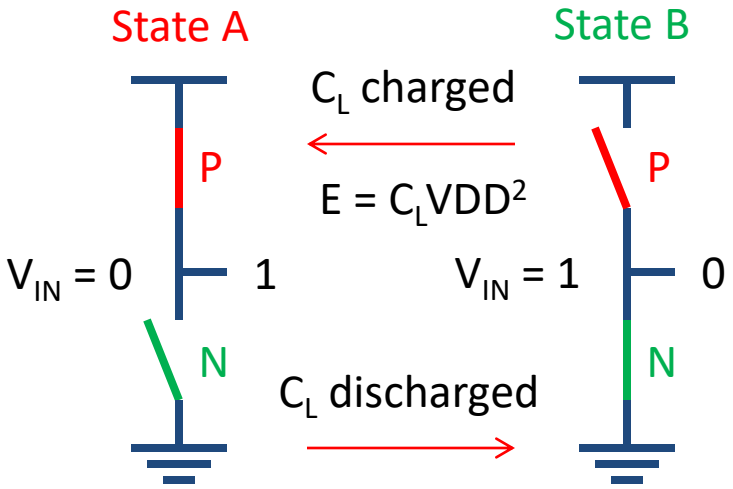
- What is the power consumption of a digital circuit (such as an inverter)?

1) Dynamic Power Consumption

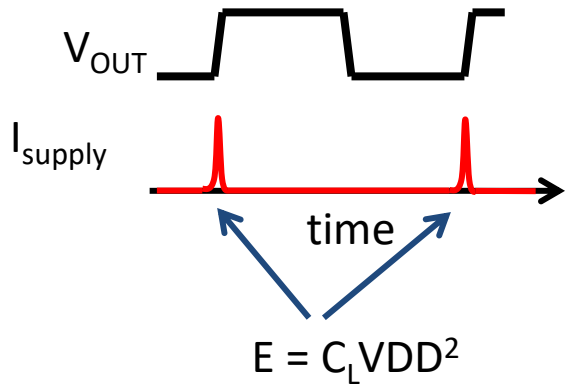


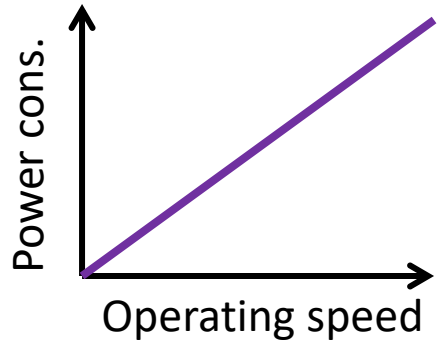
C_L represents the input capacitance of connected gates and parasitics of the wiring





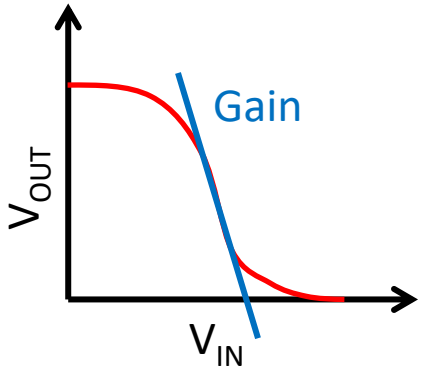
- <u>Dynamic</u> power consumption (proportional to frequency)
  - $f_{switch} C_L VDD^2$
- Minimized by:
  - Low C_L (W, L, wiring)
  - Low VDD

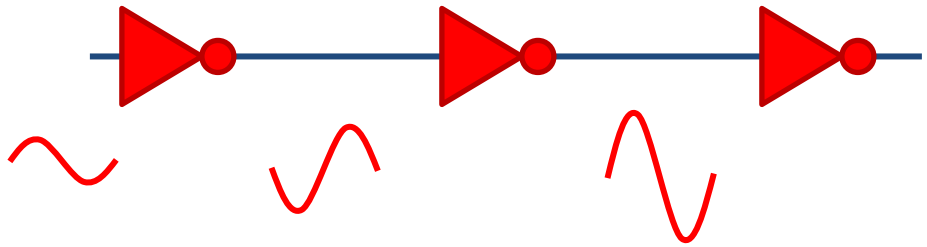




Minimize VDD

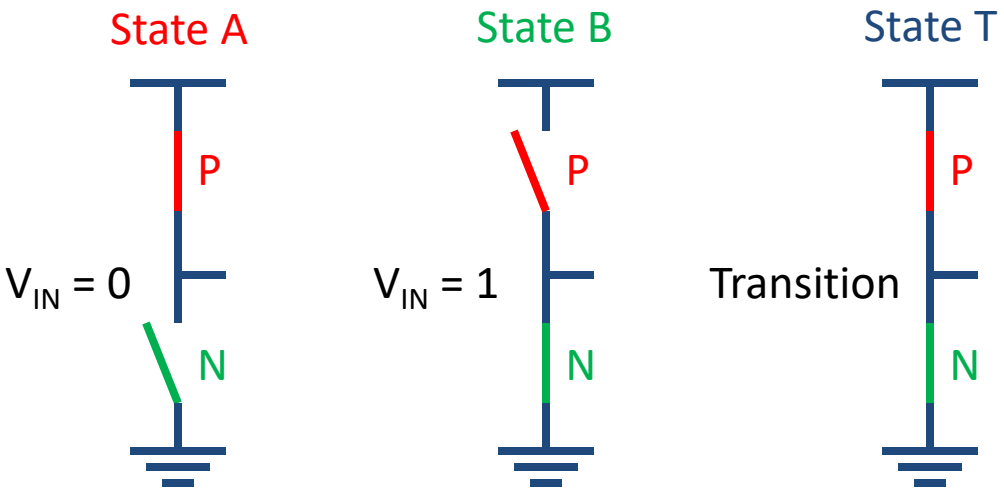
- |Gain| > 1 → Signal improves along the chain → Robustness

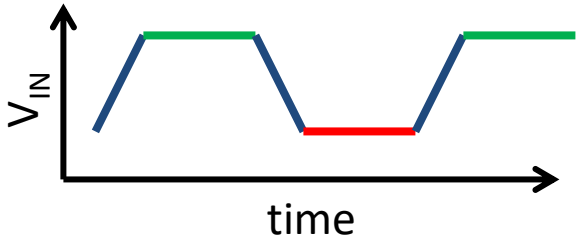




- If VDD is too low, |Gain| will become < 1
- If |Gain| < 1: signal quality degrades along a series of gates

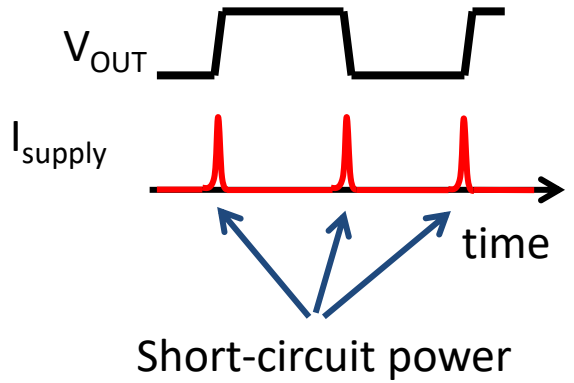
2) Short-Circuit Power Consumption

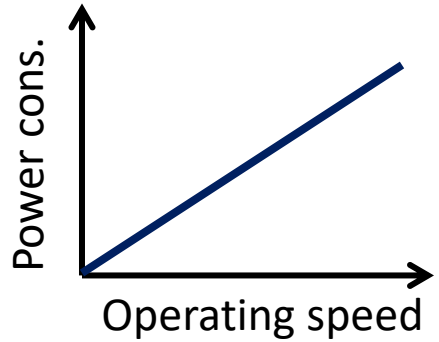




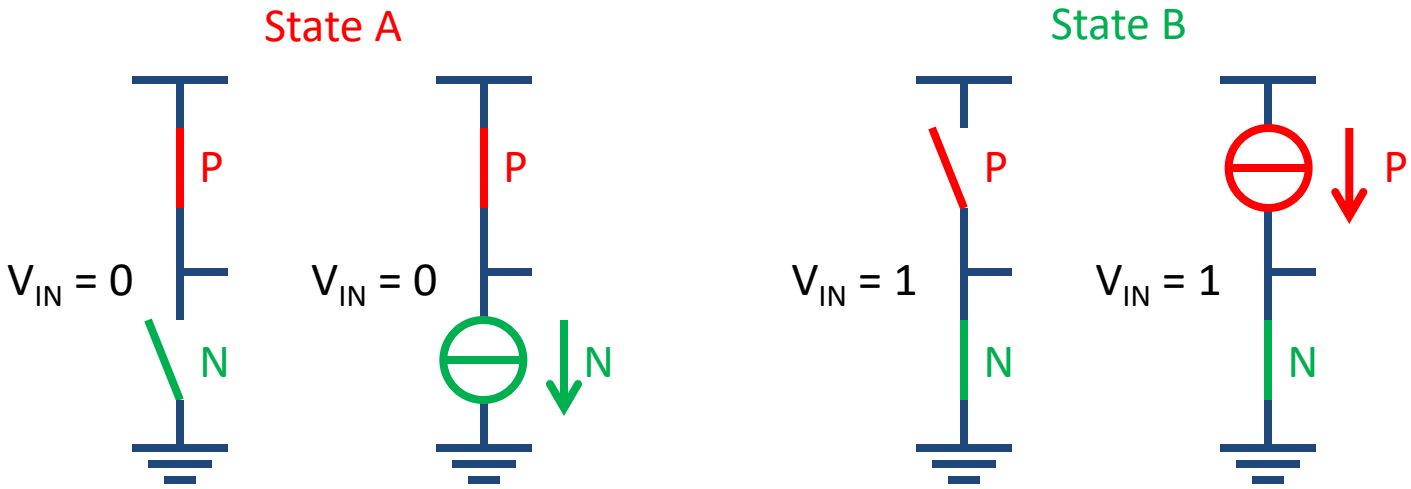
During each signal transition, both NMOS and PMOS might be *on* simultaneously, effectively creating a *short* from VDD to VSS.

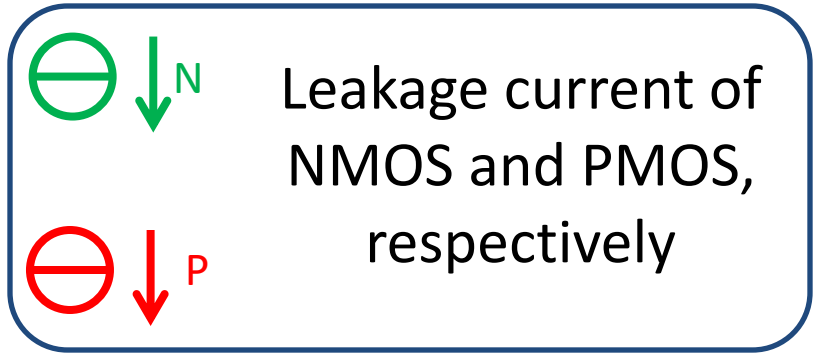
- This form of power consumption is also <u>dynamic</u>
- Minimized by:
  - Steep signal edges
  - High V_{th}
  - Low VDD



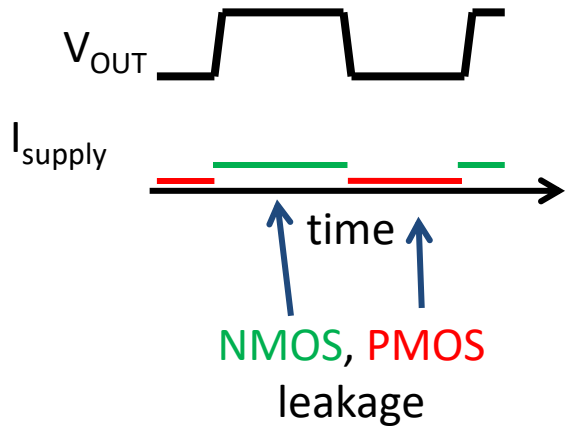


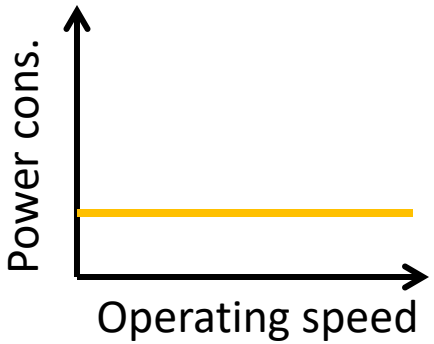
3) Leakage Power Consumption





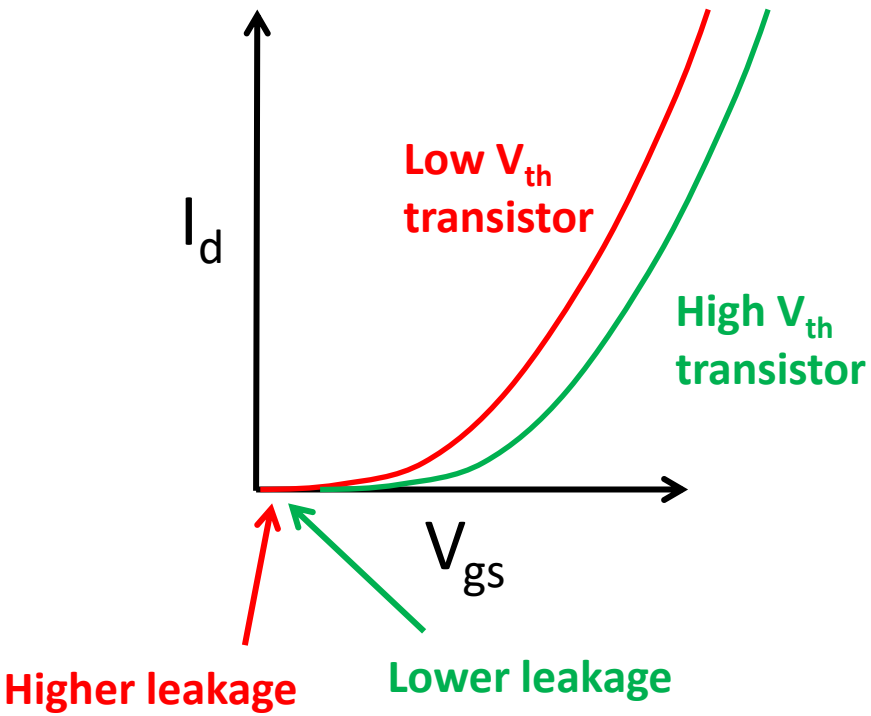
- Static form of consumption (independent of frequency)
- Minimized by:
  - Logic state (N or P leakage)
  - Low VDD, low W/L
  - High V_{th}, use V_{bulk} to increase V_{th}

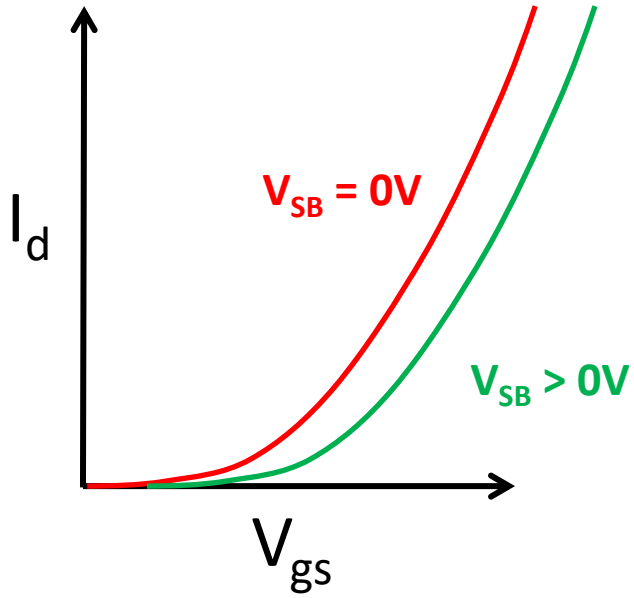




Influence of V_{th}, V_{SB}

- Higher V_{th} → Usually lower leakage
- V_{SB} (body effect) can be used to effectively increase V_{th}

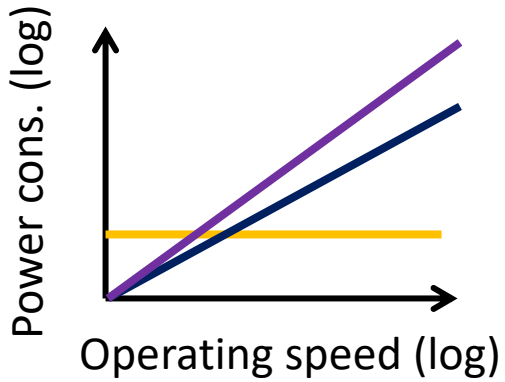




V_{th} shifted by bulk-voltage:
Mimic low V_{th} and high V_{th} devices

Total Power Consumption

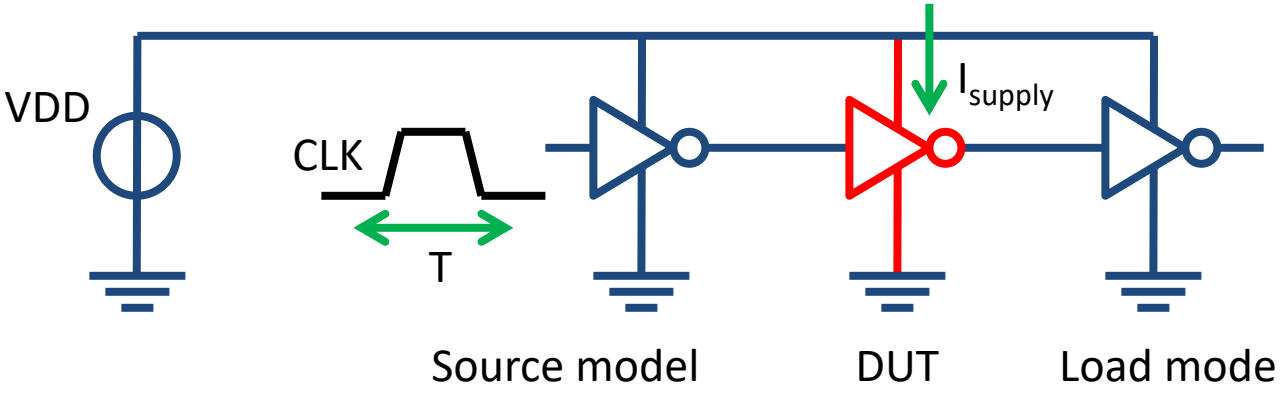
- Dynamic power + short-circuit power + leakage

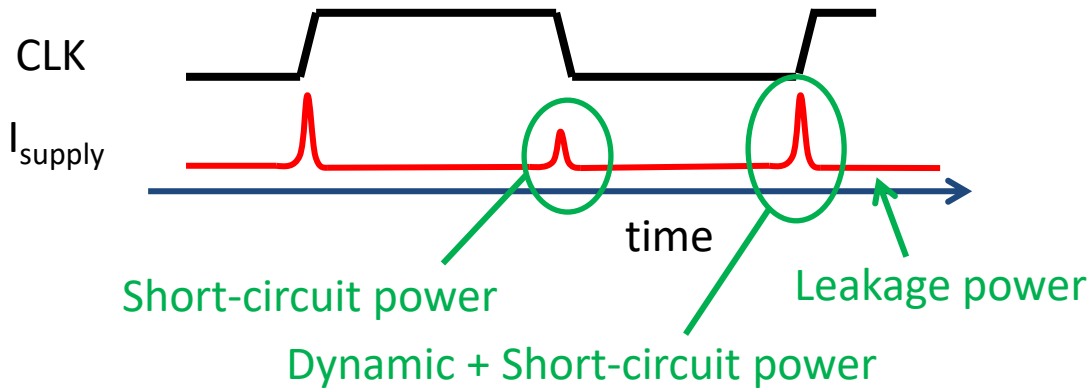


- Power optimization = trade-off!
- Low-speed applications (~kHz-range): Leakage may be dominant
  - Optimize for leakage
  - Little benefit from technology scaling (discussed later)

How to Simulate Power Consumption?

- Transient simulation; model source and load (e.g.: with another logic gate)
  - A good source model is required to have realistic signal transition edges
  - A good load model is required to have a realistic C_L



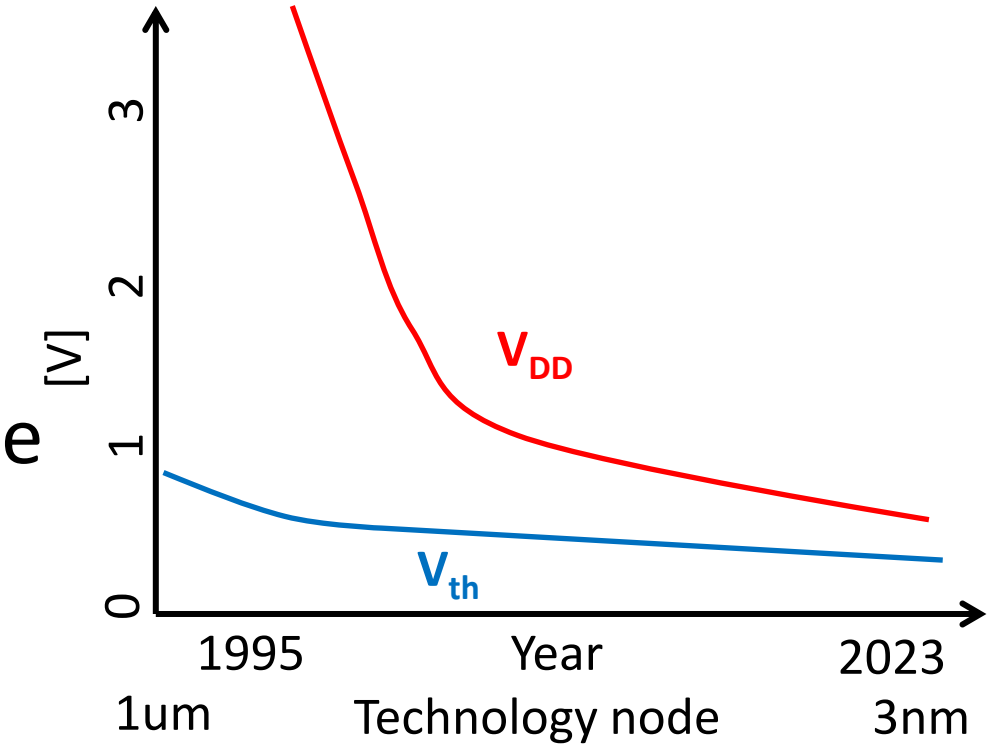


– Integrate over one full period

$$\overline{P} = VDD \cdot \overline{I_{supply}} = \frac{1}{T}\int_0^T VDD \cdot I_{supply}(t)dt = \frac{VDD}{T}\int_0^T I_{supply}(t)dt$$

Technology Level

- Moore's law / technology scaling:
  - Transistor dimensions are decreasing over time
- Area scales down
  - More complexity on same area
- Dynamic power scales down
  - Power $\propto C_L VDD^2$
- Short-circuit power may also decrease
  - V_{th} scales slowly compared to V_{DD}
- Leakage increases substantially
  - Side-effects from small dimensions



Exercise 1: Digital Power Consumption

Suppose we have a chain of 3 identical inverters. The first inverter models the source, the third inverter models the load, and the second inverter is our DUT of which we simulate the power consumption at VDD = 1V and f_{clk} = 1MHz

What will happen with the dynamic power consumption, the short-circuit power consumption and the leakage power consumption if:

a) We change f_{clk} to 2MHz
b) We change VDD to 1.2V
c) We double the W's of all transistors in all 3 inverters
d) We increase the V_{th} of all transistors in all 3 inverters

Exercise 2: Digital Power Consumption

Suppose we have simulated the power consumption of a digital inverter in a few cases, as given below:

Case	Condition	Simulated average power consumption
1	1MHz clock frequency, nominal load C_L	2nW
2	2MHz clock frequency, nominal load C_L	3.8nW
3	1MHz clock frequency, double load $2C_L$	3.6nW

a) Split the power consumption for case 1 in leakage, dynamic, and short-circuit consumption

b) How much will this inverter consume when operating with nominal load C_L at a clock frequency of 10kHz?

c) If the inverter has to operate at 10kHz, which actions could you take to reduce the power consumption?

Summary – Digital Design

- Low-power digital circuits
  - System, technology, circuit-level optimization
  - Dynamic, short-circuit and leakage power consumption
  - For biomedical applications with low frequency operation:
    - Leakage might be dominant
    - Technology scaling is (often) not very helpful

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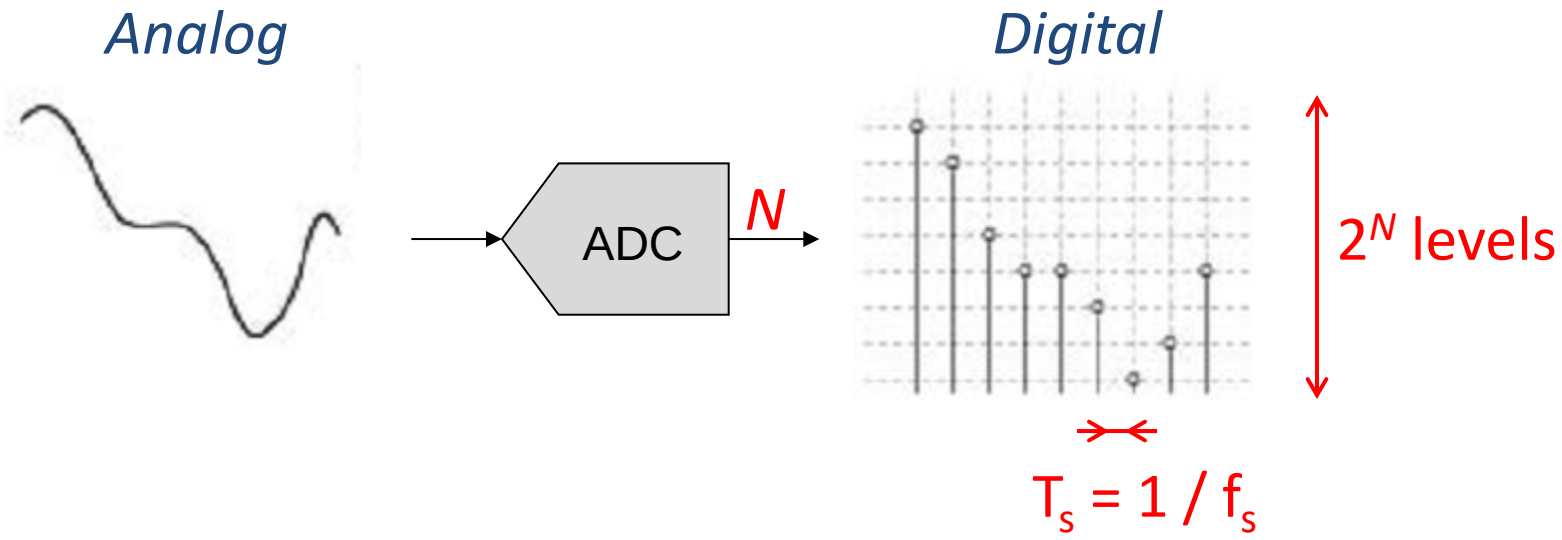
Analog-to-Digital Converters (ADCs)

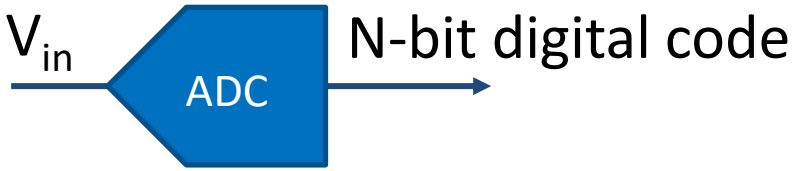


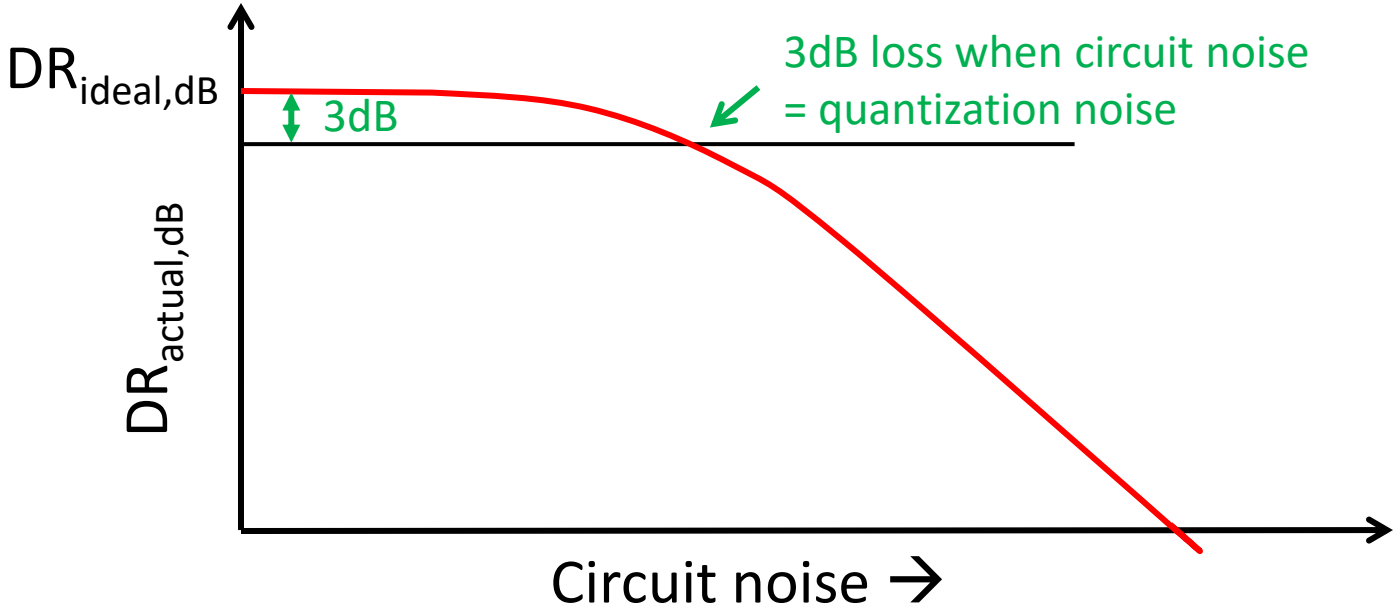
- 3 important parameters:
  - Resolution *N* [bits]
  - Sample frequency f_s [Hz]
  - Power consumption *P* [W]

Example: N = 3 has $2^3 = 8$ levels:
000, 001, 010, 011,
100, 101, 110, 111

ADC Resolution and DR

- DR of the ADC is limited by both analog and digital DR
  - Digital side: limited by # bits N: $DR_{ideal,dB} = 6.02N + 1.76$
  - Analog side: limited by circuit noise
- Overall: $DR_{actual,dB} = 6.02ENOB + 1.76$



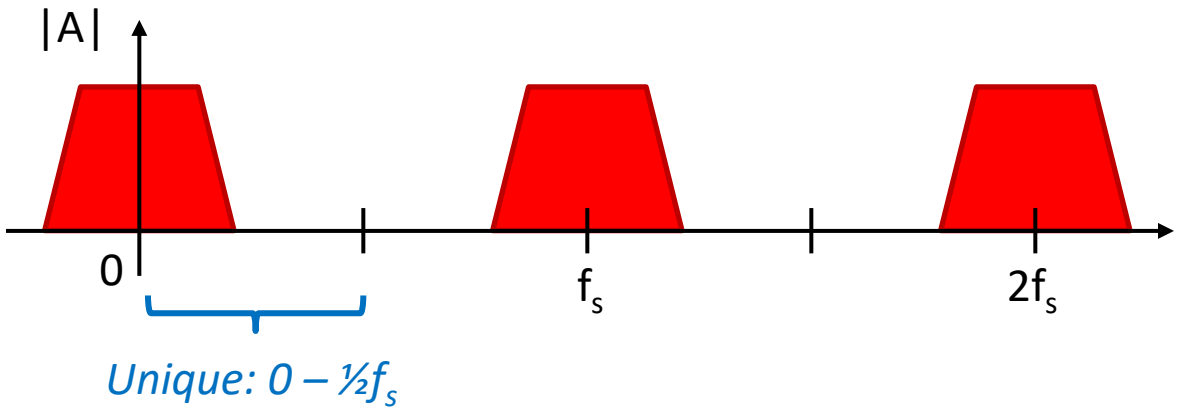


ENOB is the effective number of bits (or effective resolution) including the effects of quantization noise and circuit noise

- Ideally equal to N
- In practice smaller than N

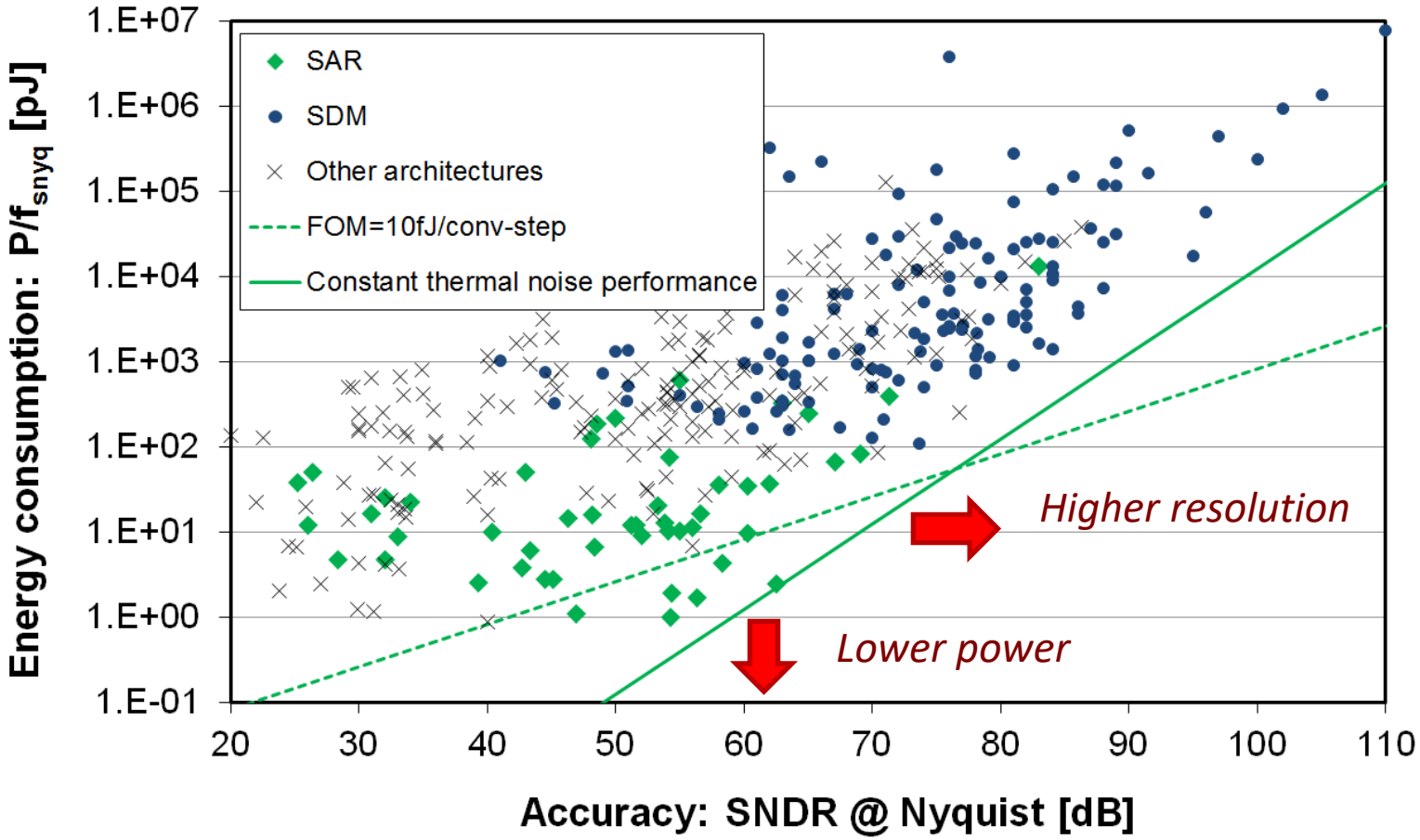
ADC Sample Rate f_s and Bandwidth *BW*

- Nyquist sampling criterium:
  - An analog signal can be reconstructed as long as the sample rate f_s is at least twice the bandwidth of the signal: BW $\leq$ ½f_s
- Aliasing:
  - When sampling an analog signal, aliasing occurs at multiples of f_s
    - Only spectrum up to ½f_s is unique, the rest is repetitive



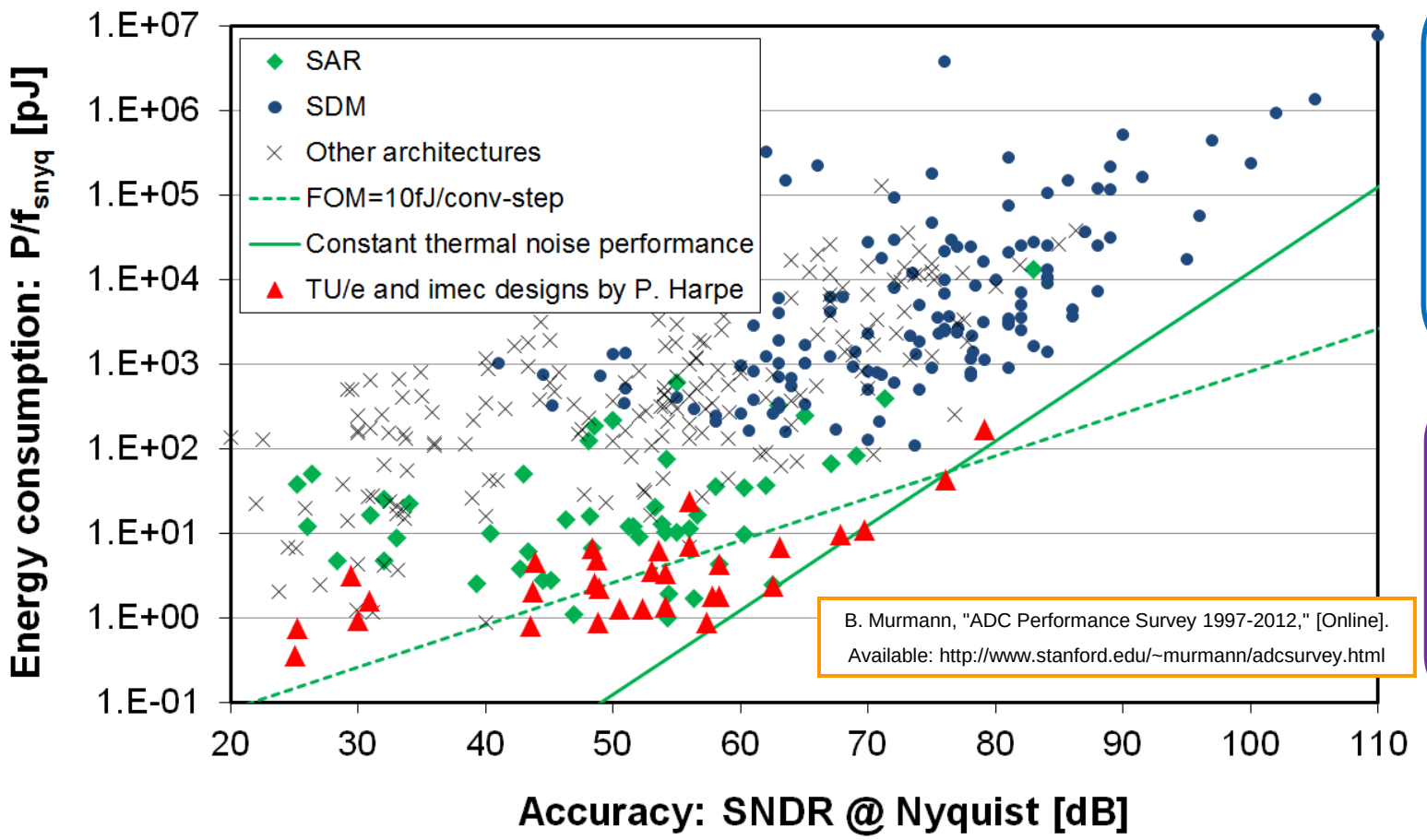
Low-Power ADCs

- SAR: Successive Approximation Architecture

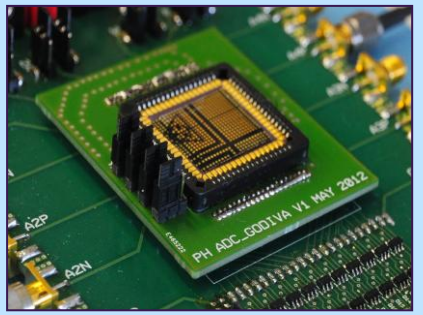


B. Murmann, "ADC Performance Survey 1997-2012," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

TU/e ADC Research

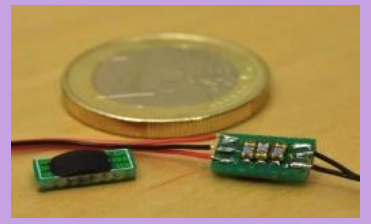


Pacemaker/ICD

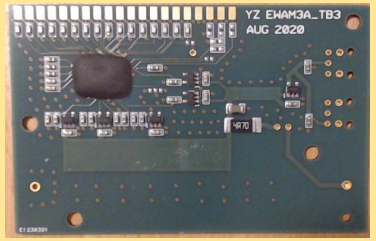


Body-Area Network Communication

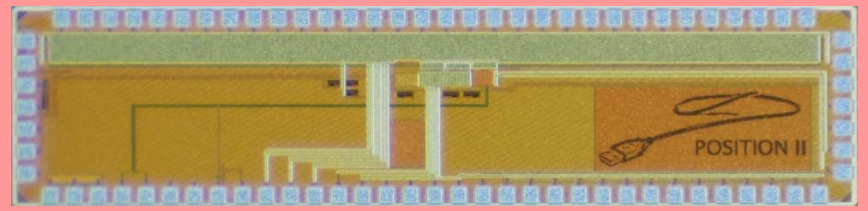
3nW ECG recording ASIC



16-channel fECG pregnancy monitor

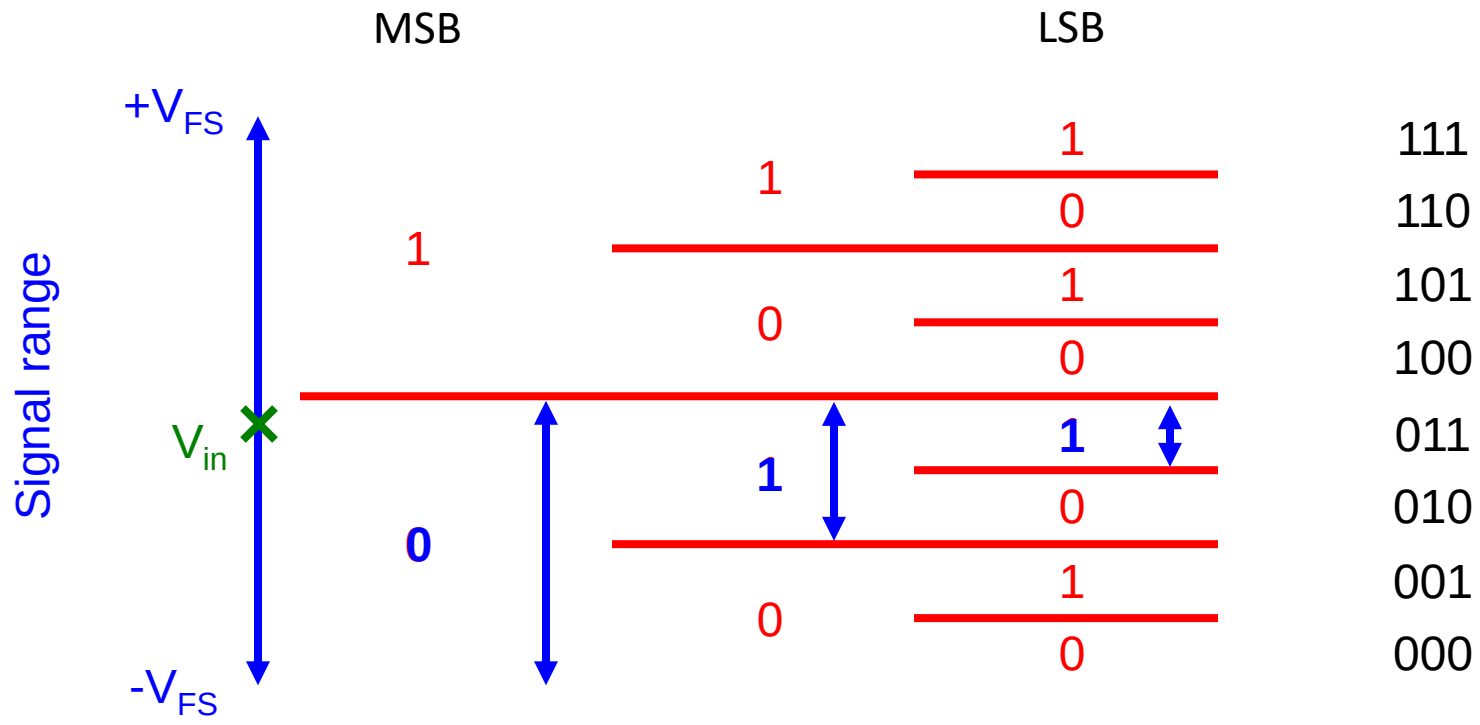


32-channel ultrasound digitizer



SAR Principle (N-bit ADC)

- Binary search to approximate the analog input in N cycles



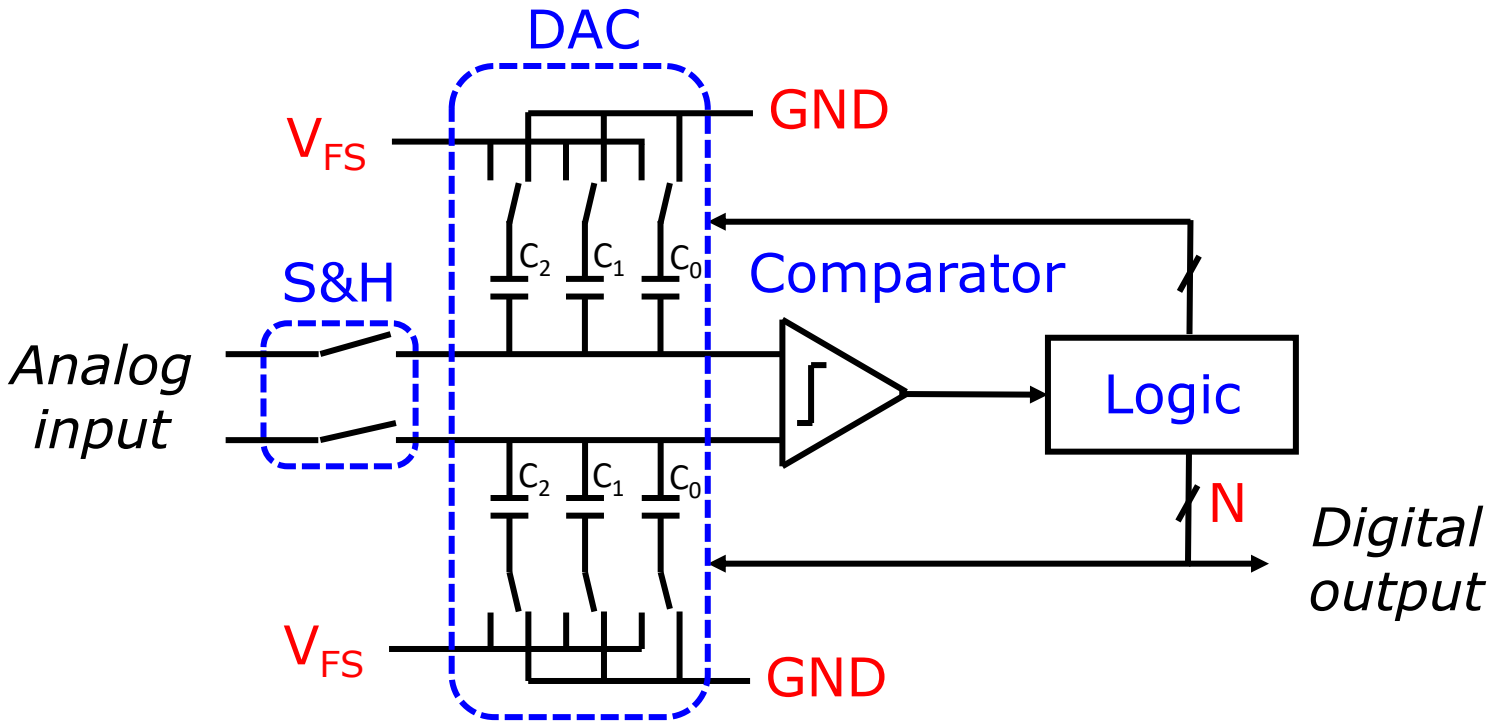
1. Set compare-level to middle of the range
2. Compare to determine one bit
3. Select remaining half of range

Example for N = 3bit

- S&H to hold input signal,
  DAC to create references, comparator, logic for algorithm

SAR ADC Architecture

1. Sample input
2. Repeat N times
    1. Compare
    2. Store result
    3. Switch DAC



Example for N = 4bit

$C_i = 2^i \cdot C_0$

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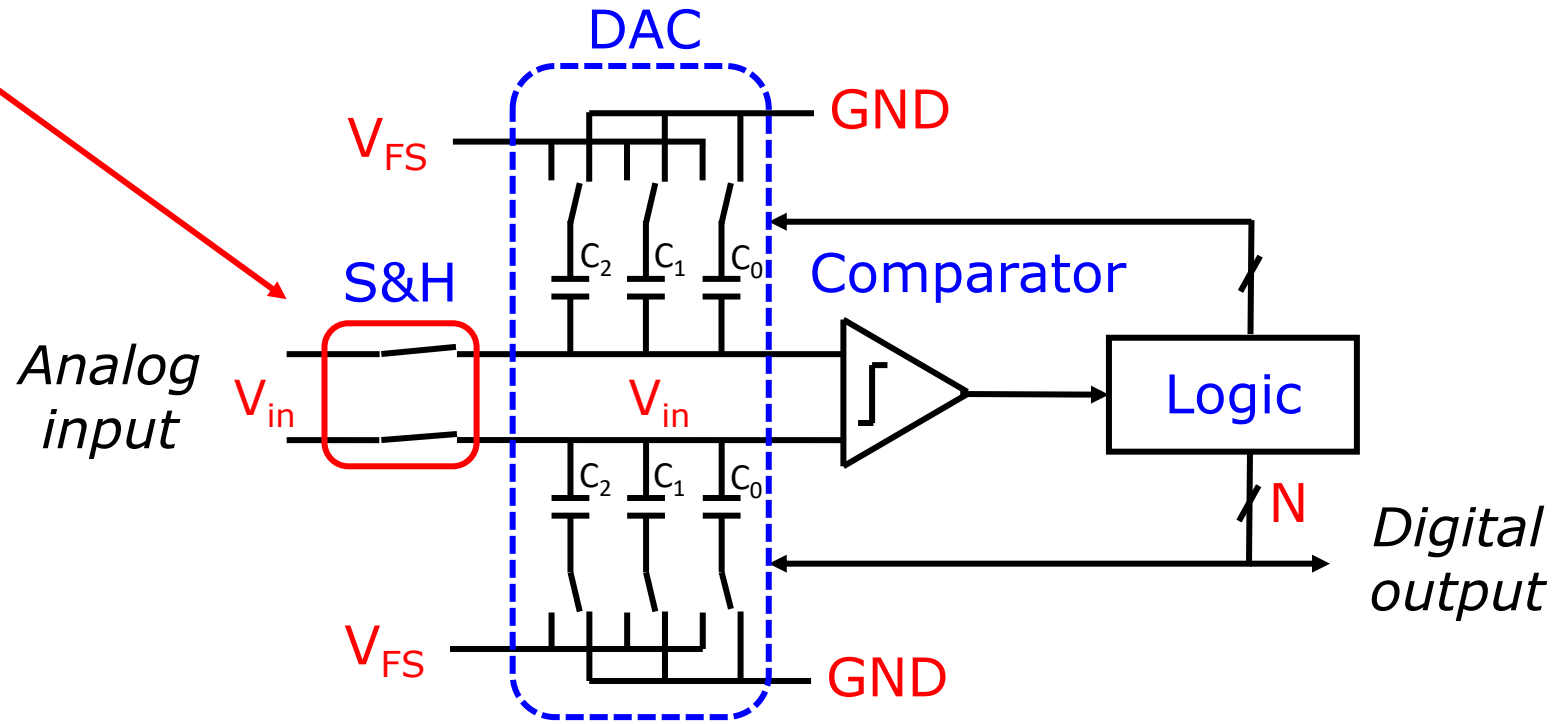

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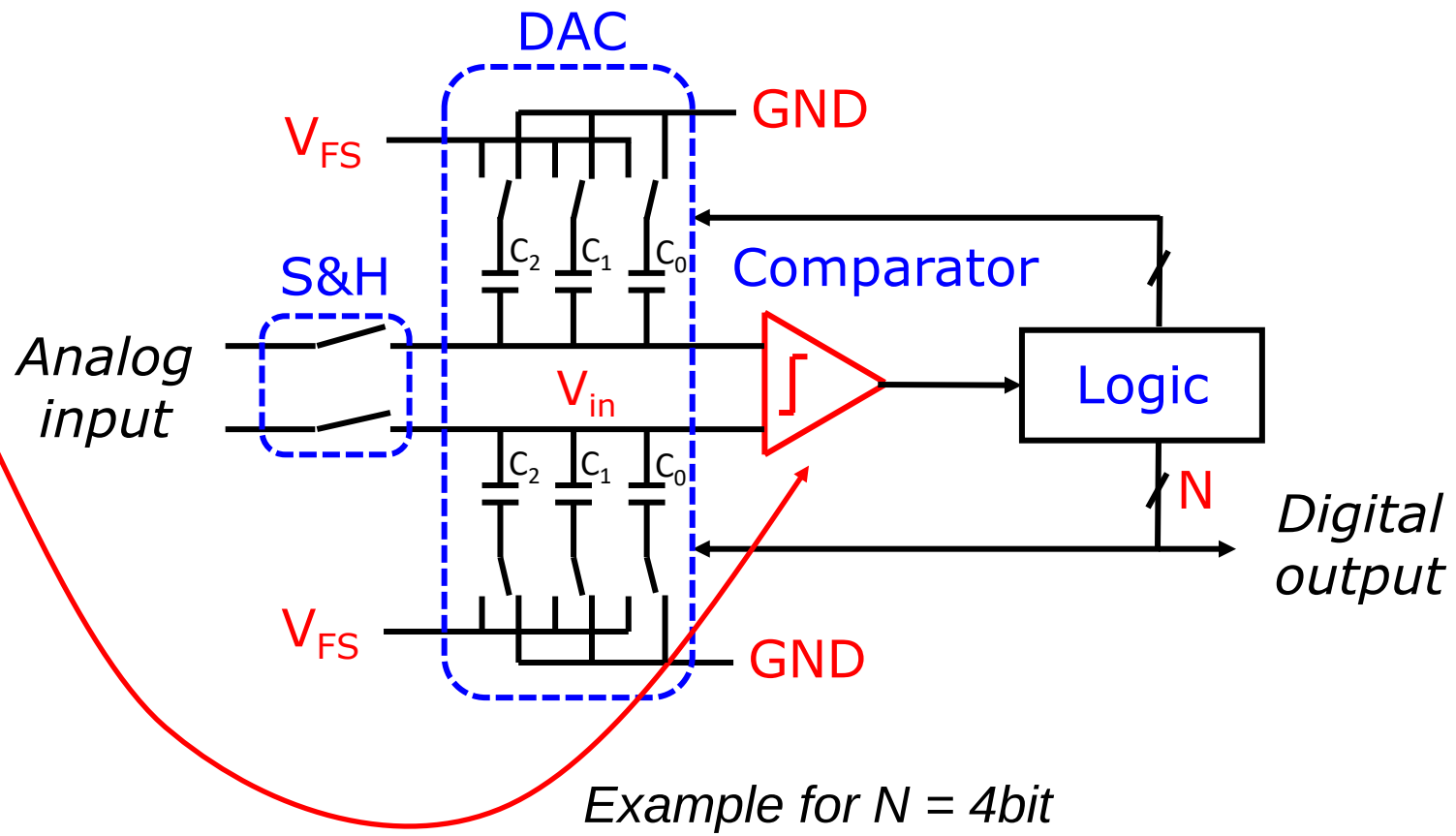

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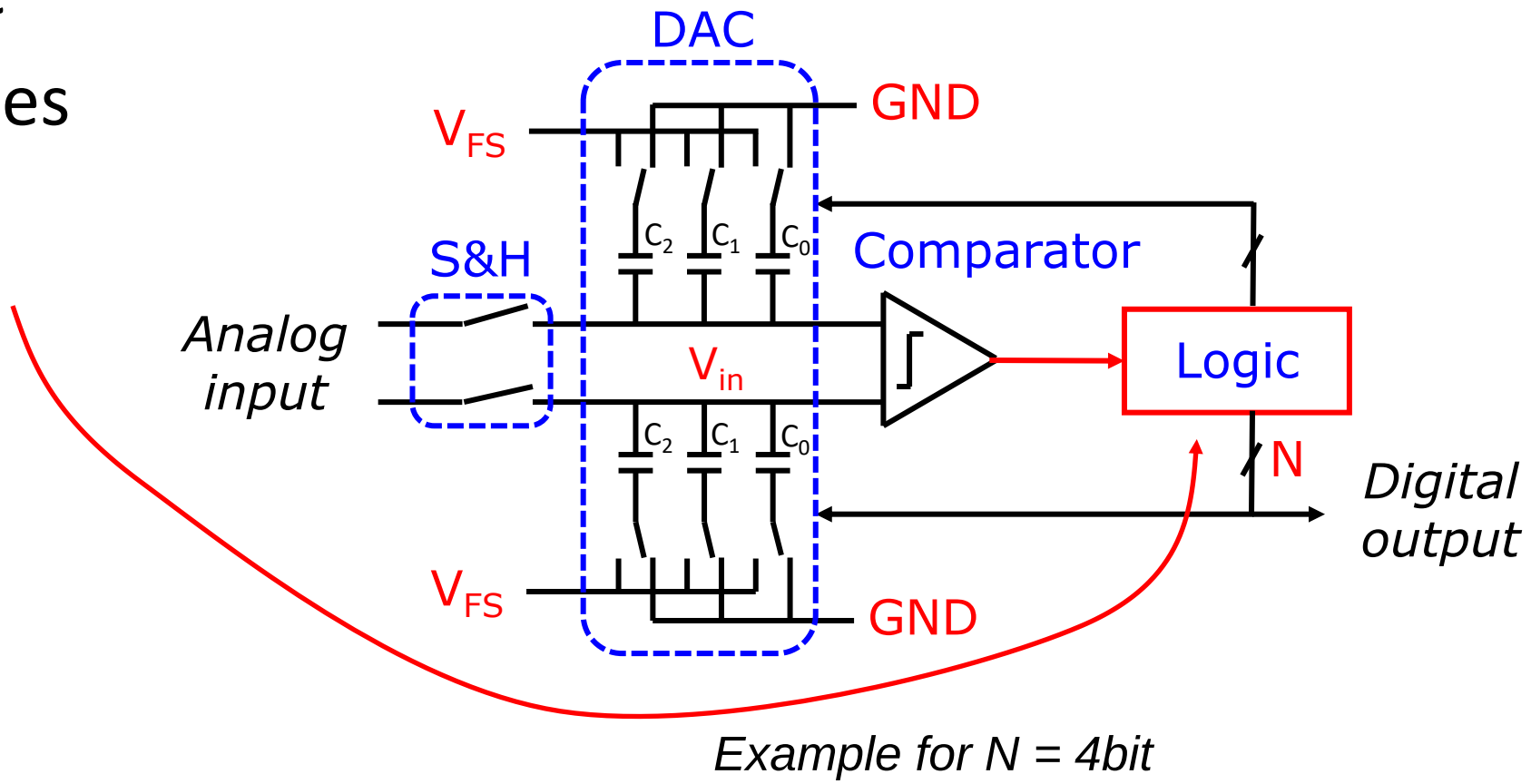

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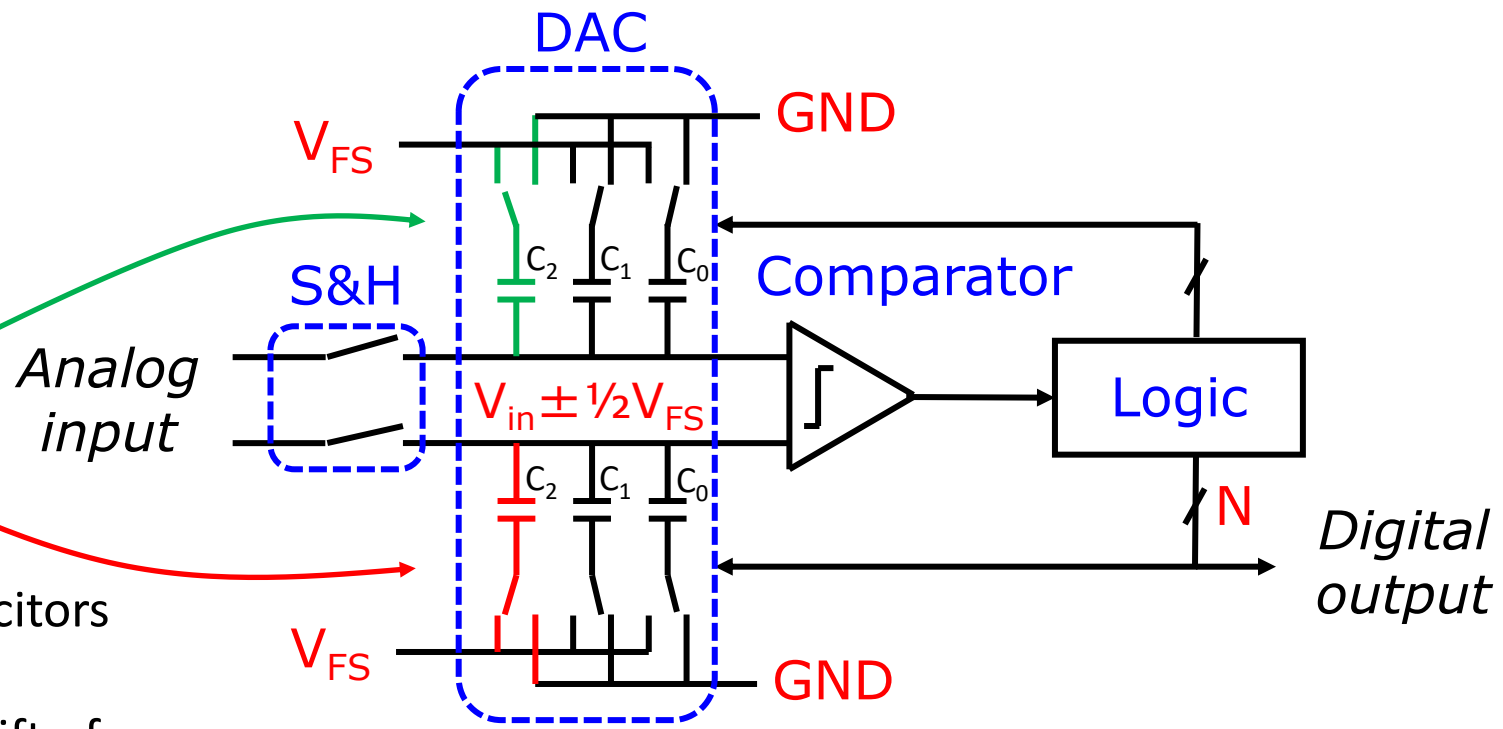


Switch one of the two capacitors from GND to V_{FS}
Creates a $+½V_{FS}$ or $-½V_{FS}$ shift of the comparison level

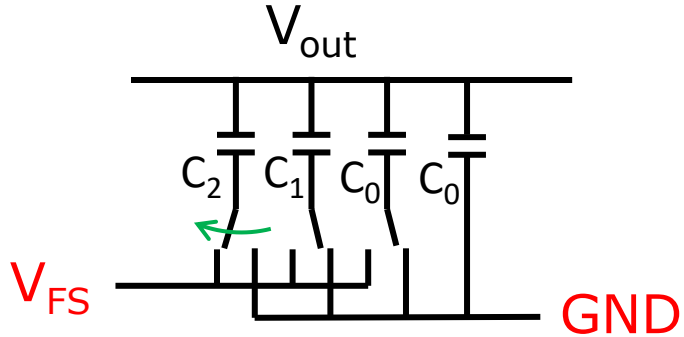
Example for N = 4bit

- We need to compare N times to get N output bits
- Because the DAC switches after the comparison, we only need an N-1 bit DAC

Digital-to-Analog Conversion

- Charge redistribution principle. N-1 capacitors for N-bit ADC
- Binary-scaled capacitors: $C_i = 2^i \cdot C_0$ and $C_{sum} = 2^{N-1} \cdot C_0$
- What happens when C_2 is switched from GND to V_{FS}?
  1. Assume before switching: $V_{out} = V_{in}$
  2. Switching C_2 causes a voltage step at the output of:
     $\Delta V_{out} = (C_2 / C_{sum}) \cdot V_{FS} = ½ V_{FS}$
  3. After switching: $V_{out} = V_{in} + ½ V_{FS}$

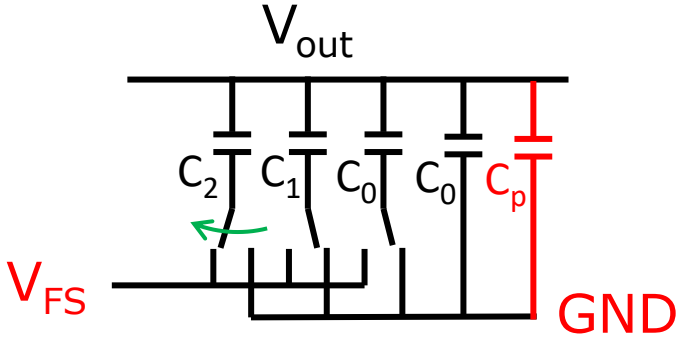
- Likewise, C_1 causes a step of $¼V_{FS}$, etc.



Example for N = 4bit

Parasitics and Full-Scale Range

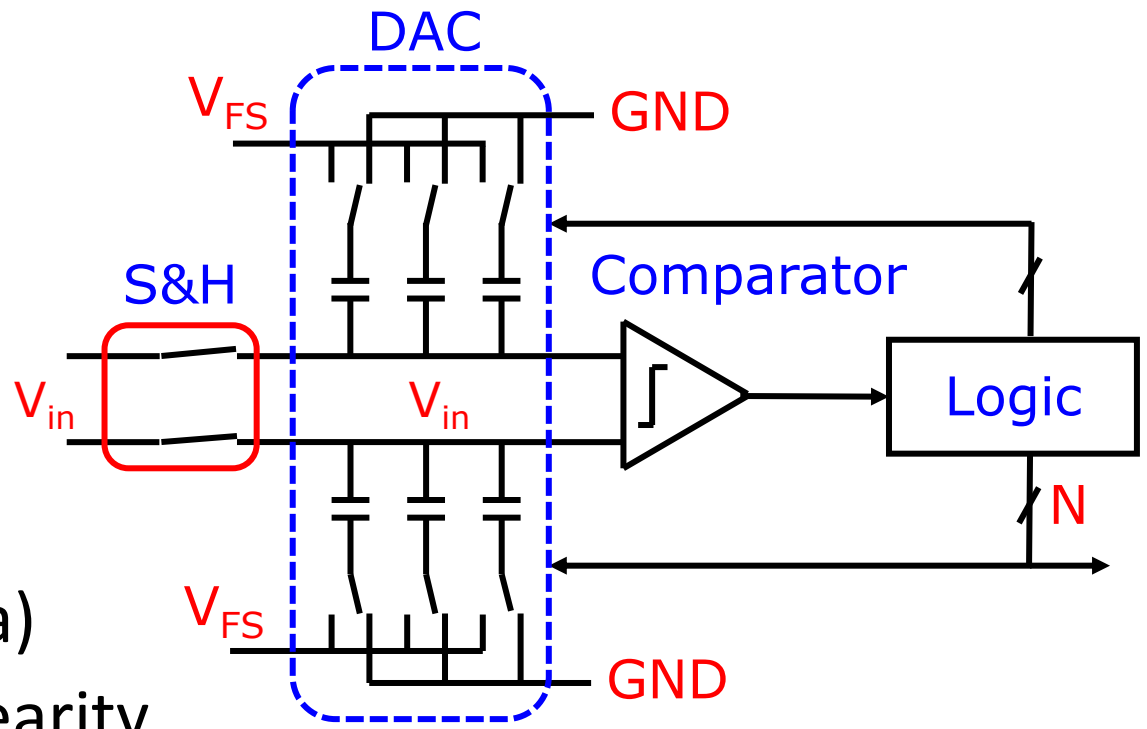
- What happens if we add a parasitic C_p to GND?
- $C_i = 2^i \cdot C_0$ and $C_{sum} = 2^{N-1} \cdot C_0 + C_p = C_{DAC} + C_p$
- What happens when a capacitor is switched from GND to V_{FS}?
  - C_2: $\Delta V_{out} = (C_2 / C_{sum}) \cdot V_{FS} = 4C_0 / (C_{DAC} + C_p) \cdot V_{FS}$
  - C_1: $\Delta V_{out} = (C_1 / C_{sum}) \cdot V_{FS} = 2C_0 / (C_{DAC} + C_p) \cdot V_{FS}$
  - C_0: $\Delta V_{out} = (C_0 / C_{sum}) \cdot V_{FS} = 1C_0 / (C_{DAC} + C_p) \cdot V_{FS}$



- Steps are still binary-scaled
- Full-scale range is reduced by a factor $C_{DAC} / (C_{DAC} + C_p)$
  - E.g.: if $C_{DAC} = C_p$, the full-scale range becomes $\pm\frac{1}{2}V_{FS}$ instead of $\pm V_{FS}$

DAC: Noise, Linearity, Power Consumption

- Sampling **noise**:
  - $P_n = kT / C_{sum}$ (for one side)
  - $P_n = 2kT / C_{sum}$ (differential)
  - Larger C_{sum} for improved noise
- **Linearity**:
  - Capacitor mismatch ($\sigma_{\%} \propto 1 / \sqrt{\text{Area}}$)
  - More area (larger C's) for better linearity
- **Power consumption**:
  - $E_{DAC} \propto C_{sum} V_{FS}^2 \rightarrow P_{DAC} \propto f_s E_{DAC}$
  - Dynamic power consumption (proportional to f_s), proportional to C_{sum}



Capacitor Design – kT/C Noise Limit

- Given a required number of bits N: $DR_{ideal} = 6.02N + 1.76$ [dB]
- $P_{signal} = \frac{1}{2} V_{FS}^2$ and $P_{noise} = 2kT / C_{sum}$ → SNR

Assuming 0.7V signal amplitude ($1.4V_{pp}$),
and kT/C noise = quantization noise (SNR = DR_{ideal})

# bits N	2^{N-1}	$C_{sum} = 2^{N-1}C_0$	C_0
6	32	0.2fF	6aF
8	128	3.3fF	26aF
10	512	52fF	104aF
12	2048	0.8pF	0.4fF
14	8192	13pF	1.6fF
16	32768	0.2nF	6.4fF

- C_{sum} and C_0 are quite small!

MIM Capacitors

- MIMCAP: Metal-Insulator-Metal Capacitor

$$C = \frac{\varepsilon_o \varepsilon_r A}{d}$$

3D view

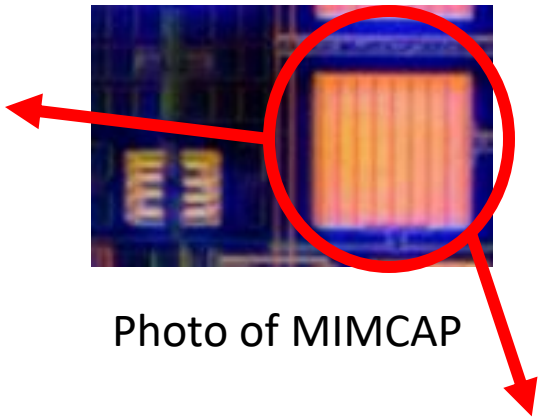
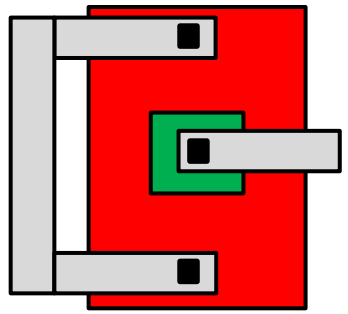


Photo of MIMCAP

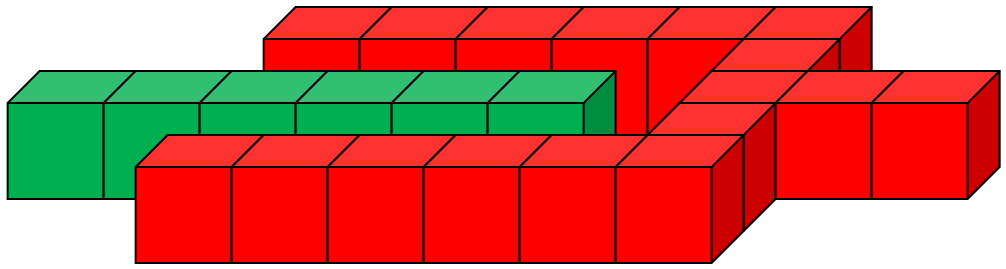
- Special component provided by foundry
- Designer can only choose A to change C
  - Other parameters are fixed
- Practice: minimum C e.g. 10 – 50fF
  - Area inefficient if the capacitor is small (see top view)



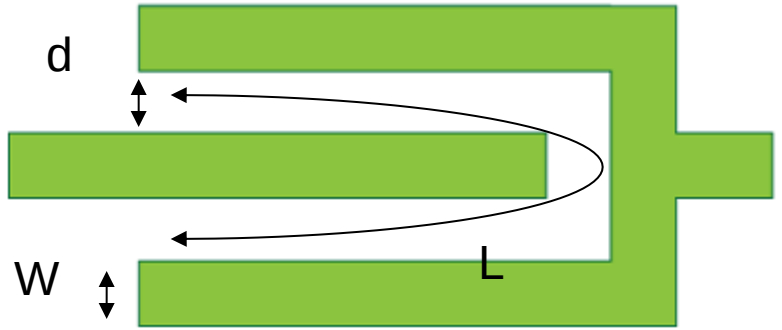
Top view

MOM Capacitors

- MOMCAP: Metal-Oxide-Metal Capacitor



3D view

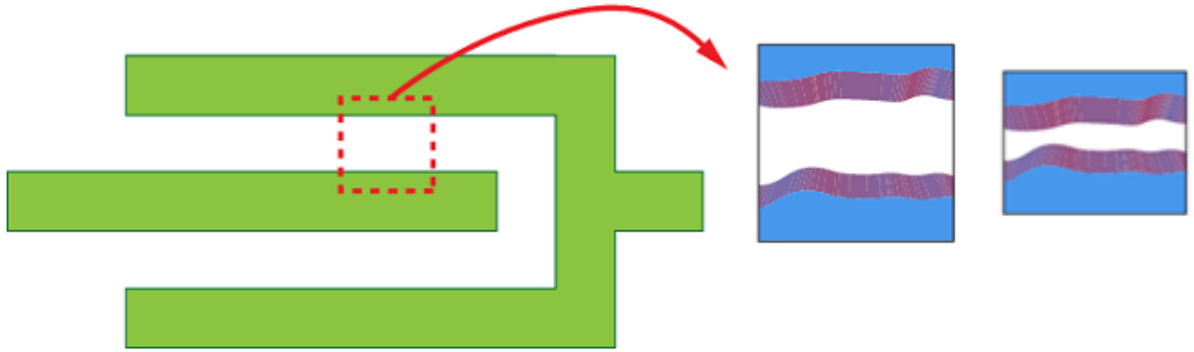


Top view

- Hand-made by the designer; can choose d, L, W
  - More freedom → Ability to optimize matching and capacitance
- No strict minimum C; even <<1fF is feasible
  - Less overhead

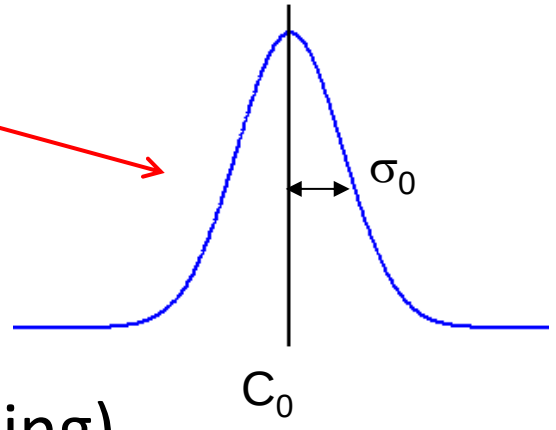
Random Capacitor Mismatch

- LER: Line-Edge Roughness



- Random fluctuation
- Capacitor mismatch leads to non-linearity

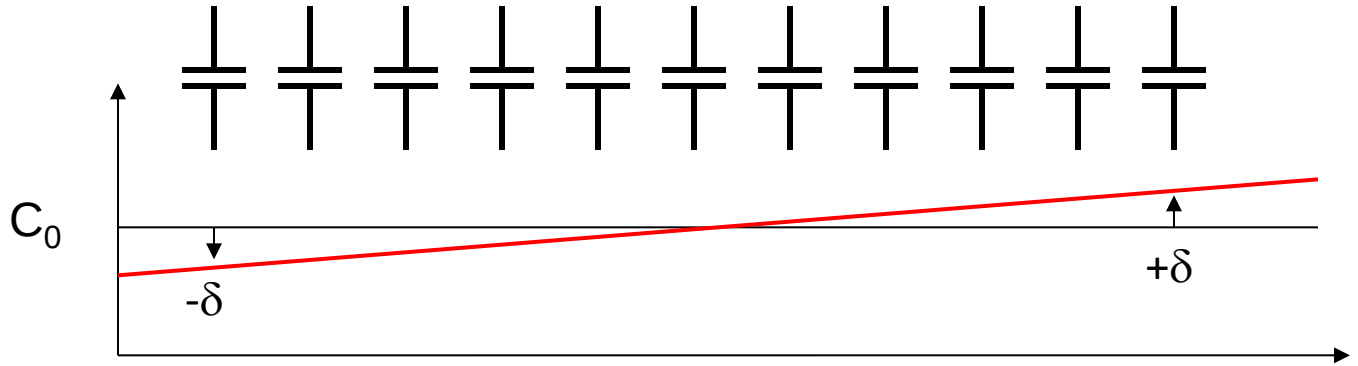
$$C : N(C_0, \sigma_0)$$



- Reduce mismatch:
  - Use larger capacitors (more area A → better matching)
  - Optimize layout (e.g. more distance d → less impact from LER)
  - Apply trimming/calibration

Systematic Capacitor Mismatch

- Layout gradients

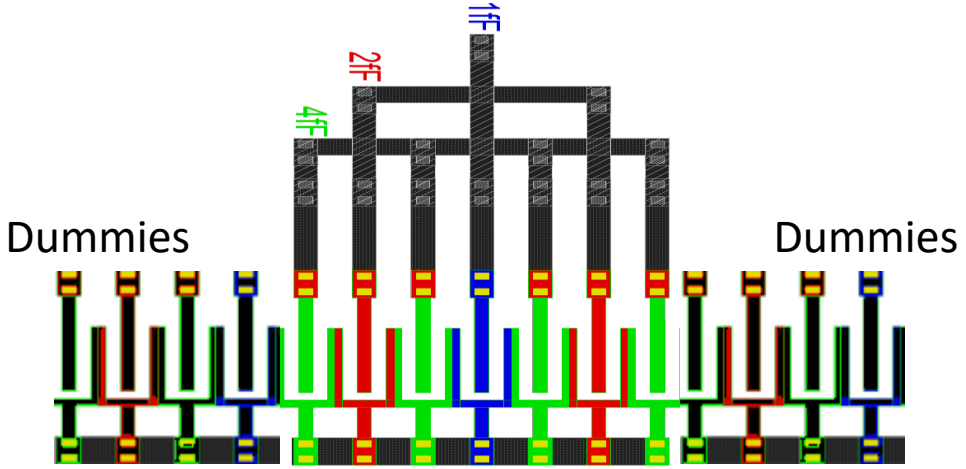


$C_0 - \delta$

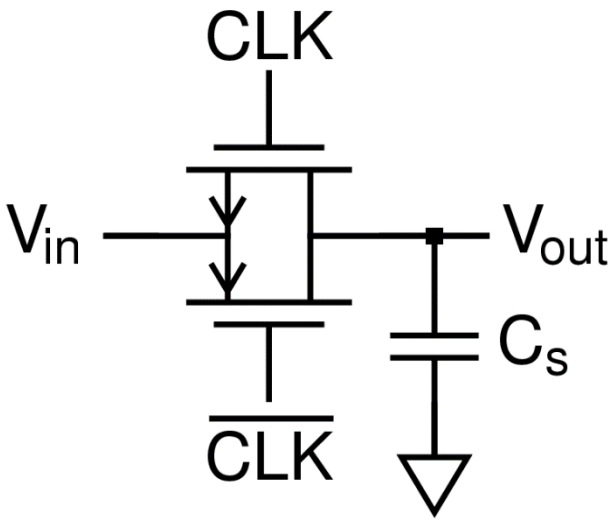
$C_0 + \delta$

$2C_0$

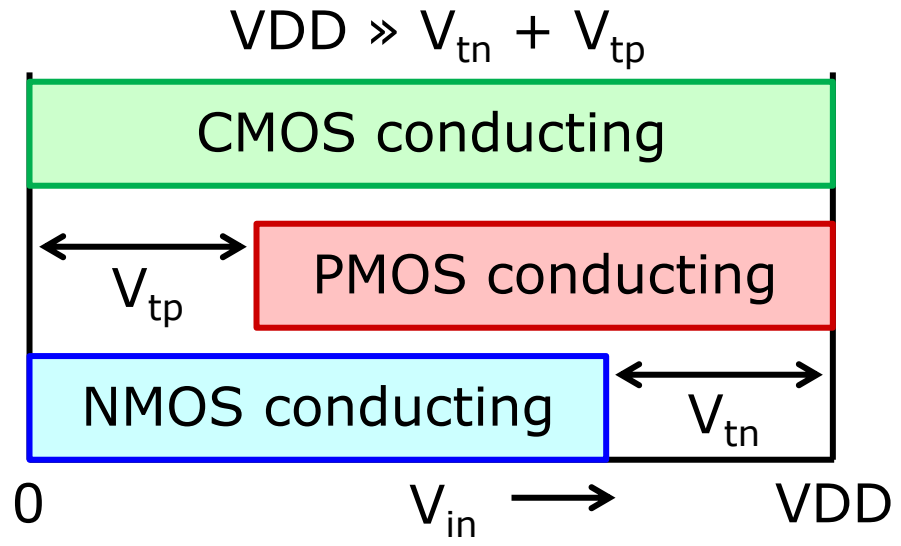
- Common-centroid approach + dummies

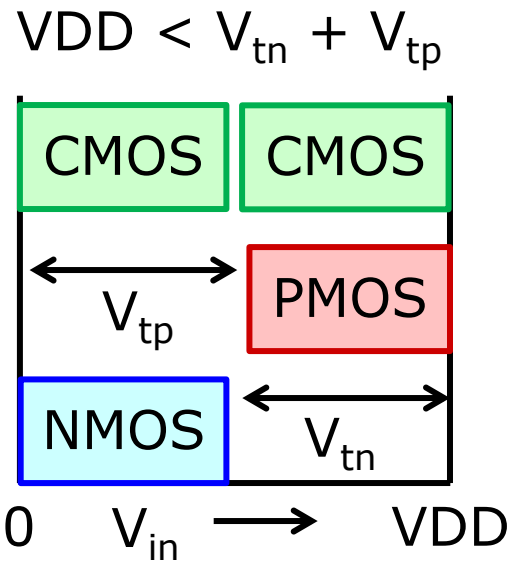


S&H Switch: NMOS, PMOS, CMOS



CLK	Mode
0	Holding
VDD	Tracking

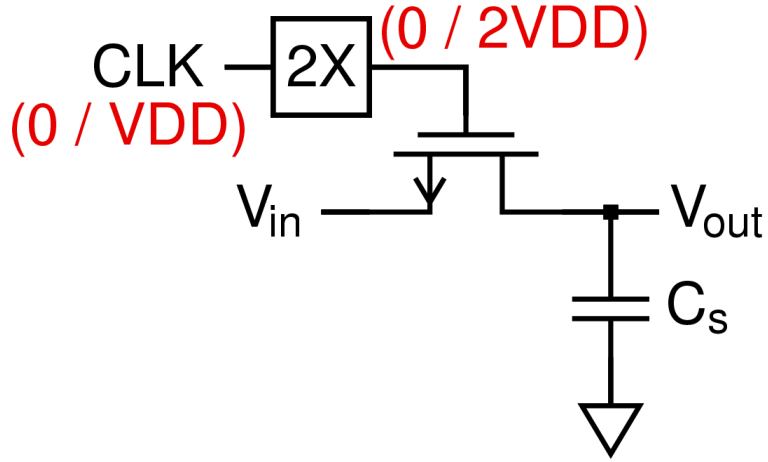




- NMOS: conducts well if $V_{in} << VDD - V_{tn}$
- PMOS: conducts well if $V_{in} >> |V_{tp}|$
- CMOS: can conduct for all V_{in} from GND to VDD
  - But only as long as VDD » V_{tn} + V_{tp}

Switch at low VDD: Clock Boosting

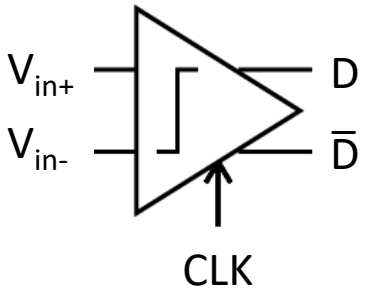
- Use NMOS transistor only as a switch
  - Increase driving voltage for NMOS switch from VDD to (e.g.) 2VDD

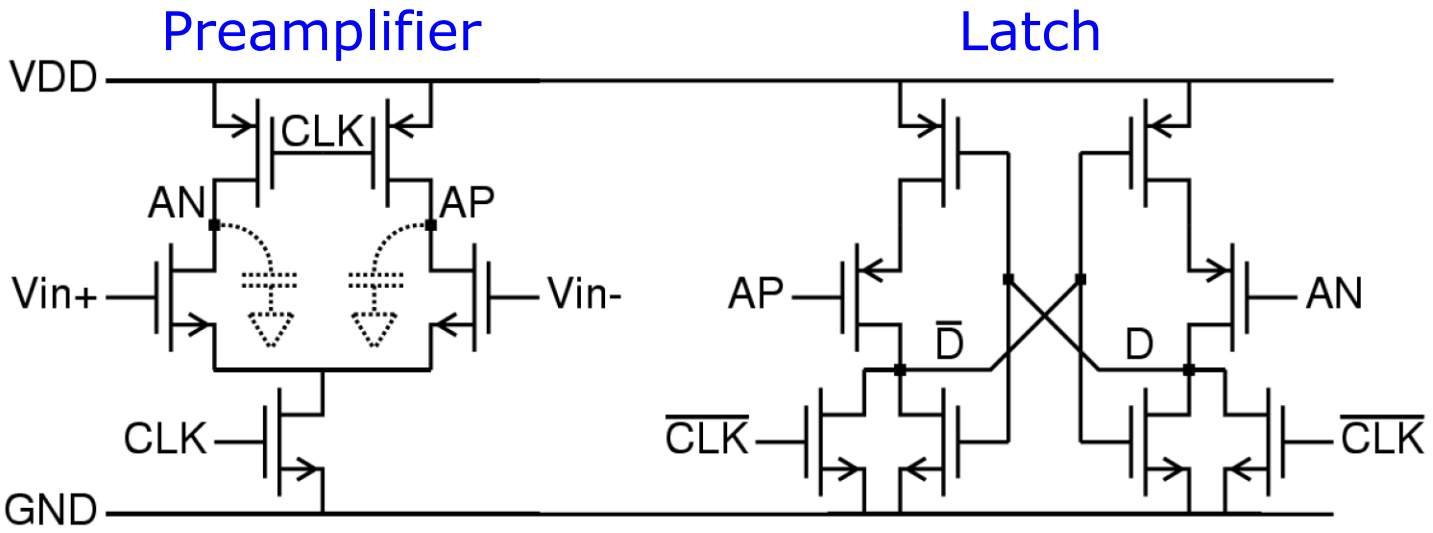


2X = Clock voltage booster

- Switch can conduct as long as $V_{in} << 2VDD - V_{tn}$
  - Since VDD is usually larger than V_{tn} → Conduction for $0V \leq V_{in} \leq VDD$

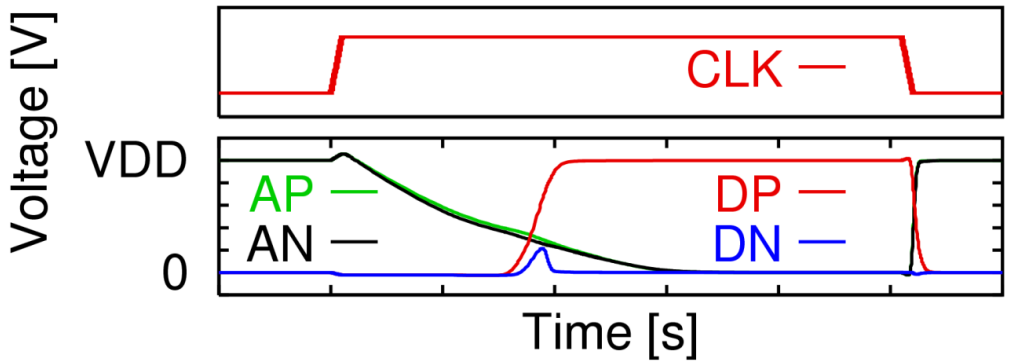
Dynamic Comparator





Van Elzakker, ISSCC 2008

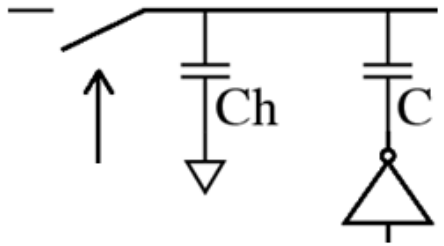
- Dynamic design: Power $\propto$ Sampling rate f_s
- Design trade-off:
  - Lower V_{IRN} → Higher power (just like other amplifiers)



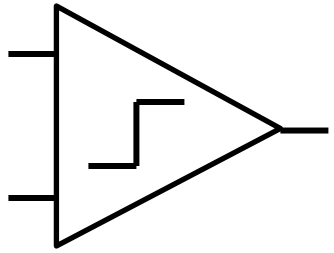
Power consumption for a SAR ADC

- Power proportional to speed (f_s) thanks to dynamic circuits
- DAC and comparator power consumption strongly related to SNR

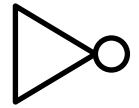
Switched cap network

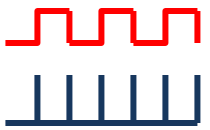


Comparator



Digital logic

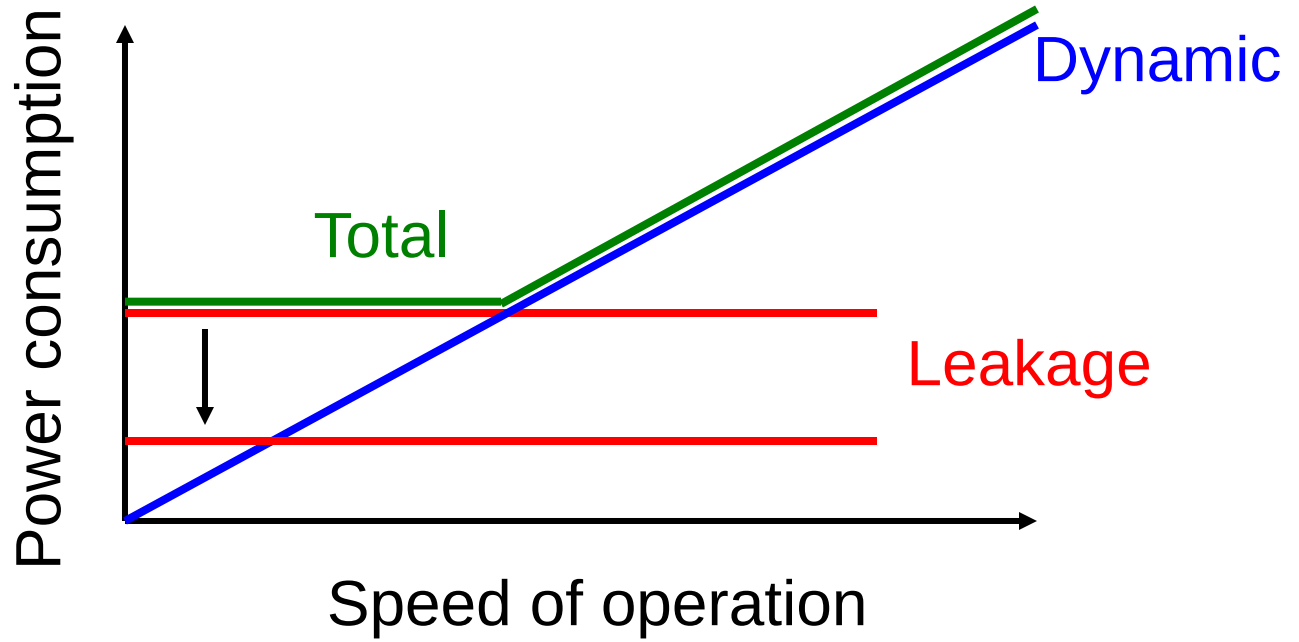


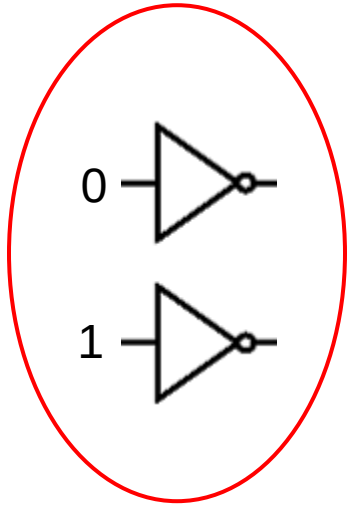


P ∝ CLK speed

Power Consumption at Low-Speed

- Power = Dynamic + Leakage (Just like digital circuits)

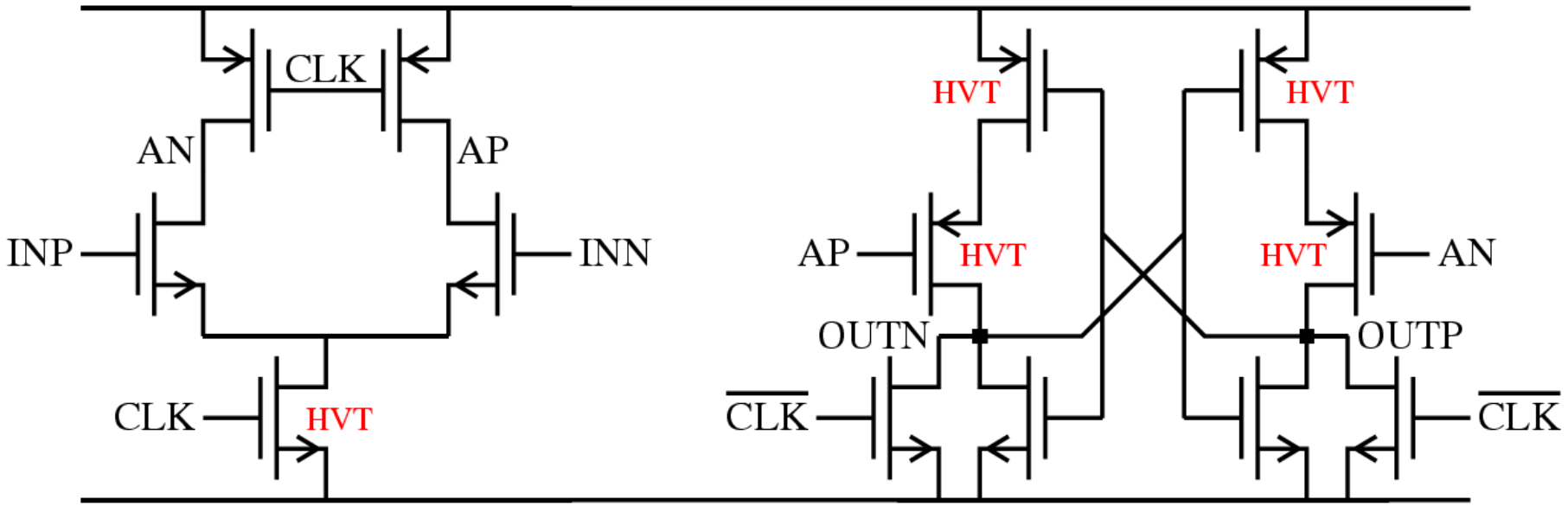




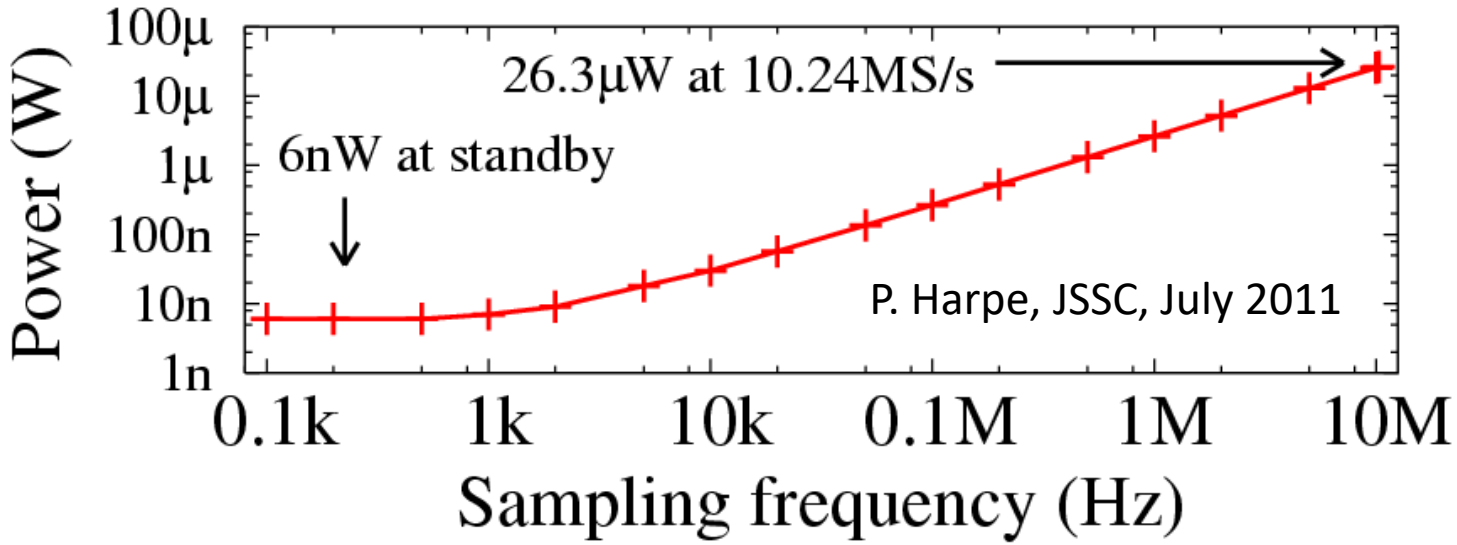
- Optimize leakage: V_{th}, W, L, transistor state, …

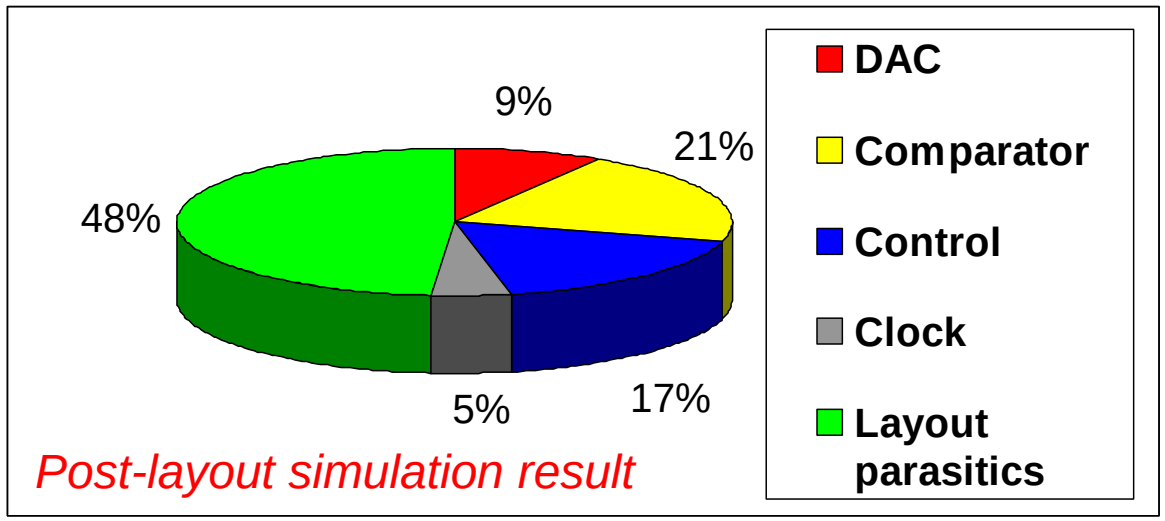
Leakage Minimization

- Smart combinations of LVT and HVT devices (low vs high V_{th})
  - HVT for those transistors that determine the leakage current
- Sizing (W, L)



Measured Power for an 8-bit ADC





90nm CMOS technology

- 48% wasted in parasitics
- For 8bit: digital power (22%) similar to analog power (30%)

Exercise 3: ADC Principles

a) Explain the principle of operation of a SAR ADC.
b) Explain the advantage and limitations of a CMOS sampling switch.
c) Explain the principle of operation of a clock-boosted sampling switch.
d) Explain the principle of operation of the dynamic comparator which was discussed earlier in this lecture.
e) To reduce the leakage consumption of said comparator, it was proposed that only some transistors need a higher threshold voltage while others don't. Explain why. Do you know why the indicated transistors (on slide 42) where changed to HVT?

Exercise 4: ADC Design

An analog signal has an amplitude of $1.4V_{rms}$ and a bandwidth of 500Hz. We want to digitize this signal with a differential SAR ADC. The quantization noise level of the ADC should stay under $0.8mV_{rms}$, and the sampling noise should stay under $0.1mV_{rms}$.

a) What are the minimum resolution N and minimum sample rate f_s that we will need?

b) What is the minimum required value for C_{sum}, and thus for C_0?

c) If we use an advanced technology node, like a 28nm process, which type of power consumption do you expect to be dominant for this ADC design and why?

d) If the V_{DD}/V_{th} ratio in our case is exactly equal to 2, can we use a CMOS sampling switch? Can we use a clock-boosted switch? Explain your answers.

e) If the V_{DD}/V_{th} ratio in our case is exactly equal to 2, can we use the dynamic comparator of which the schematic is shown earlier in this presentation? Explain your answer.

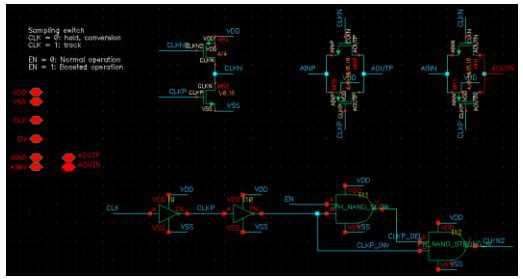
Summary – ADCs

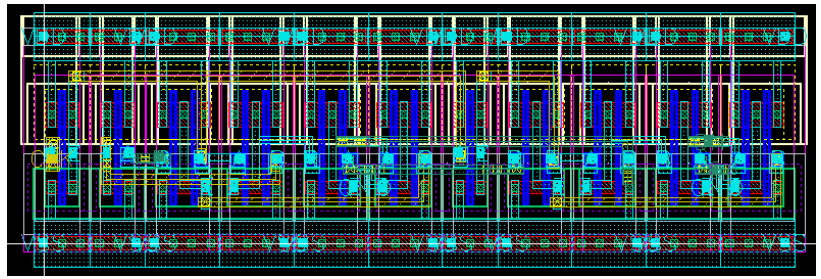
- Low power SAR ADCs
  - Capacitors
  - Switches
  - Comparator design
  - Low leakage design

Outline

- Digital design
  - Power consumption & Low-power techniques
  - Technology scaling
- Analog-to-Digital Converters (ADCs)
  - Basics
  - Low-power architectures, circuits, and techniques
- Layout techniques
  - Floorplanning, parasitics, matching
  - Impact on power consumption, accuracy, speed

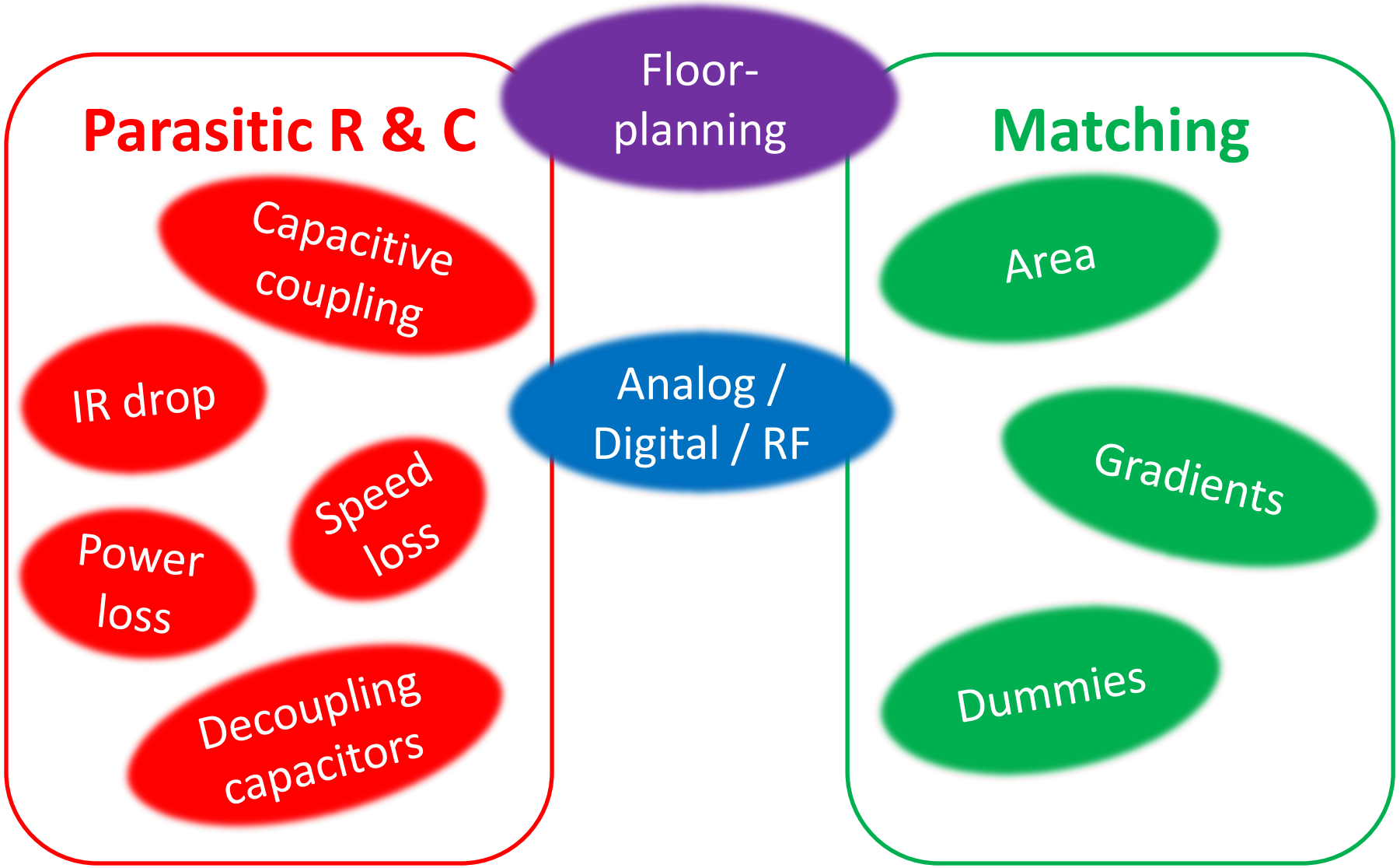
Schematic → Layout





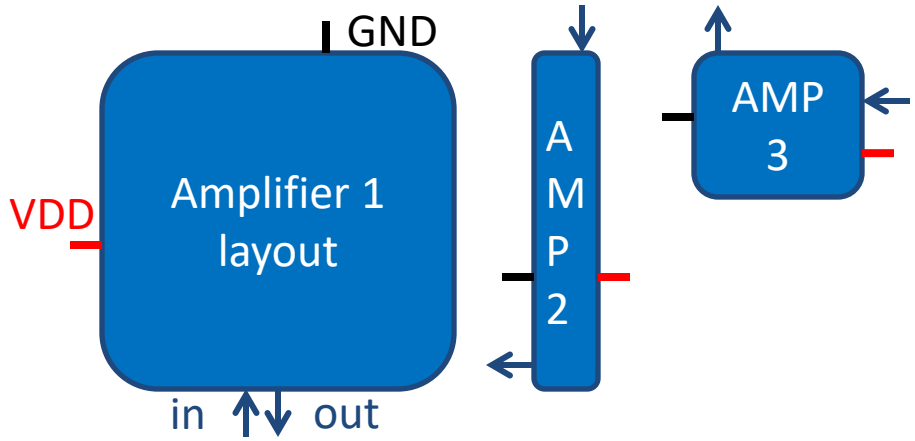
- Three main checks:
  - DRC (Design Rule Check):
    Check for manufacturability
  - LVS (Layout Versus Schematic):
    Check if layout is the same as schematic
  - RCX/PEX (Parasitic R + C Extraction):
    Extract parasitics from layout, and use for post-layout simulation

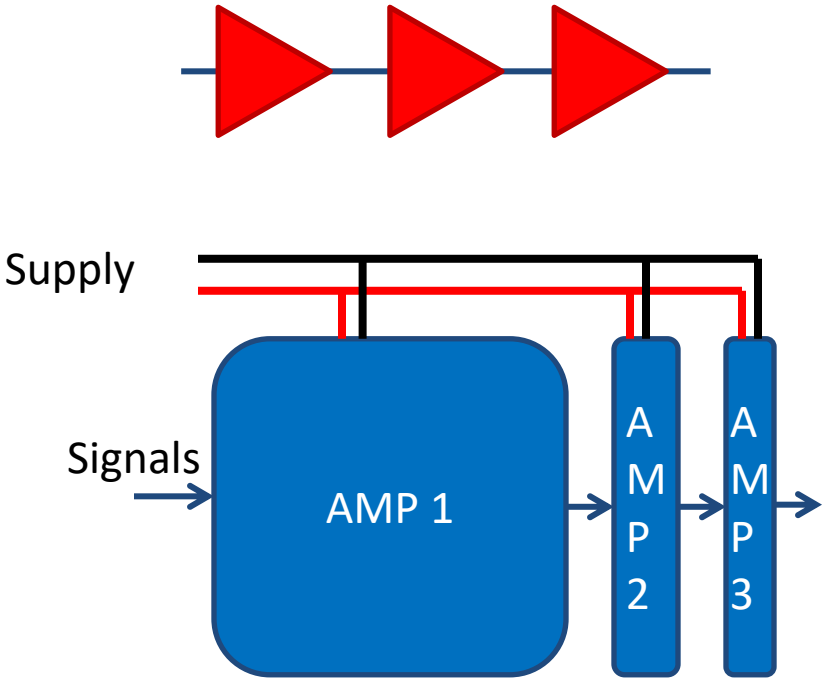
Layout Considerations



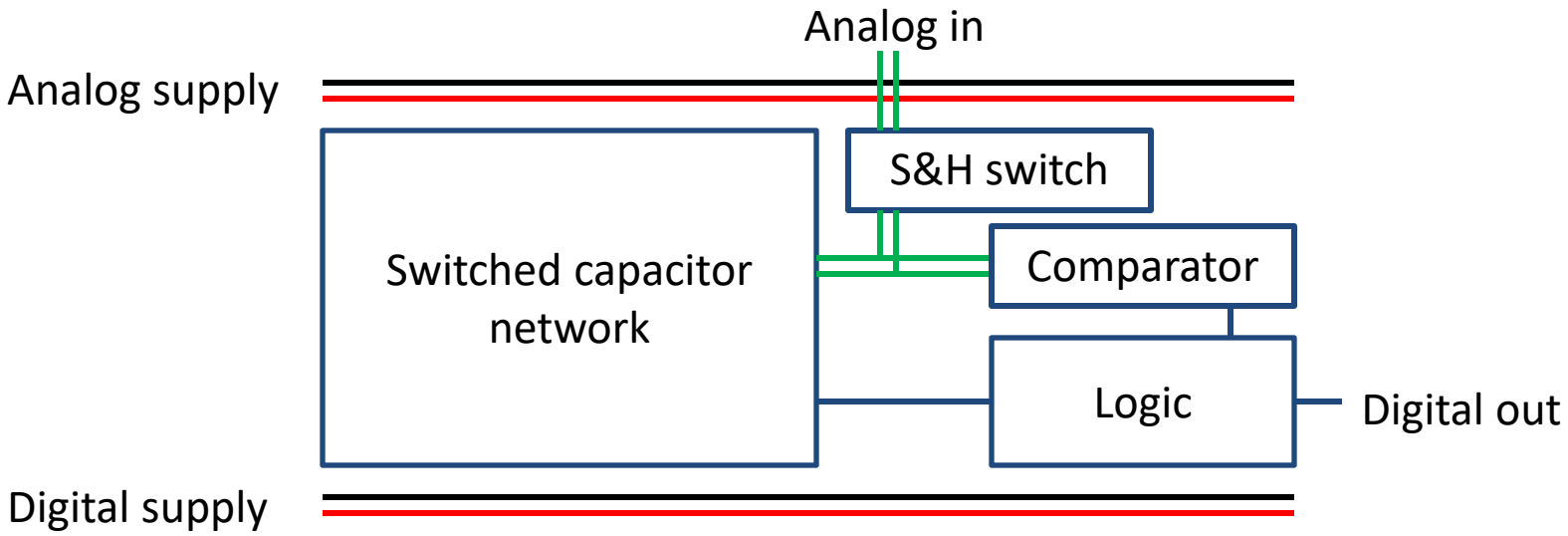
Floorplanning

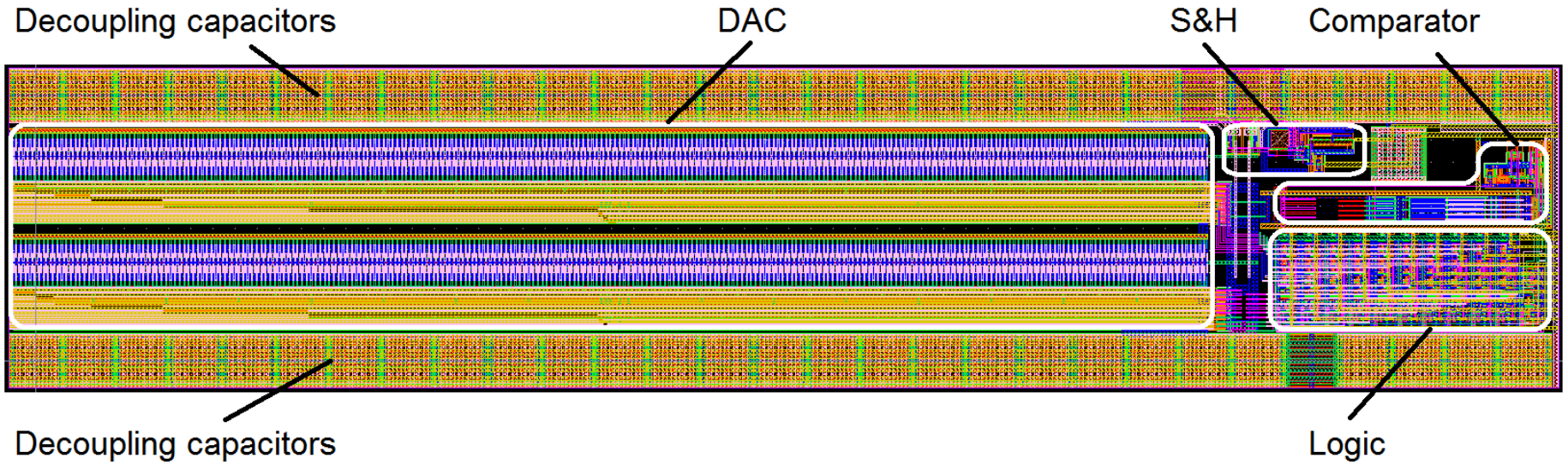
- Global plan for the location of the various blocks and the main connections
  - Critical signals (RF, analog, high-speed digital)
  - Supplies and biasing
  - Control signals





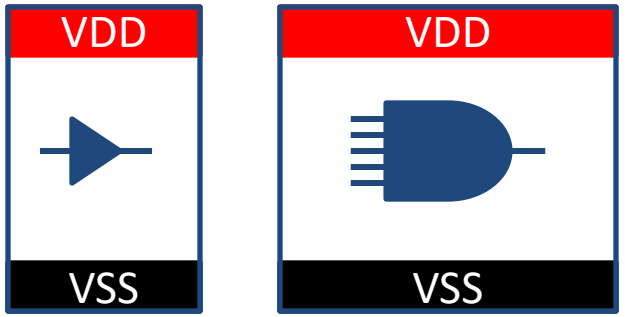
Floorplan example: ADC

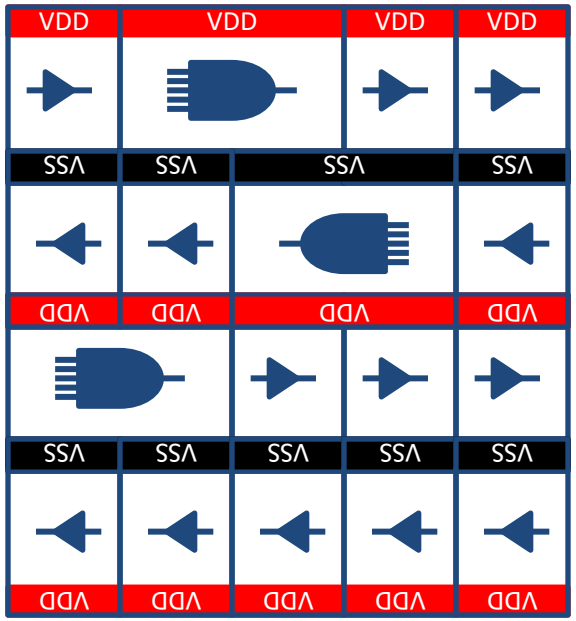




Digital Layout Style

- Dense, minimize area & interconnect length
- Matching, shielding, coupling less important
- Standard cells





- Automated place & route

Analog/RF Layout Style

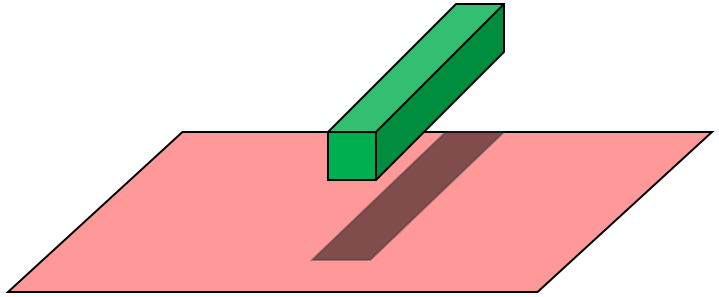
- No standard cells (large variety of cells, area, requirements)

- Low-power analog:
  - Usually still compact, but considering e.g. matching, coupling, etc.
  - Often THIN wires (minimize C) unless you have high current flows

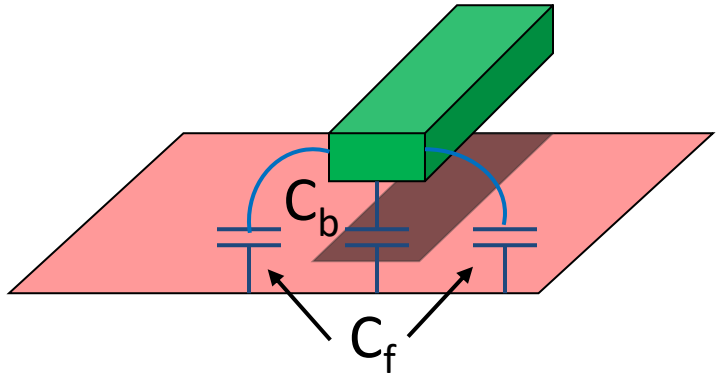
- RF (EM effects start to play a role, usually higher power levels):
  - More space, guard rings to separate devices
  - Often WIDER wires (minimize L, R)

Parasitic R's and C's

- Wire model: R & C



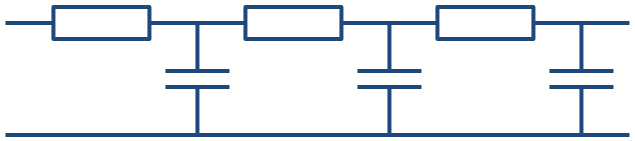
- 2x wider wire: ≈½x R, ≈2x C



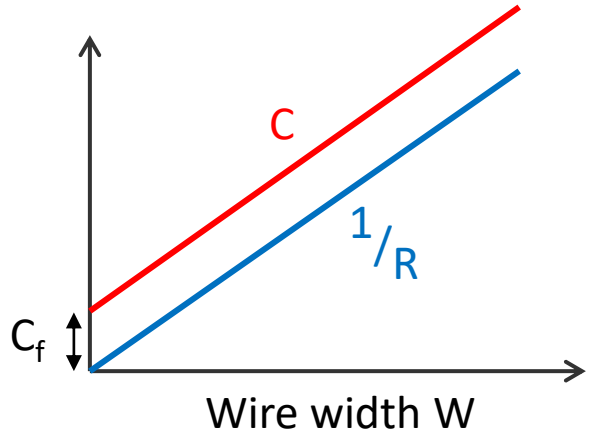
Bottom-plate capacitance (C_b) scales with W

Minimum capacitance (C_f) due to fringing

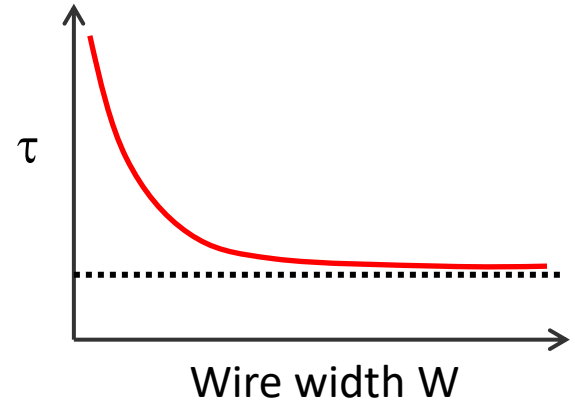
RC network model



R and C value vs width W

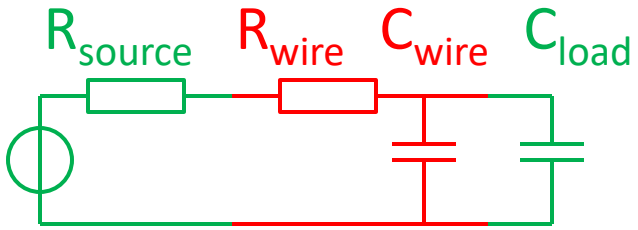


τ = RC vs width W



Digital	Min. W → Min. C_L → Min. dyn. power
Analog	Reasonably small W, unless high currents
RF	Large W → Min. τ → Max. freq.

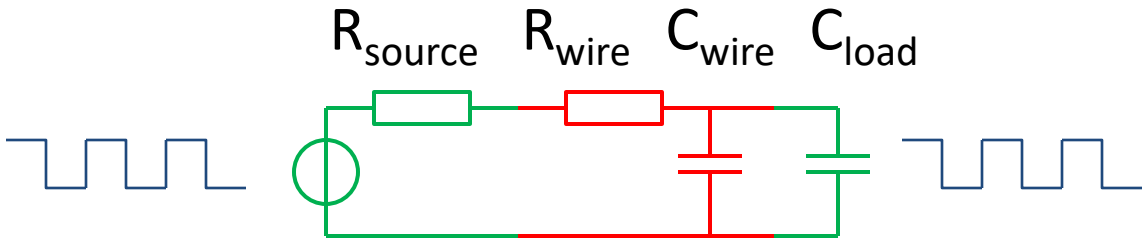
Speed Loss



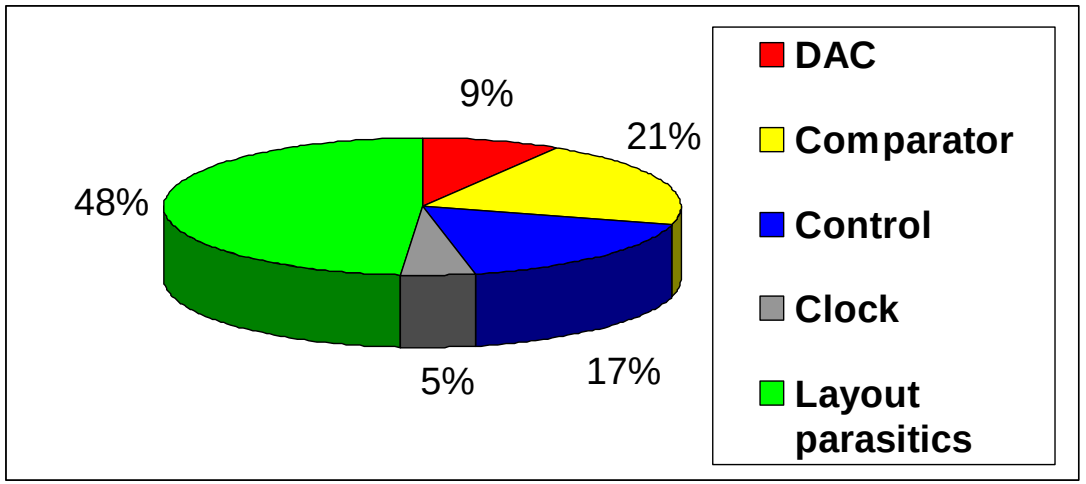
Green components model the schematic, red components model the layout parasitics

- Speed loss: RC filter, $\tau = (R_{source} + R_{wire}) \cdot (C_{load} + C_{wire})$
- Typical digital cells: R_{source} is large, C_{load} is small
  - → C_{wire} more important than R_{wire}
  - → Narrow wires, short connections
- Analog cells: depends on frequency and power level of the circuit
  - Low-power analog: often like digital, so narrow short wires
  - High frequency or high-power analog: often also cares about R_{wire}

Dynamic Power Loss: C_{wire}



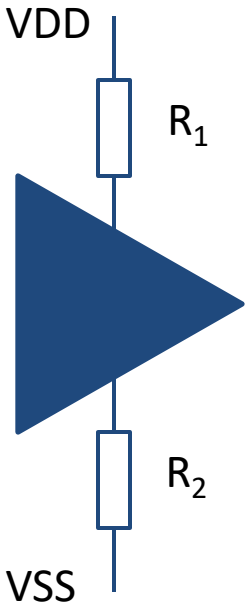
- Energy/cycle: $(C_{load} + C_{wire})VDD^2 = C_{load}VDD^2 + C_{wire}VDD^2$
- Use short en thin wires; dense layout style

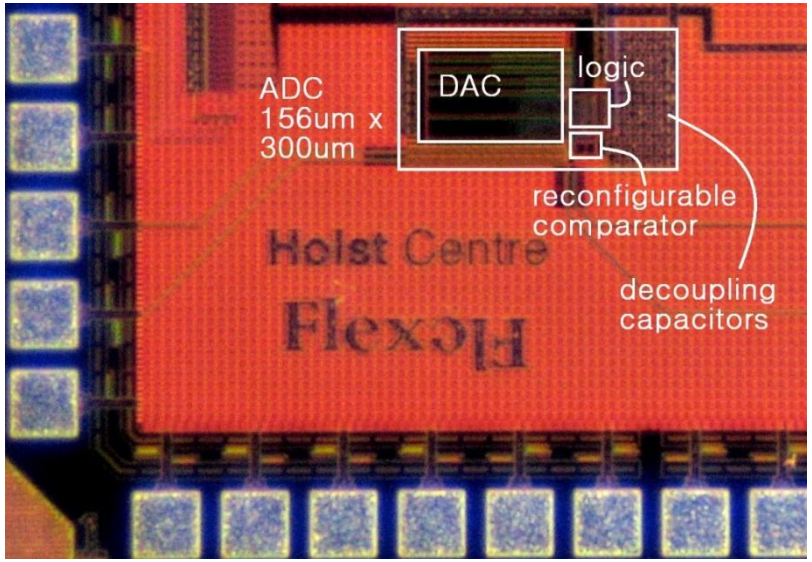


Exemplary ADC power breakdown: layout parasitics can be dominant in overall power consumption

Static Power Loss (IR Drop): R_{wire}

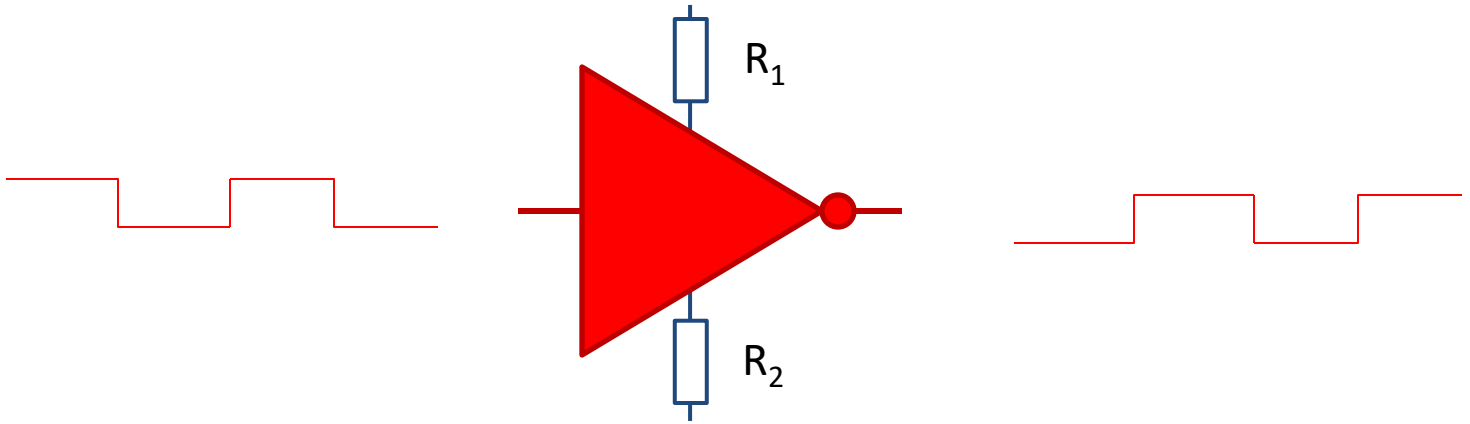
- Amplifier with DC current I_{DC} from supply



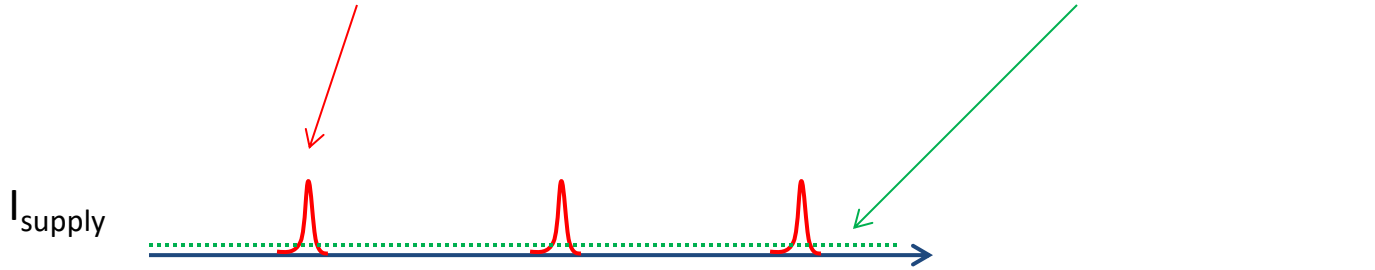


- Voltage loss due to resistors: $V_{DROP} = I_{DC}(R_1 + R_2)$
- Supply wires: wide wires to reduce R_1, R_2

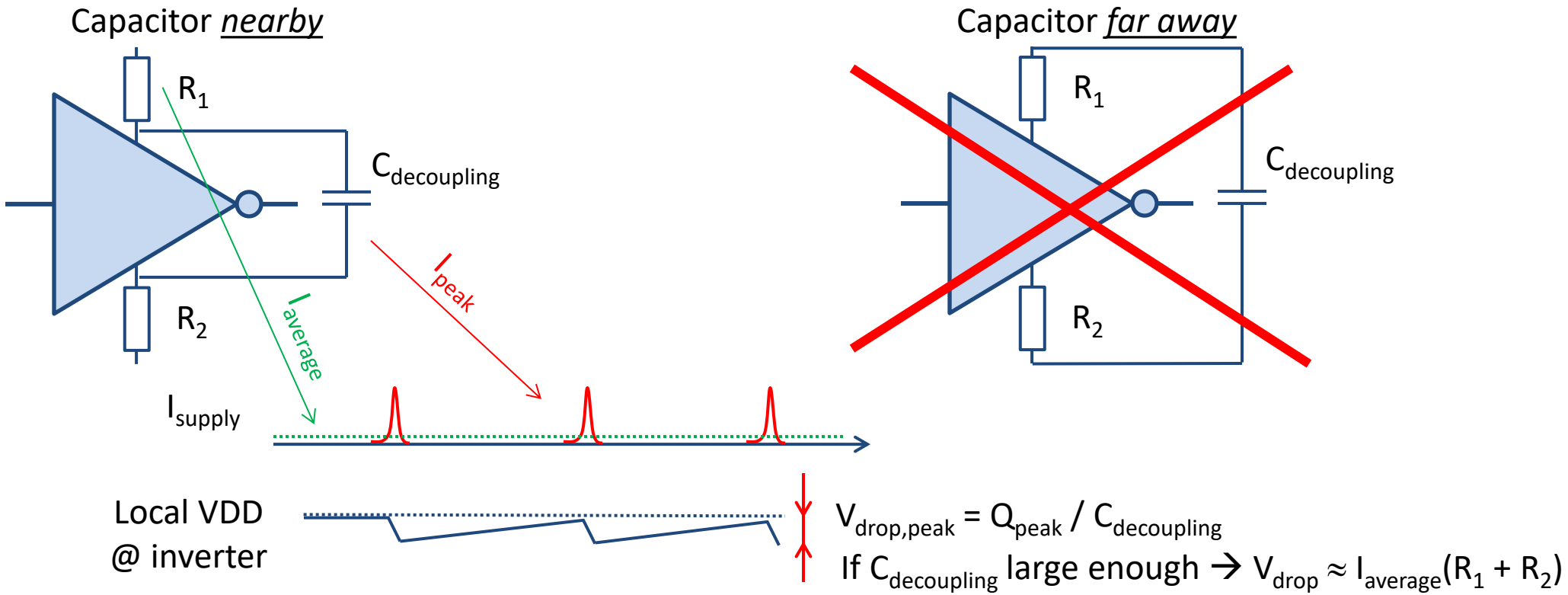
Dynamic IR Drop



- Large peak current; small average current



Supply Decoupling Capacitors



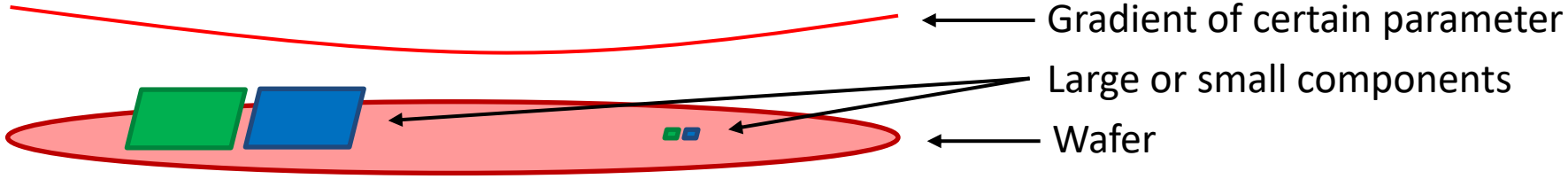
- Decoupling capacitor near the active circuit acts as a local battery for peak currents
- Only the average current now flows through the resistors, not anymore the peak →
  - Voltage drop over the resistor is now given by $I_{average}(R_1 + R_2)$ rather than $I_{peak}(R_1 + R_2)$
- C does not help to deal with peak currents if it is too far away from the active circuit!
  - So: Put C local → Include them in your floorplan!

Matching: Area

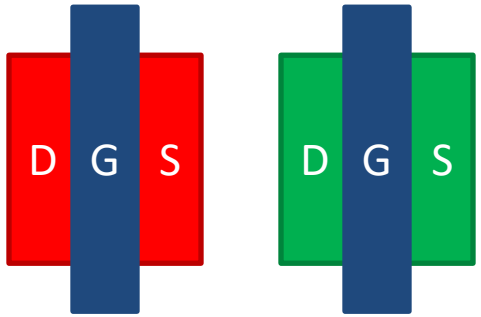
- Matching: the degree to which nominally identical components are equal to each other
  - Relevant for e.g. the two transistors in a differential pair, or an array of capacitors in an ADC
- Manufacturing imperfections result in local random mismatch, causing a random deviation of the value of each device from its nominal value
- Statistically: components with a larger area will have better matching, due to averaging: $\sigma_{\%} \propto 1 / \sqrt{\text{Area}}$
  - For example: 4x larger area yields 2x improvement in the relative matching of two devices → Precise devices are usually large

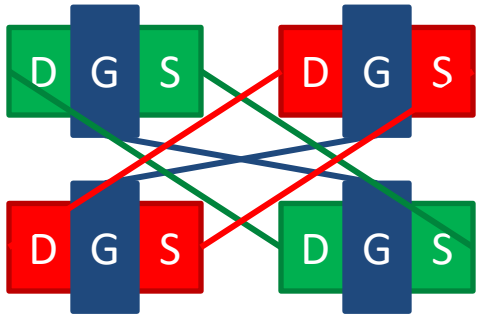
Matching: Gradients

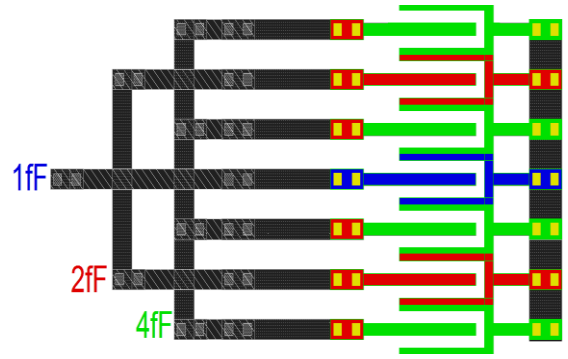
- Gradient: gradual trend over the wafer of certain parameters, such as threshold voltage, layer thickness, doping concentration, etc.
  - Trend is often reasonably linear locally (if the components are small)
  - The larger your components, the higher the impact of gradients



- Common centroid layout: solves gradient issue, but introduces wiring overhead/asymmetry of parasitics

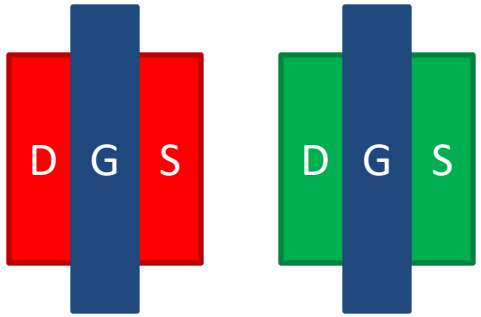




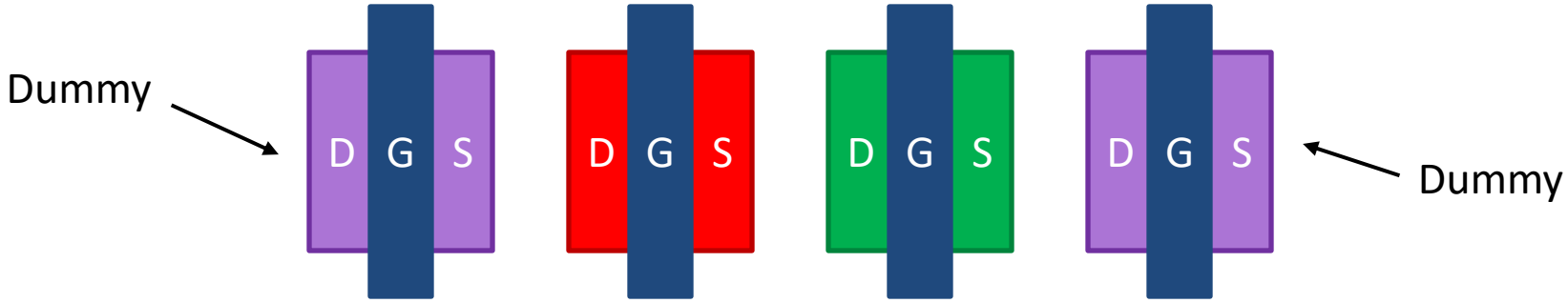


Matching: Dummies

- Mismatch due to difference in the environment:
  - Stress, capacitance, change of shape, …



- Place dummies to maintain symmetry in the environment
  - Dummies are not used, but just placed for reasons of symmetry



If You Want To Know More:

- A. Hastings - “The art of analog Layout”

Exercise 5: Parasitics

Assume the metal wiring in our IC technology has the following parameters:

- Minimum W = 0.1µm
- Sheet resistance $R_{\square}$ = 0.2Ω/sq
- Bottom plate capacitance C_b = 400µF/m^2 (per unit area)
- Fringing capacitance C_f = 160pF/m (accounting for both side walls of a wire)

a) What is the total resistance and total capacitance of a minimum-width wire with a length of 100µm?

b) If we want to make a wire of 200µm length with a time-constant τ of 4ps, how wide should it be?

c) A 1.8V voltage source provides the supply power to an amplifier that has a static power consumption of 4mW. The total length of the supply wire is 1mm. How wide should this wire be so that the supply voltage drop is less than 1% of the nominal supply voltage?

A digital circuit has only dynamic power consumption. Assume that the supply wiring has a resistance of 50Ω. The supply voltage is 1V, the peak current drawn by the digital circuit is 8mA, and the energy drawn at each clock transition is 1.6pJ.

d) If there is no local decoupling capacitance, how much peak IR drop will we have on the supply?

e) What is the required size of the decoupling capacitor to minimize the peak IR drop to 50mV?

Exercise 6: Matching

Assume we want to make a differential pair (for an amplifier) and we want to minimize the offset voltage of this pair to 0.2mV. It is given that:

- The random mismatch of the transistors produces an offset with a standard deviation of: $\sigma_{offset} = 2mV / \sqrt{(W \cdot L)}$, where W and L are the transistor dimensions in µm.
- Besides random mismatch, there is also a systematic gradient, which causes an additional offset of $V_{offset} = 0.01mV \cdot d$, where d is the centre-to-centre distance of the two transistors in µm.
- For this amplifier, we want the W and L to be equal to each other.

a) Considering only random mismatch: What is the required W and L to achieve a 3-sigma offset that remains below the target offset of 0.2mV?
b) Considering the expected gradient: is this posing a problem in this case or not?
c) Sketch a layout of how you would implement this differential pair.

Summary – Layout Techniques

- Make a floorplan!
- Parasitic resistors and capacitors
- Speed loss and power loss
- Local decoupling
- Matching: area, gradients, symmetry

Solution 1: Digital Power Consumption

Question	Dynamic power	Short-circuit power	Leakage power
a)	Doubles	Doubles	No change
b)	Increases by ≈1.44X	Increases, but cannot be quantified due to lack of information	Increases (a bit) due to higher V_{DS} of the leaky transistor
c)	Roughly doubles, as load is doubled	Roughly doubles, as the short-circuit path has about 2x lower r_{on}	Roughly doubles, as the leakage is about 2x higher
d)	Almost no change (except that C_L might change a little bit since it depends on V_{gs} and V_{th})	Reduces, since there is less conduction now	Reduces substantially

Solution 2: Digital Power Consumption

a) 1.6nW dynamic power consumption, 0.2nW short-circuit, and 0.2nW leakage

b) 0.2 + 0.01 (1.6 + 0.2) = 0.218nW

c) Leakage is by far dominant, so focus on leakage reduction techniques such as reducing VDD, increasing V_{th}, reducing W, increasing L

Solution 3: ADC Principles

a) See lecture.

b) Advantage: in principle this is a simple implementation that can achieve a rail-to-rail input swing. Limitation: it only works well if V_{DD} is well beyond 2 V_{th}.

c) See lecture.

d) See lecture.

e) Only those transistors that are in the off-state when CLK = 0, and that are in the critical current path are relevant. For the pre-amplifier, that's the single NMOS tail transistor. For the latch, that's the PMOS input pair (with the gates connected to AP, AN). The upper 2 PMOS devices in the latch are also implemented as HVT since this is more convenient in the layout (more compact), but that is not so relevant for the leakage minimization.

Solution 4: ADC Design

a) 11bit and 1kHz.

b) 828fF and 0.8fF.

c) Leakage is likely dominant, as the frequency of operation is low, and leakage is expected to be high in such an advanced technology node.

d) No, a CMOS switch won't work well, because both NMOS and PMOS transistors are off (or barely conducting) if V_{in} is in the middle of the range. A clock boosted NMOS switch will work well, because the gate is boosted to $2V_{DD}$. Since V_{th} is ½ VDD and the source voltage (V_{in}) is usually between 0V and V_{DD}, V_{gs} is always well beyond V_{th} in the on state.

e) Yes. Even though we have 3 transistors stacked in this design, this is OK, because we can design these devices in sub-threshold.

Solution 5: Parasitics

a) R = 200Ω and C = 20fF

b) W = 1.6µm

c) I_{supply} = 2.2mA, V_{drop} = 18mV, R = 8.1Ω → W = 25µm

d) V_{drop} = 8mA · 50Ω = 0.4V (theoretically, in practice the circuit likely won't work properly with such a large drop, causing the consumption to change as well)

e) 1.6pJ ($E = CV^2 = QV$) at 1V supply implies a charge of 1.6pC is taken out of the decoupling capacitor at every clock edge. The voltage drop this generates can be calculated as:
$\Delta V_{dec} = Q / C_{dec} = 1.6pC / C_{dec} = 50mV \rightarrow C_{dec} = 32pF$

Solution 6: Matching

a) W = L = 30µm

b) With the required W and L, d is at least 30µm, so this will cause a V_{offset} of 0.3mV, which is a problem.

c) For instance something as shown below (there are other options as well). Each transistor is split in 2 parallel devices, each with W = 15µm and L = 30µm. Common-centroid is necessary to deal with the gradients. It is further recommended to add dummies (in purple), as the target matching is rather accurate.