




# Development and Characterization of Thermal Compression Flip-Chip Bonding Process

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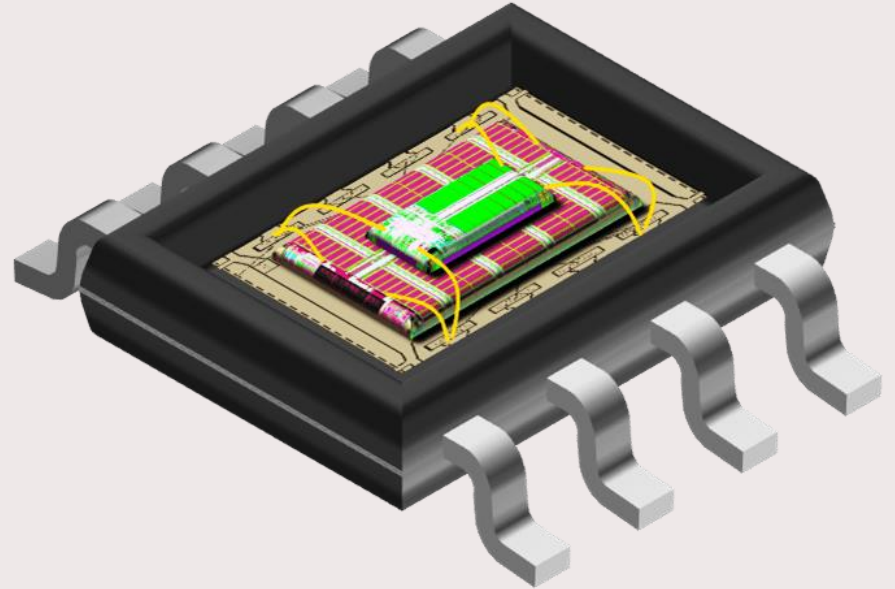


W.M. Beelaerts van Emmichoven

Electrical Engineering, IC research group

# Applications of the project

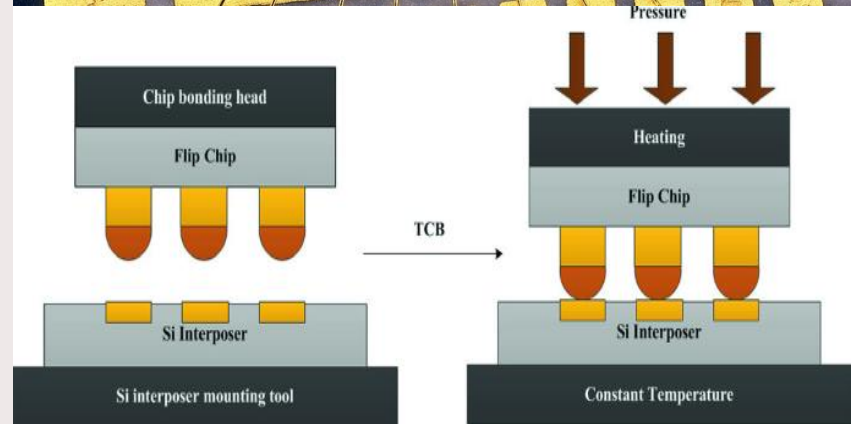
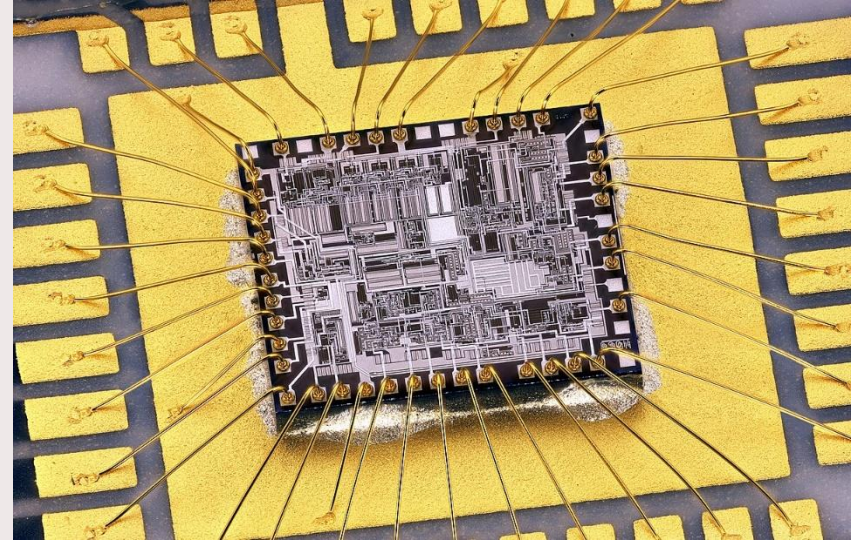
- High-tech applications
  - Speed increasingly important
  - Hardware limitations
- More and faster connections required
- Packaging





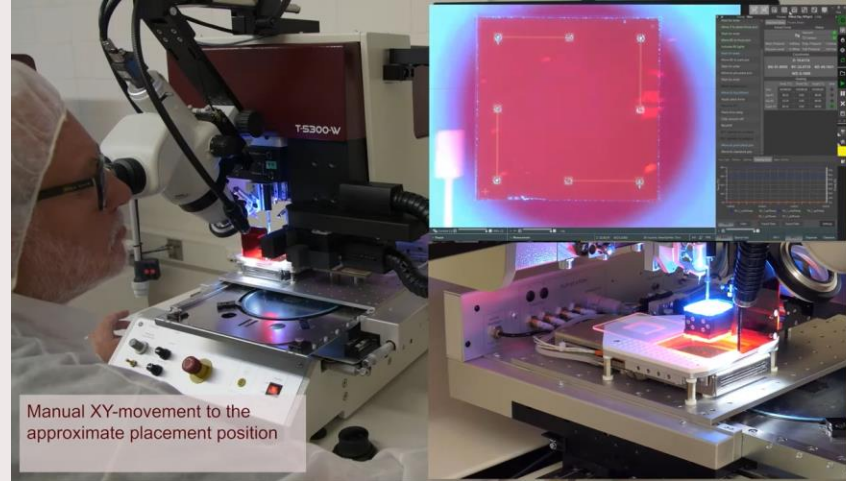
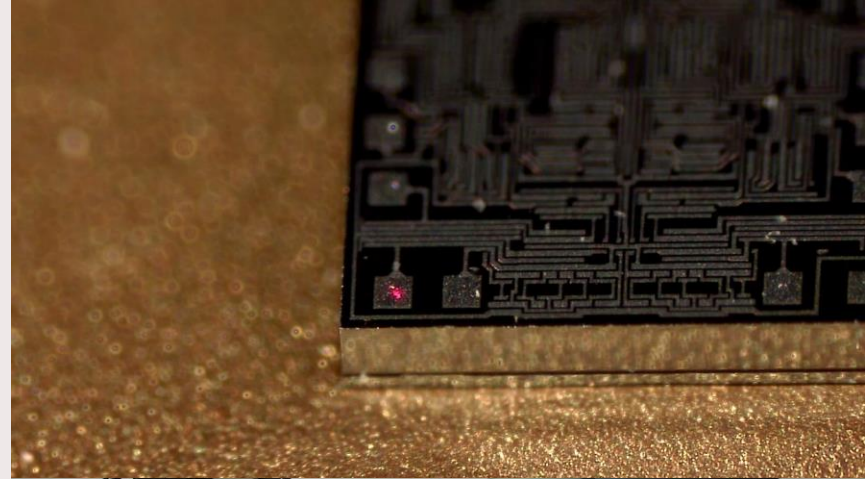
# Purpose of the project

- Flip-Chip Technology vs Wire Bonding
- More interconnections
- Shorter interconnections
- Lower propagation time
- Process existence benefits TU/e projects requiring FCT



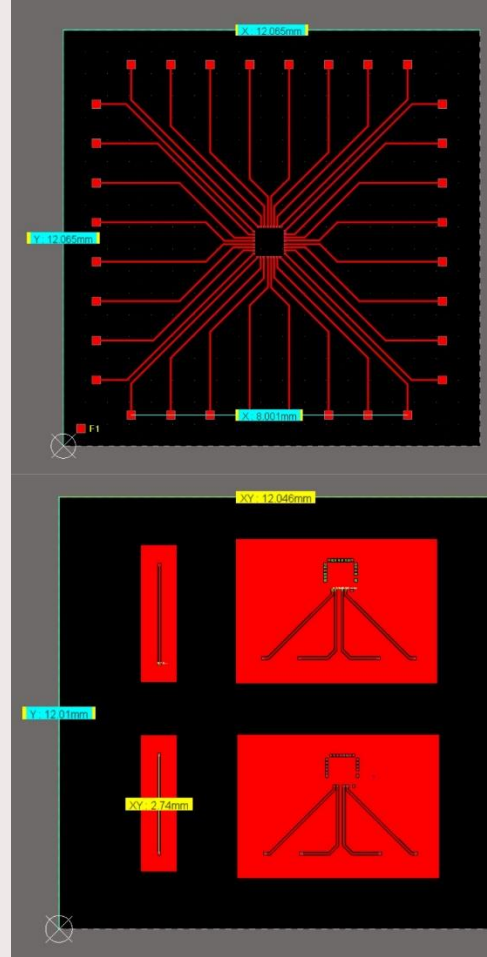
# Project setup

- Proposed process: 4 stages
  - Interposer design & production
  - Bump placement
  - Die placement
  - Testing
- Developed for IC group
  - Cleanroom
  - Electronics lab



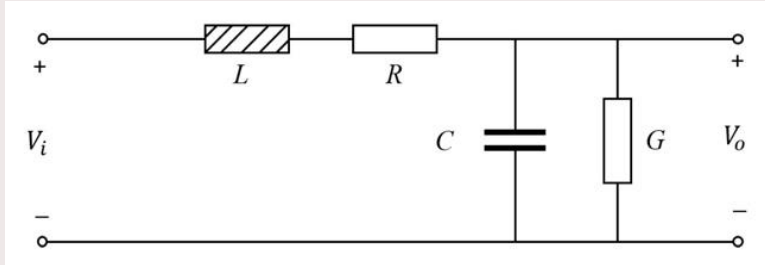
# Process developments: Interposer Design

- Glass interposer
- 2 metallization methods: sputtering and evaporation
- 2 purposes: trade-off and characteristics

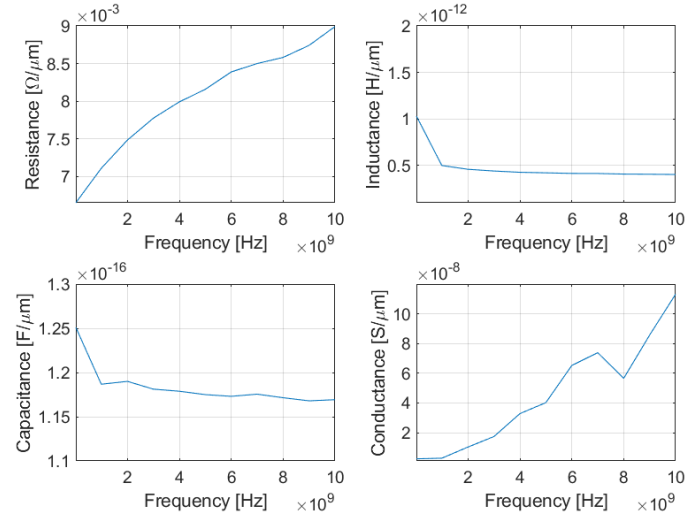


# Process developments: Interposer Characterization

- 50 nm Titanium adhesion layer
- Evaporation: lower resistance, consistent bump placement

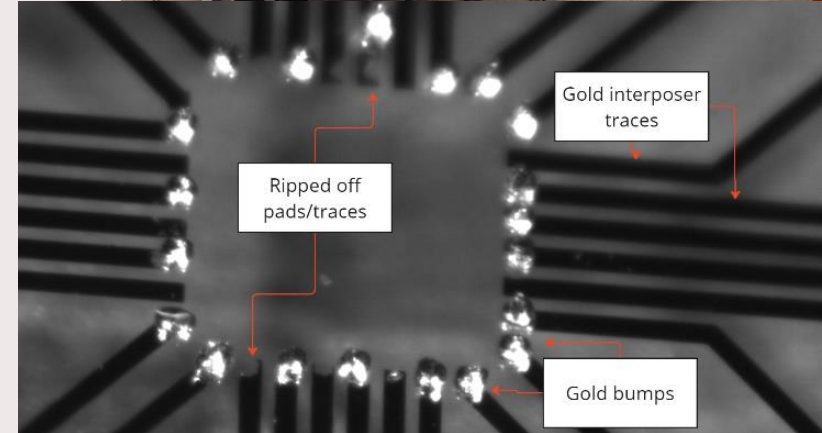
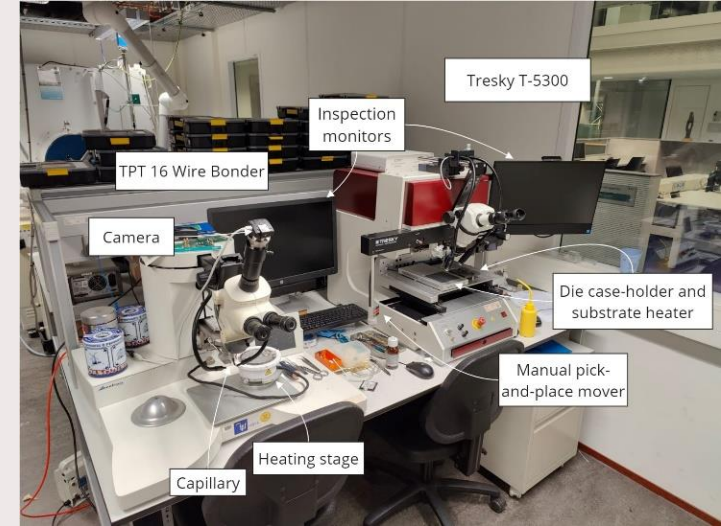


RLCG values from 10 MHz to 10 GHz



# Process developments: Bumps

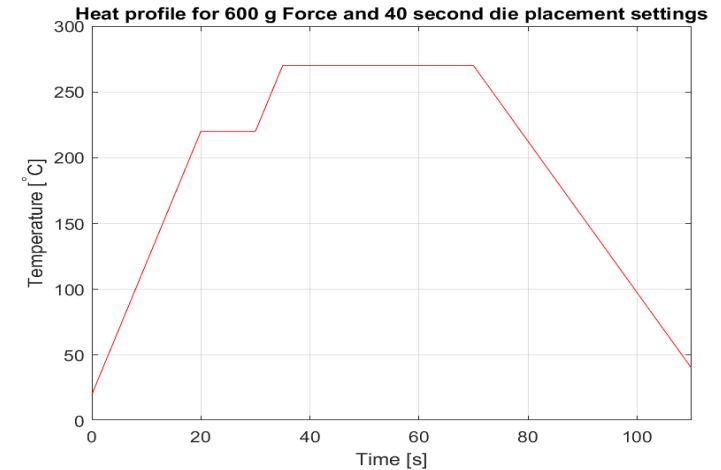
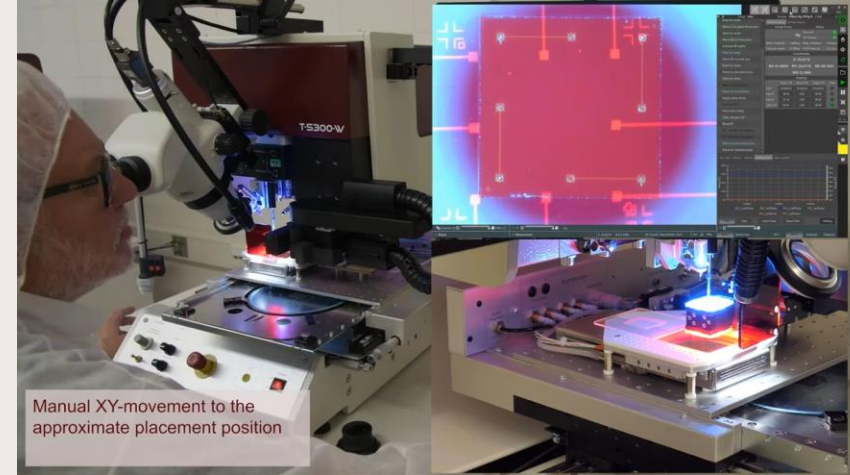
- 25 vs 17  $\mu\text{m}$  gold wire
  - Good bump quality on small gold surface areas, but bad on large areas
  - Reliable process
  - Requires pad pitch > 90  $\mu\text{m}$
  - Good bump quality on small gold surface areas, but bad on large areas
  - Unreliable process - clogging
  - 90  $\mu\text{m}$  pad pitch works
- Placement method: cursor as reference





# Process developments: Dies

- Heat profile, force and duration settings required
- Semi-successful attempt
- Weight distribution
- Metal connections confirmed





# Final remarks

- Cooperation with Accelonix recommended
- Evaporation preferred production method
- 25  $\mu\text{m}$  gold wire process most reliable, but requires pad pitch size  $> 90 \mu\text{m}$
- Future research steps:
  1. Improving and optimizing settings for bump and die placement
  2. Investigate AC behaviour of tracks at frequencies  $\gg 10 \text{ GHz}$
  3. Exploring electrical characteristics of the bumps

