Glass interposer for heterogeneous integration of flip-chipped photonic and electronic integrated circuits

Article *in* Applied Physics Letters · July 2024

DOI: 10.1063/5.0221309

CITATIONS
0

READS
191

6 authors, including:

Jean-Marc Boucaud
University of Lille
4 PUBLICATIONS **2** CITATIONS
SEE PROFILE

Cédric Durand
STMicroelectronics
79 PUBLICATIONS **667** CITATIONS
SEE PROFILE

Davide Bucci
Grenoble Institute of Technology
64 PUBLICATIONS **374** CITATIONS
SEE PROFILE

Jean-Emmanuel Broquin
Grenoble Institute of Technology
182 PUBLICATIONS **1,547** CITATIONS
SEE PROFILE

Glass interposer for heterogeneous integration of flip-chipped photonic and electronic integrated circuits

Jean-Marc Boucaud,[1,2,3] Cédric Durand,[1] Frédéric Gianesello,[1] Davide Bucci,[3] Jean-Emmanuel Broquin,[3] and Emmanuel Dubois[2,a)]

AFFILIATIONS

[1]STMicroelectronics, 850 rue Jean Monnet, F-38920 Crolles, France
[2]University Lille, CNRS, Centrale Lille, Junia, University Poluytechnique Haut-de-France, UMR 8520 IEMN – Institut d'Electronique de Microélectronique et de Nanotechnologie, F-59000 Lille, France
[3]CROMA, Université de Grenoble Alpes, UMR 5130 CNRS, Minatec-Grenoble-INP, CS 50257, 38016 Grenoble, France

[a)]Author to whom correspondence should be addressed: emmanuel.dubois@iemn.fr

ABSTRACT

In this Letter, we propose an approach to improve the packaging of electro-optical transceivers based on silicon photonics through the development of a glass interposer. This assembly platform integrates polymer optical waveguides and an integrated turning mirror that vertically redirect the optical signal in the plane of the interposer to the grating coupler of a flip-chipped photonic integrated circuit (PIC). A distinctive feature of the proposed packaging scheme is to use a conventional flip-chip technique without active alignment. Functionalities are completed with a copper redistribution layer that supports the routing of DC to millimeter wave (mmW) signals to drive the PIC. The measured loss in polymer waveguides is 1.92 dB/cm at 1310 nm, and the coupling losses associated with light propagation through the turning mirror and the PIC grating coupler are 18.7 dB. Coplanar mmW waveguides are structured on the glass interposer by cold laser ablation, yielding an attenuation of 0.3 dB/mm at 58 GHz. The most important outcome of this work is that the coupling of the optical signal from the interposer to the PIC is experimentally established. We also assessed the mmW performance of coplanar waveguides through the validation of the interposer to PIC and PIC to the interposer transition.

https://doi.org/10.1063/5.0221309

In the search for higher data rate and lower cost optical fiber communications for data centers, silicon photonics (SiPh), an electro-optical technology derived from silicon-on-insulator (SOI) CMOS technologies, is now a widely adopted solution to reduce power consumption and enhance data rates of optical links while pursuing economic viability.[1,2] To achieve data rates as high as 1.6 Tb/s,[3] electro-optical transceivers will likely rely on coarse wavelength division multiplexing (CWDM) and on 4-level pulse amplitude modulation (PAM4) to reduce the cost with respect to parallel fiber channels. However, SiPh still faces complex assembly and packaging constraints related to light coupling between the optical fiber and the on-chip waveguide that both feature largely different mode field diameters resulting in prohibitive mismatch losses.[4] To cope with this issue, two main coupling configurations exist, namely, in-plane also referred to as butt coupling (BC) and out-of-plane using grating couplers (GCs) with vertical alignment. Several solutions exist to implement BC using inverse taper waveguide to achieve adiabatic coupling. However, these solutions require hybridization with silicon nitride[5] or polymer waveguides as well as a partial removal of the back-end of line (BEOL),[6] leading to additional cost and complexity of silicon integrated circuits (ICs) chips. Beyond the complexification of the SiPh fabrication process induced by BC, these solutions need the implementation of complex functions for polarization splitting,[7] while GC intrinsically provides this functionality.[8] On the other hand, out-of-plane vertical GCs have demonstrated low loss below 1 dB (Ref. 9) and offer the advantage to be compatible with industrial on-wafer test measurements.[10] However, the use of GCs also introduces two drawbacks: (i) the former is a high sensitivity to fiber positioning, which requires

active alignment, a major contributor to assembly cost, and (ii) the latter is a narrow spectral bandwidth around 20 nm at −1 dB that proves to be incompatible with CWDM.[11] To overcome the aforementioned limitations, this Letter introduces a heterogeneous integration scheme that embeds both the photonic (PIC) and electronic (EIC) circuit dies onto a glass interposer. This interposer supports optical and millimeter wave (mmW) waveguides to propagate both the input optical signal and the RF modulation command to the PIC and also features a turning mirror to redirect the in-plane optical signal to the GC of the flip-chipped PIC. Figure 1 gives a schematic description of the proposed assembly of the PIC and EIC on the interposer. The distinctive advantages of this approach are the following: (i) passive butt alignment of the fiber to the glass interposer, (ii) integration of passive wavelength multiplexer/demultiplexer (MUX/DEMUX) on the interposer, (iii) conservative preservation of GCs with bandwidths centered on each wavelength of the CWDM channels, (iv) passive PIC flip-chip to couple light through the turning mirror, and the GC (v) leveraging on standard silicon photonics approach by keeping industrial on-wafer probing capability without adding heavy process modifications like back-end cavity for enabling butt coupling. From a scalability standpoint, it is worth noting that the ability to integrate the passive MUX/DEMUX functionality on the interposer makes it possible to orchestrate the routing of channels to wavelength-selective GCs, which not only enables multiplexing to evolve from its coarse flavor (CDWM) to its dense counterpart (DWDM) but also does it without any power extra cost. In the following, we develop the approach for fabricating an interposer incorporating optical guides, an electrical redistribution layer, and a redirection mirror. We establish the proof-of-principle of this packaging approach by validating the coupling of the optical signal from the interposer to the PIC with the photodiode integrated into the PIC, and we demonstrate the integration of a low-loss coplanar line on the same interposer and assess its mmW performance through the measurement of an interposer to PIC and PIC to the interposer transition.

Figure 2 gives an overview of the fabrication of a hybrid electrical-optical interposer, which combines polymer-based optical waveguides with a copper electrical redistribution layer (RDL) that supplies the PIC chip with the mmW control signal and DC power source. The starting substrate is a 500 μm thick Schott AF32 wafer

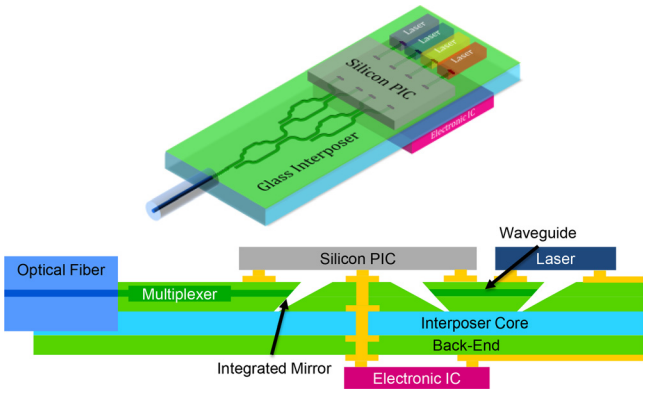

FIG. 1. Schematic description of the proposed assembly scheme of the PIC and EIC on the interposer.

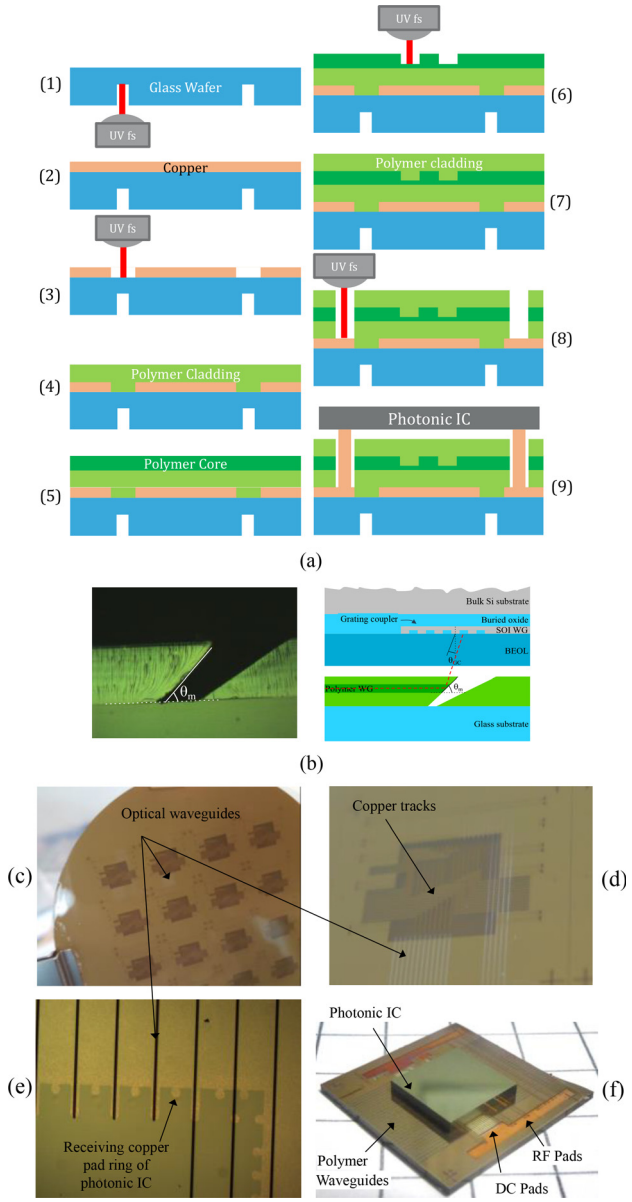

FIG. 2. (a) Complete fabrication process of the optical and electrical glass interposer (1) backside laser scribing for interposer singulation, (2) Ti/Cu sputtering of electrical RDL, (3) RDL track structuration, (4) spin-coating of bottom EpoClad layer, (5) spin-coating of EpoCore layer, (6) rib optical waveguide structuring by laser ablation, (7) spin-coating of top EpoClad layer, (8) contact holes and mirrors ablation, and (9) flip-chip bonding. (b) SEM cross-sectional view of the slanted redirection mirror based on total internal reflection and schematic representation showing the redirection of the optical signal to the PIC GC. (c) Global view of glass wafer with 16 processed interposers. (d) Single processed interposers highlighting optical guides and electrical RDL. (e) Zoom on the interposer pad ring. (f) Final functional interposer with flip-chipped PIC.

selected for its dimensional stability, transparency, and coefficient of thermal expansion close that of silicon.[12] Figure 2(a) gives the schematic sequence of fabrication that involves nine steps summarized thereafter:

(1) laser scribing of trenches on the backside of the glass wafer to facilitate chip singulation by cleaving,
(2) sputter deposition of 3.3 μm copper preceded by a 40 nm layer of titanium to promote copper adhesion
(3) structuration of the copper layer using femtosecond laser ablation to route DC tracks and mmW coplanar waveguides
(4) and (5) spin-coating of a 10 μm thick EpoClad and 8 μm thick EpoCore[13] resist layers that serves as bottom cladding and core layers, respectively,
(6) partial removal of EpoCore layer by femtosecond laser ablation to structure rib optical guides
(7) spin-coating of the top 10 μm thick EpoClad resist layer
(8) femtosecond laser selective ablation of the resist stack over the copper layer in specific areas to open contact holes to the electrical RDL and ablation of slanted trenches to shape integrated mirrors as shown in Fig. 2(b)
(9) flip-chip assembly of a silicon photonic IC from STMicroelectronics onto the functional interposer as illustrated in Figs. 2(c)–2(f).

While this fabrication process relies on glass wafers, replacing step (2) by electroless and electrolytic copper plating and steps (4), (5), and (7) by dry film lamination, panel manufacturing may become available to reduce cost.

In a similar way to the heterogeneous integration approach proposed earlier, the literature reports a few contributions describing packaging strategies based on the implementation of a glass interposer and a redirection mirror. However, the content of these papers is limited either to a simulation study,[4] to the experimental validation of the single technological building block associated the redirection mirror[14,15] or to the development of a technological co-integration scheme, associating a polymer-based optical waveguide and ultrafine copper traces for driving the modulator of a PIC with a high-frequency electrical signal.[16] In other words, no experimental demonstration exists to date, showing the coupling of the optical signal from the interposer to the GC of the PIC chip after redirection by the turning mirror. Nor is there any demonstration of continuity of the mmW control signal between the interposer and the PIC in a scheme that co-integrates optical and electrical guides on the same glass substrate. These two demonstrations are developed hereinafter.

Regarding light coupling between the interposer and the PIC, Fig. 2 details the fabricated interposer that embeds all the needed optical elements to guide the light from an external fiber to the PIC. This optical path is composed of two major elements: the polymer waveguide and the mirror. Therefore, the optical performances of both fabricated optical polymer waveguides and mirrors have now to be assessed. The waveguides insertion losses were characterized using straight waveguides across the interposer connected to a laser at one side and an optical power meter at the other side through SMF28 single mode fibers. After test bench deembedding, total insertion losses of 7.2 dB were measured on waveguides with a rib height of 7 μm, a rib width of 11 μm, a 3 μm thick base, and a length of 12.3 mm, corresponding propagation losses of 4.42 dB/cm at a wavelength of 1310 nm, after removal of mode mismatch and Fresnel reflections effects. These waveguides proved to be multimodal; however, single mode waveguides were demonstrated in Ref. 17 using the same materials and a photolithographic structuration, exhibiting 1.92 dB/cm of propagation losses at 1310 nm.

Second, the mirror optical functionality has also been demonstrated in Ref. 17, in which the vertical reflected field coming from the interposer waveguide was observed using an IR camera vertically placed above the mirror to emulate the PIC.

As the optical path of the interposer has been demonstrated to be functional in Ref. 17 for both waveguides and mirror on a standalone interposer, we then designed a PIC containing specific optical paths composed in series of:

- Figure 3(a): GC to couple light from the interposer waveguides/mirrors to the PIC, followed by single mode waveguides connected to output GC coming back to interposer mirror/waveguides.
- Figure 3(b): GC to couple light from interposer waveguides/mirrors to the PIC, followed by single mode waveguides connected to a photodiode. The generated photocurrent can then be transferred back to the interposer, thanks to electrical RDL routing.

Some optical measurements of Fig. 3(a) path were performed, confirming light coupling from interposer to PIC and conversely, thanks to mode profiles from Fig. 3(d). The multimode behavior of the polymer waveguides is also confirmed. We also measured the total losses of this structure from 1260 to 1340 nm by step of 10 nm. We could measure a minimum loss of 63 dB at 1320 nm, which is 17 dB higher than the −80 dBm noise threshold of our measurement setup. Several sources may be the cause of such high losses. Among them, we expect the misalignment between the mirrors and the GC to play an important role. Moreover, GCs are sensitive to the presented mode profile and wavelength, the latter being directly related to diffraction angle by Bragg's law. The combination of these three factors with the multimode behavior of polymer waveguides may result in such a high loss and wavelength sensitivity.

After demonstrating and evaluating the optical coupling between both chips, the association of electrical and optical coupling, as proposed in Fig. 3(b), must be demonstrated. This also allows us to consider only one optical coupling structure at a time. Figure 3(e) shows a picture of the electro-optical measurements, with butt coupling light injection into the interposer waveguides at one side and electrical measurements of the generated photocurrent at the other side. Figure 3(f) shows the I(V) characteristic of the 1290 nm test structure with the laser source turned on at 1265 nm and turned off. We can clearly observe the photocurrent generated by light exposure. However, the light on measurement is noisy. As we did not notice strong power variation of the source (thanks to a built-in power meter), we expect the noise to come from vibrations of the injection fiber, which is sensitive because of the length between the V-groove and the sample edge. To attenuate this phenomenon, we computed an average photocurrent I_{on} using all the values between −1.25 and −0.75 V, for each structure and at each wavelength point. The optical loss *OptLoss* of these test structures, from the laser source to the photodiode, is calculated using the following formula:

$$OptLoss = 10 \times \log_{10}\left(\frac{I_{on} - I_{off}}{Responsivity \times 1mW}\right) + 3dB, \quad (1)$$

where I_{off} is the current measured without light exposure at −1 V. The currents are expressed in mA, and the laser source power is 1 mW. It is noteworthy that Eq. (1) compensates by 3 dB for the presence of a Y junction in the optical path. We obtained an OptLoss of 20.97 dB at

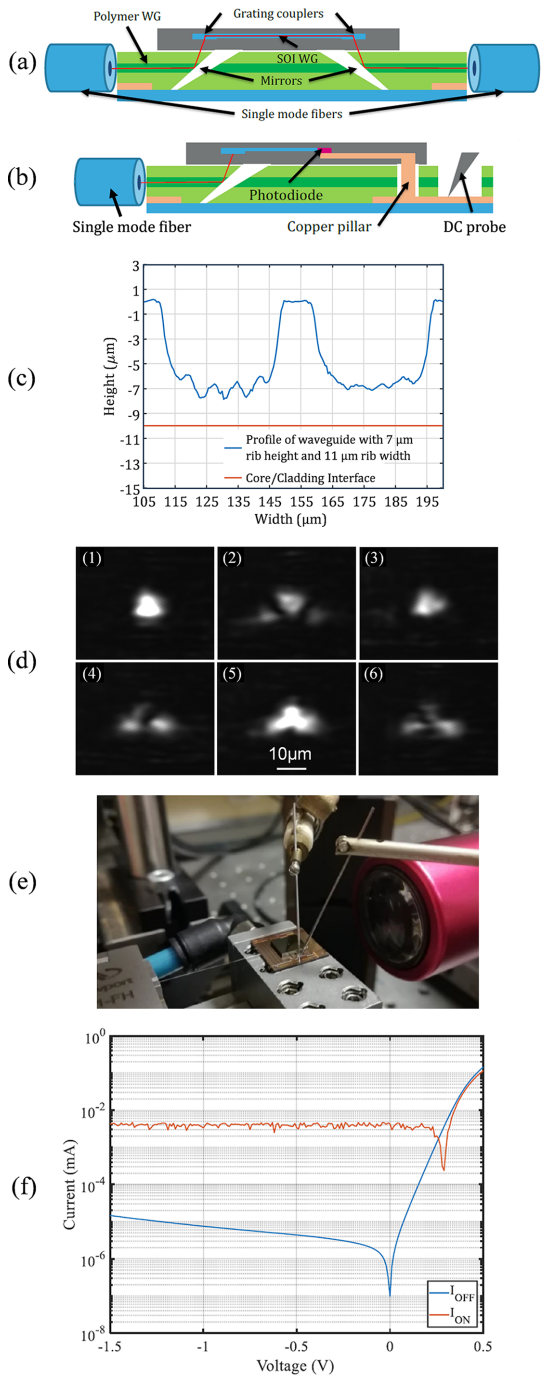

FIG. 3. Validation of optical path continuity between the interposer and the PIC. (a) Schematic of the optical path test structure. (b) Schematic of the principle of the optical coupling measurement using an embedded photodiode in PIC. (c) Measured profile of the rib waveguide with rib height and width of 7 and 11 μm, respectively. (d) Mode profiles of the optical path test structure depicted in (a) taken at following wavelengths (1) 1277, (2) 1278, (3) 1279, (4) 1280, (5) 1281, and (6) 1282 nm, the bar indicating the scale is approximate. (e) Experimental setup for characterizing the optical path using the embedded photodiode in PIC. (f) Static I(V) characteristic of the 1290 nm test structure with the laser source turned on at 1265 nm (red curve) and turned off (blue curve).

1265 nm. Based on our estimation of the polymer waveguides propagation (1.54 dB) and coupling losses (0.7 dB), we evaluate their contribution to 2.24 dB. On the silicon side, the SOI optical waveguides length is approximately 340 μm. Thus, we can simply neglect their contribution. Finally, an initial estimation of the mirror/GC coupling structure loss is 18.7 dB. This is high compared to the simulated structure and cannot compete with other available solutions. Nonetheless, the proof of concept showing the coupling of the optical signal from the interposer to the GC of the PIC after redirection by the mirror is established despite important losses that need optimization of the assembly strategy between the interposer and the PIC.

As outlined in Ref. 16, routing signals in the mmW range to drive the PIC are a major constraint in terms of frequency rise and with respect to the co-integration of the electrical RDL with layers embedding optical guides. The RDL consists in a 3 μm-thick layer of copper structured by femtosecond laser ablation. This so-called cold pulsed laser ablation regime makes it possible to define patterns free from redeposition of molten material[18] with a spot size of 10 μm in UV (343 nm). Copper ablation gives rise to tapered sidewalls that produce trapezoidal profiles, 12 μm wide at the top and 8 μm at the bottom over a thickness of 3 μm as shown in Fig. 4(a). The precision and homogeneity of laser machining are further exemplified in Fig. 4(b) that shows two coplanar waveguides (CPW) in parallel designed with a 100 μm wide central track and a 10 μm gap. The resulting full width at half maximum (FWHM) of the central track is 85 μm. Three different widths of the CPW central track were drawn at the layout level, namely, 100, 75, and 30 μm, resulting in 85, 60, and 10 μm of respective widths at half height. S-parameters of these lines have been measured over the 0.1–67 GHz range using a two port vector network analyzer (E8361A Keysight) and Infinity ground-signal-ground (GSG) probes featuring a 100 μm pitch. The extracted attenuation coefficients are given in Fig. 4(c), showing that minimum losses are achieved for the 85 μm wide CPW with 3 dB/cm at 58 GHz for a corresponding real part of the characteristic impedance of 46 Ω as illustrated in Fig. 4(d). The 60 μm wide CPW exhibits a slightly higher impedance of 47 Ω that results in a better adaptation but at the expense of the attenuation coefficient, which is 0.4 dB/cm higher at the same frequency. Finally, the 15 μm wide line has an impedance of 74 Ω and an attenuation coefficient of 4.5 dB/cm at 58 GHz, which are considered unsuitable for our application, which consists of propagating a 25 Gb/s digital signal to drive the Mach–Zehnder modulator embedded in the PIC. It can be observed that the attenuation coefficient presents periodic dips at every multiple of 8 GHz, which we attribute to standing waves. Beyond evaluating the performance of standalone CPWs on the glass interposer, two test structures consisting of a flip-chipped PIC on the interposer were evaluated with regard to the correct propagation of mmW control signals in the PIC. As illustrated in Fig. 4(e), the test structure comprises a 5.3 mm microstrip transmission line integrated in the PIC, which is connected at both ends to two 2.1 mm long and 85 μm wide CPWs on the interposer through 30 μm thick copper pillars. The same S-parameter measurement procedure as for the interposer CPWs was used. Figures 4(f) and 4(g) report insertion and return losses, respectively. Return losses below 13 dB over the entire frequency range as well as insertion losses of 7 dB at 50 GHz are obtained. Interestingly, identical frequency responses are obtained for the two test structures, demonstrating the reproducibility of the PIC flip-chip step from an electrical point of view. For the sake of

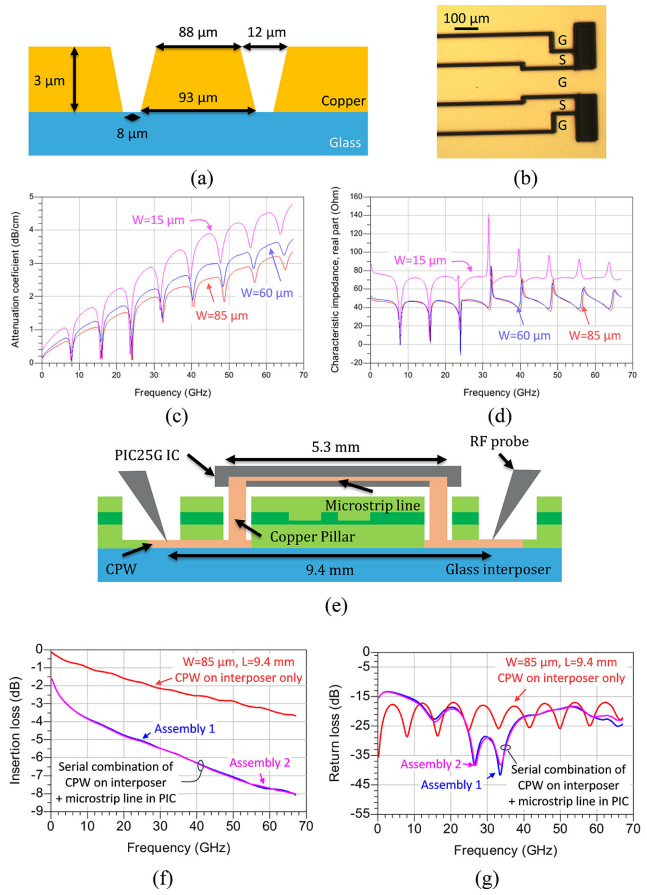

FIG. 4. Assessment of the mmW signal distribution to the PIC. (a) Schematic cross-sectional view of a CPW on the interposer after laser structuring starting from an initial design with a 100 μm central track and 10 μm gap. The resulting full width at half maximum (FWHM) of the central track is 85 μm. (b) Optical microscope view of two CPWs in parallel and their probing pads marked with the ground-signal-ground (GSG) port. (c) Measured attenuation coefficient. (d) Real part of characteristic impedance for 3 CPWs with central track featuring 15, 60, and 85 μm FWHM. (e) Schematic of the test structure for validating the serial continuity of the mmW signal along an interposer-PIC-interposer path. (f) Insertion losses and (g) return losses associated with an interposer-PIC-interposer propagation path for two separate PIC-on-interposer assembly. Comparison with insertion loss of a 9.4 mm long standalone CPW on the interposer.

comparison, the results of a standalone CPW on the interposer with a width of 85 μm and a length of 9.4 mm are also reported, showing that the limiting factor is propagation in the PIC and not on the interposer. Factory measurements have established an attenuation of 1.2 dB/mm for strip line in the PIC, while the aforementioned results of Fig. 4(c) report an attenuation of 0.27 dB/mm for the CPW on the interposer, both at 50 GHz. From these attenuation data, it is easy to calculate that the two CPW sections (2×2.1 mm $= 4.2$ mm) introduce a loss of 1.1 dB, while the strip line (5.3 mm) contributes 6.3 dB to the complete propagation path described in Fig. 4(e). The sum amounts to 7.4 dB, a slightly higher but consistent value when compared to the insertion loss directly measured at 7 dB on Fig. 4(f). Therefore, the analysis proposed above confirms that the performance of the overall propagation path is compatible with the implementation of a 25 Gb/s and above electro-optical transceiver.

In summary, a glass interposer for the heterogeneous integration of photonic and electronic integrated circuits using flip-chip assembly with passive alignment has been proposed to solve the difficult problem of fiber to PIC coupling. The interposer was fabricated using polymer and copper laser ablation in femtosecond regime. Both optical and electrical measurements provide the experimental demonstration of effective coupling of optical and mmW signals from the interposer to the PIC and conversely. Although this demonstration suffers from certain limitations due to flip-chip misalignments, a further reduction in optical path losses can be expected by using an automatic flip-chip equipment that achieves sub-micron placement accuracy, improved over the years.[19] Moreover, this demonstration of glass interposers paves the way for efficient integration of multiple chips, whether they are digital, analog, RF, or optical,[20,21] thanks to the compatibility with multi-layer electrical routing using more aggressive design rules,[22] and the utilization of Through Glass Vias (TGVs),[23] whose manufacturing processes have now reached industrial maturity.

This work was supported by (i) the STMicroelectronics-IEMN joint laboratory, (ii) the French Government through the National Research Agency (ANR) under program PIA EQUIPEX LEAF ANR-11-EQPX-0025, and (iii) the French RENATECH network on micro and nanotechnologies.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jean-Marc Boucaud: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal). **Cédric Durand:** Conceptualization (equal); Methodology (equal); Supervision (equal); Validation (equal); Writing – original draft (equal). **Frédéric Gianesello:** Conceptualization (equal); Methodology (equal); Supervision (equal); Validation (equal). **Davide Bucci:** Conceptualization (equal); Formal analysis (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **Jean Emmanuel Broquin:** Conceptualization (equal); Formal analysis (equal); Resources (equal); Supervision (equal); Validation (equal). **Emmanuel Dubois:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Supervision (lead); Validation (equal); Writing – original draft (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]S. Y. Siew, B. Li, F. Gao *et al.*, "Review of silicon photonics technology and platform development," J. Lightwave Technol. **39**(13), 4374–4389 (2021).

[2]S. Shekhar, W. Bogaerts, L. Chrostowski *et al.*, "Roadmapping the next generation of silicon photonics," Nat. Commun. **15**, 751 (2024).
[3]X. Zhou, C. F. Lam, R. Urata *et al.*, "State-of-the-Art 800G/1.6T Datacom interconnects and outlook for 3.2T," in *Optical Fiber Communications Conference and Exhibition (OFC)*, San Diego, CA (Optica Publishing Group, 2023), pp. 1–3.
[4]B. C. Chou, W. Vis, B. Khan *et al.*, "Design and demonstration of micro-mirrors and lenses for low loss and low cost single-mode fiber coupling in 3D glass photonic interposers," in *IEEE 66th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV (IEEE, 2016), pp. 497–503.
[5]B. Snyder, G. Lepage, S. Balakrishnan *et al.*, "Ultra-broadband, polarization-insensitive SMF-28 fiber edge couplers for silicon photonics," in *IEEE CPMT Symposium Japan (ICSJ)* (IEEE, 2017), pp. 55–58.
[6]R. Dangel, A. La Porta, D. Jubin *et al.*, "Polymer waveguides enabling scalable low-loss adiabatic optical coupling for silicon photonics," IEEE J. Sel. Top. Quantum Electron. **24**(4), 1–11 (2018).
[7]W. D. Sacher, T. Barwicz, B. J. F. Taylor *et al.*, "Polarization rotator-splitters in standard active silicon photonics platforms," Opt. Express **22**(4), 3777. (2014).
[8]L. B. Verslegers, A. Mekis, T. Pinguet *et al.*, "Design of low-loss polarization splitting grating couplers," in *Advanced Photonics for Communications* (2014), OSA Technical Digest Paper No. JT4A.2.
[9]C. C. Lin, A. Na, Y. K. Wu *et al.*, "Optimization of grating coupler over single-mode silicon-on-insulator waveguide to reach <1 dB loss through deep-learning-based inverse design," Photonics **11**, 267 (2024).
[10]W. Zaoui, M. F. Rosa, W. Vogel *et al.*, "Cost-effective CMOS-compatible grating couplers with backside metal mirror and 69% coupling efficiency," Opt. Express **20**, B238–B243 (2012).
[11]F. E. Ayi-Yovo, C. Durand, H. Petiton *et al.*, "Enablement of advanced silicon photonics optical passive library design leveraging silicon based RF passive development methodology," in *IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Austin, TX (IEEE, 2016), pp. 88–90.
[12]SCHOTT, see https://www.schott.com/en-ca/products/af-32-eco-P1000308/downloads for "AF32 eco ThinGlass."
[13]Micro resist technology GmbH, see https://www.microresist.de/en/produkt/epocore-epoclad-series/ for "EpoCore & EpoClad Series."
[14]A. Noriki, I. Tamai, Y. Ibusuki *et al.*, "Optical TSV using Si-photonics integrated curved micro-mirror," in *International 3D Systems Integration Conference (3DIC)*, Sendai, Japan (IEEE, 2019), pp. 1–4.
[15]A. Mistry, K. Nieweglowski, and K. Bock, "Hybrid-lithography for the master of multi-mode waveguides NIL stamp," in *46th International Spring Seminar on Electronics Technology (ISSE)*, Timisoara, Romania (IEEE, 2023), pp. 1–5.
[16]R. Zhang, F. Liu, M. Kathaperumal *et al.*, "Cointegration of single-mode waveguides and embedded electrical interconnects for high-bandwidth communications," IEEE Trans. Compon., Packag., Manuf. Technol. **10**(3), 393–399 (2020).
[17]J. M. Boucaud, Q. Hivin, C. Durand *et al.*, "Single mode polymer optical waveguides and out-of plane coupling structure on a glass substrate," in *7th Electronic System-Integration Technology Conference (ESTC)*, Dresden, Germany (IEEE, 2018), pp. 1–5.
[18]A. Bhaskar, J. Philippe, F. Braud *et al.*, "Large-area femtosecond laser milling of silicon employing trench analysis," Opt. Laser Technol. **138**, 106866 (2021).
[19]B. T. Tung, N. Watanabe, F. Kato *et al.*, "Flip-chip bonding alignment accuracy enhancement using self-aligned interconnection elements to realize low-temperature construction of ultrafine-pitch copper bump interconnections," in *IEEE 64th Electronic Components and Technology Conference (ECTC)*, Orlando, FL (IEEE, 2014), pp. 62–67.
[20]R. Santos, N. Ambrosius, R. Ostholt *et al.*, "Bringing new life to glass for wafer-level packaging applications," in *International Wafer Level Packaging Conference (IWLPC)*, San Jose, CA (IEEE, 2020), pp. 1–7.
[21]J. Müller, M. Kaltwasser, H. Bartsch *et al.*, "Glass and Glass/LTCC interposers as heterogenous integration platform," in *Pan Pacific Strategic Electronics Symposium (Pan Pacific)*, Kona, Big Island, HI (IEEE, 2024), pp. 1–7.
[22]M. Elkhouly, J. Ha, M. J. Holyoak *et al.*, "Fully integrated 2D scalable TX/RX chipset for D-band phased-array-on-glass modules," in *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA (IEEE, 2022), pp. 76–78.
[23]S. Takahashi, K. Horiuchi, S. Mori *et al.*, "Development of through glass via technology for 3D packaging," in *European Microelectronics Packaging Conference (EMPC)*, Grenoble, France (IEEE, 2013), pp. 1–4.