

Study of Interconnection Process for Fine Pitch Flip Chip

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Abstract

Today, flip chip technology is a main stream of interconnection in microelectronic packaging and market forces continue to drive toward finer pitch interconnections. In this paper, fine pitch flip chip (FPFC) interconnection technology (i.e., less than 60um pitch) will be described. Two types of 50um pitch bump (Au stud & Cu pillar) will be evaluated and two different flip-chip (FC) bonding methods will be studied. Package structures of bare die flip-chip CSP (chip scale package) and also over molded version will be studied for reliability performance and volume assembly fit. For characterization, structure analysis will be performed at each reliability read point. Finally this paper will conclude by identifying the most robust bonding method for the FPFC devices.

Introduction

Fine pitch flip chip (FPFC) packaging (i.e., less than 60um pitch) is an emerging technology for high speed portable devices, such as application processors in mobile phone and image processors in digital cameras, to meet the demands for both smaller form factors and lower cost products. A key advantage for FPFC devices is they do not need a redistribution layer (RDL) on the wafer. Therefore, current die design and manufacturing infrastructures may be used. This enables peripheral inline pitch die to be applied directly to flip chip applications. Fig.1 shows standard FPFC package configuration. And a variety of applications is shown in Fig. 2.

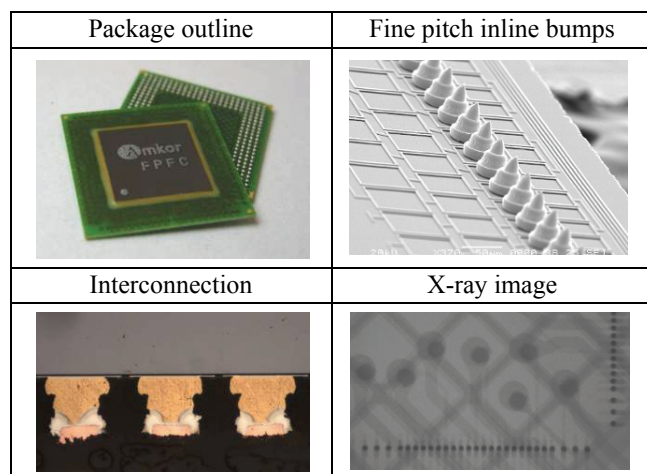


Figure 1 : Standard FPFC package structures

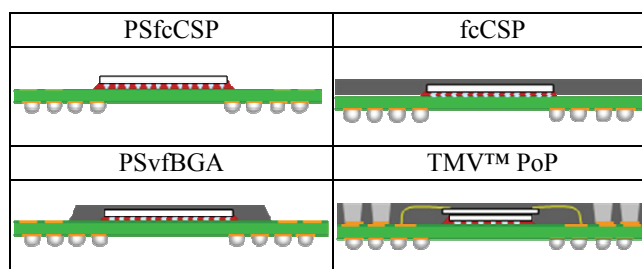


Figure 2 : Package applications using FPFC

However, due to the very fine pitch, the solder bump stand-off height must be very shallow or solder shorts may occur. To address this issue, Au stud and Cu pillar bumps are being considered for fine pitch applications to allow enough stand-off height for robust package reliability. Due to their extremely small size, these fine pitch interconnects are very fragile at the bump joint area. They are vulnerable to joint failure due to the stresses encountered during package and PWB assembly, created by the thermal mismatch between the die and the organic substrate. In this paper, two types of flip chip bonding processes using both Au stud and Cu pillar bumps will be evaluated for package characterization and reliability. The first bonding process is thermo-compression bonding with NCP (non-conductive paste) which simultaneously encapsulates the bumps and protects the vulnerable die interconnect. The second type is mass reflow with capillary underfill (CUF), which is widely used for current standard pitch flip chip applications (i.e., greater than 150um pitch). Process characterization will be evaluated by cross-section, x-ray, acoustic imaging (SAT), and open/short testing. This will be followed by package reliability testing using JEDEC MRT Level 3 preconditioning, TCB (1000cycles), HAST (96hrs), and HTS (1000hrs). Finally we will conclude and discuss the most robust FPFC bonding method for volume manufacturing.

Test vehicles

In this paper, two types of 50um pitch micro bump technologies will be used. The first one is Au stud bump which is cone shape formed by conventional gold wire ball bonding technology on the Al pad and the other type is Cu pillar bump which is comprised of Cu post and Sn/Ag cap formed by electroplating at wafer level. Fig. 3 shows both

bump images and Table 1 shows merit & demerit of each bump technology.

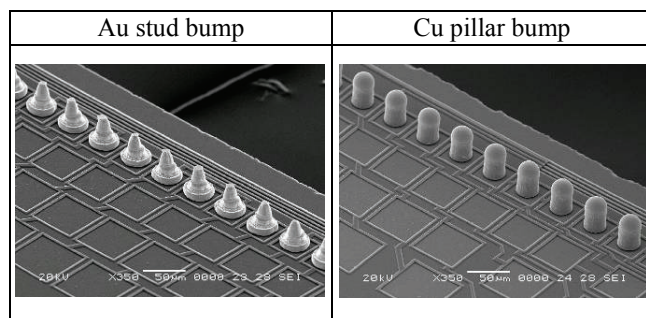


Figure 3 : 50um pitch micro bumps

Au stud bump	Cu pillar bump
Serial bumping process	Parallel bumping process (wafer level bumping)
Cost effective for low pin counts	Cost effective for high pin counts
Better solder wetability without flux material	Need flux material for good wetting
Fast IMC growth rate for Au-Sn	Relatively slow IMC growth rate compared to Au-Sn
Wider process range for FC bonding force due to gold ductility	Relatively sensitive for FC bonding force variance

Table 1 : Au stud vs. Cu pillar

The package test vehicle for this study is a 13mm x 13mm body size, 1.0mm max. height with 320 BGAs at 0.5mm pitch. The Amkor FC test die dimension is 7.62mm x 7.62mm with 0.10mm Si thickness. Die is capable of open-short testing in daisy-chain configuration and bump count is 420 peripheral bumps in 50um inline pitch. The substrate is a 4layer 1-2-1 high-density design and with 25/25um line/space and 200um via land size in 0.30mm total thickness. With these test vehicles, encapsulation material between die and substrate will be decided per the FC bonding method. Non-conductive-paste (NCP) will be used for thermo-compression (TC) bonding and capillary underfill (CUF) will be used for mass reflow (MR) process. The evaluation test matrix is described in Table 2.

Leg	Bump	Bonding method	Sample size
1	Au stud	TC + NCP	66
2	Cu pillar	TC + NCP	66
3	Cu pillar	MR + CUF	66

Table 2 : Evaluation test matrix

Interconnection process flow

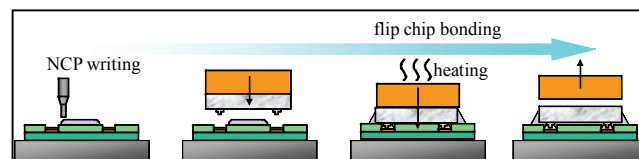


Figure 4 : TC + NCP process flow

Before the flip chip bonding processes, wafer level bumping is completed, followed by wafer thinning. The substrates are prebaked to remove volatile compounds and moisture. Figure 4 shows the interconnect process flow for the TC+NCP legs, NCP is pre-dispensed and then TC bonding using a proper heating profile and compression. The key features of the TC+NCP process are; control of bonding force and temperature profiles to simultaneously get robust FC interconnect shape and void-free NCP coverage. NCP selection is important to address above requirements and package reliability. Therefore NCP material selection and property control is critical before starting assembly. For example, the Tg, CTE1, CTE2 and modulus influence package long-term reliability performance such as Temp-Cycle life. Flip chip workability in high speed TC bonding can be controlled by NCP viscosity and cure speed. This paper briefly describes how NCP properties affect package quality.

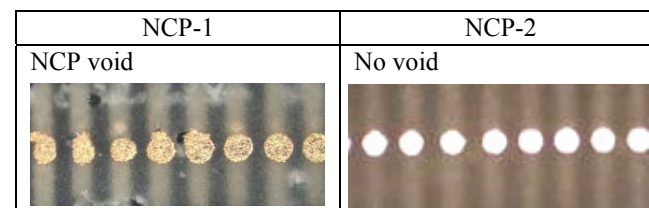


Figure 5 : NCP tiny voiding comparison

Fig. 5 shows a comparison of very tiny voiding near bump edges. NCP-1 showed many tiny voids but there is no voiding seen with NCP-2 in this study. Both FC bonding parameters and material property control can impact voiding.

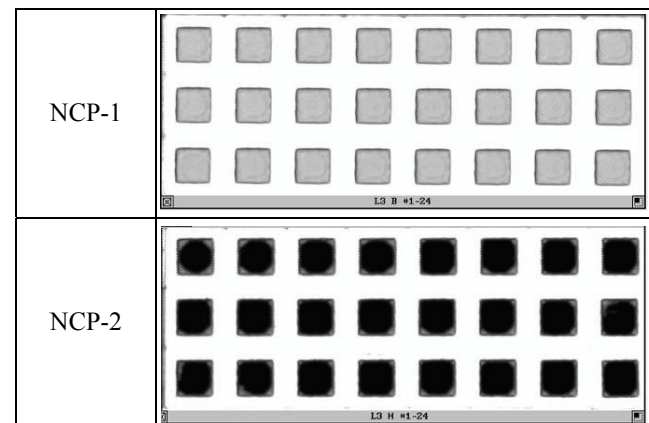


Figure 6 : SAT images after MRT L3

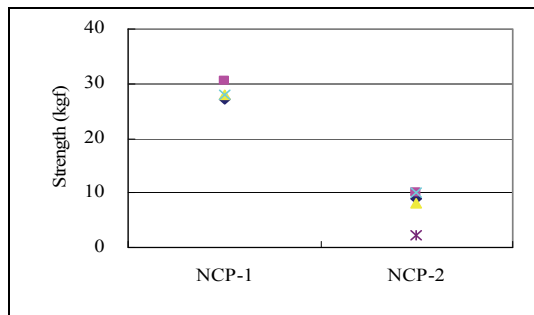


Figure 7 : Adhesion strength of NCP on die

Fig. 6 shows that NCP selection and control, are key to MRT performance. NCP-1 passed MRT L3@260°C condition without delamination. Normally bare die flip chip packages with NCP easily survive JEDEC MRT L3 condition but over-molded flip chip structures show more challenges to pass the same MRT condition. It was found that NCP adhesion property is deeply related to pass or fail in MRT conditions. Fig. 7 shows adhesion results measured by button shear testing. Therefore, we conclude that higher adhesion strength is better for MRT reliability performance.

The other process flow, MR+CUF is the same as a conventional flip chip attachment process, commonly referred to as “C4 interconnection”. Nowadays the C4 technology is being widely used for CPU applications in PC and Games but area array bump pitch is normally over 150µm. In the case of very fine pitch (i.e., 50µm) with solder bumps, it is expected that there may be unstable stand-off height, non-wet bumps and bump short failures. Therefore either Au stud or Cu pillar bumps should be used to secure stable stand-off height and prevent bump short problems. In this study, Au stud bump with a mass-reflow process was not evaluated because experience shows bump cracks can easily occur due to the brittleness of Au-Sn intermetallic compound, as shown in Fig. 8.

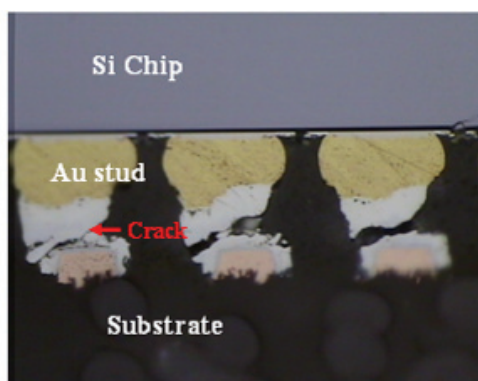


Figure 8 : Typical bump crack at Au-Sn layer

Leg 3 process flow is as follows. First, flux is applied on either chip or substrate, and then the die is placed on the substrate by using conventional flip chip bonding. The solder joints are made simultaneously by mass reflow process, and plasma treatment is performed, followed by underfill application. Finally underfill is cured.

Process Characterization

To confirm assembly characterization, x-section, x-ray, SAT and electrical open/short test were done before starting the reliability tests.

X-section is shown in Fig. 9, Through this inspection, overall joint shape, bump wetability, and misalignment can be confirmed. As a result, abnormal joints were not found but there were some tiny NCP filler entrapment between bump and substrate bump pads. It will be revealed that the trapped filler affect electrical test failure seriously.

Leg 1: Au stud TC+NCP	Leg 2: Cu pillar TC+NCP	Leg 3: Cu pillar MR+CUF

Figure 9 : X-section view of bumps

Through the X-ray inspection, there was not any specific misalignment problem for all bonding processes. Fig. 10 shows good accuracy shape of the MR+CUF process.

SAT check for voiding is very important to have reliable package performance. Since it is very fine bump pitch, very high resolution SAT machine should be required to detect micro bump to bump void which can possibly cause electrical short failure during reliability test. Through the fine SAT, there was no specific voiding in Fig. 11

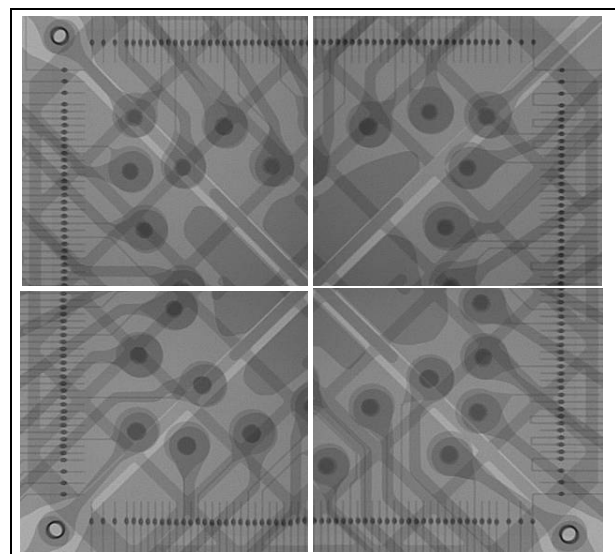


Figure 10 : X-ray inspection for MR+CUF process

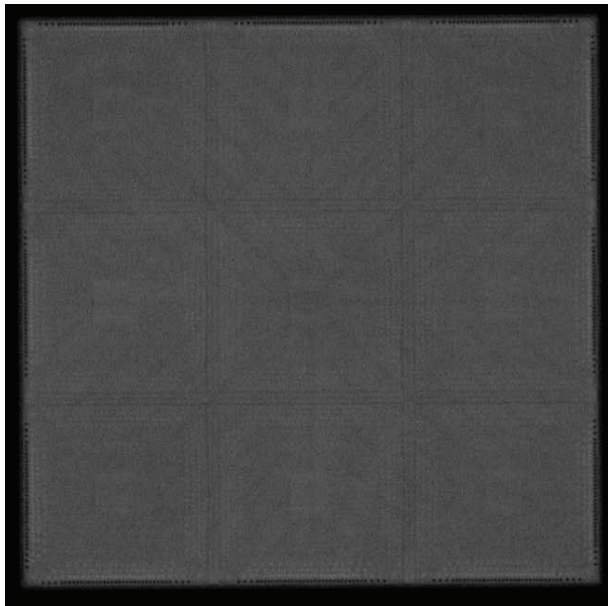


Figure 11 : Fine SAT for TC+NCP process. Peripheral 50um pitch bumps are visible and no tiny voids detected

Reliability Test

Packages were tested with JEDEC moisture Sensitivity Level 3 (MSL3) (30°C/60%RH, 192hrs) with 3X, 260°C peak reflow. After this preconditioning, additionally three kinds of long term reliability testing, i.e., temperature cycle (T/C) test (-55/+125°C, 1000cycle), and high temperature storage (HTS) life testing (150°C, 1000hrs), highly accelerated temperature humidity stress test (HAST) (130°C/85%RH, 96hrs) were performed. At all read out points, electrical open/short testing was done with pass criteria of less than 10% resistance rise compared to time-zero values. Scanning acoustic microscopy (SAT) was used to inspect package delamination after all reliability tests.

Table 3 shows final reliability results. All three legs of flip chip process passed all conditions without failure.

Leg	Precondition	HAST96	TC1000	HTS1000
1	0/66	0/22	0/22	0/22
2	0/66	0/22	0/22	0/22
3	0/66	0/22	0/22	0/22

Table 3 : Final reliability result. Reject/Sample Size

Conclusions

We have completed feasibility study for fine pitch flip chip bonding methods, using 50um peripheral inline bump pitch. We applied two types of fine pitch bumping and tested three kinds of flip chip bonding process. Through this interconnection study, we have developed flexible FPFC process solutions for both bump types. With regard to Au stud bumps, we validated that TC+NCP is a robust process. For Cu pillar bumps, we achieved good results for both TC+NCP and MR+CUF process flows. To get reliable package performance, good bump shape control and good bump encapsulation with NCP underfill for the TC+NCP

process, heating profile and bonding force control are important and NCP material property is important to reliability performance. Even when tiny NCP filler entrapment was seen, we verified that there was no problem to pass package reliability requirements. Also in this study, we achieved outstanding results with a mass reflow process and capillary underfill for a robust interconnection method.

Future work planned with fine pitch FC interconnection will address new packaging challenges including TSV (Through Silicon Via) interconnection technologies. Here tighter bump profiles in very thin die (i.e., 50um Si thickness) can create challenges for FPFC attach to substrates as well as in chip to chip stacking. For TSV applications, we anticipate evaluating 4 die and 8 die stacks. We expect one challenge is how best to control bonding height and material volume with high density multiple thin die based TSV interconnect stacks.

References

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