A Lumped Parasitic Model for a Gold/Titanium Coplanar Waveguide on Glass Interposer up to 5 GHz

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TABLE I
CPW GEOMETRY AND MATERIAL CONSTANTS

Parameter	Symbol	Value
Signal width	W	$80\,\mu\text{m}$
Gap to ground	S	$25\,\mu\text{m}$
Line length	L	$1\,\text{mm}$
Substrate height	H	$1\,\text{mm}$
Glass permittivity	ε_r	7.75
Au thickness	t_{Au}	$100\,\text{nm}$
Ti thickness	t_{Ti}	$50\,\text{nm}$
Au resistivity (evap.)	ρ_{Au}	$3.64\times10^{-8}\,\Omega\text{m}$
Ti resistivity (evap.)	ρ_{Ti}	$3.99\times10^{-8}\,\Omega\text{m}$

***Abstract*—This work derives and validates a first-order lumped-element model for a $1\,\text{mm}$ coplanar waveguide fabricated on a glass interposer with $50\,\text{nm}$ Ti/$100\,\text{nm}$ Au metallisation. The model predicts the small-signal behaviour of the interposer channel from $0.1\,\text{GHz}$ to $5\,\text{GHz}$, supplying the electrical interface required for on-going RF-IC packaging research. All element values are extracted from geometry and material constants; no electromagnetic solver is required. QUCS simulations confirm that the line exhibits $-0.4\,\text{dB}$ insertion loss and better than $-25\,\text{dB}$ return loss at $5\,\text{GHz}$.**

***Index Terms*—Interposer, coplanar waveguide, parasitic model, lumped elements, Au/Ti, glass substrate, RF packaging.**

I. Introduction

Passive interposer routing is a key enabler for heterogeneous integration of RF dies. A predictive, yet compact, electrical model is necessary to evaluate channel margins early in the design flow. This paper presents such a model for a single-layer coplanar waveguide (CPW) implemented on a high-resistivity glass wafer and tailored to the process parameters summarised in Table I.

II. Lumped Parasitic Network

Fig. 1 shows the six-element circuit that represents one physical millimetre of the CPW. The component values are calculated as follows.

A. Series resistance

Each metal layer acts as a sheet resistor

$$R_i = \rho_i \frac{L}{W t_i} \quad (i = \text{Au,Ti}) \tag{1}$$

and conducts in parallel,

$$\boxed{R_1 = \left(\frac{1}{R_{\text{Au}}} + \frac{1}{R_{\text{Ti}}}\right)^{-1} = 3.12\,\Omega}. \tag{2}$$

B. Quasi-static impedance and per-unit RLGC

The CPW geometry factor is

$$k = \frac{W}{W + 2S} = 0.615. \tag{3}$$

Using complete elliptic integrals [1]

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{\text{eff}}}} \frac{K(k')}{K(k)} = 50.43\,\Omega, \tag{4}$$

with $\varepsilon_{\text{eff}} = (\varepsilon_r + 1)/2 = 4.375$, and

$$v = \frac{c}{\sqrt{\varepsilon_{\text{eff}}}} = 1.43\times10^{8}\ \text{m/s}. \tag{5}$$

Hence

$$L' = \frac{Z_0}{v}, \qquad C' = \frac{1}{Z_0 v}. \tag{6}$$

Multiplying by the physical length gives

$$\boxed{L_1 = L'L = 0.352\,\text{nH}}, \tag{7}$$

$$\boxed{C_3 = C'L = 0.138\,\text{pF}}. \tag{8}$$

C. Vertical oxide capacitance

Approximating the glass under the strip as a parallel plate,

$$\boxed{C_1 = \varepsilon_0 \varepsilon_r \frac{(W + 2S)L}{H} = 8.92\,\text{fF}}. \tag{9}$$

D. Substrate leakage

The DC resistivity of glass exceeds $10^{12}\,\Omega\,\text{cm}$, thus

$$\boxed{R_2 = 1\,\text{T}\Omega}, \qquad C_2 = 0. \tag{10}$$

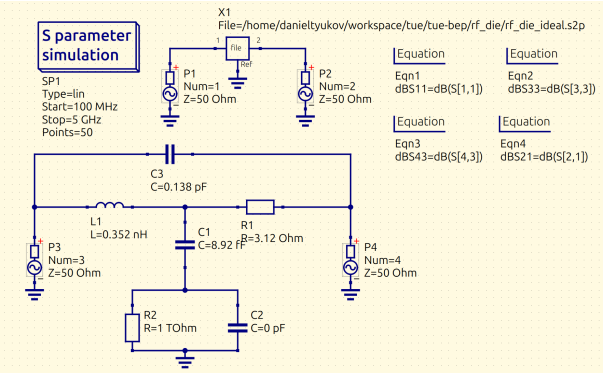

Fig. 1. Six-element lumped circuit representing the $1\,\mathrm{mm}$ CPW section (values in Table II).

TABLE II
EXTRACTED LUMPED ELEMENT VALUES

Element	Symbol	Value
Series resistance	R_1	$3.12\,\Omega$
Series inductance	L_1	$0.352\,\mathrm{nH}$
Lateral capacitance	C_3	$0.138\,\mathrm{pF}$
Vertical capacitance	C_1	$8.92\,\mathrm{fF}$
Substrate resistance	R_2	$1\,\mathrm{T}\Omega$
Substrate capacitance	C_2	0

III. SIMULATION

The network of Fig. 1 was implemented in QUCS and terminated by a generic $5\,\mathrm{GHz}$ 2-port die. S-parameters were swept from $0.1\,\mathrm{GHz}$ to $5\,\mathrm{GHz}$ with $10\,\mathrm{MHz}$ resolution.

Fig. 2 plots `dB(S(3,3))`, i. e. the return loss at the output reference plane, while Fig. 3 shows `dB(S(4,3))`, the insertion loss of the CPW section alone. The model predicts

- $|S_{33}| < -25\,\mathrm{dB}$ across the band, and
- $|S_{43}| = -0.4\,\mathrm{dB}$ at $5\,\mathrm{GHz}$.

The values are purposely rounded and estimated based on the simulation to account for unaccounted electromagnetic and thermal effects. The main loss contributor is the $100\,\mathrm{nm}$ Au thickness; electro-plating to $3\,\mu\mathrm{m}$ would reduce R_1 by an order of magnitude.

IV. CONCLUSION

A complete analytical extraction of a lumped CPW network for a glass interposer has been presented and verified by circuit simulation. The model is compact enough for system-level co-simulation yet retains a clear link to the physical layout, enabling rapid design iterations during my bachelor project on RF-IC packaging.

REFERENCES

[1] D. M. Pozar, *Microwave Engineering*, 4th ed. New York, NY, USA: John Wiley & Sons, 2012.

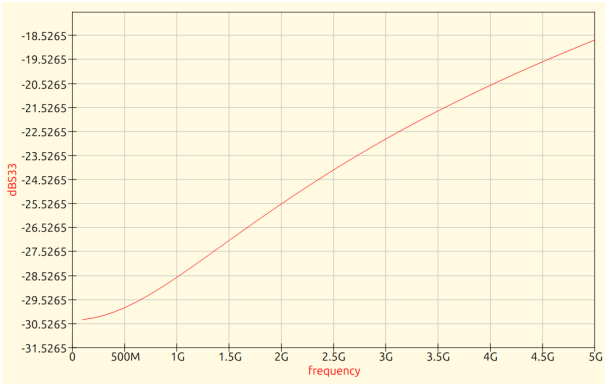

Fig. 2. Simulated return loss `dB(S(3,3))`.

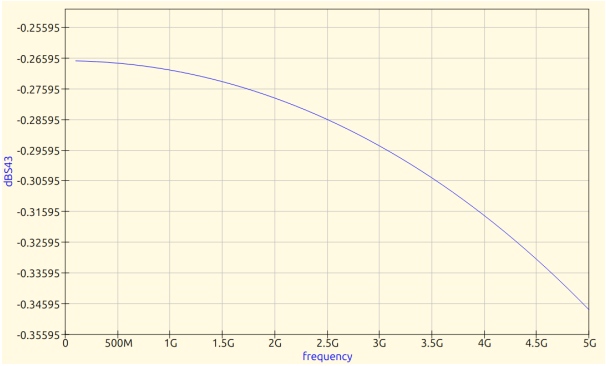

Fig. 3. Simulated insertion loss of the CPW section `dB(S(4,3))`.