# Effects of Underfill Material Properties on the Reliability of Solder Bumped Flip Chip on Board with Imperfect Underfill Encapsulants

John H. Lau, S-W. Ricky Lee, Chris Chang and Chien Ouyang
Express Packaging Systems, Inc.
1137-B San Antonio Road
Palo Alto, CA 94303

**Abstract**

The effects of underfill material properties on the reliability of solder bumped flip chip on printed circuit board (PCB) with imperfect underfill encapsulants were studied in this paper. Three different types of underfill imperfections were considered; i.e., (1) interfacial delamination between the underfill encapsulant and the solder mask on the PCB (crack initiated at the tip of underfill fillet), (2) interfacial delamination between the chip and the underfill encapsulant (crack initiated at the chip corner), and (3) the same as (2) but without the underfill fillet. Five different combinations of coefficient of thermal expansion (CTE) and Young's modulus with the aforementioned delaminations were investigated. A fracture mechanics approach was employed for computational analysis. The strain energy release rate at the crack tip and the maximum accumulated equivalent plastic strain in the solder bumps of all cases were evaluated as indices of reliability. Besides, mechanical shear tests were performed to characterize the shear strength at the underfill-solder mask interface and the underfill-chip passivation interface. The main objective of the present study is to achieve a better understanding of the thermo-mechanical behavior of flip chip on board (FCOB) assemblies with imperfect underfill encapsulants.

## 1. Introduction

The reliability of solder bumped flip chip on PCB with a ***perfect*** underfill encapsulant has been demonstrated by many researchers through thermal cycling tests, mechanical tests, shock and vibration tests and computational modeling, for instance, see [1-11]. However, due to the manufacturing processes such as fluxing, cleaning, dispensing and curing, and out-gassing of PCB, underfill defects in the form of voids, cracks, and missing fillets are quite common. In the present study, our objective is to investigate the effect of underfill material properties on the reliability of solder bumped flip chip on PCB with ***imperfect*** underfill encapsulants.

To simulate the imperfections of underfill encapsulant, three interfacial delamination cases, namely, (1) separation between the underfill encapsulant and the solder mask on the PCB (crack initiated at the tip of underfill fillet), (2) separation between the chip and the underfill encapsulant (crack initiated at the chip corner), and (3) the same as (2) but without the underfill fillet, were modeled. For the effects of underfill material properties, a series of computational parametric study with five different combinations of CTE and Young's modulus were performed. A fracture mechanics approach together with finite element method was employed for computational analysis. Under a fixed uniform thermal loading, the strain energy release rate at the crack tip and the maximum accumulated equivalent plastic strain in the solder bumps with respect to progressive crack growth were evaluated and compared. The present analysis revealed some peculiar fracture behaviors along the aforementioned interfaces.

In addition to numerical modeling, an attempt was made to characterize the interfacial shear strengths between the underfill and the solder mask and between the underfill and the chip passivation, respectively. These quantities were obtained from mechanical shear tests and microscopic inspection. The results of the present study have led to a better understanding of the thermo-mechanical behavior of FCOB assemblies with imperfect underfill encapsulants.

Table 1: Material Properties for Finite Element Modeling

| Properties | E (GPa) | ν | α (ppm/°C) |
|---|---|---|---|
| FR4 | 22 | 0.28 | 18 |
| 63Sn/37Pb | 32-0.088*T(°C) | 0.4 | 21 |
| Si | 131 | 0.3 | 2.8 |
| Cu | 82.7 | 0.35 | 17 |
| Al | 69 | 0.33 | 22.8 |
| Underfill | see Table 2 | 0.35 | see Table 2 |
| Passivation | 4.2 | 0.35 | 47 |
| Solder Mask | 6.9 | 0.35 | 19 |

Table 2: Combinations of Underfill Material Properties

| CASE | E (GPa) | α (ppm/°C) |
|---|---|---|
| 1 | 6 | 30 |
| 2 | 3 | 30 |
| 3 | 9 | 30 |
| 4 | 6 | 20 |
| 5 | 6 | 40 |

## 2. Finite Element Modeling and Fracture Mechanics Analysis

The problem under investigation was a flip chip on board assembly. However, the present methodology could be applied to problems with flip chip in package (FCIP) configuration. The detailed dimensions of the FCOB assembly are given in Figure 1. To study the present problem, a commercial finite element code, namely, ANSYS, was

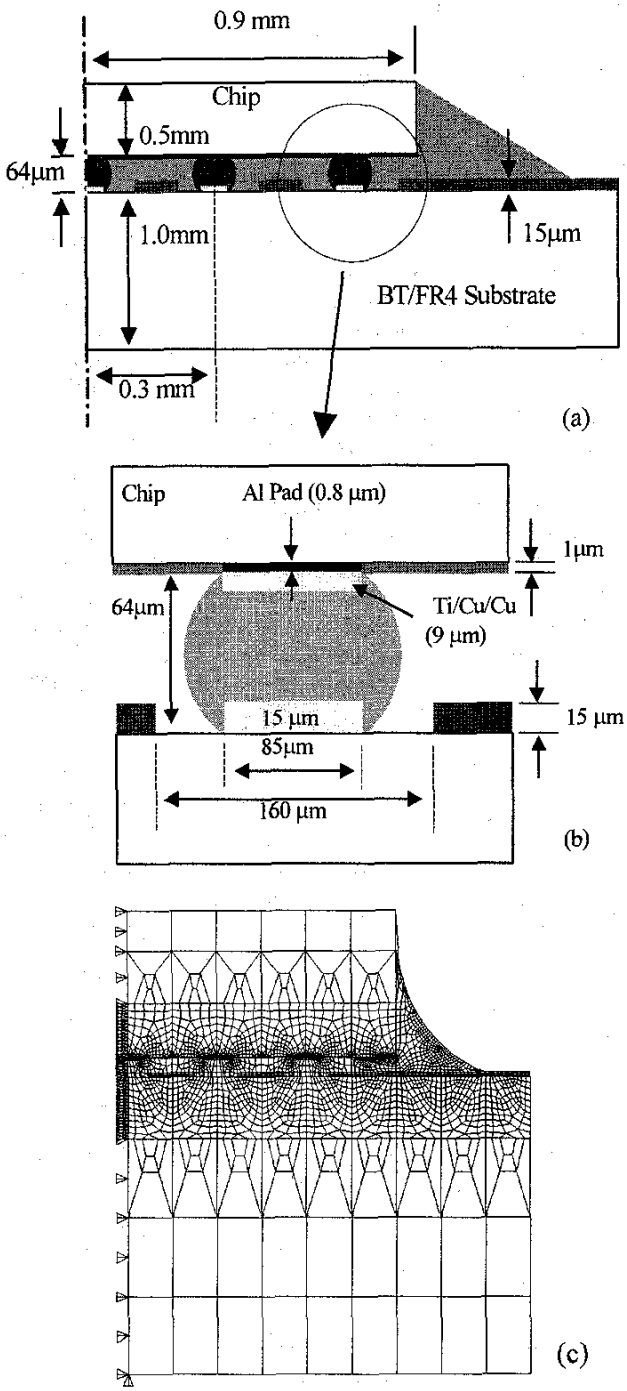


Figure 1: (a) Cross-section of FCOB assembly showing dimensions of various constituents, (b) close-up diagram around a solder bump, (c) meshes of finite element model

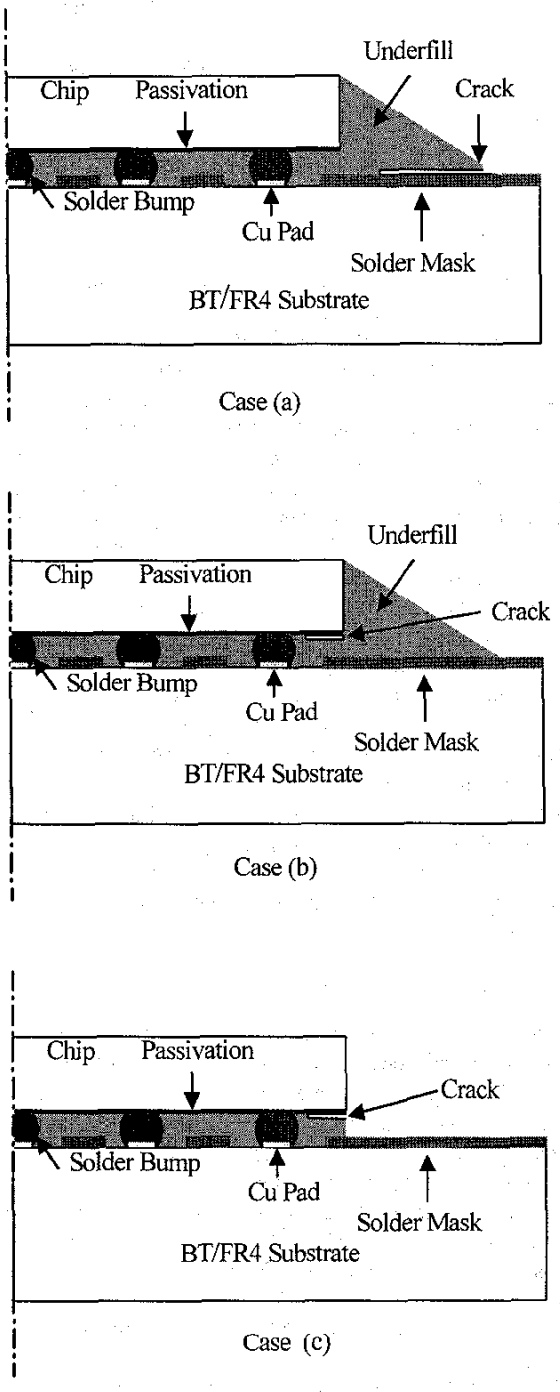


Figure 2: Three types of underfill imperfections under investigation, (a) delamination between the underfill and the solder mask, (b) delamination between the underfill and the chip passivation (with fillet), (c) delamination between the underfill and the chip passivation (no fillet)

employed. A two-dimensional model was established as shown in Figure 1(c) using 8-node plane strain elements. It should be noted that all detailed assembly structures such as chip, Al pads, passivation, under bump metallurgy (UBM), solder bumps, Cu pads, and solder mask were modeled in the finite element analysis. Besides, due to the symmetry in the assembly structure, only half of the cross-section was considered. The material properties used in the computational modeling are given in Table 1. Except that the eutectic solder (63Sn/37Pb) was a temperature-dependent elasto-plastic material [12], all other constituents were considered as linear elastic materials. Since the scope of the present study was to investigate the effects of underfill material properties, five different combinations of CTE and Young's modulus as shown in Table 2 were studied.

Another main objective of this study was to investigate the behaviors of imperfect underfill encapsulant. The imperfections under consideration were three types of interfacial delaminations as illustrated in Figure 2. These defects might be introduced from surface contamination and poor underfill encapsulation process. The initial defect could be just a localized flaw, but might extend to large area of delamination after the application of thermo-mechanical loading. In order to simulate such kind of manufacturing defects, certain special treatment must be implemented in the finite element model. In the present analysis, an array of double nodes were built-in along the specific interface of interest. A series of models with various ranges of double nodes were established to simulate the progressive crack growth of delamination. In order to prevent the interpenetration between the crack surfaces, contact elements were installed at certain critical locations on the delaminated surfaces.

Since crack propagation was simulated in the computational model, a fracture mechanics approach was adopted in the present analysis. The strain energy release rate at the crack tip (G) of each crack length was calculated. The evaluation of G is rather straightforward. By definition, G is the change of strain energy per unit crack growth. By running two analyses with a small increment in the crack length and evaluating the total strain energy of each case, the value of G could be calculated. In addition to strain energy release rate, the maximum accumulated equivalent plastic strain ($\varepsilon_p$) in the solder bumps at each crack length was also evaluated as an index of reliability. In total there were 15 cases (5 combinations of underfill material properties x 3 types of imperfections) in the present study. For each case under investigation, a temperature drop of 110→25°C was applied. The aforementioned two quantities (G and $\varepsilon_p$) were evaluated with respect to progressive crack growth for the comparison of reliability.

### 3. Effects of Underfill Material Properties on Imperfect FCOB Assemblies

The results of computational analysis are presented in Figures 3-8 for three types of underfill imperfections, respectively. Figure 3 shows the progressive crack growth along the interface between underfill encapsulant and solder mask. The scale factor for the presentation of deformation is 50. The material properties of underfill are E = 6 GPa and CTE = 30 ppm/°C. It should be noted that the shown mesh is a cut-out from the global model for better demonstration. The growth of delamination can be clearly observed. Figures 4 and 5 illustrate the progressive crack growth along the interface between underfill and chip for the case with and without encapsulant fillet, respectively. The attributes of demonstration of these two figures are the same as those of Figure 3. It is observed that the crack opening in the case with encapsulant fillet is not significant while the case without fillet has larger crack opening. Judging from the shown deformation, it is obvious that the FCOB assembly without encapsulant fillet is much more critical than the case with fillet.

Detailed comparison for the effects of underfill material properties are given in Figures 6-8. From Figure 6(a), for the cases with delamination between underfill encapsulant and solder mask, it can be seen that the strain energy release rate always increases with respect to the crack growth. This is an indication of unstable crack and will lead to catastrophic failure at the end. Therefore, such kind of damaging mechanism should be avoided. Figure 6(b) shows that the maximum plastic strain in the solder increases with respect to the crack growth. This is due to the fact that longer crack reduces the load transfer to the underfill and, hence, leads to more loading on the solder bumps. This figure also reveals that underfills with higher Young's modulus (9 GPa) and higher CTE (40 ppm/°C) should result in poorer solder bump reliability.

Figure 7(a) shows a convex shape for the strain energy release rate. This phenomenon indicates that, under a fixed loading, the crack will be arrested (stop) after propagating a certain length. In other words, the delamination will not grow further unless the loading is increased. Besides, the values of G are much lower than those shown in Figure 6(a). Therefore, this type of imperfection is not as damaging as the previous case. On the other hand, the trends and magnitudes of maximum accumulated equivalent plastic strain in Figure 7(b) seem similar to those in Figure 6(b). However, it should be noted that the higher values of $\varepsilon_p$ are based on the assumption that the delamination would grow to the corresponding length. If the crack were arrested beforehand, the larger $\varepsilon_p$ values would have never been reached.

Figure 8 presents the results for the case without encapsulant fillet. The general trends are similar to those for the case with fillet. However, although the strain energy release rate shows possible crack arrest behavior, the values of G are much higher than the other two cases. Furthermore, the values of $\varepsilon_p$ are the highest among the three cases under investigation. Therefore, this type of imperfection is definitely unfavorable and should be avoided.

Among all combinations of material properties investigated in this series of parametric study, the best case (based on the smallest $\varepsilon_p$) is the FCOB assembly with

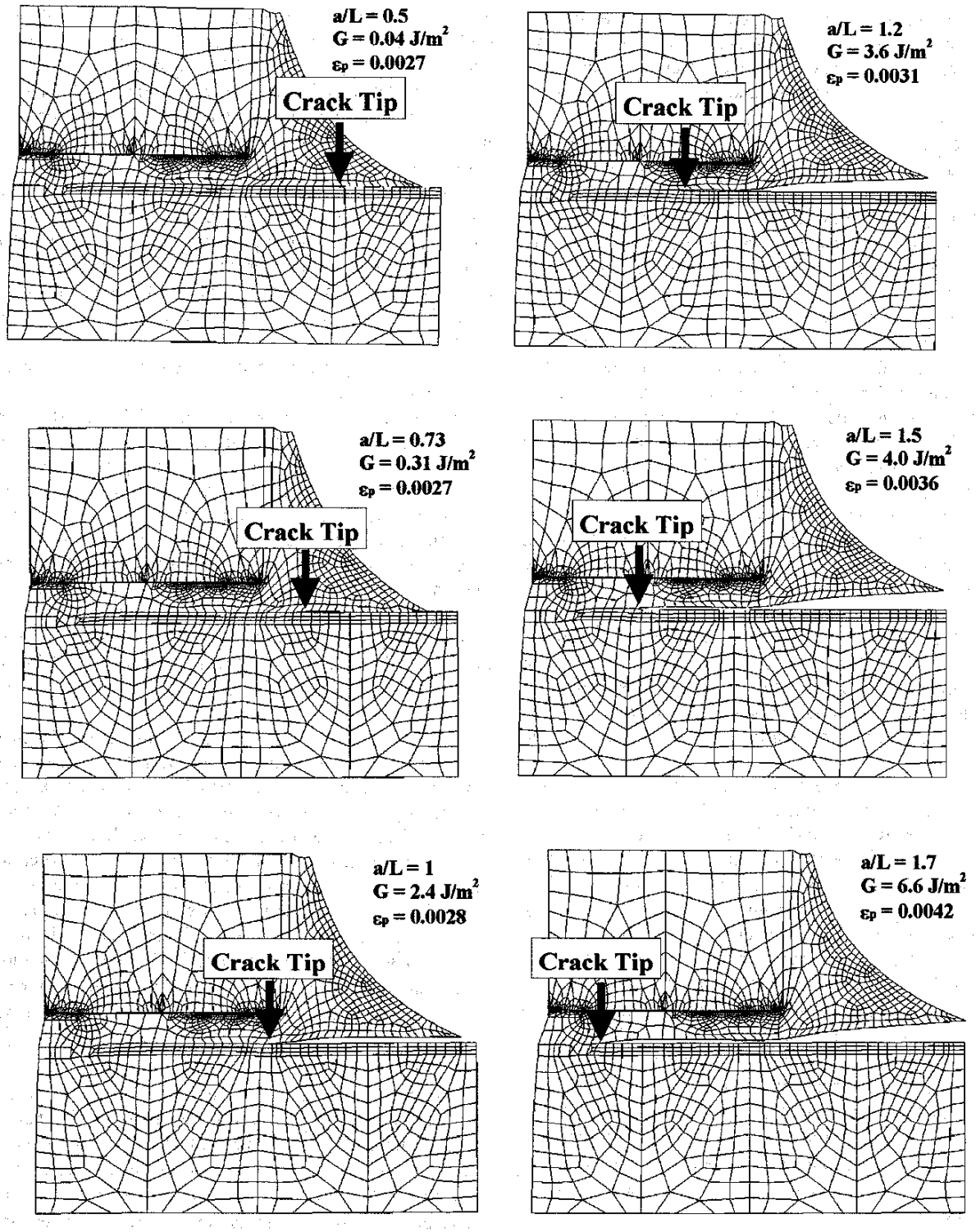


Figure 3: Progressive crack growth along the interface between the underfill encapsulant and the solder mask (a: crack length, L: solder bump pitch, G: strain energy release rate, $\varepsilon_p$: maximum accumulated equivalent plastic strain)

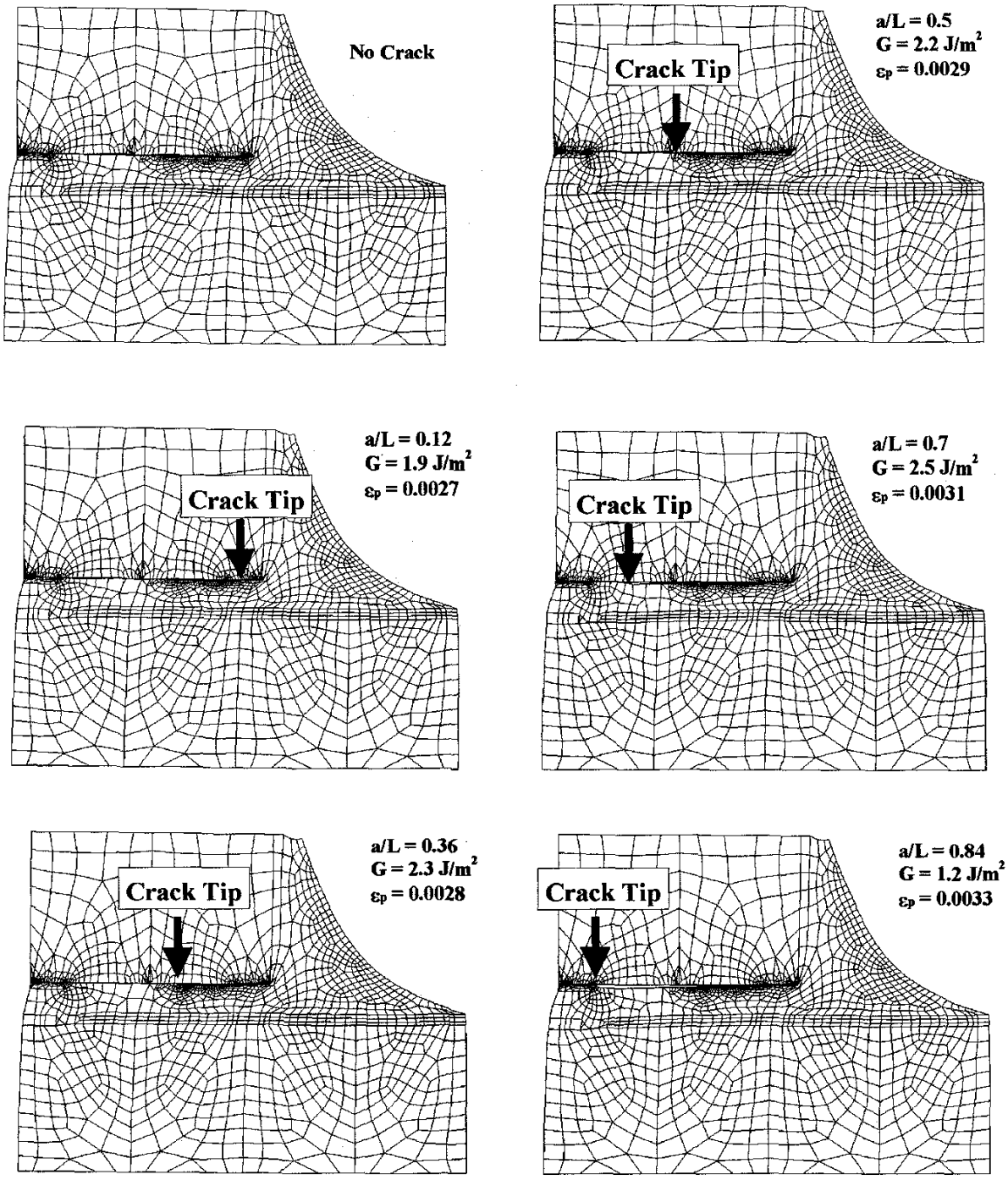


Figure 4: Progressive crack growth along the interface between the underfill encapsulant and the chip passivation (a: crack length, L: solder bump pitch, G: strain energy release rate, $\varepsilon_p$: maximum accumulated equivalent plastic strain)

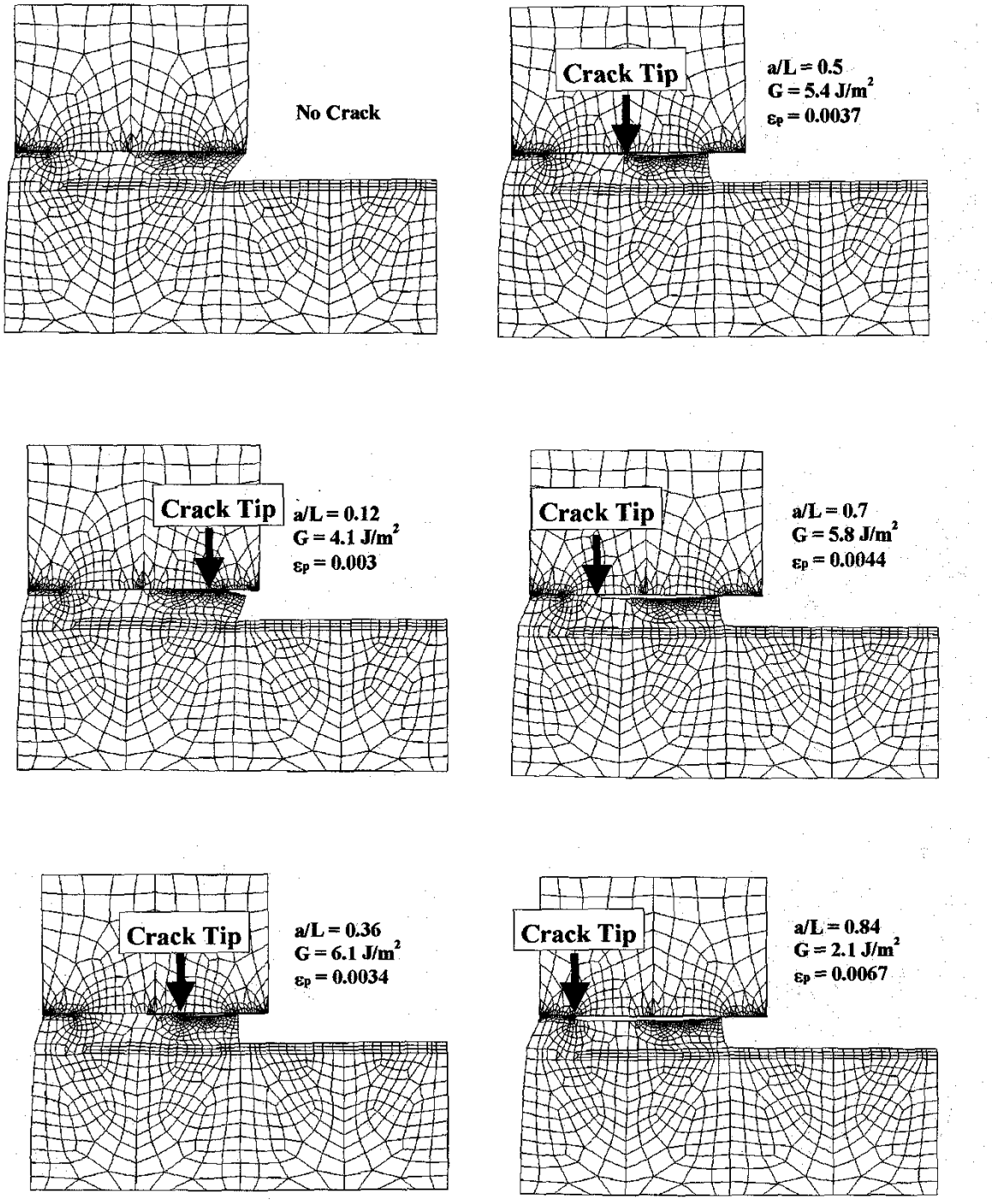


Figure 5: Progressive crack growth along the interface between the underfill encapsulant and the chip passivation (no fillet) (a: crack length, L: solder bump pitch, G: strain energy release rate, $\varepsilon_p$: maximum accumulated equivalent plastic strain)

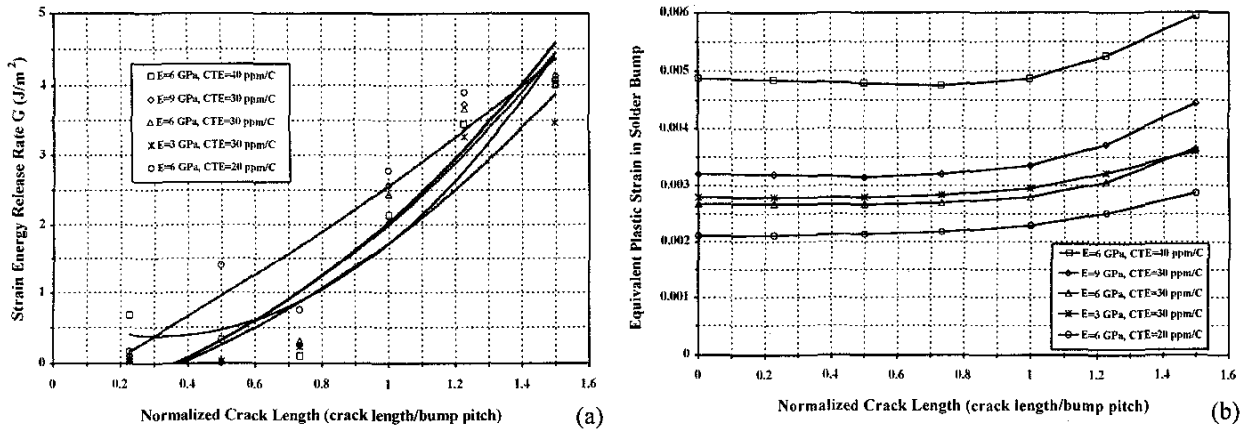


Figure 6: Results of computational analysis with delamination along the interface between the underfill and the solder mask (a) strain energy release rate at the crack tip, (b) maximum accumulated equivalent plastic strain in the solder bump

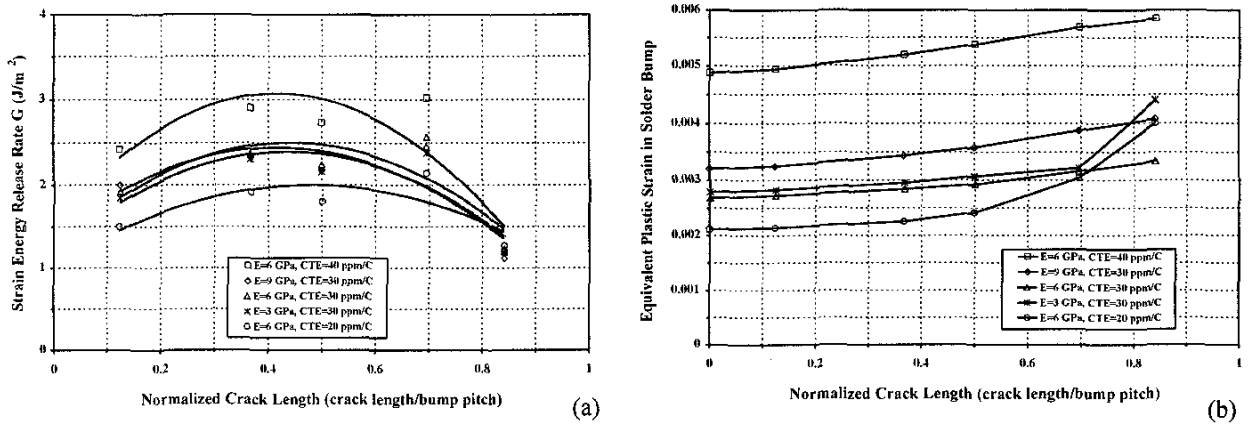


Figure 7: Results of computational analysis with delamination along the interface between the underfill and the passivation (a) strain energy release rate at the crack tip, (b) maximum accumulated equivalent plastic strain in the solder bump

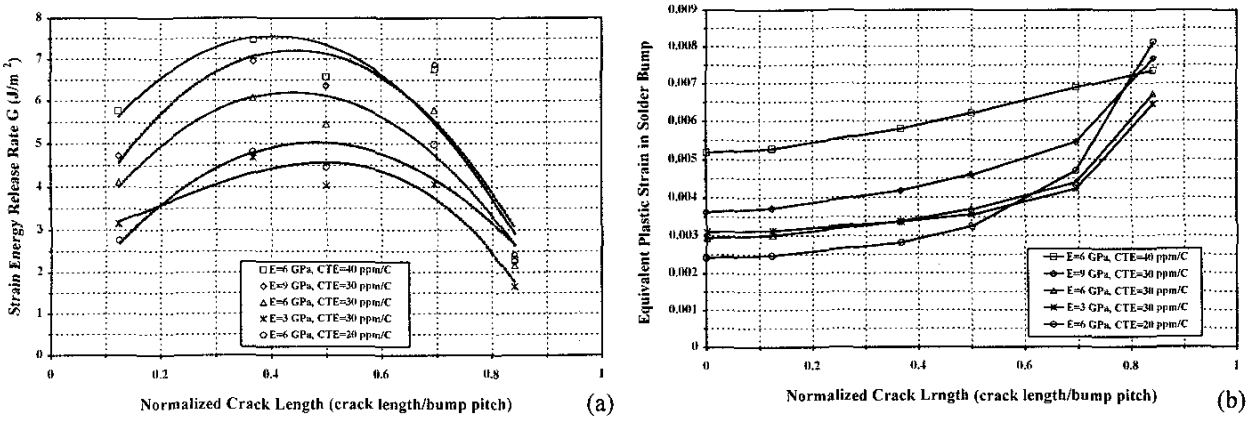


Figure 8: Results of computational analysis with delamination along the interface between the underfill and the passivation (no fillet) (a) strain energy release rate at the crack tip, (b) maximum accumulated equivalent plastic strain in the solder bump

underfill of E = 6 GPa and CTE = 20 ppm/°C. When the CTE of underfill becomes larger, the $\varepsilon_p$ increases. However, due to the filler contents, most underfill materials available nowadays have CTE larger than 20 ppm/°C. Therefore, the next best case with underfill of E = 6 GPa and CTE = 30 ppm/°C should be more practical. On the other hand, for fixed CTE (30 ppm/°C), the $\varepsilon_p$ will be raised if the Young's modulus of underfill increases is larger than 6 GPa in the present study. This is because the encapsulant becomes too stiff. As a result, due to the local thermal expansion/ contraction of underfill material, excessive loading will be exerted on the solder bumps (considering the thermal stress is the product of thermal strain and Young's modulus).

It should be pointed out that, for all cases considered in the present study, the maximum accumulated equivalent plastic strain was less than 1% and the strain energy release rate was relatively small. It seem that, even with the presence of the three types of imperfections under investigation, the solder bumps should be reliable for use at most operating conditions. This is because the chip size in the present analysis was rather small (see Figure 1). Once the chip size becomes larger, because of the increase in the distance from the neutral point (DNP), the solder bump reliability of FCOB assemblies with the aforementioned imperfections may become a critical issue.

Table 3: Results of Shear Tests on the Interface between the Underfill Encapsulant and the PCB Substrate

| # | Area ($mm^2$) | Peak Load ($kg_f$) | Shear Strength (MPa) | Failure Mode |
|---|---|---|---|---|
| 1 | 9.76 | 28.8 | 28.9 | Crack occurs between the solder mask and the BT substrate |
| 2 | 12.1 | 35.8 | 29 | |
| 3 | 11.2 | 36.6 | 32.1 | |
| 4 | 5.62 | 17.7 | 30.9 | |
| 5 | 8.19 | 23.8 | 28.5 | |
| 6 | 7.02 | 15.5 | 21.6 | |
| 7 | 7.41 | 28.5 | 37.6 | |

## 4. Interfacial Shear Strength between Solder Mask and Underfill Encapsulant

In addition to numerical modeling, efforts were made to characterize the interfacial shear strengths between the underfill and the solder mask and between the underfill and the chip passivation, respectively. These quantities were obtained from mechanical shear tests and microscopic inspection. Figure 9 shows the test set-up for determining the adhesion strength between the solder mask on the PCB and underfill encapsulant. The specimen consists of a PCB, a flat hard subject (2 mm x 1.5 mm x 2.4 mm), and an underfill encapsulant and is subjected to a shear force (as shown in Figure 9) in a Royce Instrument. The PCB is 0.5 mm thick and made of BT (bismaleimide triazine) resin with a thin layer (< 25.4 μm) of solder mask. The underfill material is made of epoxy resin with 60% silica filler content and the filler size is less than 10 μm. The Young's modulus and CTE of the underfill material are 6 GPa and 30 ppm/°C, respectively.

The assembly process of the specimen is very simple. Place a drop of the underfill material on top of the BT PCB and then place the hard subject on top of the underfill. A light-weight metal is placed on top to the hard subject to ensure good contact and a standoff height of 50 μm. The whole configuration is put into a curing oven (150 °C) for 30 minutes.

The test results are shown in Table 3 and the typical failure mechanism (the top surface of the BT PCB) is shown in Figure 10. It can be seen that the epoxy-glass of the BT PCB is obvious. That means the adhesion strength between the underfill and solder mask is stronger than that between the solder mask and epoxy-glass. In Table 3, the values in the Area-column represent the areas where solder mask got peeled off. The values in the Shear Strength-column represent the adhesion strength between the solder mask and epoxy-glass and their average value is about 30 MPa. Therefore, the shear strength between the underfill and solder mask should be much larger than 30MPa.

Table 4: Results of Shear Tests on the Interface between the Underfill Encapsulant and the Chip Passivation

| # | Area ($mm^2$) | Peak Load ($kg_f$) | Shear Strength (MPa) | Failure Mode |
|---|---|---|---|---|
| 1 | 3.82 | 20.4 | 52.2 | Crack occurs in the underfill & between the underfill and the chip passivation ($Si_3N_4$) |
| 2 | 3.88 | 20.6 | 52.2 | |
| 3 | 5.14 | 26.2 | 50.0 | |

## 5. Interfacial Shear Strength between Chip Passivation and Underfill Encapsulant

A mechanical shear test as shown in Figure 11 was performed to characterize the interfacial shear strength between the passivation and the underfill materials. It is noted that the materials, assembly process and the dimensions of the specimen are exactly the same as those in the last case except that the PCB is replaced by a very large silicon chip. The silicon chip is 0.5 mm thick with a very thin layer (1 μm) of $Si_3N_4$ passivation. During the test, the peak loading force ($P_u$) at failure was recorded. After the test, optical microscope was used to inspect the failed surfaces at both sides. Table 4 shows the test results and Figure 12 shows the failure mechanism (the top surface of the chip with the passivation intact and some underfill encapsulant). In this case, the underfill encapsulant is broken into pieces, some remain on the flat hard subject and some remain on the passivation of the chip.

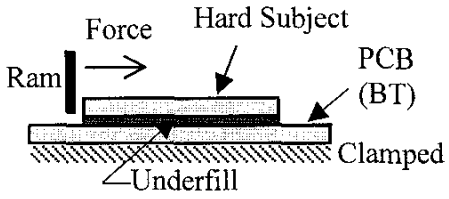


Figure 9: Test set-up for shear strength between solder mask and underfill encapsulant

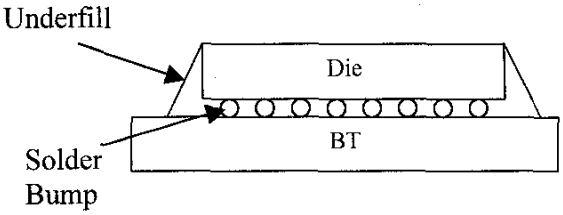


Figure 13: Cross-section view of FCOB assembly

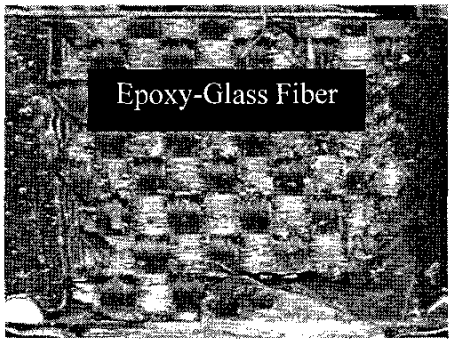


Figure 10: Fracture surface on BT after shear test

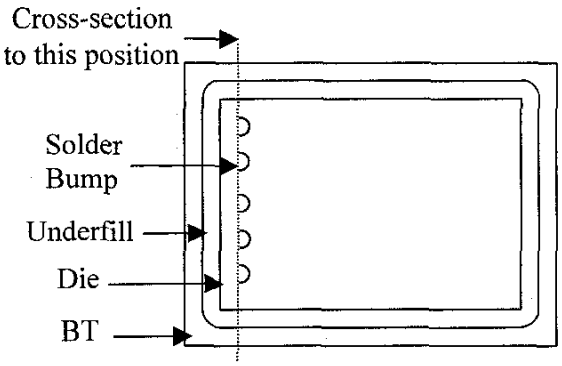


Figure 14 : Position of cross-section (top view)

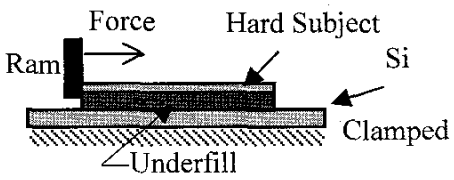


Figure 11: Test set-up for shear strength between passivation and underfill encapsulant

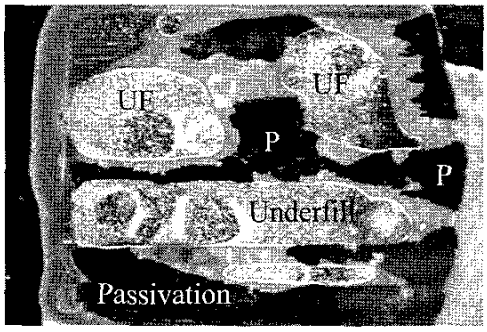


Figure 12: Fracture surface on Si after shear test

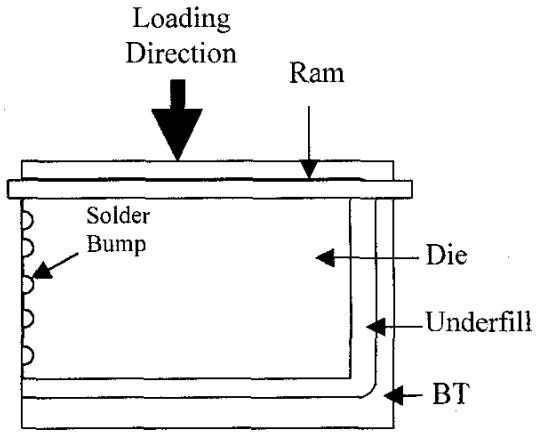


Figure 15: Shear loading direction of the specimen

Thus, the adhesion between the silicon and passivation is stronger than that between the passivation and the underfill encapsulant. The values in the Area-column represent the areas of underfill.

For the calculation of interfacial shear strength, the failure surface is divided into three regions, namely, the separation between the passivation and the underfill, the separation between the underfill and the upper substrate, and voids. Obviously the voids could not take any loading during the test. Therefore, the peak failure load was contributed by the shear strengths of aforementioned two interfaces. It is extremely difficult to identify each interfacial strength with a precise close-form solution. However, an engineering estimation with a simplified model ($P_u = \tau_1 * A_1 + \tau_2 * A_2$) is feasible. Where $\tau_1$ and $\tau_2$ are the shear strength of passivation-underfill interface and underfill-top substrate interface, respectively. Also, $A_1$ and $A_2$ are the areas corresponding to $\tau_1$ and $\tau_2$, respectively. $P_u$ could be recorded during the test; $A_1$ and $A_2$ could be measured after the test. With two independent tests, $\tau_1$ and $\tau_2$ could be calculated ($\tau_1 \approx 52$ MPa). In fact, a third test was conducted to check the validity of this model. The results turned out to be consistent ($\tau_1 \approx 50$ MPa). Therefore, the shear strength between silicon and passivation should be larger than 50 MPa.

## 6. Load–Displacement Response of a Solder Bumped FCOB Assembly

A flip chip assembly (chip size=4.7x4.2 mm) including chip, underfill, and BT substrate was cross-sectioned to the center of a row of solder bumps. The cross-section was fine-polished for subsequent inspection. This procedure is necessary in order to clearly observe the crack path after the shear test. Figures 13 and 14 illustrate the side view and the top view, respectively, of a cross-sectioned flip chip assembly. The Royce Instruments Model 550 was used to perform the mechanical shear tests. The shear wedge was placed very close to the substrate and against one edge of the solder bumped flip chip with underfill on the BT substrate. The speed of the shear wedge was 0.001 inches/second. Figure 15 shows the shear direction from the top view after cross-sectioning to the specimen. The experiment must be conducted with great care. Otherwise, the cross-sectioned sample will be shattered dramatically. A typical load-displacement curve of solder bumped flip chip on board with underfill is presented in Figure 16. One minor and one major reduction in loading force are observed along the curve. The former should correspond to the crack initiation in the fillet of the underfill while the latter the crack propagation causing the final failure of the whole assembly.

Figure 17(a) is a cross-section view of overall flip chip assembly after the shear test. The CTE of the underfill is 28.6 ppm/°C. To highlight the local failure mechanism, four zoomed pictures from the cross-section are made, see Figures 17(b) to 17(e). Figure 17(b) shows that the crack was initiated from underfill outside the package, and then propagated through the interface between $Si_3N_4$ passivation and underfill. Figure 17(c) reveals that the crack continued to extend through the interface between $Si_3N_4$ passivation and underfill, then passed through a void of the underfill, and caused copper pad to be peeled off. Figure 17(d) indicates that the crack broke the solder bumps. Figure 17(e) shows that the crack cut through underfill and went all the way along the interface between underfill and solder mask.

From these observations of the shear test, failure may appear at (i) interface between $Si_3N_4$ passivation and underfill, (ii) interface between copper pad and BT, (iii) solder bumps, and (iv) interface between underfill and solder mask.

## 7. Summary and Recommendations

The effects of underfill material properties on the solder bump reliability of FCOB assembly with imperfect underfill encapsulants were studied in this paper. Three different types of underfill imperfections and five combinations of underfill material properties were considered. A finite element modeling together with fracture mechanics approach was employed for computational analysis. The strain energy release rate at the crack tip and the maximum accumulated equivalent plastic strain in the solder bumps of all cases were evaluated as indices of reliability.

It was found that the underfill encapsulant without fillets is the most damaging manufacturing defect. Also, the delamination between the underfill and the solder mask on the substrate is unfavorable. On the other hand, the separation between the chip and the underfill (but with encapsulant fillet) seems to result in less threat than the other two types of imperfections. However, all strain energy release rates and maximum accumulated equivalent plastic strains obtained in the present study were relatively small. This is mainly because the chip size under investigation was rather small. Further study using larger chip sizes should be conducted to re-confirm the concerned effects on solder bump reliability of FCOB. Also, efforts should be made in the future to pursue three-dimensional modeling for more accurate stress analysis.

The general scope of the present study was to achieve a better understanding of the thermo-mechanical behavior of FCOB assemblies with imperfect underfill encapsulants. In addition to computational modeling, an attempt was made in the present study to characterize the shear strength at the underfill-solder mask interface and the underfill-chip passivation interface. A number of mechanical shear tests were performed and some preliminary testing results were obtained. It was found that the shear strength between the underfill and the solder mask should be much larger than 30MPa and the shear strength between the silicon and the passivation is no less than 50 MPa. These data should be valuable for the future stress analysis on the FCOB assembly. Also, such kind of efforts should be encouraged and will continue. After all, without interfacial strength and toughness, the computational modeling can only serve for the purpose of qualitative study. Therefore, in order to achieve the predictive capability by numerical simulation, further research activities in material characterization are essential and required.

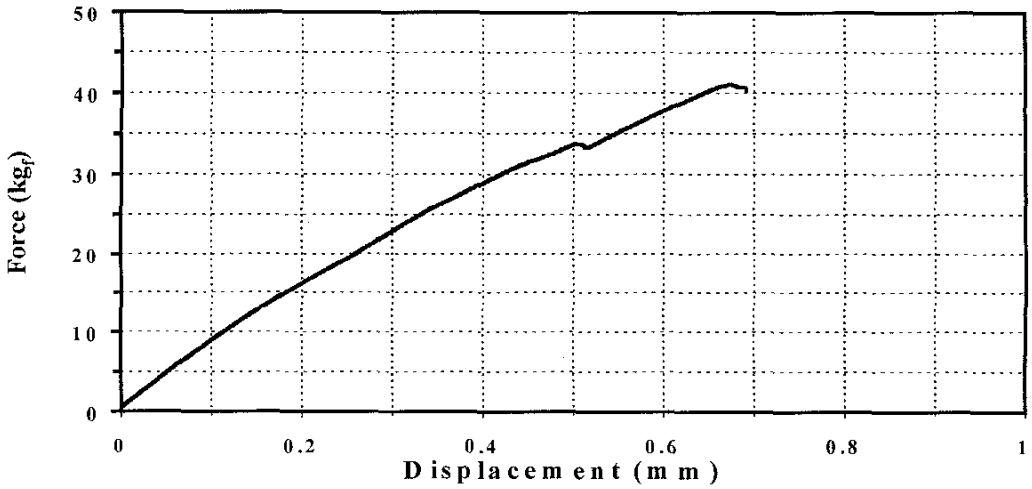


Figure 16: Load-displacement curve from the mechanical shear of a flip chip assembly

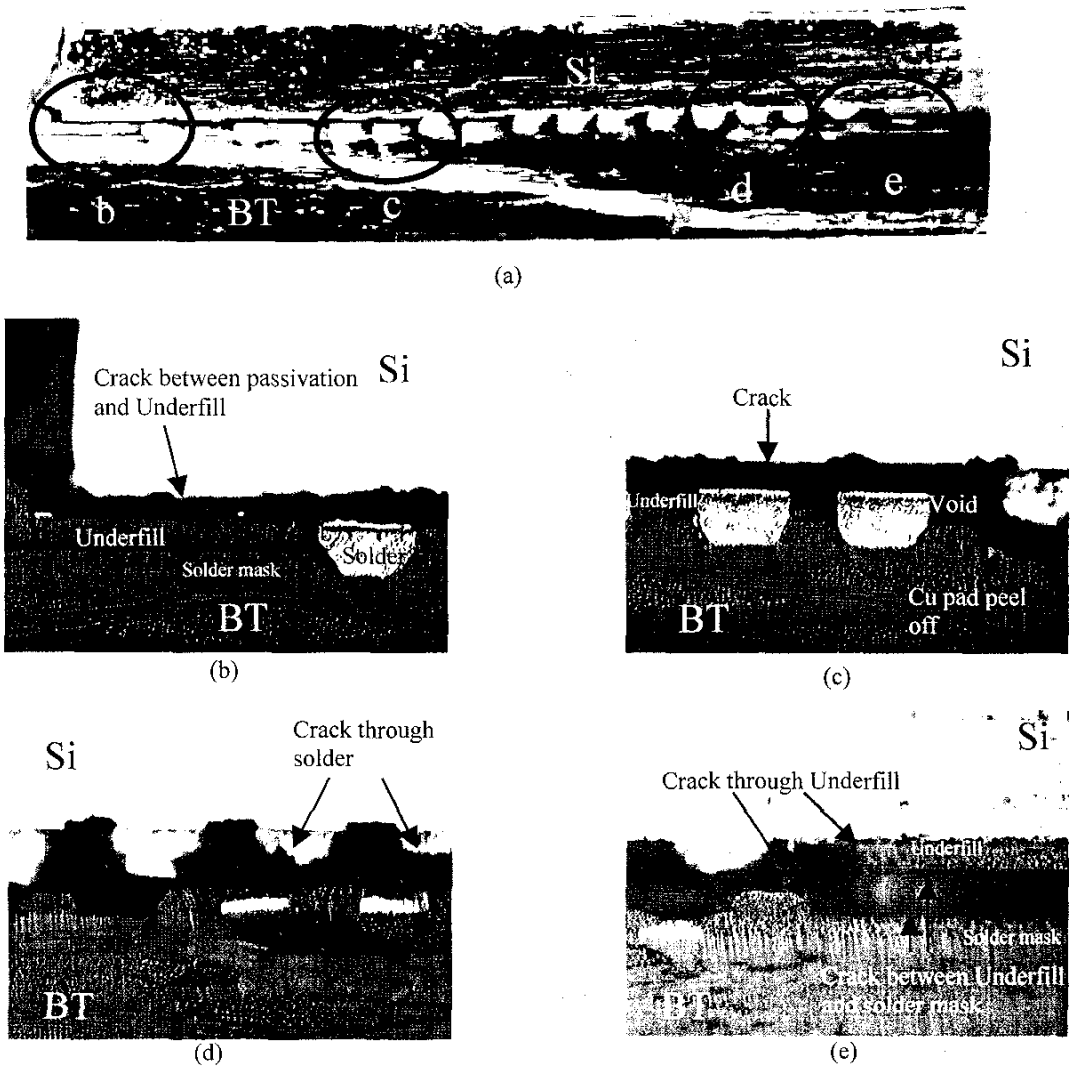


Figure 17: (a) Overall view of the cross-section after the shear test; (b) to (e) close-up pictures showing local failure mechanisms

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