DANIEL NG

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Education

University of British Columbia **Expected Graduation: May 2029**
BASc in Electrical Engineering (Co-op, available May 2026) *Vancouver, BC*

Professional Experience

Norsat International Inc. **June 2025 – August 2025**
Hardware Intern *Richmond, BC*

- Performed gain, power saturation, 1-dB compression point, spurious emissions, third-order intermodulation distortion, and noise figure characterization on 20+ 40W, 50W, and 80W Ku-Band Block-Up Converters using Keysight PNA-X Vector Network Analyzers, Signal Analyzers, RF jigs, and multimeters to verify hardware parameters.
- Performed RF power calibration by sweeping DAC codes controlling voltage-variable attenuation and PA bias while monitoring output power and stability.
- Assembled and reworked BUCs and LNBs at the PCB and PCBA levels, performing fine-pitch SMT and THT soldering and microscopic inspection on MMIC chips to meet production quality standards.
- Verified and troubleshooted SSPA boards by conducting continuity tests and cross-referencing schematics to identify and rectify DC bias instability and RF path discontinuities, ensuring 100% yield for high-power MMIC stages.

Formula UBC Racing Design Team (Electrical & Firmware)

Project Lead: Timing Gates | *Embedded C, Schematic Capture, Altium Designer* **September 2025 – Present**

- **Leading the full design cycle** of a 650 nm laser gate receiver in Altium, mentoring two MechE students to develop optomechanical shrouding coupled with a **custom analog front end** (photodiode+transimpedance amplifier (TIA)+Schmitt trigger) to maintain 3.3V CMOS logic and 2.4GHz communication between master-slave ESP32-S3 MCUs.
- Characterizing baseline photodiode thermal dark current and TIA voltage noise to calibrate an adjustable hysteresis threshold via potentiometer, targeting a 20dB Signal-to-Noise Ratio (SNR) and a Bit Error Rate (BER) of $< 10^{-7}$ to ensure reliable high-speed data integrity between MCUs.

Projects

RISC-V Single Cycle CPU | *SystemVerilog, Altera DE10-Lite FPGA, Quartus Prime, Questa* **December 2025**

- Architected and implemented a Single-cycle RISC-V processor in SystemVerilog with memory-mapped I/O onto Altera's DE10-Lite with functioning register file, ALU, and control unit, supporting a 10-instruction subset of the RISC-V ISA.
- Wrote a self-checking non-synthesizable testbench with assertion-based verification to verify instruction-level correctness and used Questa to trace signals through the synchronous timing datapath.

Tron Legacy Cycle Game | *C, Altera DE10-Lite FPGA, MMIO, VGA* **November 2025**

- **Developed a custom VGA graphics driver** using Memory-Mapped I/O (MMIO) to manage frame buffers, rendering dynamic light traces and a gameplay perimeter while maintaining high-speed pixel updates.
- Implemented an interrupt-driven control scheme for human input, utilizing an Interrupt Service Routine (ISR) to handle asynchronous pushbutton events, significantly reducing input latency compared to traditional polling.
- Engineered an autonomous robot opponent with predictive collision logic; the algorithm performs real-time memory reads of the VGA buffer to scan for obstacles and dynamically updates movement vectors to avoid crashes.

Autonomous Retrieval System | *SolidWorks, Arduino, C/C++, Hand tools* **January 2025**

- **Developed embedded C firmware** for Arduino Uno to interface the HC-SR04 sensor and SG90 servo motor, enabling **successful** fully autonomous target detection and retrieval given a 15V power constraint.

Technical Skills

Digital Design/HDL/Low-Level: SystemVerilog, RISC-V Assembly, FSM Implementation & Design
Embedded Systems: ESP32 and 8051-family MCUs, C Embedded Firmware Development, RV32 Bare Metal Programming, MMIO
Design Tools: Quartus Prime, Questa/ModelSim, Altium Designer, CPUlator
Hardware & Lab: VNA, Signal Analyzer, PCB Design and Rework, SMT/THT Soldering, Oscilloscope, Multimeter