Ministry of Science and Technology 109th Academic Year College Student Research Program

Research and Implementation of an 8-bit Signed Carry-Saved Adder

Final Report

Academic Unit： National Sun Yat-Sen University Department of Electrical and Computer Engineering

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Abstract

This research investigates the relevant techniques for an 8-bit signed carry-saved adder, with a focus on achieving low power consumption, high-speed operation, and compact layout area. Virtuoso, Calibre, and PEX simulation software were used for post-layout simulations, and the design was implemented using UMC 0.18 μm process technology. The chip layout without PAD resulted in an area of 201.641 x 160.863 μm², and with PAD, the area increased to 1047 x 1047 μm². The average current consumption of the circuit is 0.965 mA, with a power consumption of 1.737 mW.

Keywords: Carry-saved adder, signed adder

Preface

The 20th century witnessed rapid advancements in Integrated Circuits (ICs), and with the development of complex semiconductor and communication technologies, Very-Large-Scale Integration (VLSI) has found extensive applications in everyday life. The design of VLSI circuits is typically automated using Electronic Design Automation (EDA), becoming a significant research area in the field of electrical engineering.

In various arithmetic operations widely applied in VLSI, the adder serves as a fundamental building block. Subtraction can be accomplished by complementing the input and utilizing addition, multiplication is a series of additions, and division involves a series of subtractions. Adder designs are modular, with an 8-bit adder composed of 1-bit adders, and 1-bit adders constructed using logic gates [1].

Adders serve as the foundational building blocks for processors requiring extensive computational processing. Improving the performance of adders is crucial in optimizing the overall design of integrated circuits. Consequently, various types of adders have been designed, including Ripple Carry Adder (RCA), Carry Lookahead Adder (CLA), Carry Select Adder (CSA), Carry Skip Adder (CSK), and Carry Save Adder (CSA), all aimed at enhancing adder performance.

The logical concept of adders in circuits can be explained using half adders and full adders: a half adder utilizes one AND gate and one XOR gate to perform the addition of bit values of the addend and augend, along with the carry input, resulting in the sum and carry outputs. To account for the carry input, a full adder is composed of two half adders, with input values of addend, augend, and carry input, yielding sum and carry outputs.

By cascading n full adders, an n-bit adder is formed, known as the Ripple Carry Adder (RCA). It has the advantage of having a simple structure and circuit, but its computational complexity scales linearly with the number of bits, n. To optimize the adder and enhance computational speed, n full adders can be operated in parallel. The Carry Lookahead Adder, Carry Select Adder, and Carry Skip Adder belong to this category [2].

A signed adder can handle both positive and negative numbers by designating the highest-order bit in an n-bit representation as the sign bit (0 for positive, 1 for negative). The remaining n-1 bits represent the numerical magnitude. The encoding methods for negative values include sign-and-magnitude, 1's complement, and 2's complement. Due to the sign bit's inability to directly participate in arithmetic operations, separate hardware circuitry is required to determine the sign for sign-and-magnitude arithmetic, making it less suitable for logic-based adders. Although the 2's complement representation simplifies circuit design, it introduces end-round-carry during addition, necessitating two adder operations, resulting in increased delay and area in the adder's structure. To reduce critical path delay, parallel prefix computation can be employed to perform simultaneous carry generation and propagation. By applying the multiply-

accumulate (MAC) structure commonly used in floating-point arithmetic, area can be saved and critical path delay reduced [3-5].

Comparing the four types of adders in terms of calculation speed and chip area complexity, the Carry Select Adder (CSA) exhibits the fastest speed, followed by the Carry Skip Adder (CSK), then the Carry Lookahead Adder (CLA), and the Ripple Carry Adder (RCA) as the slowest. However, the Ripple Carry Adder has the lowest chip area complexity, followed by the Carry Skip Adder, then the Carry Select Adder, and the Carry Lookahead Adder as the most complex [6].

To reduce the delay caused by a large number of carry propagations and enhance circuit calculation speed, researchers have proposed the Carry Save Adder (CSA). In the CSA, the carry is treated as the output of the addition rather than being propagated as an intermediate value to the higher bits. This approach minimizes carry propagations to only the final step, avoiding the need for n carry propagations. The CSA's characteristic is a constant delay, independent of the number of bits, n. Consequently, for 8-bit and 16-bit adders, the CSA's calculation speed is faster than the Carry Lookahead Adder (CLA). However, for 64-bit and 128-bit adders, the CSA's calculation speed becomes slower than the Carry Lookahead Adder [7,8].

The CSA reduces the delay of input bits to higher-order full adders, thus reducing the overall delay of the full adder's sum and carry outputs. However, it comes with the drawback of a larger layout area. On the other hand, the signed adder experiences increased delay and larger layout area due to redundant sign representations. Considering these aspects, this study aims to achieve low power consumption, high-speed operation, and a compact layout area. To this end, an 8-bit signed Carry Save Adder is proposed, and its performance is evaluated through post-layout simulations using Virtuoso, Calibre, and PEX software, implemented with UMC 0.18 μm process technology.

Design of an 8-bit Signed Carry-Saved Adder

The Carry Save Adder (CSA) is a three-input adder used for three-input addition. It first adds the corresponding bits of the inputs, generating the sum and carry values for each bit. By storing the carry values and adding them to the sum of the next bit, the entire addition process is completed. Taking Figure 1 as an example, with inputs X[7:0], Y[7:0], and Z[7:0], the adder first performs addition on the corresponding bits of X, Y, and Z (i.e., X[0] + Y[0] + Z[0], X[1] + Y[1] + Z[1], and so on), generating the sum (sum[7:0]) and carry values (C[7:0]) for each bit. Next, it adds the previous carry value (C) with the sum of the next bit (sum) (i.e., C[0] + sum[1], C[1] + sum[2], C[2] + sum[3], and so on), ultimately obtaining the result of the three-input addition.

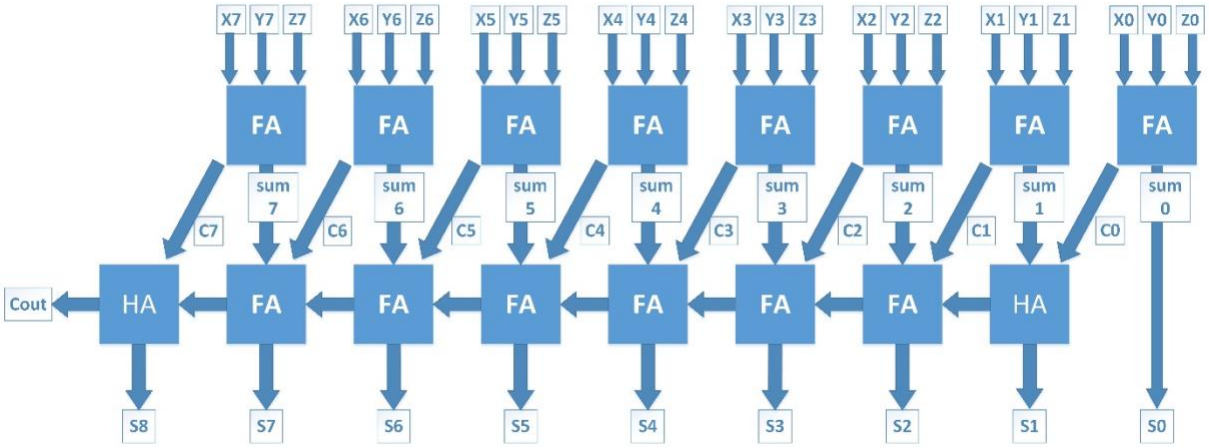


Figure 1: Principle of Carry-Saved Adder

This research employs UMC 0.18 μm process technology for the design and implementation. The layout design and simulation of the 8-bit signed Carry Save Adder are conducted using the Full Custom Flow (as shown in Figure 2), comprising the following main steps:

1. Circuit Simulation: Using Virtuoso, the circuit schematic is created, including NMOS, PMOS, input and output pins (I/O Pins), capacitors, voltage sources (VDD and GND), signal sources, etc. For larger circuits, symbols or blocks are used to represent detailed sub-circuits. The circuit is then simulated using HSPICE. HSPICE simulation detects transient and transient errors, ensuring the proper functioning of the circuit, and allows immediate corrections to circuit issues.

2. Layout Design: Virtuoso is utilized for the layout design, aligning the structure of the circuit schematic to configure the metal wires to achieve an equivalent layout. Design Rule Check (DRC) and Layout Versus Schematic (LVS) tests are performed. DRC tests geometric relationships between layers in the layout to ensure compliance with chip manufacturing rules. LVS compares the layout to the circuit schematic to verify the correct placement of components and interconnections.

3. Layout Simulation: Post-extraction (PEX) converts the layout into a netlist, incorporating signal sources and simulation parameters. The layout is then simulated using HSPICE simulator. HSPICE simulation allows for pre-simulation of the three critical parameters affecting chip performance—process (P), system voltage (V), and temperature (T)—to anticipate potential outcomes and enhance chip reliability.

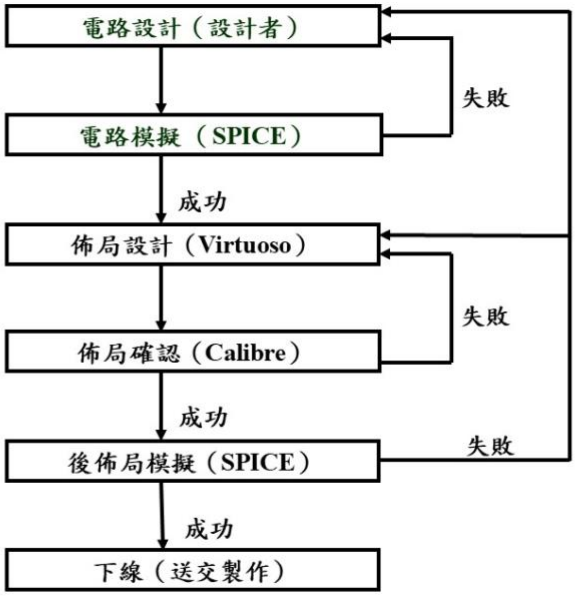


Figure 2: Customized Full Flow Chart [9]

The design architecture of the 8-bit signed Carry Save Adder in this research (as shown in Figure 3 for the conceptual architecture and Figure 4 for the circuit architecture) consists of components such as 2's complement, MUX, DeMUX, Decoder, DFF (D flip-flop), Carry Save Adder, and Buffer.

As depicted in Figure 3, the numerical input is 8 bits long, where the first 7 bits INPUT[6:0] represent the pure numerical value, and the 8th bit INPUT[7] indicates the sign, with 1 representing negative and 0 representing positive (the numerical input range is from -127 to +127). The output range is between -381 and +381, thus employing a 10-bit two's complement representation for the output value.

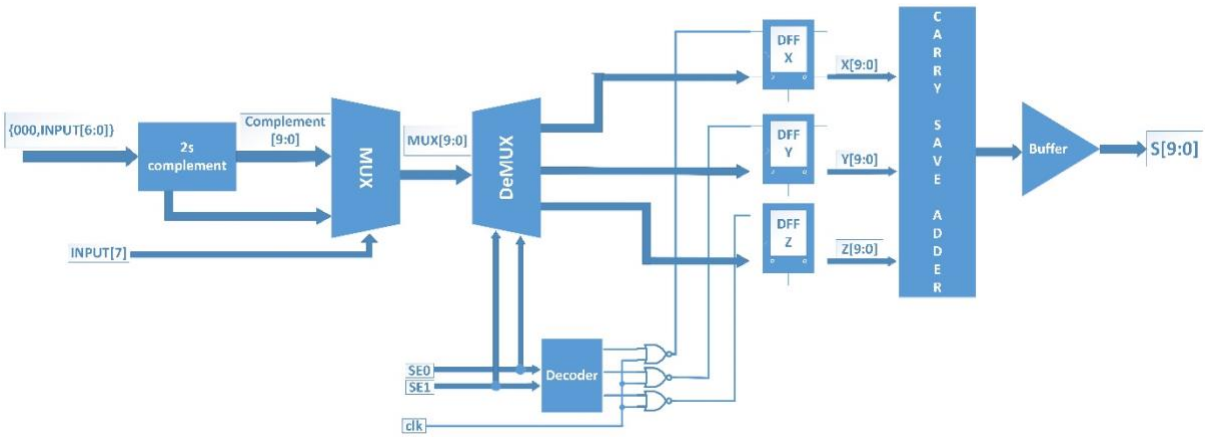


Figure 3: Architecture of the 8-bit Signed Carry-Saved Adder

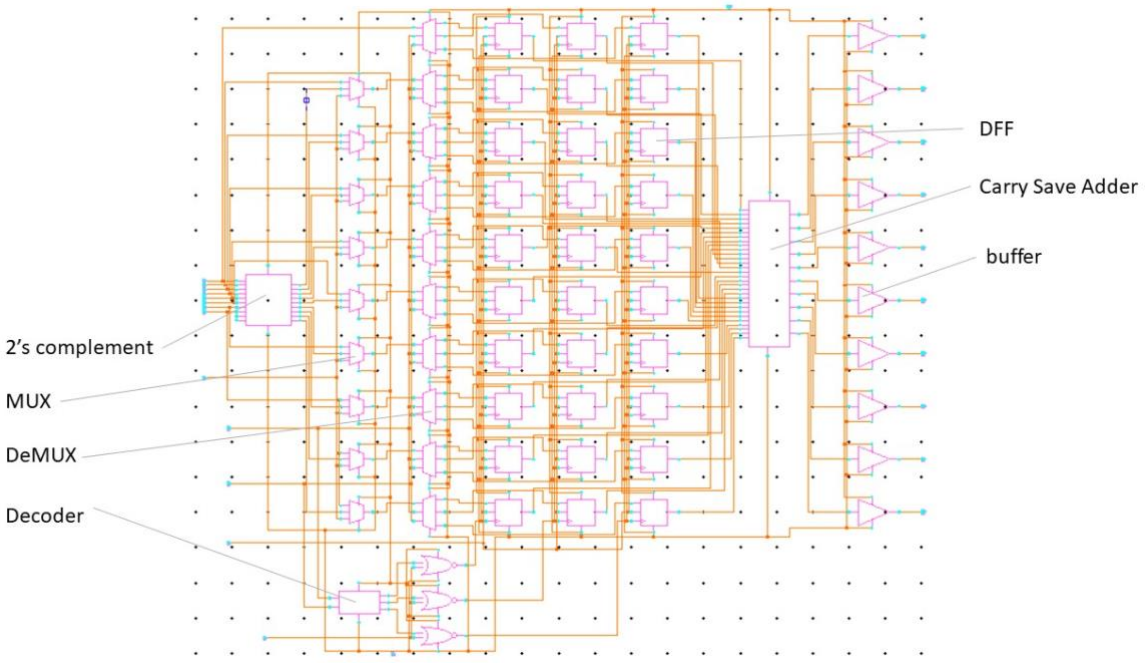


Figure 4: Circuit Diagram of the 8-bit Signed Carry-Saved Adder

In this architecture, since the output is represented in 10-bit two's complement format, the input numerical values are first converted into the 10-bit two's complement representation before performing the Carry Save Adder operation. The input consists of two parts: a 1-bit sign INPUT[7] (indicating positive or negative) and a 7-bit pure numerical value INPUT[6:0]. To represent the numerical value in 10-bit format, the 7-bit numerical value INPUT[6:0] is extended with three leading zeros to form a 10-bit value {000, INPUT[6:0]}, which is then subjected to 2's complement operation.

The sign bit INPUT[7] serves as a control bit for the MUX, which selects either the initial input value or the 2's complement value. If INPUT[7] is 1 (indicating a positive sign), the MUX selects the initial input value. If INPUT[7] is 0 (indicating a negative sign), the MUX selects the value obtained after 2's complement operation.

Next, the control bits SE1 and SE0 are used to write the 10-bit value (from the previous stage) into three sets of D flip-flops X, Y, and Z through the DeMUX. When SE1 = 0 and SE0 = 0, the DeMUX stores the value into D flip-flop X[9:0]. When SE1 = 0 and SE0 = 1, the DeMUX stores the value into D flip-flop Y[9:0]. When SE1 = 1 and SE0 = 0, the DeMUX stores the value into D flip-flop Z[9:0]. When SE1 = 1 and SE0 = 1, no storage operation is performed.

The timing of the D flip-flops is also controlled by SE1 and SE0. The Decoder is designed to output 0 for the corresponding control bits (i.e., when SE1 = 0 and SE0 = 0, Decoder outputs out0 = 0, and the rest out1, out2, and out3 are 1). Therefore, when SE1 = 0 and SE0 = 0, out0 generates 0, which, when passed through a NOR logic gate with the external clk, produces a clock signal with a phase opposite to the external clk. This controlled clock signal is used to control the storage operation in D flip-flop X. When SE1 and SE0 are different from 0, out0 generates 1, which, when passed through a NOR logic gate with the external clk, results in a constant value of 0. In this case, D flip-flop X will not store any external value due to the absence of a clock signal.

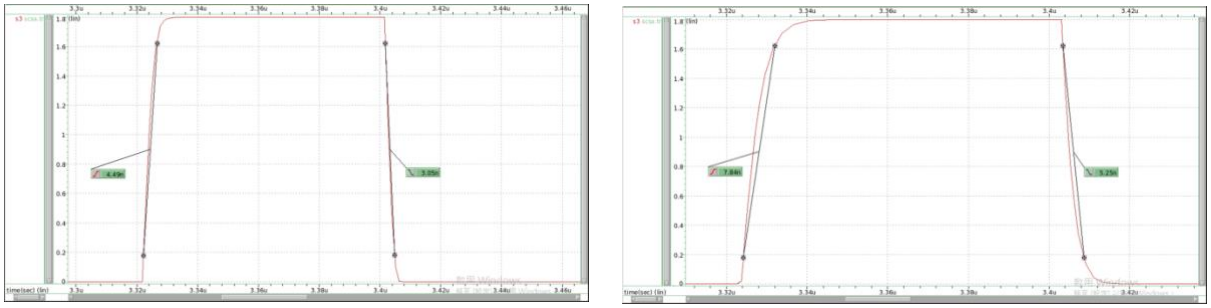
Finally, the Carry Save Adder takes D flip-flops X[9:0], Y[9:0], and Z[9:0] as inputs, calculates the result, and passes it through a Buffer, obtaining the final output S[9:0].

Simulation Results and Analysis

In this research, the layout simulation results were conducted using Virtuoso, Calibre, and PEX software. The circuit was fabricated at Taiwan Semiconductor Research Institute (TSRI) under the chip number U18-109C-E0040, using the UMC 0.18 μm process and employing the SB32 package.

Due to the three fabrication runs per year for the U18 process at TSRI (February, July, and October), this research submitted the design for fabrication in October 2020. The chip fabrication process takes about five months, and the chips are expected to be returned around March 2021. As a result, there is not enough time for this research to conduct chip measurements. Therefore, the analysis in this research is based on the simulated circuit results.

In the study, the output was connected to a 20 pF capacitive load (as shown in Figure 5), and the pre-simulated rise time was measured to be 4.49 ns, and the fall time was 3.05 ns. On the other hand, the post-simulated rise time was found to be 7.84 ns, and the fall time was 5.25 ns.



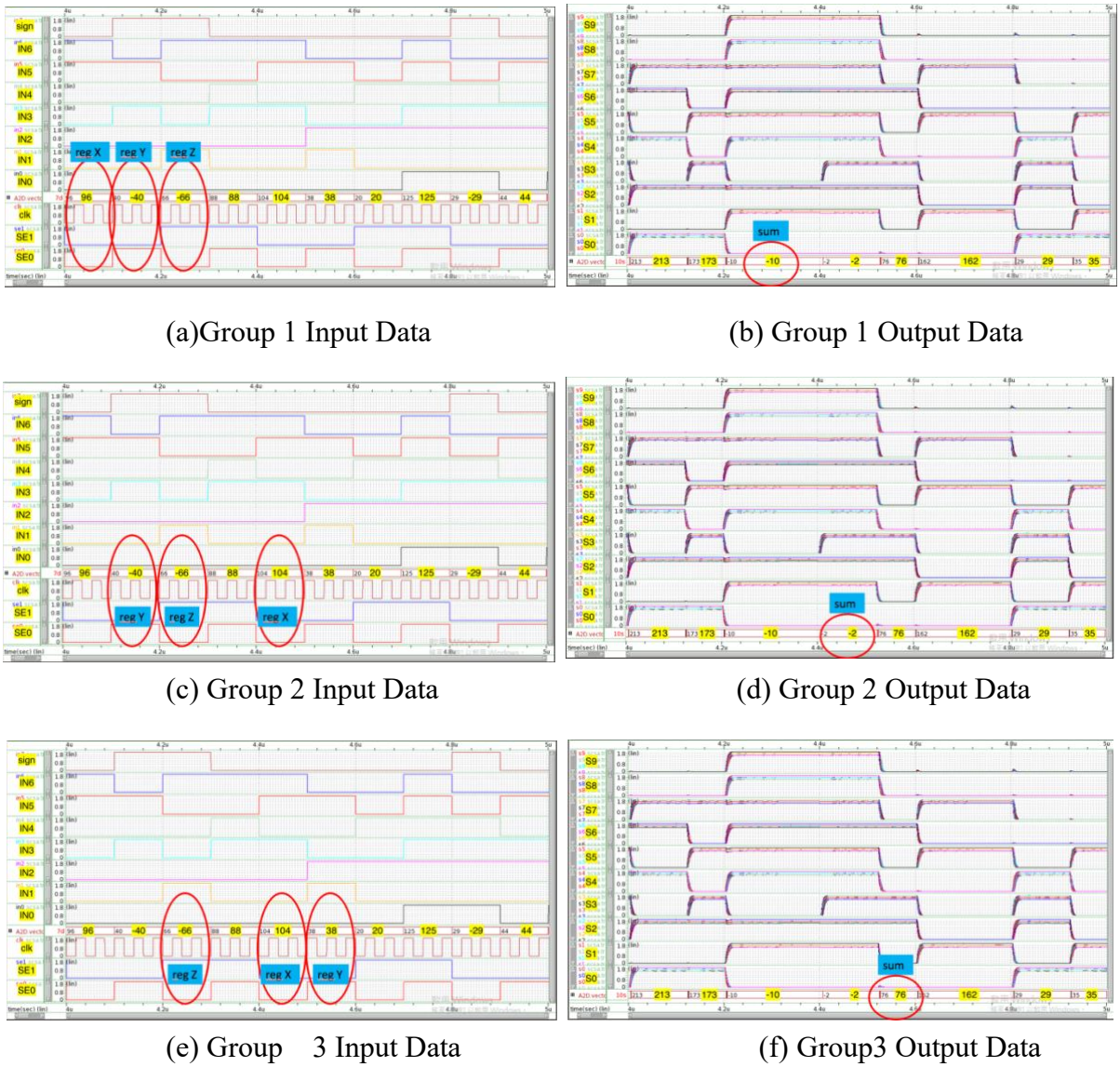
(a)pre-sim (b)post-sim

Figure 5: Rise and Fall Times for Pre-simulation and Post-simulation

The circuit functionality simulation is conducted using the clock signal "clk," with {sign, IN[6:0]} as the input. SE1 and SE0 are used as control signals, and their combination varies over the cycle. When (SE1, SE0) = (0,0), the input value is stored in register X; when (SE1, SE0) = (0,1), the input value is stored in register Y; when (SE1, SE0) = (1,0), the input value is stored in register Z; when (SE1, SE0) = (1,1), no storage operation is performed. The output S[9:0] represents the sum of the values in registers X, Y, and Z.

Figure 6 shows the results of three sets of tests performed on the 8-bit sign-extended carry-save adder with the layout and post-layout simulation, considering the process variation (TT, FF, SS, FS, SF), temperature variation (0 oC, 25 oC, 100 oC), and voltage variation (1.8 V ± 10%). In Figure 6(a), the input is 96, and (SE1, SE0) = (0,0), so 96 is stored in reg X. The input is -40, and (SE1, SE0) = (0,1), so -40 is stored in reg Y. The input is -66, and (SE1, SE0) = (1,0), so -66 is stored in reg Z. Therefore, the output is 96 + (-40) + (-66) = -10 [Figure 6(b)]. In Figure 6(c), when the input is 88, (SE1, SE0) = (1,1), so 88 is not stored in any

register. When the input is 104, (SE1, SE0) = (0,0), so reg X is updated to store 104, while the values in reg Y and reg Z remain unchanged. Thus, the output is 104 + (-40) + (-66) = -2 [Figure 6(d)]. In Figure 6(e), the input is 38, and (SE1, SE0) = (0,1), so reg Y is updated to store 38, while the values in reg X and reg Z remain unchanged. Therefore, the output is 104 + 38 + (-66) = 76 [Figure 6(f)].



(a)Group 1 Input Data (b) Group 1 Output Data

(c) Group 2 Input Data (d) Group 2 Output Data

(e) Group 3 Input Data (f) Group3 Output Data

Figure 6: Three Sets of Test Results with PAD after Layout

Based on the results of the three sets of random addition tests, it can be concluded that the designed 8-bit signed carry-save adder can accurately perform the addition function.

The chip layout is shown in Figures 7 and 8. The area of the circuit without the PAD is 201.641 x 160.863 μm², and with the PAD, the area becomes 1047 x 1047 μm². The average current of the circuit is 0.965 mA, and the power consumption is 1.737 mW.

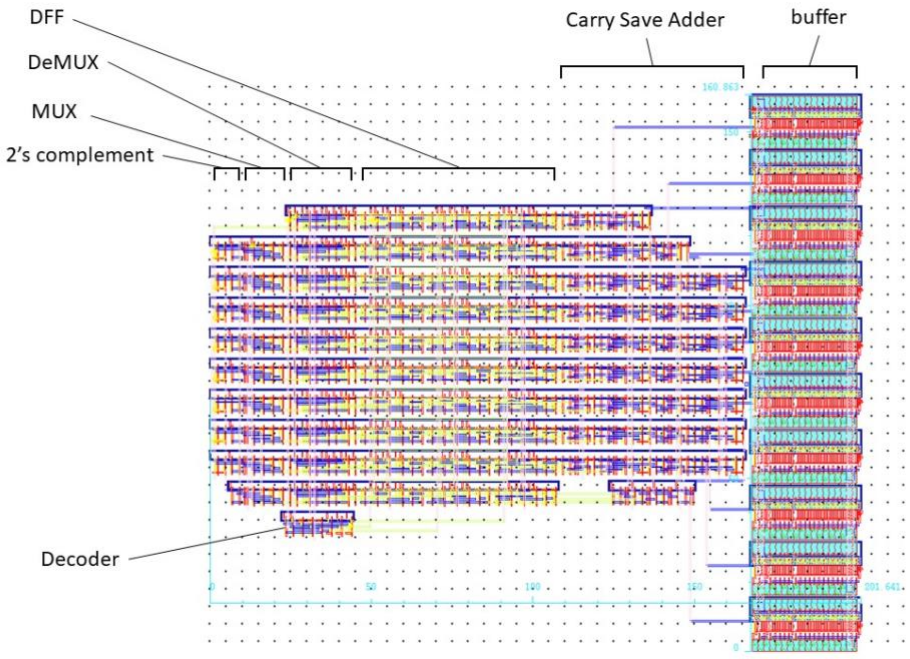


Figure 7: Chip Layout without PAD

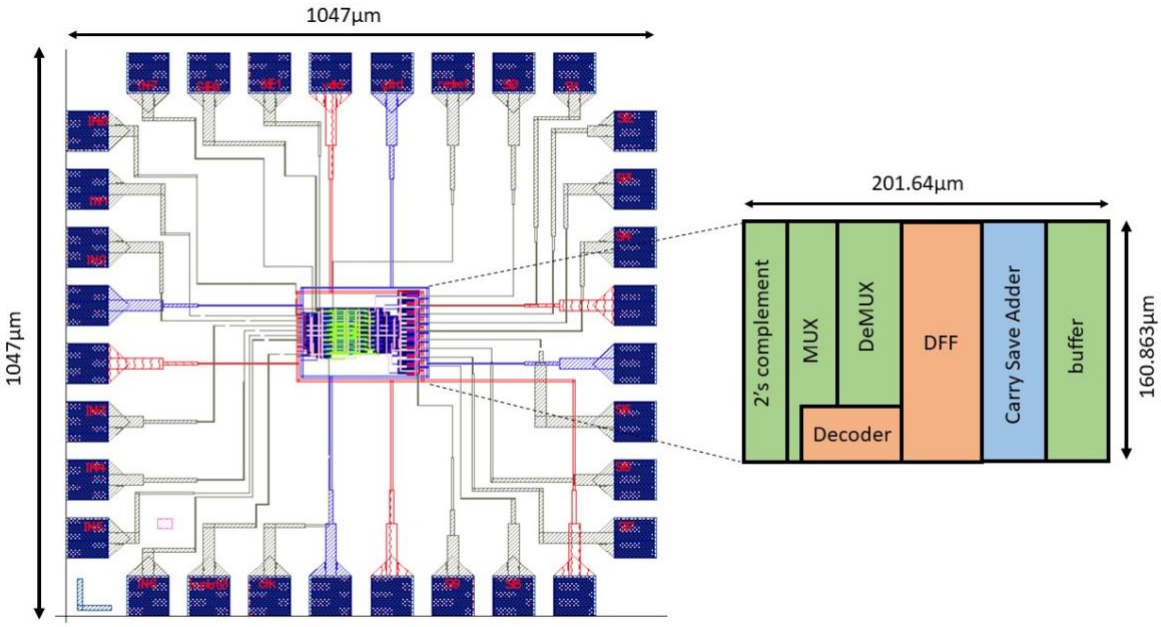


Figure 8: Chip Layout with PAD

Based on the measured data, the performance of the proposed carry-save adder in this research is compared with three other types of adders: Ripple Carry Adder (RCA), Carry Lookahead Adder (CLA), and Carry Select Adder (CSLA). The comparison results are summarized in Table 1, and the performance of the adders is analyzed using a custom-defined Figure of Merit (FOM).

From the analysis results, it can be observed that the Ripple Carry Adder (RCA) has the smallest delay, and the proposed carry-save adder in this research comes in second. In terms of average power consumption, the Carry Lookahead Adder (CLA) has the lowest power, and the proposed carry-save adder is the second lowest. Overall, the proposed carry-save adder has the highest FOM value among the four adders, indicating better performance compared to the others.

Table 1: Performance Comparison of Adders

	RCA [10]	CLA [11]	CSLA [12]	本研究
年份	2012	1999	2015	2021
製程技術 (nm)	180	600	350	180
操作電壓 (V)	1.8	3	3.3	1.8
電晶體數量	352	105	582	516
延遲 (ns)	1.005	1.28	14.034	1.19
平均功率 (uW)	904	460	808	468
FOM*	0.387	0.178	0.051	0.927

註：*FOM = $\frac{1}{\text{延遲} \times (\frac{\text{平均功率}}{\text{電晶體數量}})}$

Conclusion

In this research, an 8-bit signed carry-save adder was implemented using a full custom software approach. The study followed a rigorous research methodology, including architecture selection, circuit simulation, circuit layout, post-layout simulation, and fabrication. Through extensive testing, the developed adder circuit demonstrated correct functionality for addition operations and proved to be highly valuable for various applications.

Comparing with other types of adders such as Ripple Carry Adder, Carry Lookahead Adder, and Carry Select Adder, the proposed carry-save adder stands out in its ability to simultaneously add three numbers. Unlike other adders that require two additions sequentially, the proposed carry-save adder completes the addition of three numbers in a single operation. As a result, the proposed adder exhibits superior performance in terms of delay and average power consumption, achieving the highest Figure of Merit (FOM) value.

Overall, the study showcases a well-planned and executed research approach, leading to the development of an efficient and versatile carry-save adder with significant practical value.

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