Tutorial 4
Basic Amplifying Stages and Current Mirrors

1 Introduction

Analog circuits are formed by many transistors and passive devices. Identifying what each device is doing maybe challenging if it is not done in a systematic way. In a previous tutorial the analog circuits were separated in two main groups: the signal path and the DC biasing. Making this distinction is of fundamental importance because it helps us to identify what each part of the circuit is doing and define its characteristics. The objective of this tutorial is to give a better understanding of the basic stages that are found in the signal path, in other words, all the circuits that perform signal processing. These stages are the common-source (CS), common-gate (CG) and common-drain (CD) configurations. These stages are the basic building blocks found in more complex circuits and hence a good knowledge about them is fundamental. This tutorial also includes typical current mirror configurations since besides DC biasing they are also found extensively in the signal path.

2 Amplifying Stages

2.1 Common-Source Stage

Open the schematic 'CS_stage'. You will see 2 NMOS CS stage setups as shown in Figure-1. The transistors dimensions are 150 um/0.15 um and have biasing currents of 724.4 uA.

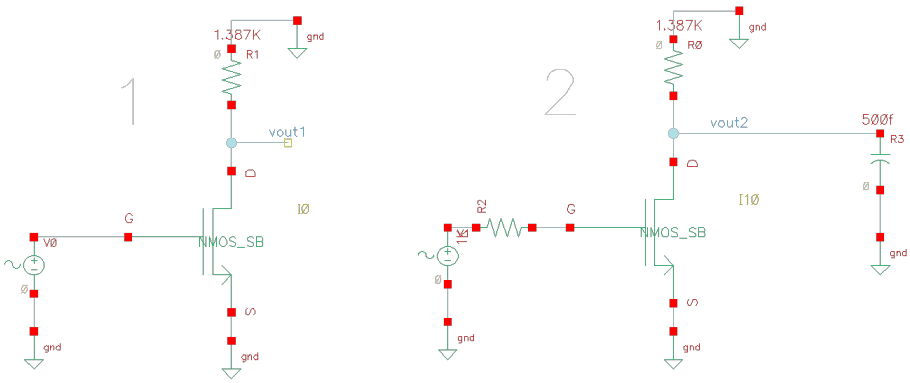

Figure 1: Setups for analysing CS stage

As you might have figured out by now, these transistor dimensions and biasing points were used in the last tutorial. The important biasing points, small signal parameters and figures of merit of this transistor are given in Table-1 for a quick reference.

The DC voltage gain of the CS stage is given by:

$$Av = gm \cdot RL \quad (1)$$

$$\text{where } RL = rds||R1 \quad (2)$$

Let's assume that you want a gain $Av = 10$ (20 dB). Then, for gm =11.85 mS and $rds = 2.156$ kΩ you will need $R1 = 1.387$ kΩ (RL = 843.8 Ω). Now you

VGS	500 mV
VDS	400 mV
IDS	724.4 uA
gm	11.85 mS
rds	2.156 KΩ
Cgs	98.67 fF
Cgd	48.78 fF
Cdb	91.53 fF
f_T	25 GHz
Av_o	25.5

Table 1: Important parameters (W/L=150 um/0.15 um)

will verify if this is correct by simulating the setup of Circuit-1. Launch ADE L and load the state 'Av_BW_noise_1'. Disable the 'noise' analysis from analyses section and 'input referred noise voltage' from the output section. The ADE L window will look similar to the one shown in Figure-2.

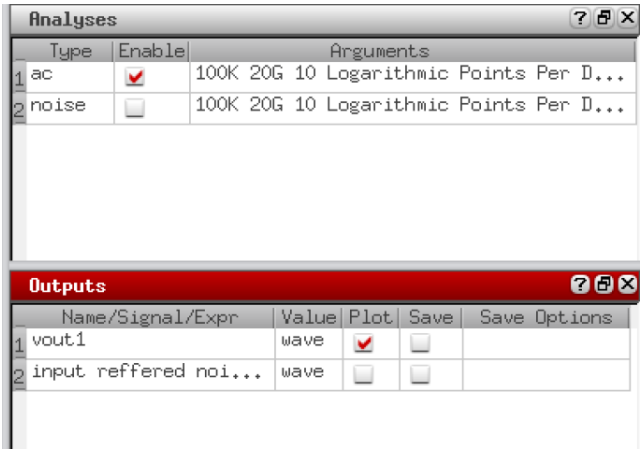

Figure 2: AC analysis form for Circuit-1

The result of the AC analysis of Circuit-1 is shown in Figure-3. The low frequency gain is approximately 20 dB as expected.

The next part will be to evaluate the bandwidth of this CS stage, but in a more realistic environment. A 1 kΩ source resistance (R2) and 500 fF load capacitance were added to the transistor of Circuit-1, as shown in Circuit-2. The bandwidth of the circuit can be estimated by using the open RC constant method. There are two ways of doing this: calculating the RC constant for each capacitor in the circuit or calculating the RC constant for each node in the circuit. Both methods are equivalent and should give the same results. You will use both in this exercise to prove this statement.

2.1.1 First Method [1]

The associated time constants for each capacitor are:

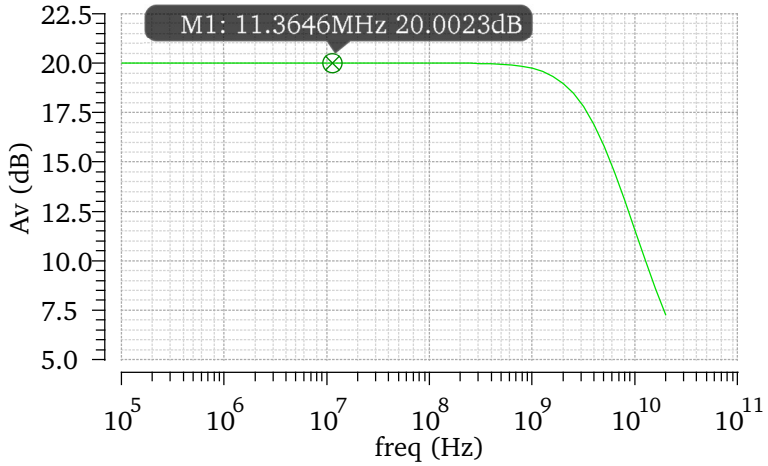

Figure 3: AC gain of Circuit-1

$$\begin{aligned} Tgs &= Cgs \cdot R2 \\ &= 98.67 \text{ ps} \end{aligned} \tag{3}$$

For Tgd, remember that Cgd comes with Miller effect and hence appear magnified by $(1 + gm.RL)$ at the input.

$$\begin{aligned} Tgd &= Cgd \cdot (1 + gm \cdot RL) \cdot R2 + Cgd \cdot RL \\ &= 577.68 \text{ ps} \end{aligned} \tag{4}$$

$$\begin{aligned} Tdb &= (Cdb + 500\text{f}) \cdot RL \\ &= 498.65 \text{ ps} \end{aligned} \tag{5}$$

$$\begin{aligned} BW &\approx \frac{1}{2\pi(Tgs + Tgd + Tdb)} \\ &= 135.4\text{MHz} \end{aligned} \tag{6}$$

2.1.2 Second Method [2]

The circuit has only 2 nodes with RC associated constants: (1) at the gate and (2) at the drain.

At node (1):

$$\begin{aligned} T(1) &= R2 \cdot [Cgs + (1 + gm.RL) \cdot Cgd] \\ &= 635.25 \text{ ps} \end{aligned} \tag{7}$$

At node (2), Cgd multiplied by $[1+1/(gm \cdot RL)] \approx 1$:

$$T(2) = RL \cdot (Cdb + Cgd + 500f) \quad (8)$$
$$= 540.29 \text{ ps}$$
$$BW \approx \frac{1}{2\pi[T(1) + T(2)]} \quad (9)$$
$$= 135.3\text{MHz}$$

Both methods have approximately the same results and it is up to you to decide which one suits your needs. Care must be taken in larger circuits since resistance levels may change for instance when there is source degeneration (you will see these situations the next sections).

Now let's see how good was our previous approximations. In the ADE L window, load the sate 'Av_BW_noise_2'. Disable the 'noise' analysis from analyses section and 'input referred noise voltage' from the output section and run the simulation. The AC simulation results from Circuit-2 are shown in Figure-4 with the marker showing a 3-dB bandwidth of 151.5 MHz, close to our calculated value.

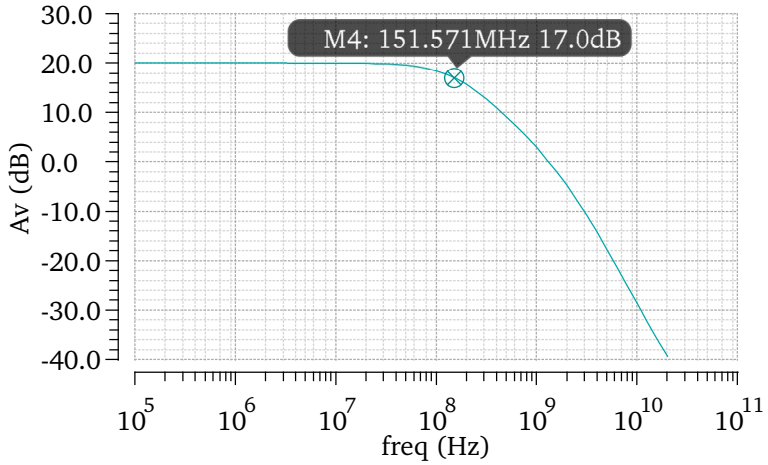

Figure 4: AC gain of Circuit-2

Now you will do the noise analysis of the CS stage in Circuit-1. Load the 'Av_BW_noise_1' state but this time enable the 'noise' analysis from analyses section and 'input referred noise voltage' from the output section and disable the 'ac' analysis and 'Av' output. Moreover, enable the noise contribution from the load resistance ($R1$) in the schematic of Circuit-1. The input referred noise has been plotted from 100 kHz to 20 GHz and is shown in Figure-5.

The effect of R1 on the input referred noise (vn_{in}^2) can be found as:

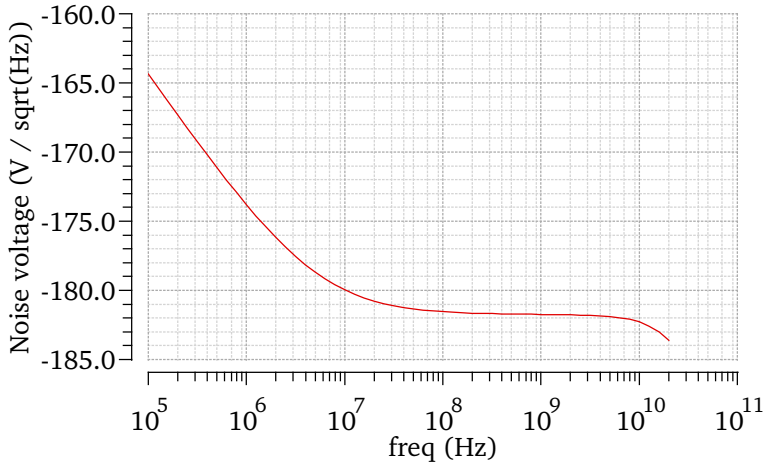

Figure 5: Noise response of Circuit-1

$$vn_{in}^2 = \frac{4\kappa T\gamma}{gm} + \frac{4\kappa TR1}{(gm \cdot RL)^2} \quad (10)$$

$$= \frac{4\kappa T}{gm}\left(\gamma + \frac{R1}{gm(R1||rds)^2}\right) \quad (11)$$

if $rds >> R1$ then: (12)

$$vn_{in}^2 = \frac{4\kappa T}{gm}\left(\gamma + \frac{1}{gm \cdot R1}\right) \quad (13)$$

which means that in order to minimise the contribution of the load, the resistor should be maximised. To check the impact of the load in the noise performance of the system it is possible to make a list of noise contributors once the noise analysis has been performed. In the ADE L window, select 'Results' → 'Print' → 'Noise Summary'. It will open a form. Fill the form as shown in Figure-6 and in 'Filter' select 'Include All Types' and press OK.

The resultant noise summary is shown in Figure-7. The biggest noise contributor is the thermal noise of the transistor. The total noise contribution of the load resistor is 12% and then comes the flicker noise of the transistor. The integrated noise summary at the bottom shows the total integrated noise voltage within the chosen bandwidth (100 kHz - 1 GHz). Try printing the noise summary again, but this time change the upper frequency limit to 1 MHz. Can you figure out why the contribution of flicker noise to total integrated noise increased so drastically?

The CS stage has the best noise performance. As seen in previous tutorial, beside voltage and transconductance this configuration provides very high current and transimpedance gain. Accordingly, the output noise appears attenuated when it is referred to at the input. In conclusion, the CS stage has large amplifying capabilities and therefore very low input referred noise. Let's analyse CG and CD stages and do some comparisons.

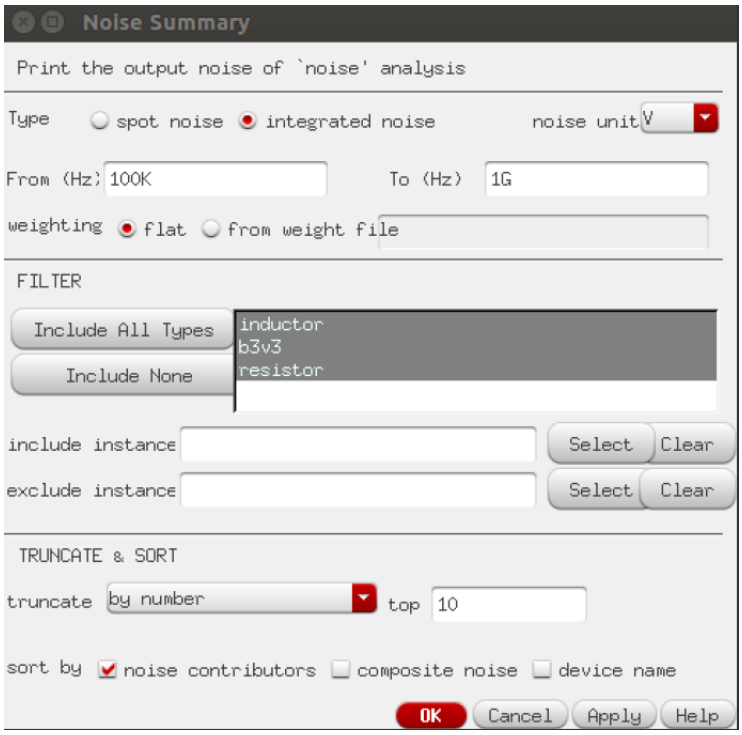

Figure 6: Form for printing noise summary

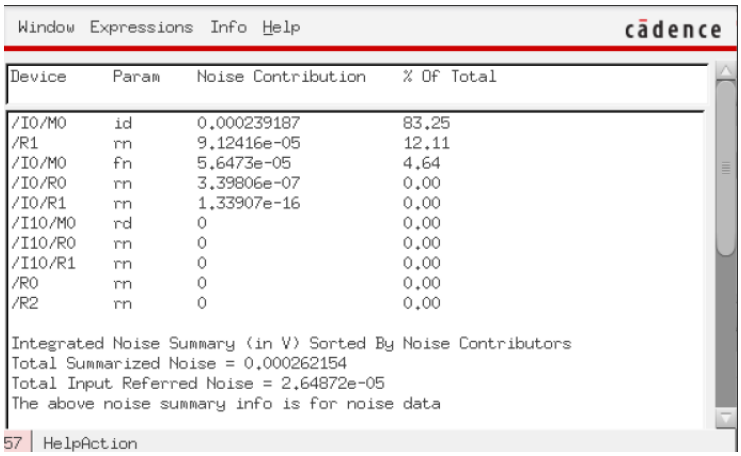

Figure 7: Noise summary of Circuit-1

2.2 Common-Gate Stage

Open file "CG_stage". Like in the previous case, two circuit setups are provided as shown in Figure-8.

Before analysing the gain and bandwidth, let's have some remarks about this configuration. When connected as in Circuit-1, the input current from the AC source is the same as the drain-source current. You can say that the CG

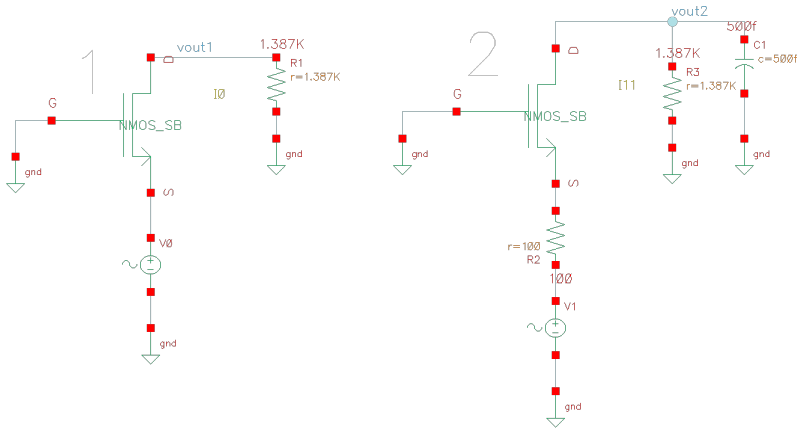

Figure 8: Setups for analysing CG stage

configuration is sinking the current from the source and sending it to the output. The first conclusion is that this topology does not have current gain, i.e. Ai = 1. The CG stage is therefore also known as a current buffer. The voltage gain on the other hand can be calculated as:

$$I_{in} = \frac{V_{in}}{1/gm} = gm \cdot V_{in} \tag{14}$$

$$V_{out} = I_{in} \cdot RL = gm \cdot V_{in} \cdot RL \tag{15}$$

$$Av = \frac{V_{out}}{V_{in}} = gm \cdot RL \tag{16}$$

which is the same as in the CS case. Accordingly, you can set R1 = 1.387 kΩ. To verify this, launch ADE L and load the state 'Av_BW_noise_1'. Disable the noise analysis and the noise output variable and run the simulation. The result of the simulation is shown in Figure-9 and as expected, the gain is around 20 dB.

Now let's calculate the bandwidth of the CG stage of Circuit-2, in which a source resistance and a load capacitance is added to make it more realistic. Notice that in contrast to the CS stage, the addition of R2 has direct impact on the DC gain since now the source current is reduced. Don't fix that now, instead let's find the bandwidth of this circuit. The second method will be used for that purpose. Again, node (1) is defined as the source terminal of the MOS, and node (2), the drain terminal of the MOS.

At node (1) the resistance to ground is equal to (R2 || 1/gm):

$$\begin{aligned} T(1) &= (R2||1/gm) \cdot [Cgs + (1 + Av) \cdot Cdb] \\ &= 18.96\text{ps} \end{aligned} \tag{17}$$

The source degeneration causes an increase in output resistance so that $RL = [(1 + gm \cdot R2) \cdot rds]||R3 = 1.071k\Omega$:

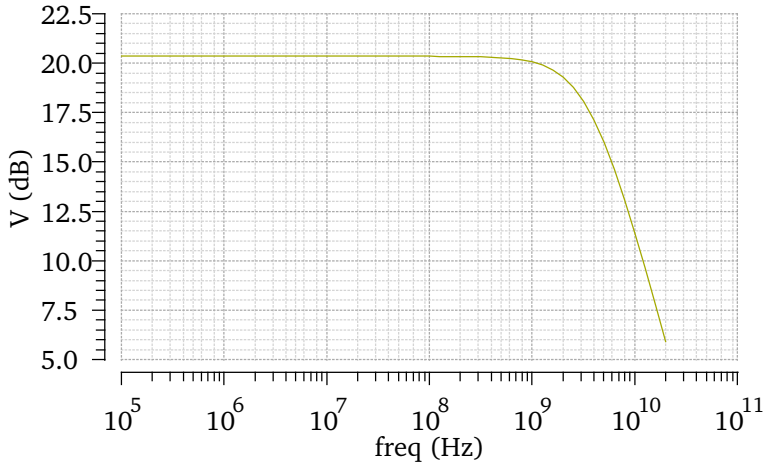

Figure 9: AC gain of Circuit-1

$$\begin{aligned} T(2) &= RL \cdot (Cgd + Cdb + 500f) \\ &= 616\text{ps} \end{aligned} \tag{18}$$

(The term Cdb has a pessimistic value since the source degeneration reduces its value in the same proportion as rds increases)

$$\begin{aligned} BW &\approx \frac{1}{2\pi[T(1) + T(2)]} \\ &= 250.65\text{MHz} \end{aligned} \tag{19}$$

Lets verify this, load the ADE L state 'Av_BW_noise_2'. Disable the noise analysis and the noise output variable and run the simulation. The simulation result in Figure-10 indicate that 3-dB bandwidth is 267.8 MHz, close to our calculated value.

Now, lets do the noise analysis of Circuit-1. Load the ADE L state 'Av_BW_noise_1' but this time disable the ac analysis and ac gain output and enable the noise analysis and the noise output. Run the simulation.

The noise performance is found in Figure-11. If you compare this plot and the one of the CS stage you will conclude that they are the same. However, you know that this circuit does not have current gain and hence something is missing in the analysis since noise currents at the output are not attenuated when referred to the input.

You can visualise this problem if you simulate the input referred noise current. Since Ai = 1, all the noise currents at the output are directly referred to the input. Also, different than in the CS stage, the problem happens at all frequencies, and not only at high-frequencies. You can visualise that by replacing the input voltage source of Circuit-1 with an input current source. Then, changing the 'Input Noise' of 'noise' analysis from voltage to current and selecting the newly placed input current source from the schematic. You can ask the assistant if you have any problems doing that.

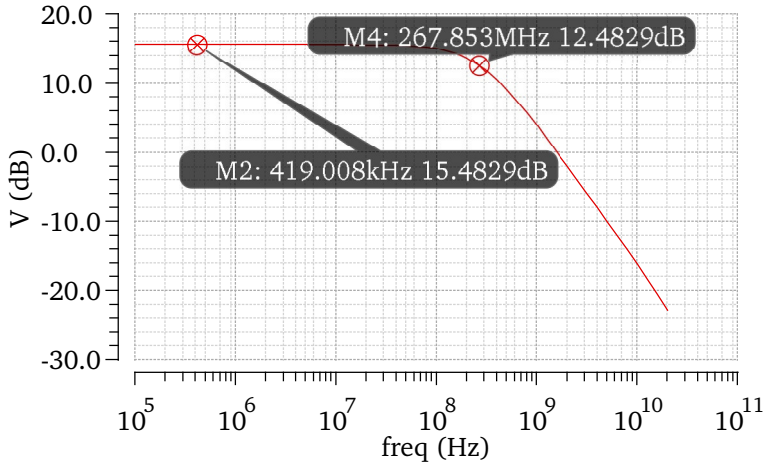

Figure 10: AC gain of Circuit-2

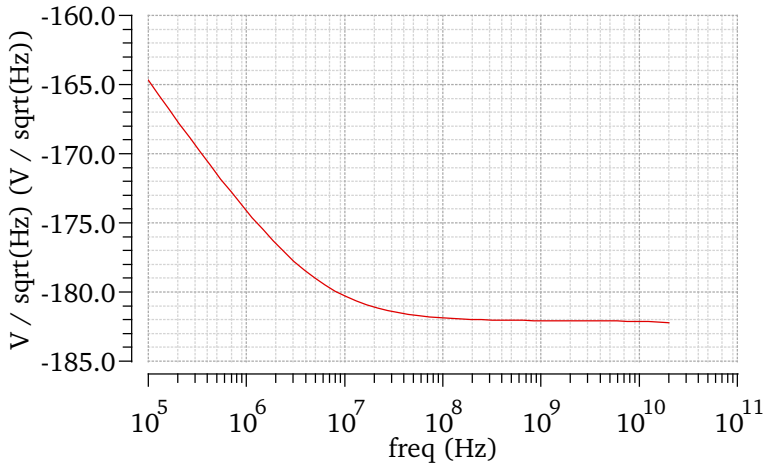

Figure 11: Input referred noise voltage of Circuit-1

Run the simulation again and take a closer look at the input referred noise current as shown in Figure-12.

The noise current from $R1$ ($in^2_{R1} = 4kT/R1$) is directly referred to the input. Therefore large resistors minimise the noise. The input referred noise current has a value of -230 dB which looks like an inoffensive number, but it is not. Two considerations should be done here. First, remember that the total input voltage noise is calculated using:

$$V_{noise} = vn\_real(ZS) + vn + in \cdot ZS \tag{20}$$

Hence, the current contribution can grow very fast depending on the source impedance. Also, many times when processing currents, the circuits loads are current mirrors with diode connected loads. The noise current of these transistors is $4\kappa T\gamma gm$ which in practice can be seen like the noise current of a resistor

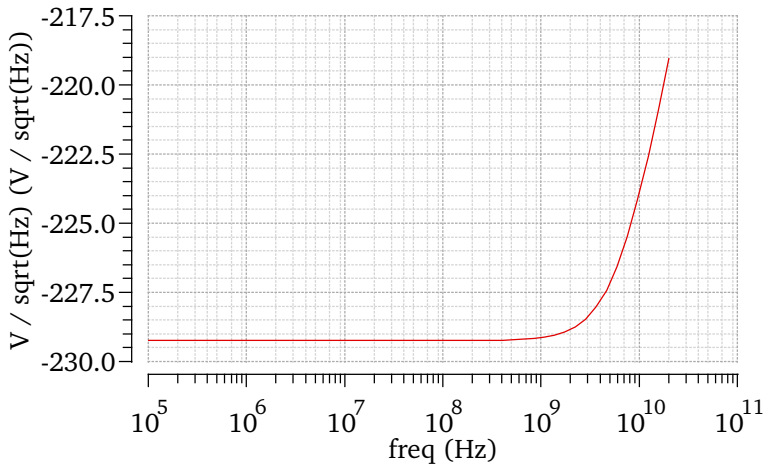

Figure 12: Input referred noise current of Circuit-1

1/gm with an excess of noise γ. Normally 1/gm is a small number which consequently causes a lot of noise.

The list of noise contributors in the integrated noise from 100 KHz - 1 GHz is plotted and is shown in Figure-13.

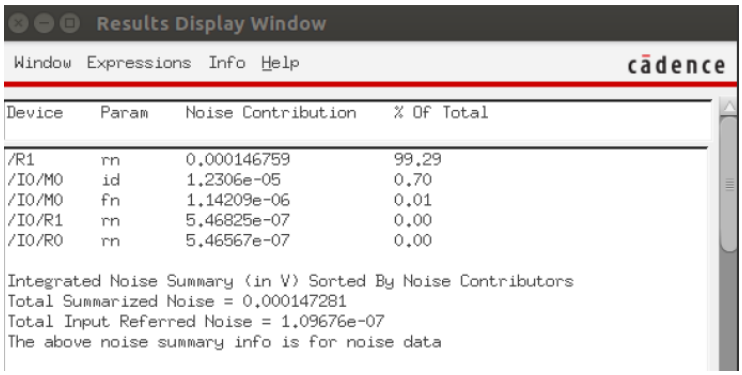

Figure 13: Noise summary of Circuit-1

Almost all the noise is contributed due to $R1$. What happened to the current noise of the transistor?!

2.3 Common-Drain Stage

Open schematic "CD_stage". Like in the previous cases, two circuit setups are provided as shown in Figure-14.

Like in the previous case, let's have some remarks about this configuration. The CD stage can be seen as a source-degenerated configuration. The transconductance in a degenerated stage is:

$$gm_{deg} = \frac{gm}{1 + gm \cdot Rs} \tag{21}$$

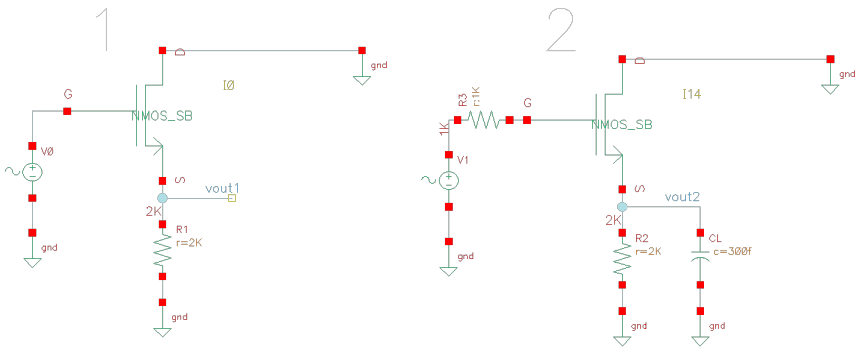

Figure 14: Setups for analysing CD stage

Where Rs is the source degeneration resistance ($R1$ in this case). In the CD stage, $R1 \gg 1/gm$ so that $gm_{deg} \approx 1/Rs$. The value of V_{out} can be found as:

$$V_{out} = V_{in} - gm_{deg} \cdot Rs \approx V_{in} \quad (22)$$

$$A_v = \frac{V_{out}}{V_{in}} = 1 \quad (23)$$

The stage has a voltage gain close to 1 and hence it is called a voltage buffer. Before simulating the gain and bandwidth, a note of caution should be made. The presence of capacitance at the source of the CD stage introduces a zero in the transfer function which may happen at frequencies close to or lower than those of the dominant poles. Consequently, our method of open time constants may not give a correct result for some capacitive combinations. The presence of this zero in the transfer function is also responsible for inductive behaviour and negative resistance at the input impedance. Although this characteristics may be useful and can be exploited in some applications (oscillators for instance), they are more commonly undesirable in circuits with feedback loop since they can compromise the stability.

Now, let us simulate the gain of Circuit-1. Launch ADE L and load the state 'Av_BW_noise_1'. Disable the noise analysis and the noise output variable and run the simulation. The result of the simulation is shown in Figure-15 and as expected, the gain is around -0.67 dB, close to 0 dB.

Now, Circuit-2 will be used to calculate the bandwidth of the circuit in a more realistic environment. Notice that a load capacitor of 300 fF has been added. Let's use the open time constants method to estimate the bandwidth. The input of the circuit is defined as node (1) and the output as node (2).

At node(1):

Note that there is something interesting about Cgs in this configuration. Assuming an ideal voltage gain of 1, the amplitude and phase of the voltage at the terminals of Cgs is the same. Accordingly, no current flows through Cgs. In this context you can conclude that the ideal CD stage cancels completely the Cgs capacitor which brings a big advantage in the achievable bandwidth (This is why the use of CD stages is a popular technique to extend bandwidth in circuits). In practice Cgs is not totally cancelled due to limited degeneration,

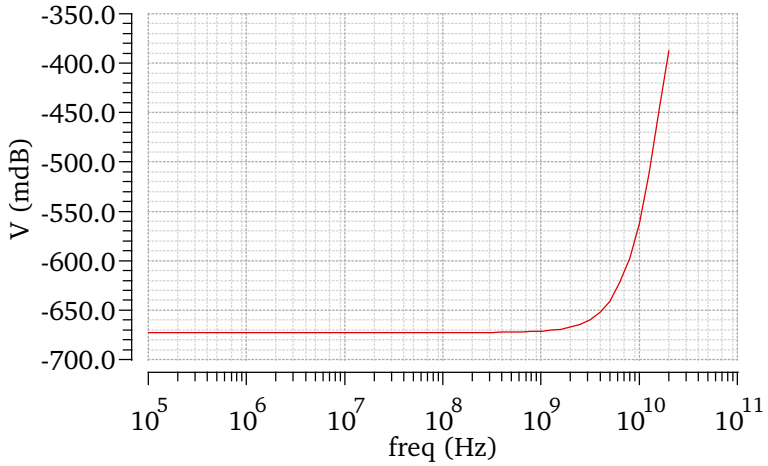

Figure 15: AC gain of Circuit-1

but it is strongly reduced to a value of $Cgs/(1 + gm.R1)$. Accordingly:

$$\begin{aligned} T(1) &= R3\left(Cgd + \frac{Cgs}{1 + gm \cdot R1}\right) \\ &= 56.4 \text{ ps} \end{aligned} \tag{24}$$

At node (2):

$$\begin{aligned} T(2) &= (R2||1/gm)(Cgs + Cdb + 3pfF) \\ &= 25.3 \text{ ps} \end{aligned} \tag{25}$$

and the bandwidth:

$$\begin{aligned} BW &\approx \frac{1}{2\pi[T(1) + T(2)]} \\ &= 1.94 \text{ GHz} \end{aligned} \tag{26}$$

Lets verify this, load the ADE L state. 'Av_BW_noise_2'. Disable the noise analysis and the noise output variable and run the simulation. The simulation result in Figure-16. The time-constant estimation was very conservative in this case since the simulation says 2.6 GHz. Remember that in reality there is a zero in the transfer function that is improving the frequency response.

Before simulating the noise characteristics, let's have some remarks on the expected noise performance. The CD stage has a voltage gain of 1, and hence any noise voltage at the output is directly referred to the input without any attenuation. Load the ADE L state 'Av_BW_noise_1' and enable the noise analysis and output and run the simulation. The noise characteristics of the CD stage can be found in Figure-17. The noise voltage looks equal to the CS stage.

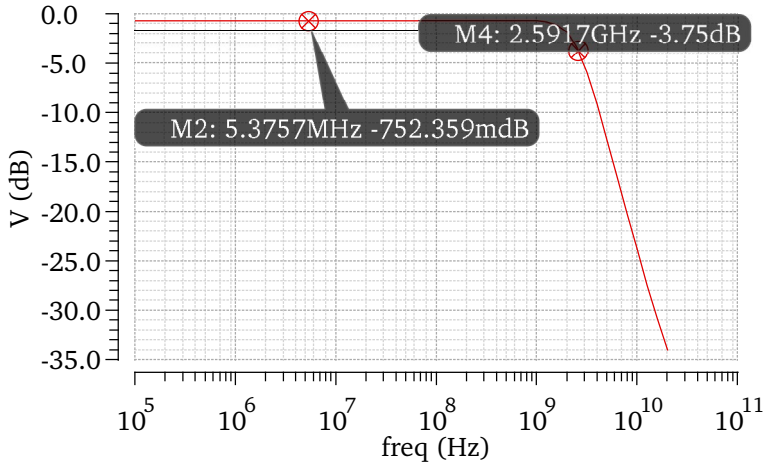

Figure 16: AC gain of Circuit-2

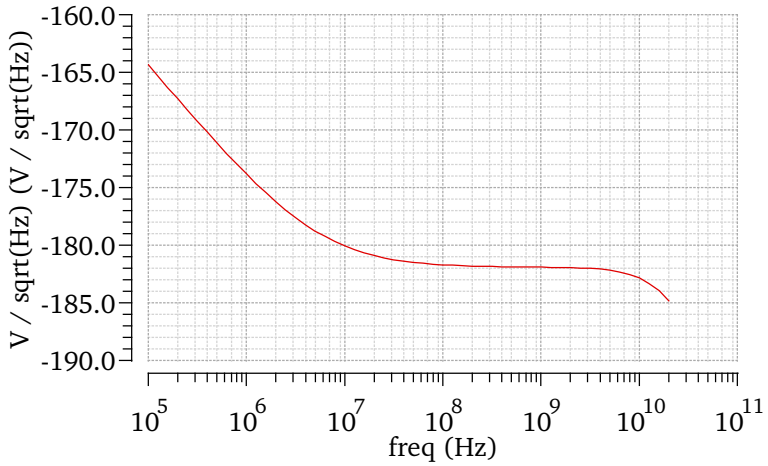

Figure 17: Input referred noise voltage of Circuit-1

Now, put a resistor of 2 kΩ in the branch labeled 'vout1' such that its one end is connected to the source of the transistor and the other end is open. Replace the label 'vout1' from the source of the transistor to the open end of the resistor and run the noise simulation again. Check the high frequency noise floor. It has increased as compared to the last case. Guess by what amount?! Try plotting the integrated noise summary from 10 MHz to 1 GHz and look at the noise contribution of this newly place resistor.

In essence, similar to CG stages, the CD stage has the disadvantage that it directly refers one of the output noise sources without attenuation; hence, they should not be used as input stages if low noise performance is required. Moreover, the CD stage has high input impedance and therefore its input referred noise current is similar to the CS stage. Notice that Cgd reduces the impedance at high frequencies. At very high frequencies the noise current grows rapidly and dominates.

3 Current Mirrors

Current mirrors have many uses in analog design. They are extensively used to provide DC bias currents to the signal path circuits. In addition, they are used to amplify, add, and copy AC signals. The current mirror can be thought of as a current-controlled current source (CCCS). As any current source, its performance improves when the output impedance is high. In this tutorial, you will study the performance of a few current mirror setups.

3.1 Basic Current Mirror

Open schematic "Basic_Current_Mirror". There are three simulation setups as shown in Figure-18.

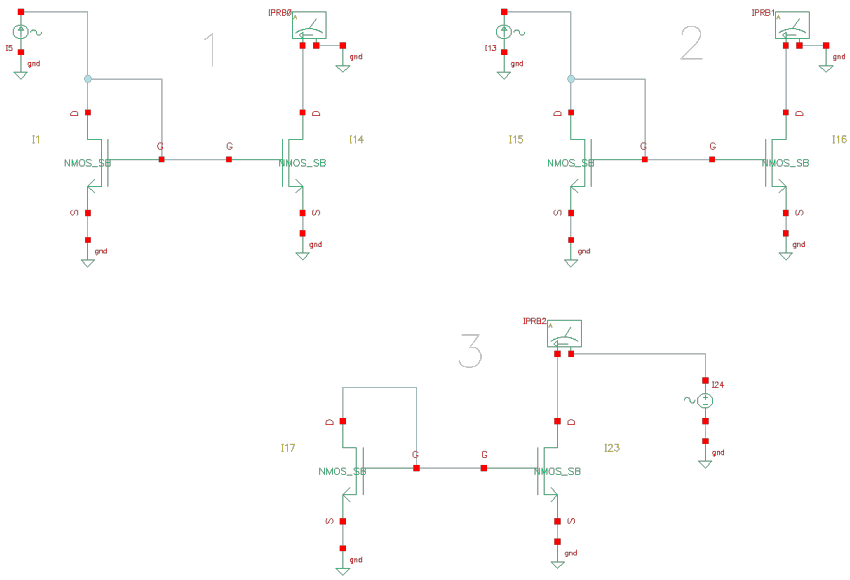

Figure 18: Setups for analysing basic current mirror stages

Circuit-1 is a 1:1 current mirror. Circuit-2 is a 1:2 current mirror and Circuit-3 is a setup to measure the output impedance of a basic 1:1 current mirror. You can press 'q' and check the sizes and biasing currents of each transistor. Verify that for Circuit-2 the width and biasing current of the transistor (I16) containing the output current is twice than that of the transistor (I15) containing the input current.

Launch IDE L and load the state 'Ai1_Rout'. Run the simulation. You will see three different curves. Split the curves in three different plots. The first plot labelled (I0) shows the current gain of Circuit-1 (output current is equal to the current gain as the magnitude of the input current is 1) as shown in Figure-19.

The current gain is close to 1 (0 dB). Why is there a small difference? The small difference is caused by the fact that the input impedance Rin is not exactly $1/gm$, but it is $Rin = rds||1/gm$. Also, note that the capacitances start shunting current at high frequencies and attenuating the output current.

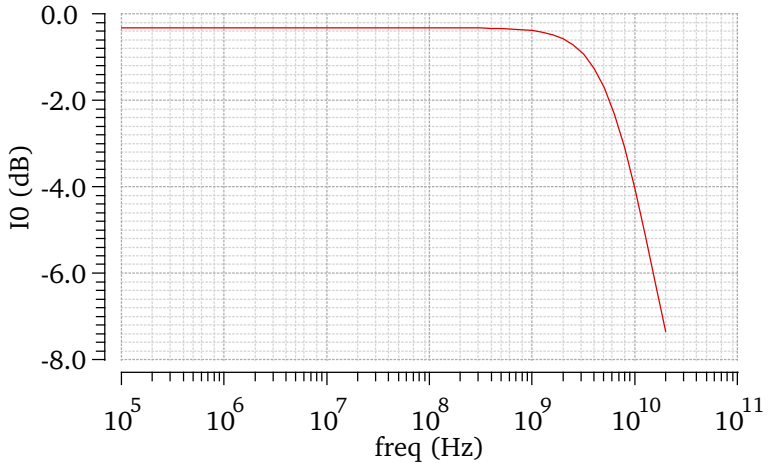

Figure 19: Current gain of Circuit-1

Amplifier current mirrors are designed by changing the sizes and biasing of the input and output transistors. The plot in Figure-20 labelled (I1) shows current gain of Circuit-2 in which the width and bias current of the input transistor has a ratio of 1:2 with respect to the output transistor. Figure-20 shows that DC gain is around 5.7 dB, close to 6 dB(2) as expected.

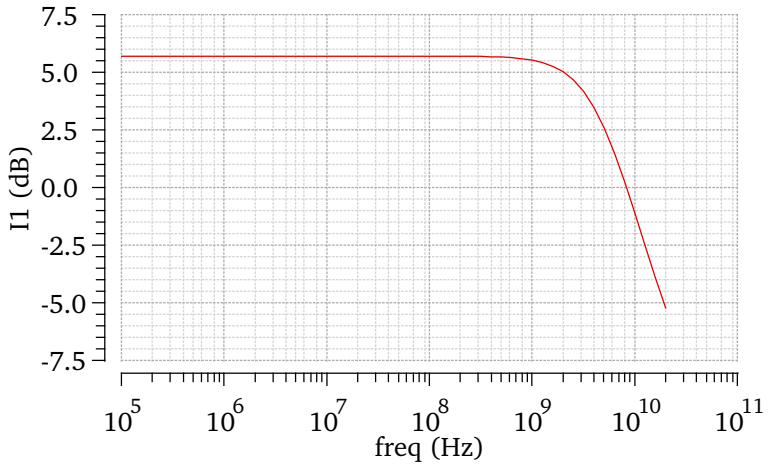

Figure 20: Current gain of Circuit-2

Finally the output impedance of the basic current mirror is simulated using Circuit-3 and is shown in Figure-21.

The output resistance at DC is 2.156 kΩ, which is equal to rds. At higher frequencies, the parasitic capacitance at the drain reduces the impedance considerably. This problem is particularly serious at high frequencies and requires careful consideration in RF circuit design.

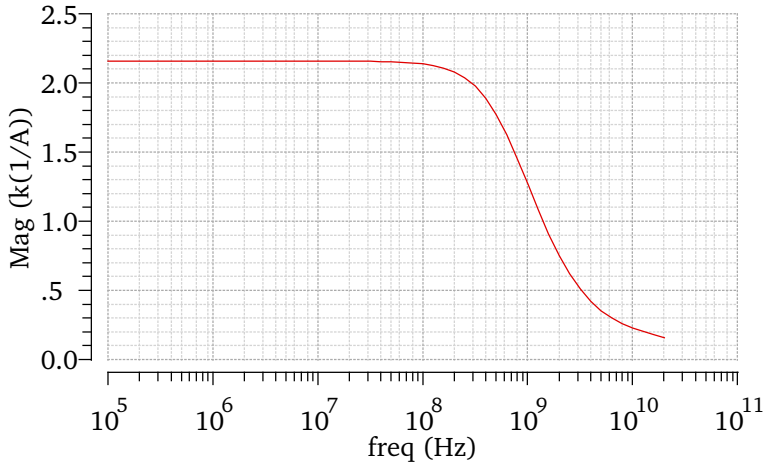

Figure 21: Output resistance of basic current mirror using Circuit-3

3.2 Current Mirrors with Source Degeneration

Open the schematic "Current_Mirror". The schematic is shown in Figure-22. There are two simulation setups: a basic current mirror with resistive degeneration (Circuit-1), and a cascode current mirror (Circuit-2). All of the transistors have the same dimensions, so basically only 1:1 mirrors are demonstrated here.

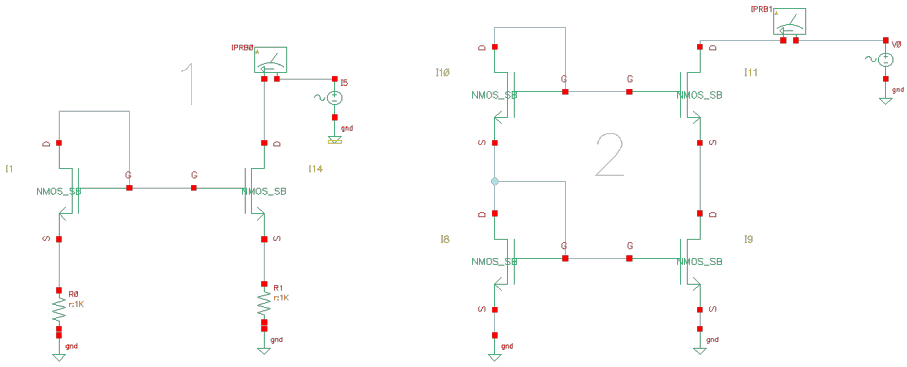

Figure 22: Setups for analyzing advanced current mirror stages

Before running the simulations, let's have some general remarks about the degeneration of CS stages. The analysis of each configuration can be done mathematically using PI models and node analysis. These methods are totally valid from the theoretic point of view. However, here we will resort to some basic analytical tools coming from the negative feedback theory that renders rigorous mathematical demonstrations unnecessary. These tools will not be explained here (You will have a separate tutorial on the negative feedback). A resistance at the source of a CS stage adds negative feedback to the circuit and improves some of its characteristics, for instance accuracy in the transconductance and improvement in the input and output impedance. The feedback factor (β) of a

resistive source degenerated CS stage (as the output stage in the current mirror of Circuit-1) is:

$$\beta = -Rs \tag{27}$$

where Rs is the value of the source degenerating resistor. The loop gain (Aβ) of the CS stage with source degenerating transistor is:

$$A\beta = -gm \cdot Rs \tag{28}$$

The modified transconductance (gm_{mod}) of CS stage with source degenerated transistor is:

$$gm_{mod} = \frac{gm}{1 - A\beta} = \frac{gm}{1 + gm \cdot Rs} \tag{29}$$

where the factor $(1 + gm.Rs)$ is the total correction due to the negative feedback. This factor also improves the output resistance to:

$$R_{out} = rds(1 + gm \cdot Rs) + Rs \tag{30}$$

The second term is usually much smaller than the first term in (30). Therefore, it can be reduced to:

$$R_{out} = rds(1 + gm \cdot Rs) \tag{31}$$

Lets verify this by plotting the output resistance of Circuit-1 with the source degeneration resistor. Launch ADE L and load the state 'R_out'. In the outputs section uncheck all outputs except 'Rout0' and run the simulation. The result of the simulation is shown in Figure-23. From (31) the output resistance of the source degenerated current mirror of Circuit-1 is R_{out} =2.156 k(1+11.85m×1k) = 27.7 kΩ. Figure-23 shows that Rout is 29.2 KΩ, very close to our calculations.

The output resistance of the cascode current mirror in Circuit-2 is $R_{out} = rds \cdot (1 + gm \cdot rds) = 57.23$ kΩ (or 59.4 kΩ if you insist on more accuracy and use (30) instead). Run the simulation again but this time select only 'Rout1' in 'Outputs' section. Figure-24 shows that input impedance is 62 kΩ, which is still reasonably close to our hand calculation taking in consideration the crude simplifications that were done. The difference arises due to the diode connected transistors that give a marginal contribution to the loop gain.

4 Cascode Amplifiers

In most of the cases, the gain specifications of amplifiers cannot be achieved using the basic single stages described above. A solution is to stack basic amplifying stages so that their cascoded gain accomplishes the requirements. The price to pay for this improvement can be voltage overhead, power consumption, or instability issues. In this tutorial, we will concentrate on one configuration

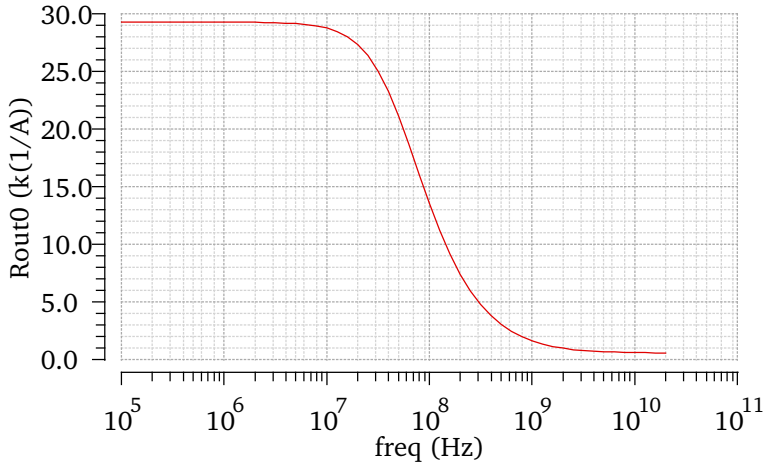

Figure 23: Output resistance of Circuit-1

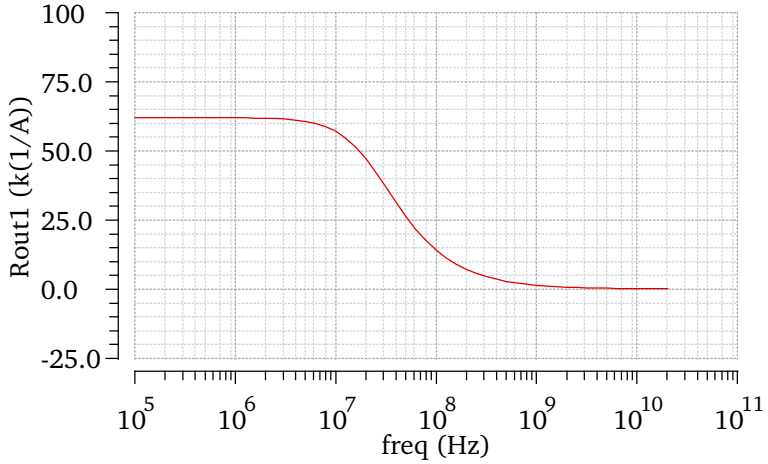

Figure 24: Output resistance of Circuit-2

that is commonly found in CMOS analog design: the cascode amplifier. This configuration stacks a CS stage and a CG stage on top of each other. Commonly, the biasing current that is used for the CS stage is also reused in the CG stage. Accordingly, the improvement comes without power consumption penalty. The reader should be however warned that this is not always the case since sometimes it is beneficial to bias the CS and CG stages separately.

Open the schematic 'Cascode_Amplifiers'. There are three circuit setups ready for simulations as shown in Figure-25.

The gain of the cascode configuration is:

$$V_{out} = V_{in} \cdot gm \cdot R_{out} \tag{32}$$

$$A_v = \frac{V_{out}}{V_{in}} = gm \cdot R_{out} \tag{33}$$

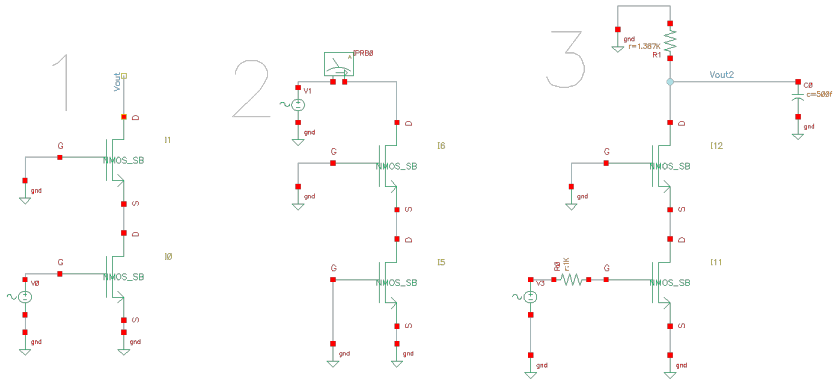

Figure 25: Setups for analyzing cascoded amplifier stages

where R_{out} is the output resistance. For now, assume that there is an ideal current source providing biasing (in a separate tutorial biasing techniques and their impact on the circuit performance will be demonstrated). R_{out} is given as:

$$R_{out} = (1 + gm \cdot rds) \cdot rds = 55.08 \text{ k}\Omega \tag{34}$$

Launch the ADE L state 'Av_BW_noise'. Select the 'ac' analysis and 'Rout' as an output and run the simulation. Th result of the simulation shown in Figure-26 gives an output resistance of 60.6 kΩ.

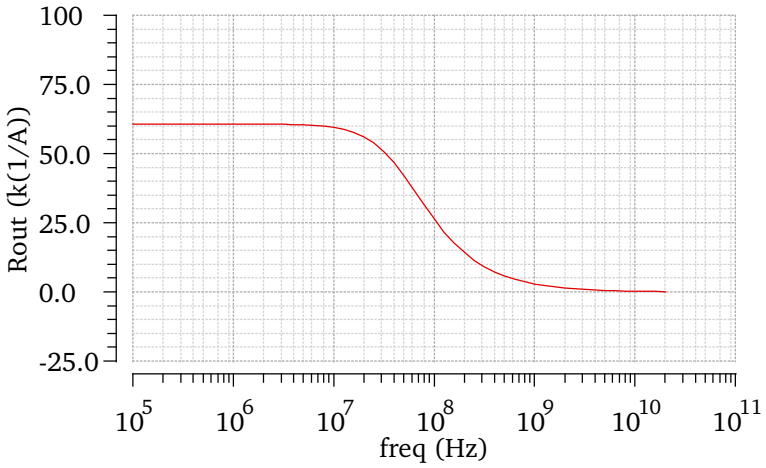

Figure 26: Output resistance of cascode stage simulated using Circuit-2

The voltage gain of this cascode amplifier is $A_v = gm \cdot R_{out} = 652.1$ (56.3 dB) under the assumption of an ideal biasing. Select the output 'Av' and rerun the simulation. The simulated voltage gain of the amplifier shown in Figure-27 is equal to 56.8 dB, close to our hand calculated value.

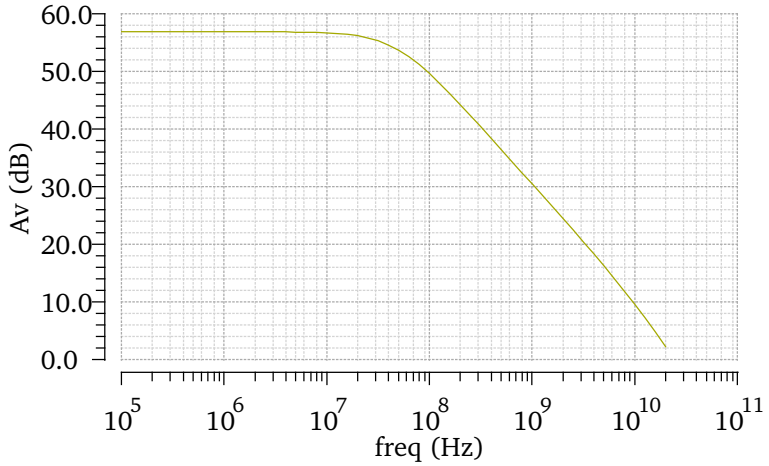

Figure 27: AC gain of Circuit-1

The bandwidth of the cascode amplifier can be estimated by using the open time constants method. For comparison reasons, the setup of Circuit-3 has the same source and load resistances and capacitances as was in the CS stage.

Node (1) is the gate of the CS stage, node (2) is the drain of the CS stage, and node (3) is the drain of the CG stage. Note that at node(1) the miller capacitor Cgd is reduced in comparison to the CS stage since the input impedance of the CG stage is only $1/gm$.

$$\begin{aligned} T(1) &= R0 \cdot (Cgs + Cgd(1 + gm \cdot (1/gm))) \qquad (35) \\ &= 196.2 \text{ ps} \\ T(2) &= (1/gm||rds) \cdot (Cgs + Cgd) \approx 1/gm \cdot (Cgs + Cgd) \qquad (36) \\ &= 11.9 \text{ ps} \end{aligned}$$

At node (3) the effect of Cdb depends on the connection of the source and bulk. If they are connected together (triple-well) then Cdb appears in parallel to rds and hence it is also "improved" by the loop gain. This means that Cdb appears divided by the loop gain $(1 + gm.rds)$=26.5. If the bulk and source are separately connected (twin- well) then Cdb is out of the loop and appears completely in parallel to the output. In this case, the self biased transistor is of the triple-well type so:

$$\begin{aligned} T(3) &= (R1||R_{out}) \cdot (Cgd + 500\text{f}) \approx R1 \cdot (Cgd + 500\text{f}) \qquad (37) \\ &= 761.1 \text{ ps} \end{aligned}$$

$$\begin{aligned} BW &\approx \frac{1}{2\pi[T(1) + T(2) + T(2)]} \qquad (38) \\ &= 164.2 \text{ MHz} \end{aligned}$$

Select the output 'Av2' and rerun the simulation. The result of the simulation shown in Figure-28 shows a 3-dB bandwidth of 190 MHz, close to the predicted value.

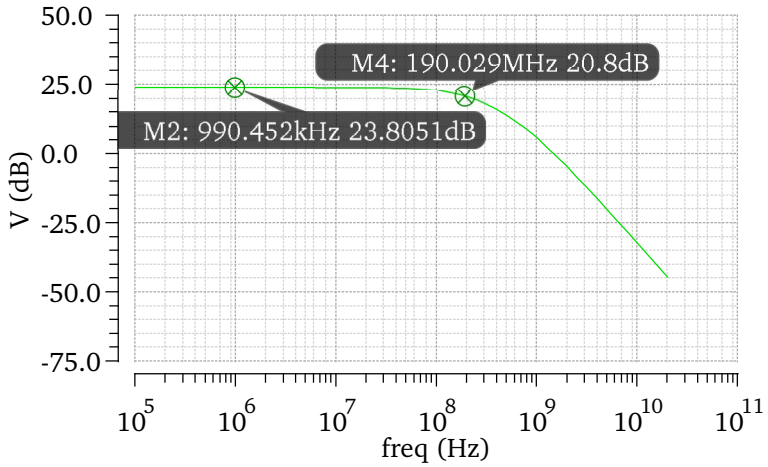

Figure 28: AC gain of Circuit-3

The increase of bandwidth due to reduction of Miller capacitance, Cgd is an important benefit of the cascode configuration. Cgd is a very non-linear parasitic component, and its reduction also improves the linearity of the circuit. In addition, the cascode decouple the input and output nodes, that in the CS stage are directly connected by Cgd. This direct connection in a CS stage introduces a right plane zero that contributes to the instability. The cascode isolate the input and output nodes, and split their poles by sending the input pole to a higher frequency and the input pole to a lower frequency. This behaviour is very welcoming for stability purposes as it will be shown in further tutorials.

Finally, let's check the noise performance of the cascode stage of Circuit-1. Select the 'noise' analysis and the 'Input referred voltage' output and run the simulation. The result of the simulation is shown in Figure-29.

The noise performance of the cascode stage is basically the same as the CS stage. Plot the table of the noise contributors in an integrated noise from 100 kHz - 1 GHz. The noise contributors are shown in Figure-30. Can you tell why the noise contribution of I1 is orders of magnitude smaller than I0?

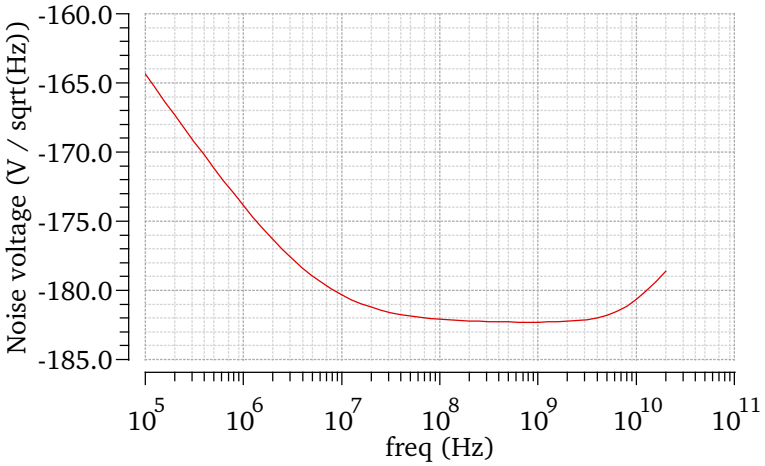

Figure 29: Noise voltage of Circuit-1

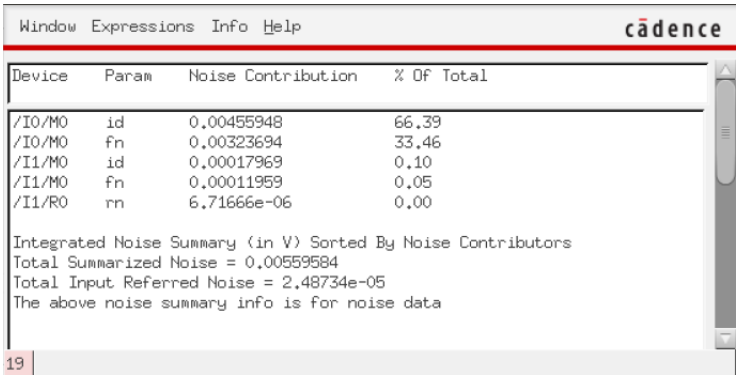

Figure 30: Noise contributors in Circuit-1

References

[1]-Lee,T.H. 2004. *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press.
[2]-Razavi,B. 2001. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill International Edition.