

# Tutorial 0

## Introduction to the Cadence Virtuoso environment

### 1 Installation of the PDK

#### 1.1 Introduction

The Cadence Virtuoso Platform is used for the design of full custom integrated circuits. It consists of tools for schematic entry, behavioral modeling, circuit simulation, layout design, physical verification and parasitic extraction. For the Virtuoso tools to work properly information about the used process is required. A PDK (Process Design Kit) contains all the necessary information to design a circuit from the schematic entry down to layout. In particular it contains:

- Technology information like the number of metal layers and their thickness.
- Physical verification rules: DRC (Design Rule Check), LVS (Layout Versus Schematic) etc.
- Parasitics Look-up tables for the layout parasitic extraction.
- Device models for an accurate circuit simulation.
- Extra packages like digital cell libraries (fully characterized digital gates like inverters, Flip-Flops etc).

Throughout this course the LFOUNDRY150nm CMOS process by LFOUNDRY will be used. The main features of this process are:

- minimum device length: 150nm
- 6 routing metal layers
- 1 thick metal for the fabrication of inductors
- 1 MIM layer between METAL5 and METAL6 for the fabrication of MIM capacitors (Metal-Insulator-Metal)
- various transistor flavors. In this course the nmos\_hs\_4 and nmos\_ll\_4 will be mainly employed. Both of them operate under a 1.8V supply with the first one intended for standard applications and the later for low-leakage ones.

## 1.2 Installation Instructions

1. To install this PDK you have to login in one of the AFS servers intended for courses (preferably to malavita).

```
ssh -Y <username>@malavita.sys.ict.kth.se
```

In general it is preferable to work from the KTh Kista campus in order to exploit the high bandwidth. If nevertheless you have to work from home, you may choose a faster encryption:

```
ssh -X -C -c blowfish-cbc,arcfour <username>@malavita.sys.ict.kth.se
```

2. Create a project directory (i.e. /IL2238) and enter it.

```
mkdir IL2238
```

```
cd IL2238
```

3. Create a symbolic link to the PDK directory:

```
ln -s /afs/kth.se/misc/projects/ict/ektlab/PDK/LFOUNDRY/PDK_LF150i_V2_0_0/
```

4. Invoke the installation script:

```
./PDK_LF150i_V2_0_0/tools/installation/workarea.PDK_LF150i_V2_0_0
```

5. The script will ask for the absolute path to the PDK. Type:

```
./PDK_LF150i_V2_0_0
```

and press <ENTER>.

6. Then you will be asked to specify the absolute path to the work area directory. Just select the default by pressing <ENTER>.
7. As for the metalization module, select option 0 (6 metals)
8. Since you'll only be working with Cadence tools type "C" and press <ENTER>
9. When you will be asked for the ciranova plugin, select the default (option 0) and press <ENTER>.

```
@malavita IL2238]$ ./PDK_LF150i_V2_0_0/tools/installation/workarea.PDK_LF150i_V2_0_0
**LFoundry*****
HINT: You may cancel this script any time with <CTRL-C>

Setup routine for a PDK working area
[V2.0.0]

Specify absolute path to the PDK.
The last directory in tree should be "PDK_LF150i_V2_0_0".
[/afs/kth.se/home/p/a/pancha/IL2238] ? /PDK_LF150i_V2_0_0

Specify absolute path to the work area directory.
Selecting an existing directory means to update the work area.
[/afs/kth.se/home/p/a/pancha/IL2238] ? |
```

Figure 1: Installation script

10. Copy the PDK's initialization script. This script provides the path to the tools' binaries.

**cp /afs/kth.se/misc/projects/ict/ektlab/PDK/LFOUNDRY/init64.sh .**  
*The dot in the end of this command denotes that the target destination of the copying process is the current directory.*

11. Your PDK is now installed and you can start using it!

## 2 Starting virtuoso

What does *Cadence virtuoso* do?

*Cadence virtuoso* is a tool suite for the development of custom IC (Integrated Circuits) designs. It comprises of the following tools:

- Virtuoso Schematic Editor. It significantly facilitates the design entry with a set of built-in capabilities: component libraries, sophisticated wire-routing, hierarchical design, etc.
- Virtuoso Analog Design Environment (ADE). It enables electrical and statistical analysis and characterization by providing the interface to the industry's favorite simulators (Spectre, HSPICE, etc).
- Virtuoso Layout Suite. It eases the generation of a layout for a schematic entry with a set of various modules (connectivity guides, floorplanning, automatic generation of some topologies, etc) . It also provides built-in tools for physical verification and parasitic extraction.
- Virtuoso Visualization and Analysis. It is a waveform display and analysis tool that facilitates the characterization of a circuit.

To start **virtuoso** you have to source the initialization script (init64.sh). Login to your working directory (IL2238) and type:

```
source init64.sh
```

To invoke virtuoso type:

```
virtuoso &
```

## 2.1 Command Interpreter Window

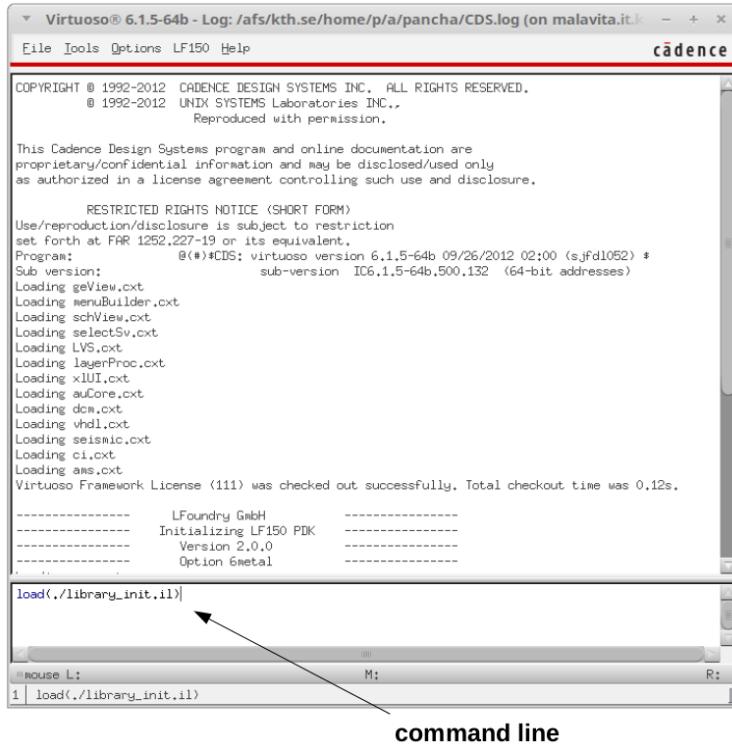


Figure 2: CIW

The Command Interpreter Window (CIW) is the first window that opens when starting Cadence. It is a gateway to all the virtuoso tools and plugins both graphically and through a command line. It also reports possible errors in some applications.

## 2.2 Library Manager

The components that comprise a design, known as cells, are organized in libraries. The Library Manager is used to access/edit/delete libraries or their containing cells. To facilitate the preview of a library's content, its cells are divided into categories.

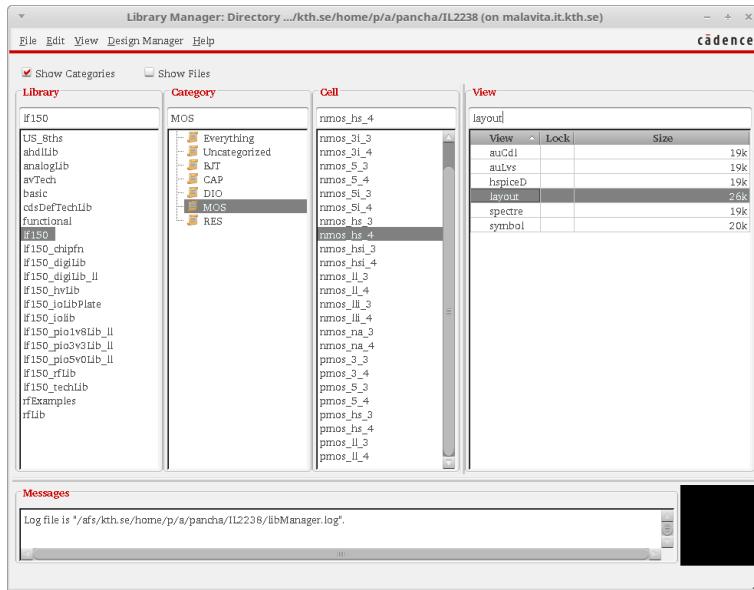


Figure 3: Library Manager

Each cell is comprised of different views, for example layout, symbol, etc. each one used by a specific operation. In particular:

- auCdl : It is used to translate a schematic entry into a netlist.
- auLvs : It is used during the Layout-vs-Schematic checks (LVS) as well as during parasitic extraction.
- hspiceD, spectre : They create a link to the device models used by the corresponding simulators: HSPICE and spectre.
- symbol : It is used during schematic entry

Typically, the Library Manager window pops up automatically every time virtuoso is initialized. If that is not the case, you can invoke it from the CIW: Tools→Library Manager.

### 3 Creating a Schematic Entry

In general, creating a schematic entry is the first step in the design of an IC, followed by designing the layout. For practical reasons it can be divided in 4 steps:

1. Create the design-library in the Library Manager.
2. Generate the circuit schematic.
3. Create a testbench to simulate the circuit.
4. Generate a config view of the testbench for use with the "Hierarchy Editor".

5. Simulate the circuit.

### 3.1 Creating the library

1. From the Library Manager go File→New Library. A window like in Fig. 4 will pop-up.

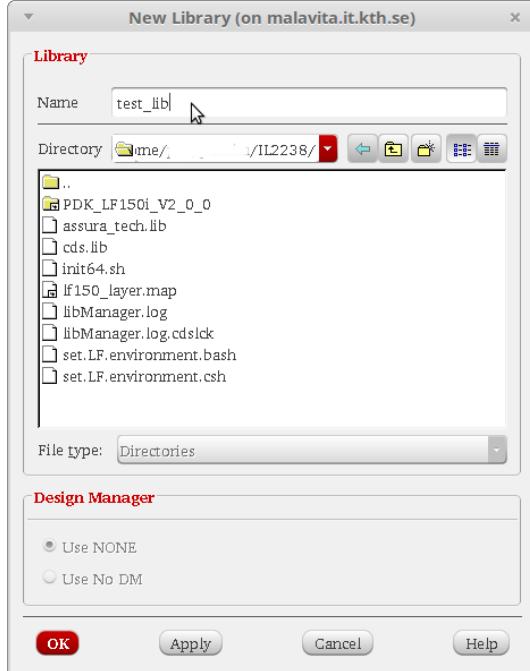


Figure 4: Create a New Library

2. In this example, the library will be named "test.lib". You will also be asked whether you wish to attach "test.lib" to a Technology File (see Fig. 5).

Click on "Attach to an existing Technology library", press OK and select "lf150\_techlib" (LFOUNDRY 150nm process): (Fig. 5).

3. At this point, you should create a cell within "test.lib". To do so, in the Library Manager window select the newly created library and then click on: File→New→Cell View. In the window that pops up fill in the fields as illustrated in Fig. 6.

4. Once you have created the inverter cell in the Library Manager, an empty schematic is created (Fig. 7).

5. Press on the "Check and Save" button As the name applies through this function, a sanity check is performed in the design before it is saved.

6. Creating categories for a library facilitates the organization of the consisting cells. To create a category, click on File->New->Category. Assuming you want to categorize the inverter cell in "digital\_cells", fill in

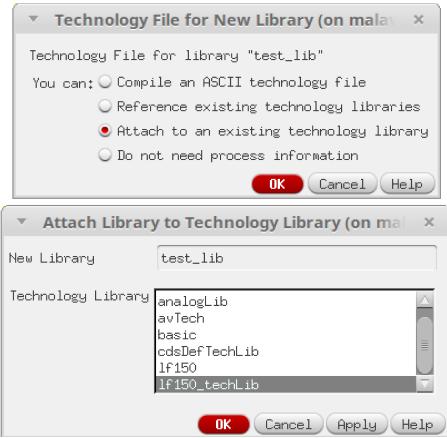


Figure 5: Attach a Library to a Technology Process

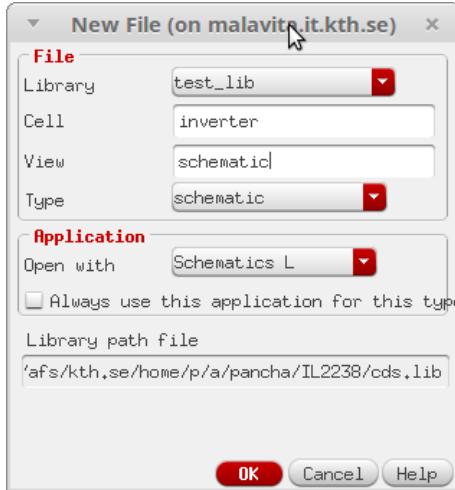


Figure 6: Create a Cell

”digital\_cells” in the field ”Category Name” as shown in Fig. 8. Then select inverter from the ”Not in Category Field” and transfer it to the ”In Category” field.

Click on the ”Show Categories” box in the Library Manager. It should now look like Fig. 9.

### 3.2 Generating the circuit schematic

1. At this stage we will work mainly on the ”Virtuoso Schematic Editor”. Open the schematic view of the inverter cell by double clicking on it. We are going to draw the schematic of a CMOS inverter.
2. Press ’i’ to insert a new instance of a device. Select ”Browse” and then the symbol view of **the nmos\_hs\_4** cell that is located in the lf150 library

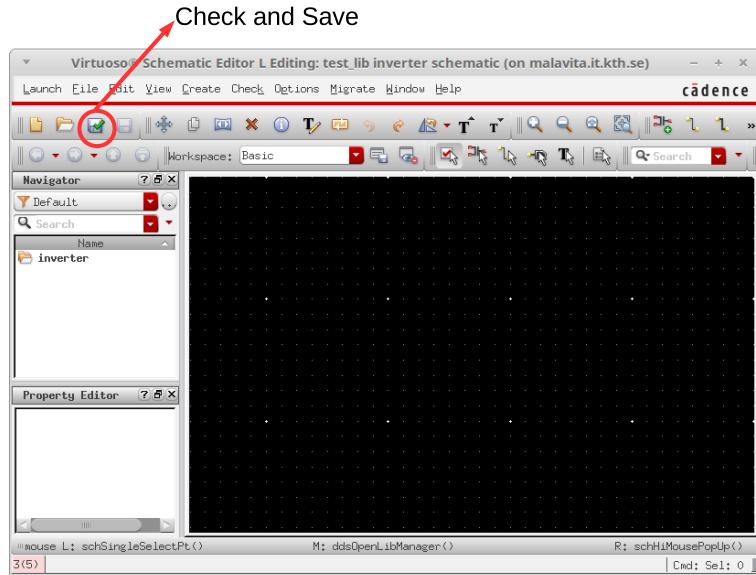


Figure 7: Check and Save

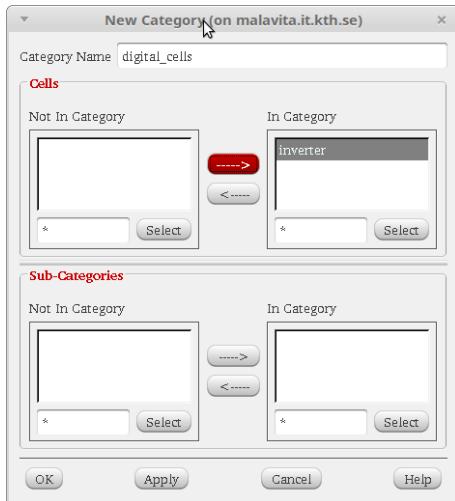


Figure 8: Create Categories

under the MOS category (see Fig. 10). Place it anywhere you wish in the schematic editor. You may change the parameters of the device such as its width (finger width) or length from the "Add Instance" window.

3. Else, if you need to check/modify the device parameters at any point during the generation of the schematic you can select the component by left-clicking on it and pressing "q". Then the "Edit Object Properties" window comes up which is similar to the "Add Instance" window. For this tutorial set the length of the nmos device at 150nm and its finger width at 400nm. Do not change the rest of the parameters! **NOTE:** You

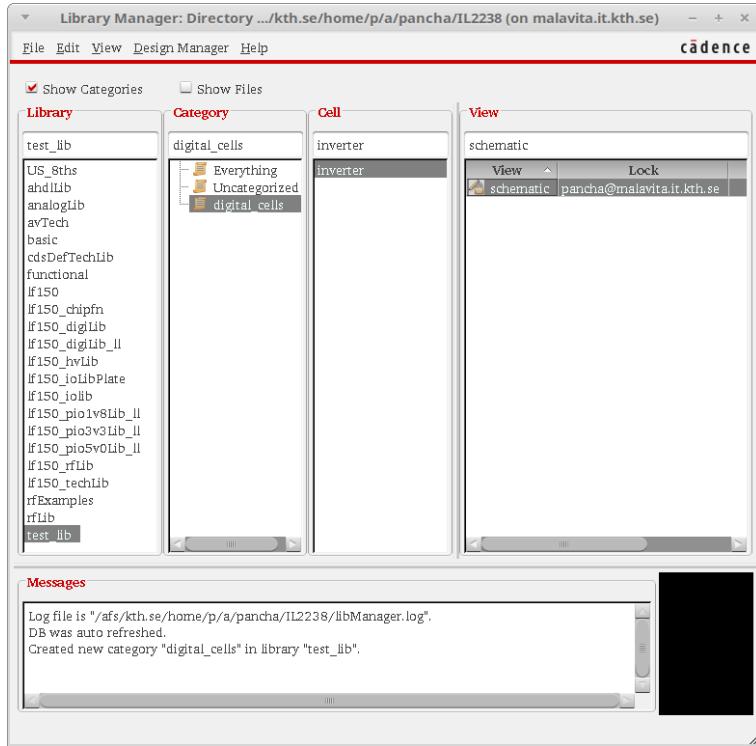


Figure 9: Library Manager with Categories

should not include units when updating the component parameters. For instance, to set the nmos length at 400nm just type in the corresponding field: 400n . The units are automatically set by the tools.

4. Repeat the previous step for the pmos transistor (**pmos\_hs\_4**). Set its length equal to 150nm and its finger width to 800nm.
5. After you place a component you may want to move it to another place. Press 'm', then select the component you want and move it to its new place.
6. You may also want to rotate the symbol (useful when drawing the schematic of current mirrors or differential pairs). In that case, select the component you wish to rotate, click on the arrow next to the "rotate" button in the toolbar (see Fig. 11) and select the rotating option that suits best in your case:
  - Rotate Right
  - Rotate Left
  - Flip Horizontal
  - Flip Vertical

**NOTE:** It is important to draw schematics that are easy to follow (as the ones you can see in the literature and in publications)

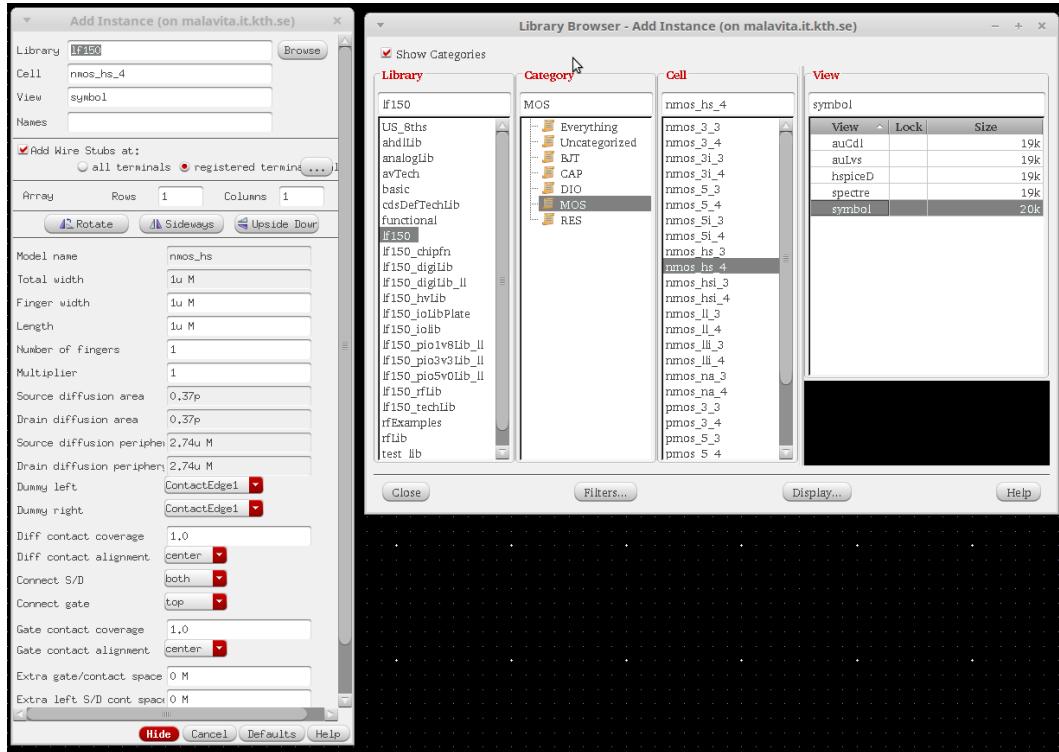


Figure 10: Inserting an nmos transistor

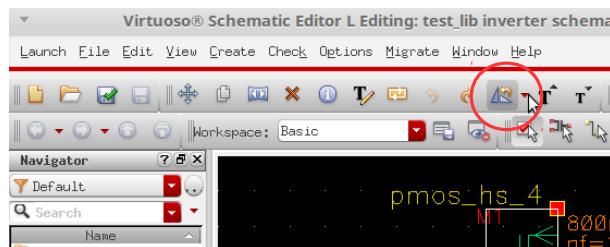


Figure 11: Rotate a component

7. After placing the components you should move on with connecting them. This is done with wires. To create a wire press 'w' and click on the point where you want the connection to start. You will notice that a wire is created and it is expanding according to the move of your mouse. Click again on the point where you want the connection to terminate. Connect the devices as shown in Fig. 12.
8. Following the drawing of the wires, you must create pins in your schematic. Pins play a pivotal role in the design as they are used by the tools to define its connectivity (inputs, outputs, supply). To insert a pin press 'p'. The "Add Pin" windows pops up as depicted in Fig. 13.

In the field "Pin Names" type the name you wish to assign to each pin.

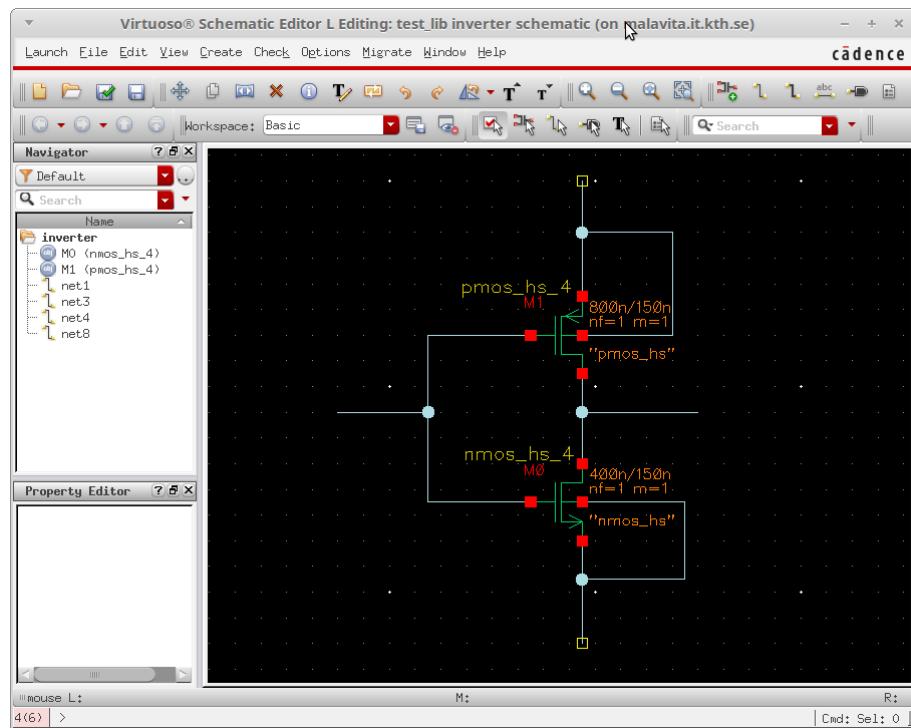


Figure 12: Device connection

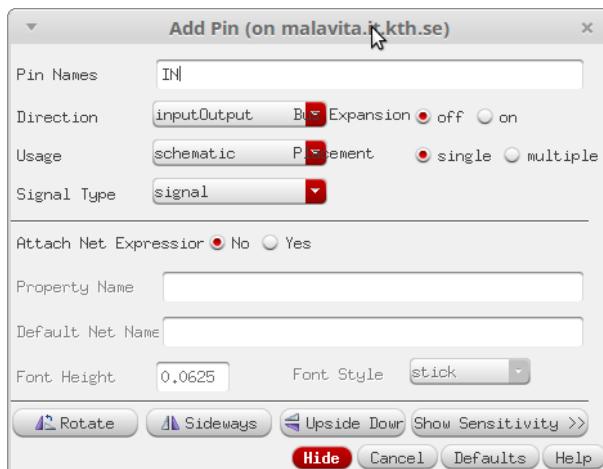


Figure 13: Insert Pins

In this example, the pin that corresponds to the input of the inverter will be named "IN". As far as the pin direction is concerned, for simplicity we set it to `inputOutput`.

9. Add the rest of the pins: "OUT" for the inverter output, "VDD" for the circuit's supply voltage and "VSS" for the reference node. The schematic

should now look like Fig. 14:

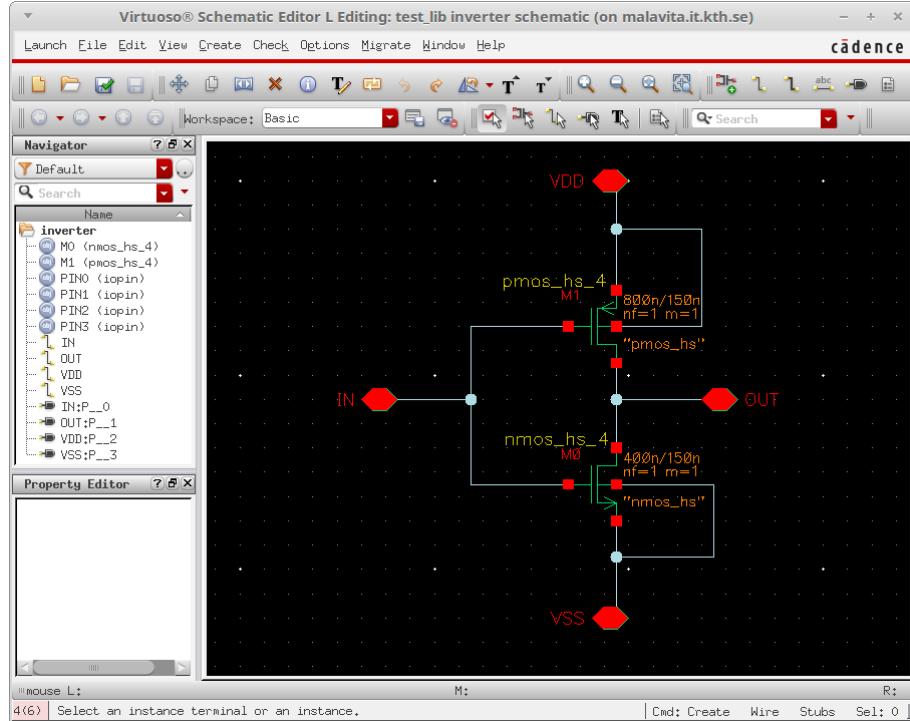


Figure 14: Final Schematic of an Inverter

- After completing the previous steps, a symbol for this circuit schematic should be created. That way:

- The inverter schematic can be embedded in other designs, enabling thus the hierarchical design concept.
- Various testbenches can be created to study the performance of the circuits.

To create a symbol click on Create→Cellview→From Cellview in the Virtuoso Schematic Editor toolbar. Do not change the default settings (see Fig. 15). Press OK.

Now Fig. 16 will pop-up. Here you can select the exact position of the inverter's pins. For simplicity, we will place all of them on the top side of the symbol. Once you are done, press OK and the circuit's symbol will open (see Fig. 17).

### 3.3 Creating a test-bench

A testbench can facilitate the circuit's simulation considerably. It is a new schematic cell that contains the inverter's symbol, some passive components (voltage/current sources and a load). If no testbench is created, we should instead remove the pins from the original schematic, place the voltage/current sources, run some simulations and then put the pins back. To create a testbench:

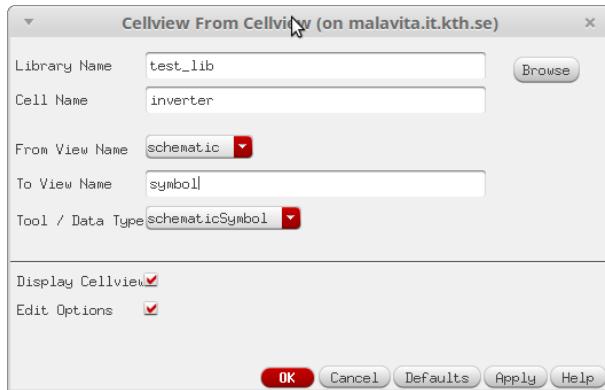
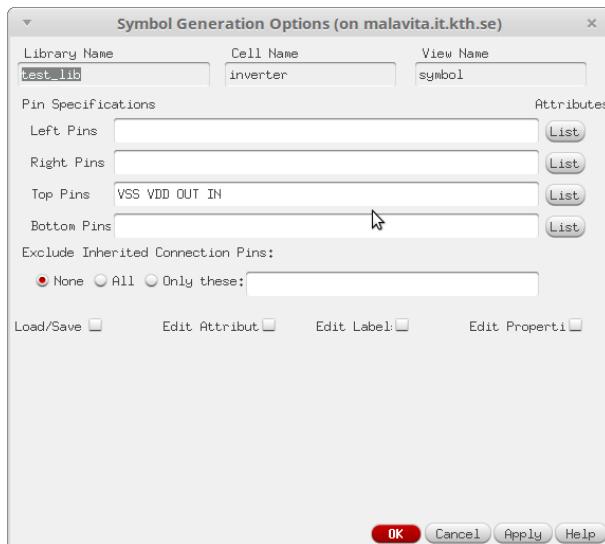


Figure 15: Create Symbol

Figure 16:  
Define the pins-position in the symbol

1. Go to the Library Manager and create a new cell inside the same library ("test\_lib"). In the field "Type" select "schematic" (see Fig. 18).
2. Insert the inverter's symbol that was created before. To do so, press 'i' and then click on the Browse button. Select the inverter's symbol (see Fig. 19) and insert it in your schematic.
3. Add the rest of the passive components (you can find them in the analogLib) and build the circuit shown in Fig. 20. These components are:
  - vdc: It provides a DC voltage and we employ it as the circuit's supply. To set its value, fill in 1.8 in the **DC Voltage** field of its properties.
  - gnd: It is used as a ground for the circuit.

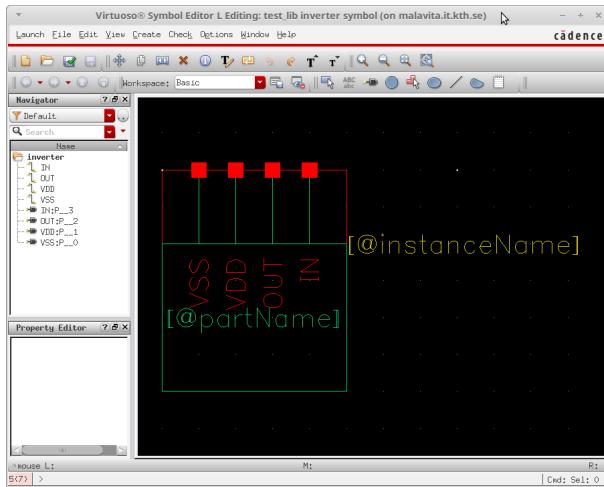


Figure 17: Inverter's symbol

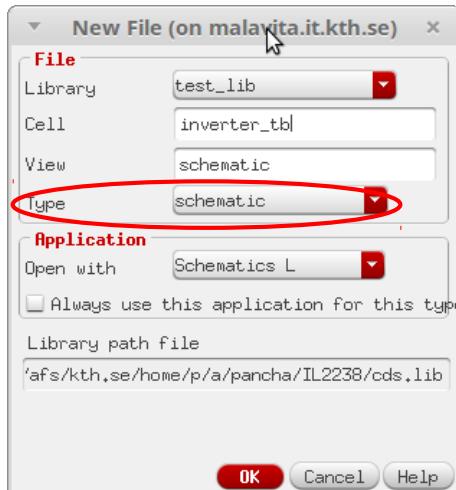


Figure 18: Create a Testbench cell

- vpulse: It provides a pulse-shaped voltage waveform. Its properties should be: **Voltage 1 = 0**, **Voltage 2 = 1.8**, **Period = 1/Freq**, **Pulse width = 1/(2\*Freq)**. Freq is a variable that will be set during the simulation setup (more in Section: 3.5).
  - cap: It is an ideal capacitor. Set its capacitance value to 5f.
4. In general it is useful to assign labels to the most critical nets in a schematic in favor of an easier simulation setup. As we will see in the coming section, the net names will be used in the calculation of some performance metrics. To name a net, press 'l' and write the name you wish in the field: "Names" (see Fig. 21). Then click on the net. You will notice that a label is now placed on top of that net.

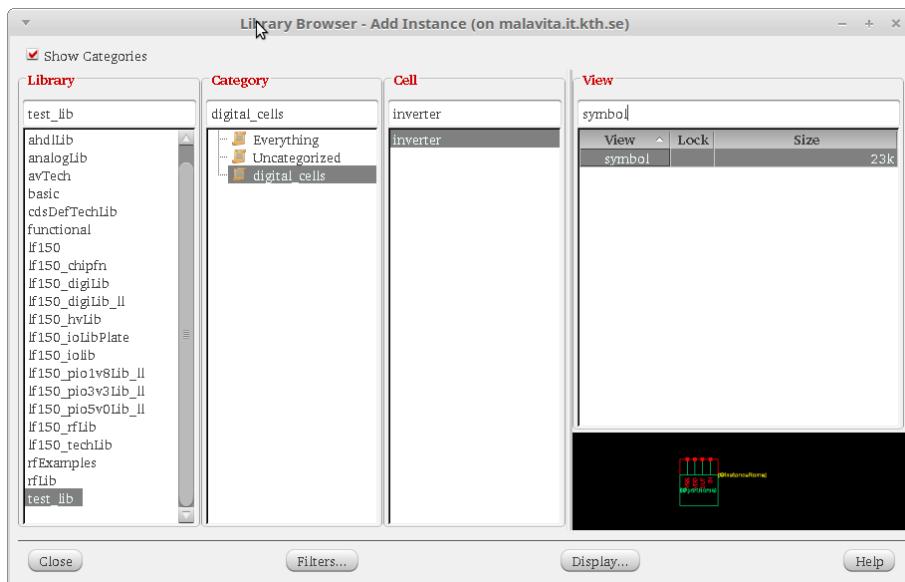


Figure 19: Insert the Inverter Symbol

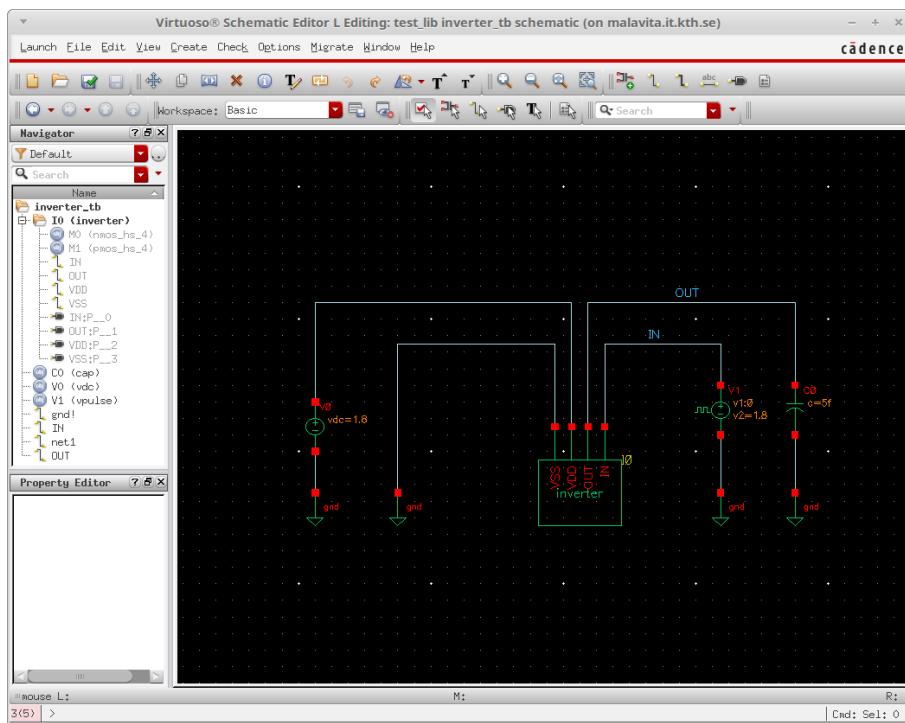


Figure 20: Final Schematic of the inverter's testbench

5. You can move inside the inverter symbol by pressing 'e' and clicking on it. If you wish to go back press "Ctrl" + 'e'.

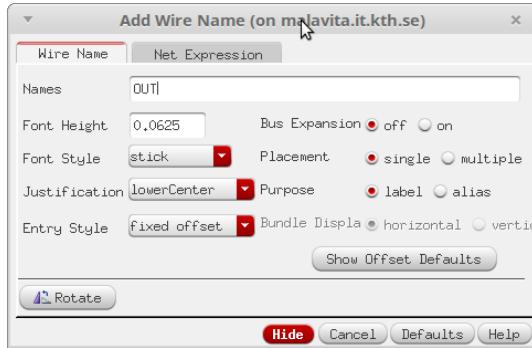


Figure 21: Adding labels to nets

### 3.4 Creating a config view

Now that the testbench schematic is ready, we will create a config view to be used with the Hierarchy Editor. Config view is used when the cells in a design are implemented in different ways (different views in the Library Manager) such as schematic, Verilog, av\_extracted etc. In particular, it enables us to select the implementation of each cell (view) that will be used during simulation. For example, config view is used to study the effect of layout parasitics on a design. This can be achieved simple by changing a component's view from schematic to av\_extracted. The latter is obtained after parasitic extraction. To create a config view:

1. Go to the Library Manager and select the "inverter\_tb" cell. Then go File→New Cell. Fill in the window that pops up as in Fig. 22.

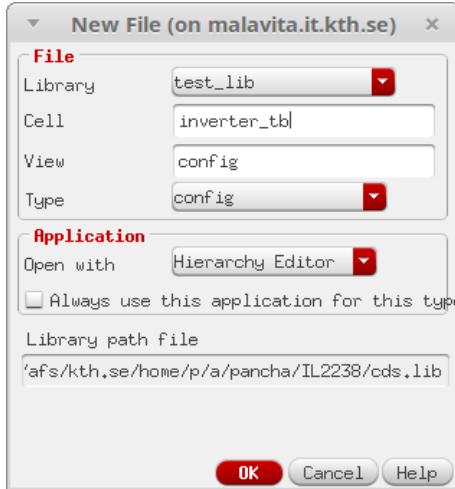


Figure 22: Creating a config view

2. In the new configuration window that pops up (Fig. 23) click on the "Use Template" button and select spectre in the "Name" field.

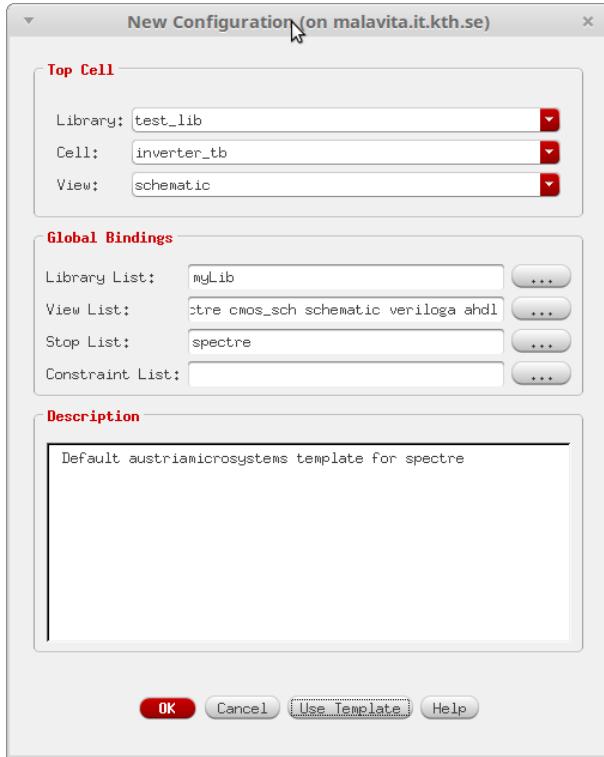


Figure 23: New Configuration Window

3. The "Virtuoso Hierarchy Editor" window will now look as in Fig. 24. The main idea is that you can set the view of every cell in a design by right-clicking on the "View Found" field in the "Cell Bindings" section and choosing Set Cell View. **NOTE:** Save the settings by pressing the corresponding button. Else, the config view will not be created.
4. To open the cell double click on its config view in the Library Manager. The "Open Configuration" window will pop-up. You may choose to open:
  - Either only the schematic view (Virtuoso Schematic Editor).
  - Or the config view (Virtuoso Hierarchy Editor window) that allows you to switch between the different views of the design's components.
  - Or both.

In this example we open both windows (see Fig. 25 and Fig. 26).

### 3.5 Simulation Setup

For the circuit simulation the Analog Design Environment (ADE) will be used which invokes the spectre simulator (based on the SPICE engine). To setup the simulations:

1. In the Virtuoso Schematic Editor click on Launch→ADE L and the Virtuoso Analog Design Environment window will pop-up (see Fig. 27).

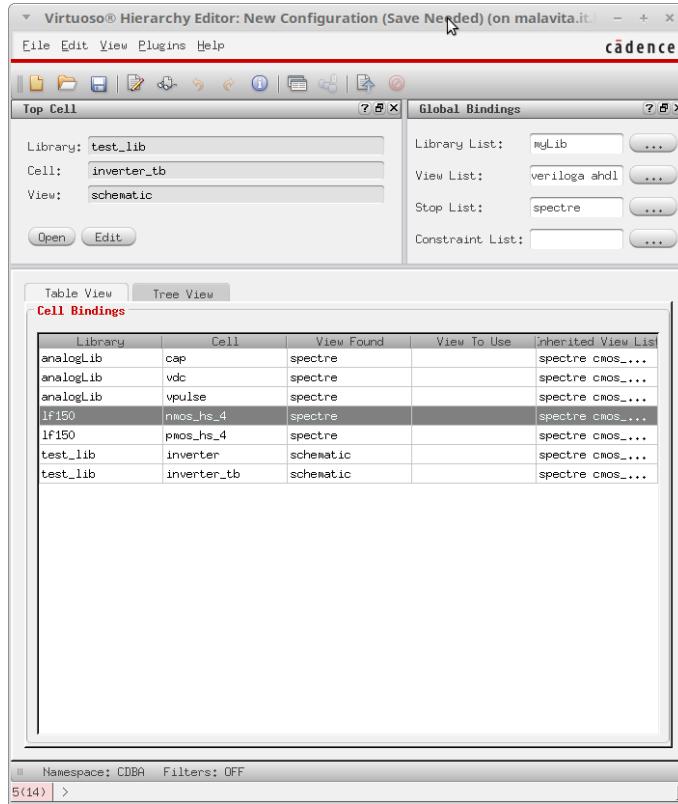


Figure 24: Virtuoso Hierarchy Editor Window

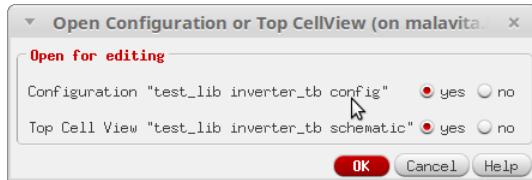


Figure 25: Opening a config view

2. Typically the paths to the Model libraries have been set during the installation of the PDK. If however you want to access/modify them click on Setup→Model libraries.
3. As you recall from Section 3.3 we didn't define the frequency of the input signal, but instead used the variable *Freq*. To be able to run a simulation this variable must be first defined. Click on Variable→Copy From Cellview. You will notice that *Freq* is now inserted in the section "Design Variables" in the left side of the ADE window. Set its value to 1GHz (see Fig. 28).
4. The DC analysis is used to calculate the DC operating points and node voltages whereas the transient analysis is used to see the circuit's response

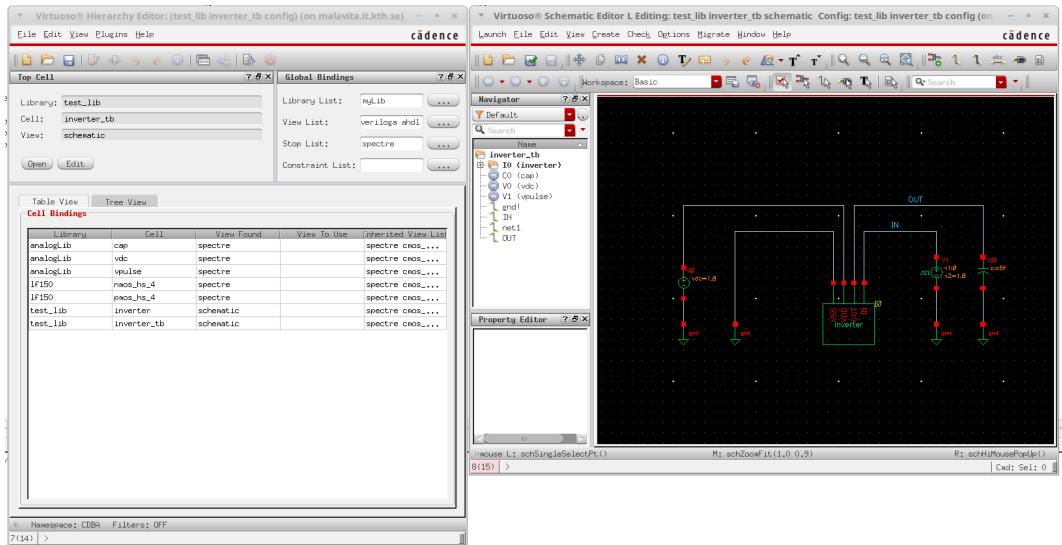


Figure 26: Virtuoso Hierarchy Editor and Virtuoso Schematic Editor windows

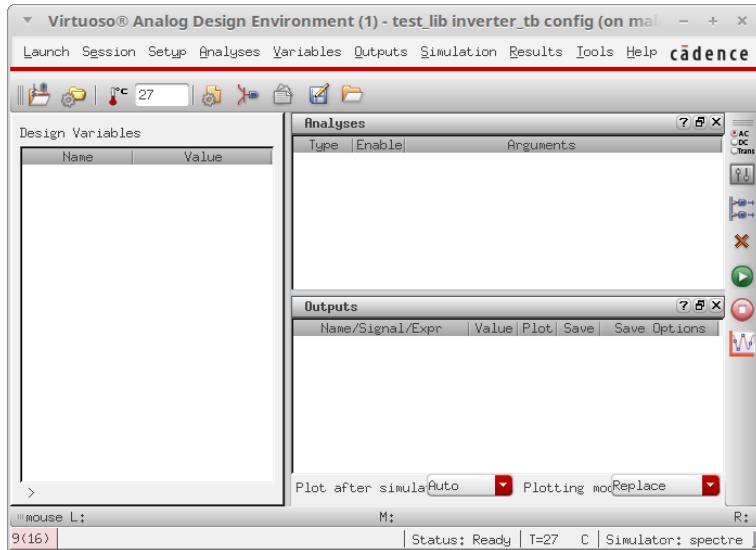


Figure 27: Virtuoso Analog Design Environment window

to a time varying input signal (in this case a pulse waveform). To setup the analysis just click on the "Choose Analysis" icon on the top right side of the ADE window (see Fig. 28). Listed below are the instructions to set-up the DC and the transient analysis:

- **dc analysis:** Click on the "Choose Analysis button and select the DC analysis. Select also the Save DC operating points option.
- **transient analysis:** Select the tran analysis. Select moderate accuracy and set the the stop time of the analysis to 4ns according to the

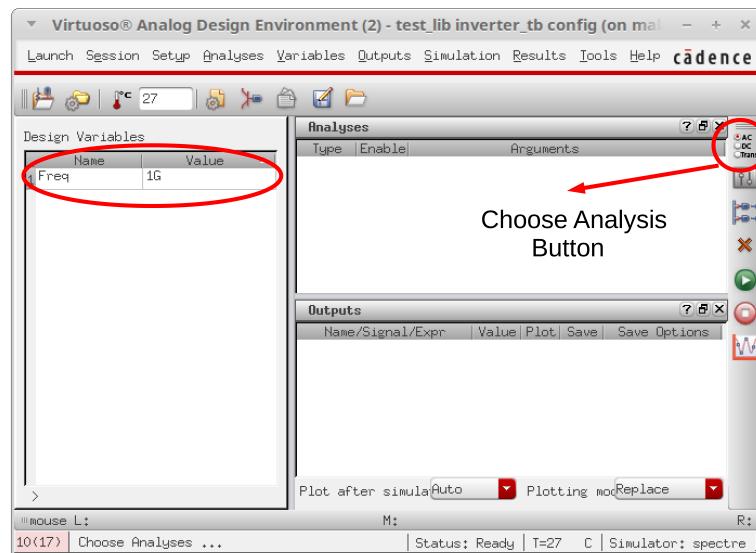


Figure 28: Setting the Design Variables

input frequency of 1GHz (that way, a few periods can be seen)

5. To set up the waveforms that will be plotted once the simulation is over: Click Outputs→To be Plotted→Select on Schematic. To select the input and output nets just click on them in the schematic window and then go back to the ADE window. By now it should be clear to you why it is helpful to label the nets. When selecting the nets you will notice that their color will change. If you want to plot a current waveform just click on the node flown by this current. You will notice that a circle is created around this node.
6. The ADE window now looks like Fig. 29.
7. At this point it would be wise to save the simulation setup so that you don't have to go through the same procedure the next time you simulate the design. Click on Session→Save State. Set the Save State Option to Cellview instead of Directory and hit OK (see Fig. 30).
8. To run the simulation simply click on the Netlist and Run button (see Fig. 29).
9. Once the simulation has finished the Visualization and Analysis window will pop-up.
10. Here are some useful tips for handling Virtuoso Visualization and Analysis.
  - To plot each graph in different axes, just right click on the name of a graph (for example /IN) and then go Move to→New Strip.
  - To change the color of a graph right click again on its name go to Color and select your preferred color.

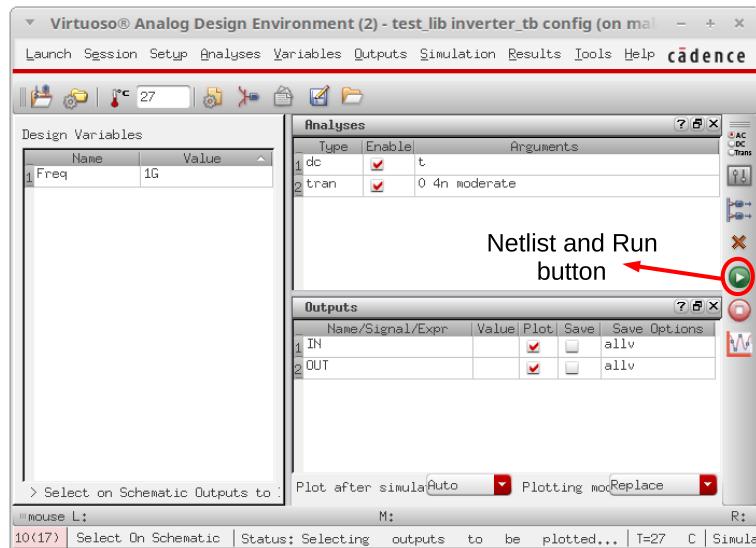


Figure 29: ADE window after setting the analysis and the outputs

- To zoom in right click and drag around the area you want to zoom in. To return to the original preview press 'f'.
- Some times it's really useful to use markers to calculate for example the distance between two points on the graph. To place them press 'a' and you will notice that a marker appears on the graph. Drag and drop it to the point you want. Press 'b'. A second marker appears at a random point on the plot. Drag and drop it to the desired position. The vertical and horizontal distance between the two markers, dy and dx is automatically calculated (Fig. 32).

11. You can export the results to a text file so that they can be analyzed by other tools like MATLAB or EXCEL. To do so click on: File→Open Results. The simulated results are in a psf file format which is located under:

<home\_directory>/simulation/<cell\_name>/<view\_name>/

In this example, the name of the cell is **inverter\_tb** and the view name **config**.

You will observe that the available results are divided into categories to help organization (see encircled region in Fig. 33). Let's suppose we want to export the output voltage result. Firstly, create a folder in your wok directory and name it "datasheets". Then go back to the Visualization and Analysis window and double click on the tran folder under the signals tab (see encircled region in Fig. 33), select "OUT" and right click on it. Select export, and save the results. The results are saved in .csv file format that can be imported in EXCEL.

12. The calculator is the main tool to form expressions and analyze the simulated data. It can be accessed from the main Visualization and Analysis by clicking on Tools→Calculator. The "calculator" window can be seen

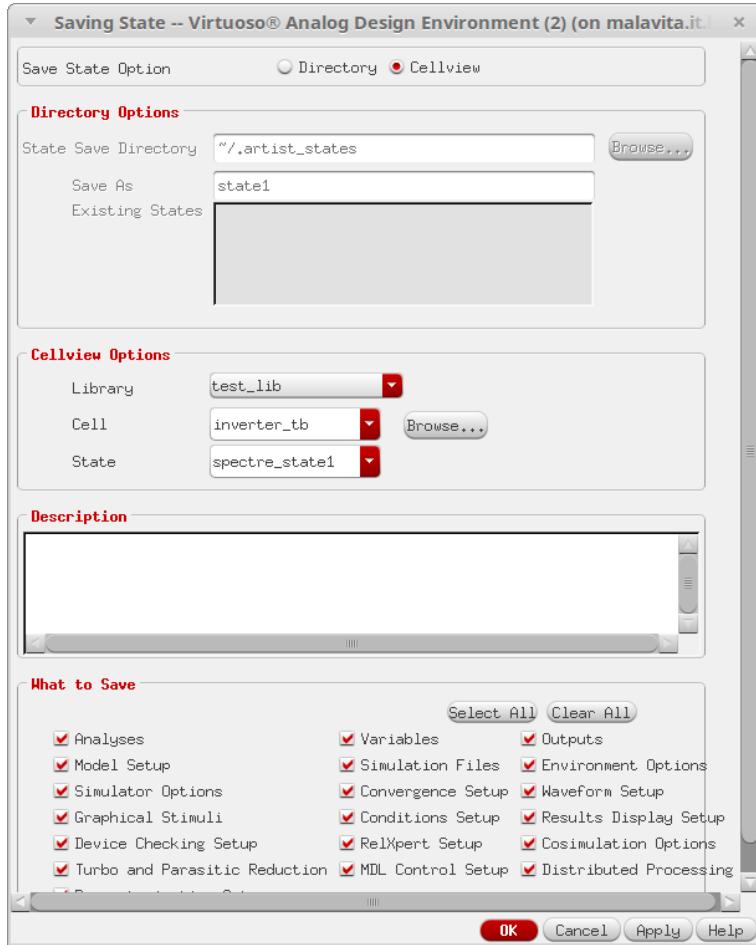


Figure 30: Save current ADE state

in Fig. 34. In this example we will calculate the rise time of the output voltage. To do so:

- Since we are analysing the output voltage of the inverter click on the vt button of the Insert signals section of the calculator and then select the output net from the schematic. You will notice that the expression `VT("/OUT")` is printed in the expression area. Press "ENTER" to save this expression in the stack.
- Switch to the Function Panel in the bottom of Fig. 34. Select the `riseTime` function and fill in the necessary fields as shown in Fig. 35.
- Press OK
- Click on the table button ("Evaluate the buffer and display the results in a table") which is located in the left of the "Append" button (Fig. 35).
- The rise time is found equal to 75.03ps (Fig. 36).

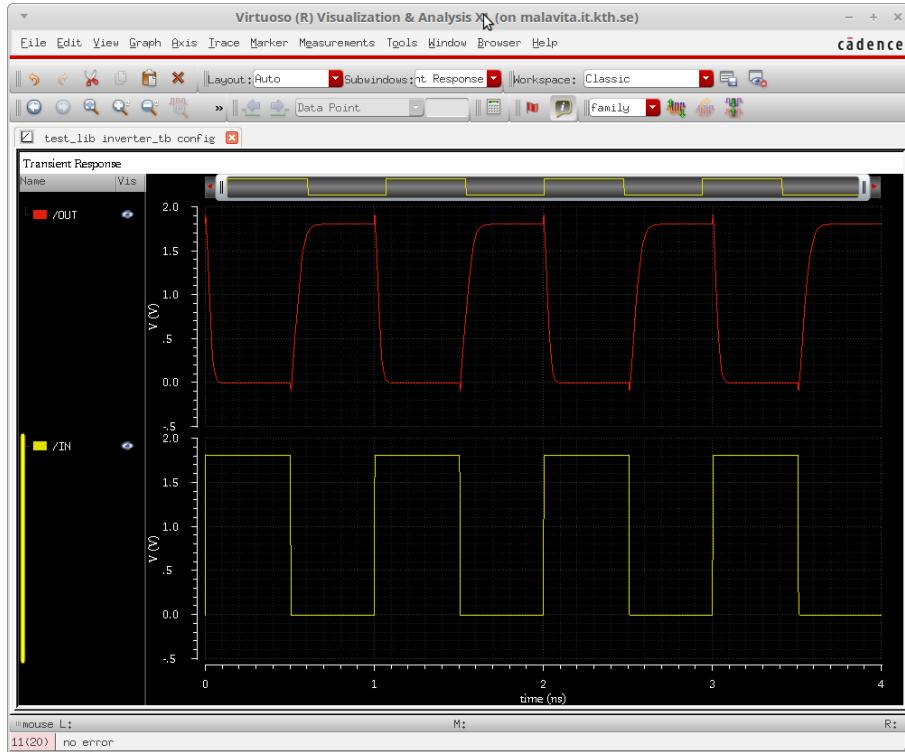


Figure 31: Virtuoso Visualization and Analysis window

- (f) As described previously, you can save the results in a .csv file format.

## 4 Copying Libraries

Sometimes, in a group project, it is needed to copy a library from one user to another, let's say from Zivadin to Antigoni. There are four steps to do that:

1. Zivadin should give Antigoni access rights to read his library (zivLib).
2. Antigoni should create a link to Zivadin's library (zivLib) in her Cadence environment.
3. Antigoni should create a new library (antlib)
4. Antigoni should copy the contents of Zivadin's library (zivlib) to her new library (antlib).

These steps will be described in more details below.

1. Zivadin gives Antigoni access rights to read his library.

In a terminal, Zivadin should:

- Go to his library's directory

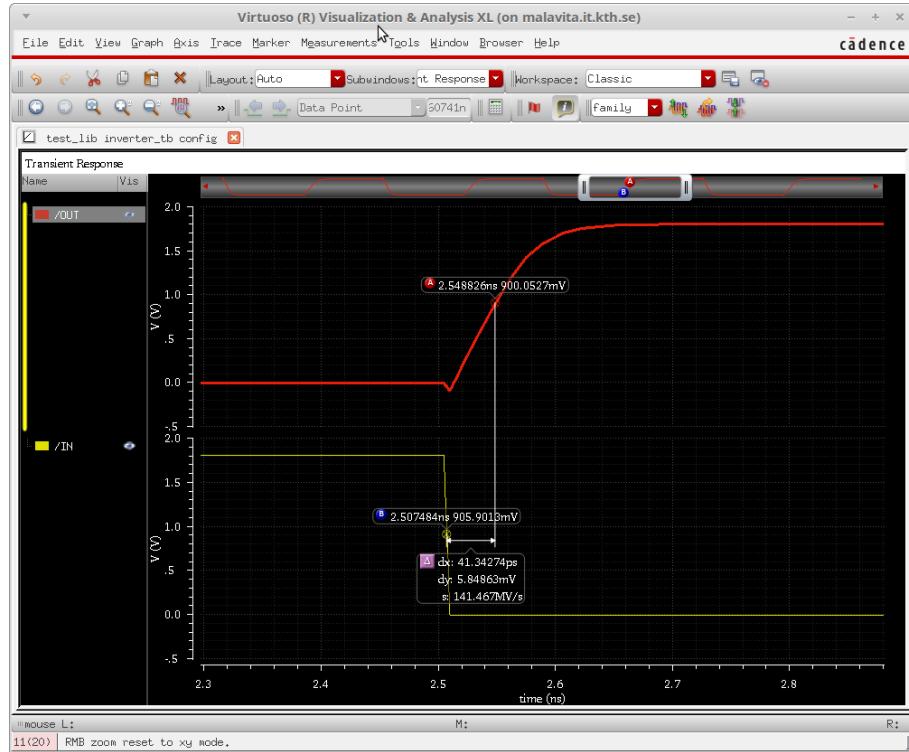


Figure 32: Placing markers in a waveform

- Type the following command:  
`textcolorredfind . -type d -print -exec fs setacl antigoni_username rl \;`
- Do not forget to change "antigoni\_username" to the actual username of the user. Note that this command will not copy the ADE simulation states

2. Antigoni creates a link to Zivadin's library in her Cadence environment
  - From CIW select Tools→Library Path Editor...
  - Under Library type Zivadin's exact library name (zidLib) and under Path type the exact path where Zivadin's library is found.
  - After saving the changes, Antigoni should see zivLib in her library manager.
3. Antigoni creates a new library in her Library Manager, named antLib as described in Subsection 3.1.
4. Antigoni copies the contents of Zivadin's library to her new library. Else, she will not be able to modify the contents of his library.  
 To do so,

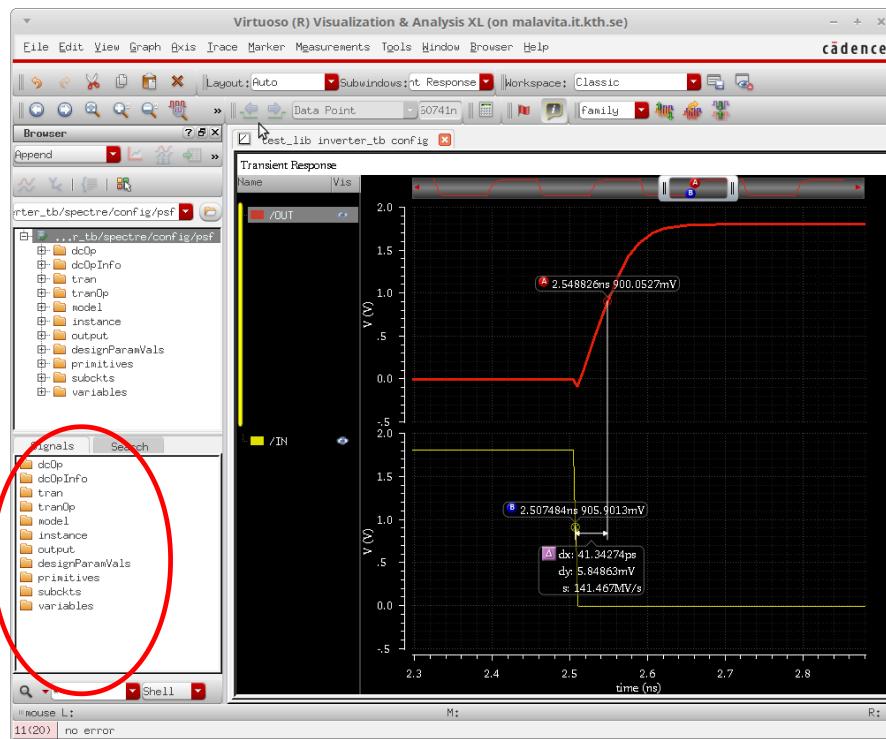


Figure 33: Categorized simulation results

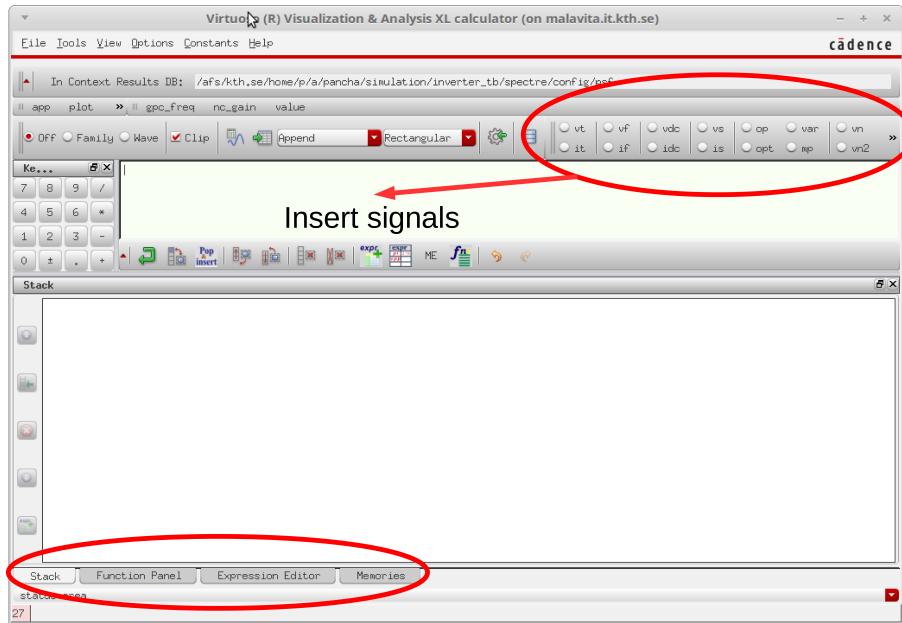


Figure 34: Calculator Window

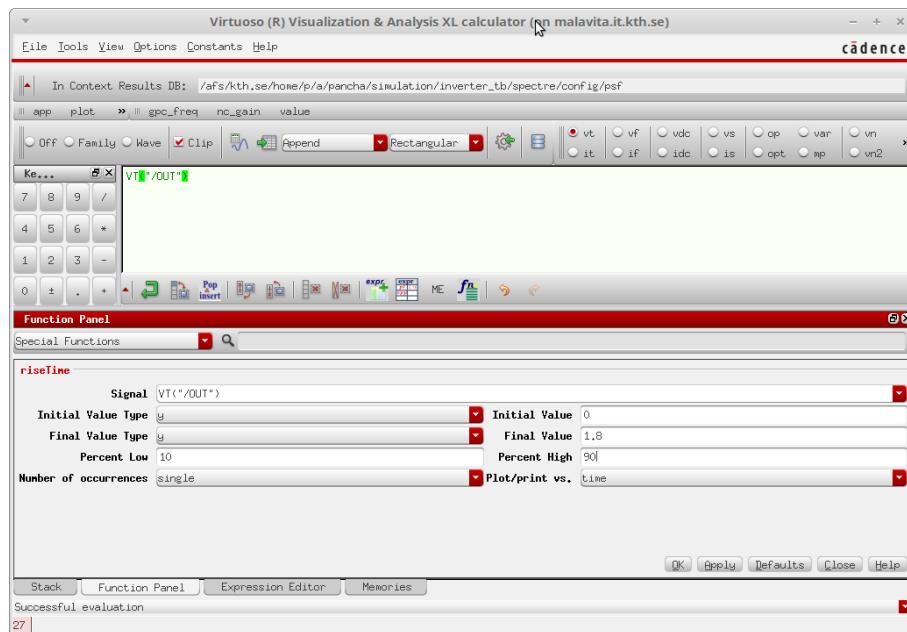


Figure 35: Setup the riseTime function

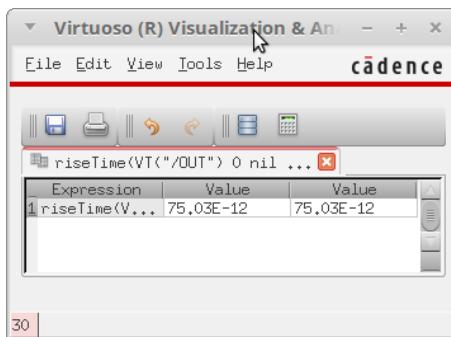


Figure 36: Print Rise Time

- She will right-click on zivlib in the Library Manager and select Copy... . Then she must set the fields "From" and "To" of the pop-up window as well as, click on the "Update Instances" option.
- Antigoni has now Zivadin's library contents in her own local library. Note that the same procedure can be followed regarding the copying of cells from one library to another.

## References

- [1] “Cadence Design Systems,” Available: [https://en.wikipedia.org/wiki/Cadence\\_Design\\_Systems](https://en.wikipedia.org/wiki/Cadence_Design_Systems)
- [2] Cadence tools, “User Guides,” Available: [/afs/kth.se/pkg/cadence/ic/6.1.5/doc](http://afs/kth.se/pkg/cadence/ic/6.1.5/doc)