Tutorial 5
Differential Amplifiers, Opamps, and OTAs

October 31, 2017

1 Introduction

The objective of the following tutorial is to familiarize you with typical analog circuit blocks that are extensively found in the literature. These circuits do not work alone. They are part of a negative feedback systems, so a background on negative feedback will improve your understanding. The first part of the tutorial consists of simulating some differential pairs and a single stage opamps. The idea is to understand differential and common mode gains as well as the the current-mirror load technique. Then, a single ended opamp and OTA are designed for a feedback voltage amplifier. Finally, the design of a differential integrator using a two stage folded differential OTA is presented and its design is described step by step.

Note: *This note applies when you start working on your project and will not be needed for completing tutorial 5. If you encounter problems with the DC operating point when you replace the self-biased transistors and biasing network with real transistors then you need to refer to the Tutorial 5 Appendix on how to perform an STB analysis. If you see a significant drop in the open-loop gain on a Bode plot then go back to the schematic and annotate the DC operating point. This will help you debug the problem.*

2 Schematic Simulation Setup

2.1 Differential Pair

Open the schematic view in the "DIFFERENTIAL" cell. There are 4 simulation setups, as shown in Fig-1, and they are : 1) the differential mode gain, 2) the common mode gain, 3) the diff. amplifier with PMOS loads and 4) the diff. amplifier with current-mirror load. The setups use the same 150 nm CMOS transistor from the previous tutorials.

Launch ADE L and load the state 'AC states' as shown in Fig-2. The voltage gain of the differential amplifier Av_{diff} is the same as in the CS-stage $Av = g_m R_{out}$. The differential transconductance on the other hand is half the transconductance of the CS-stage $g_{m,diff} = g_m/2$. The differential gain is then calculated as follows:

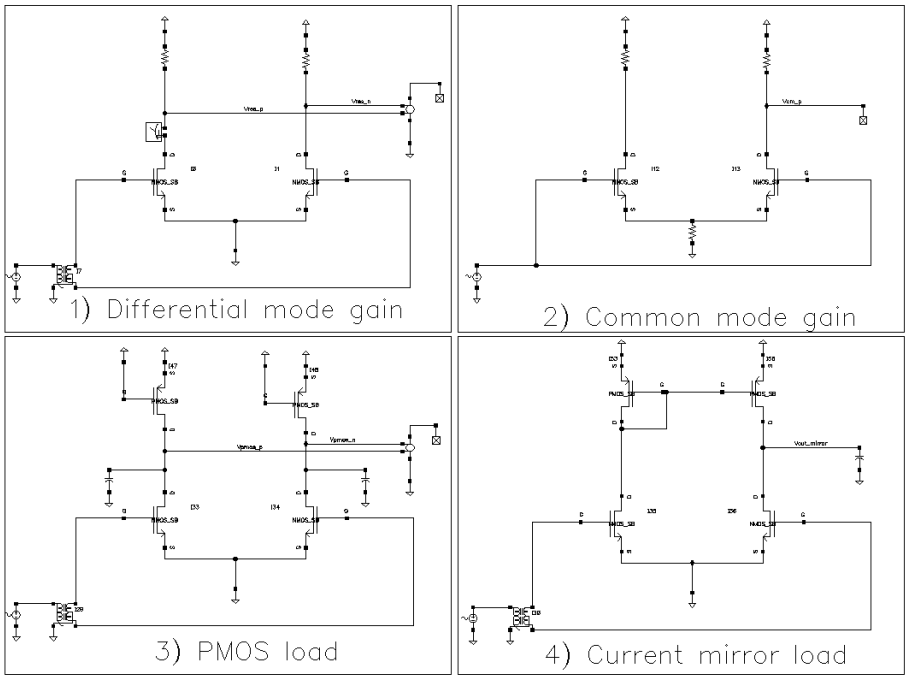

Figure 1: Schematic view in the "DIFFERENTIAL" cell.

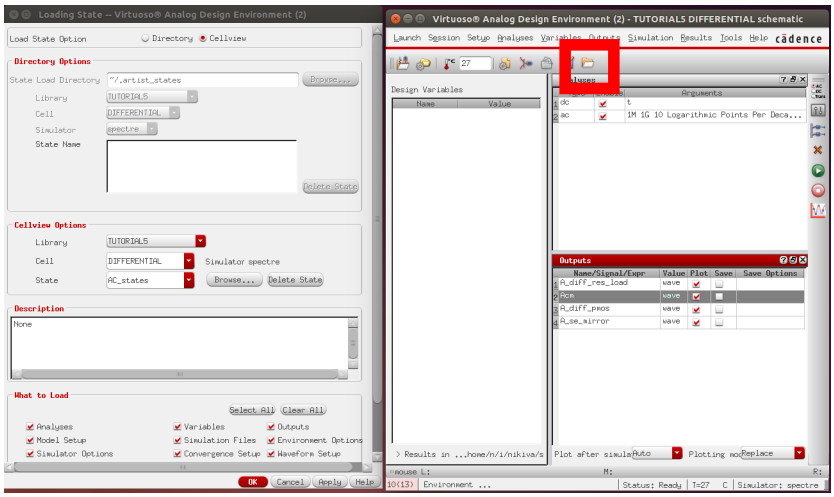

Figure 2: Loading the saved state for AC analysis.

$$Av_{diff} = g_m \cdot R_{out} = g_m \cdot (5k\Omega || r_{dsn}) = 11.85mS \cdot (1.5k\Omega) = 18.25 \quad (1)$$

$$Av_{diff,dB} = 20log(18.25) = 25.2dB \quad (2)$$

$$g_{m,diff} = 5.92mS \quad (3)$$

Run the simulation. The differential gain $A_{\text{diff-gain-res-load}}$ with the resistive load is 25 dB as it can be seen from Fig-3.

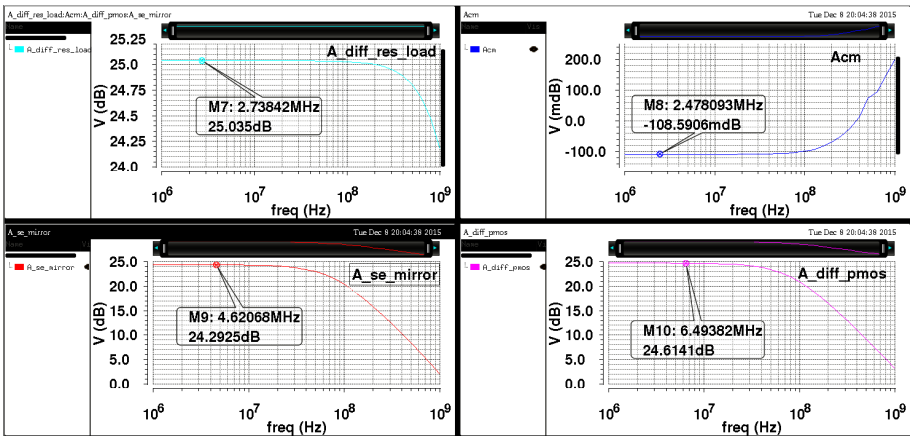

Figure 3: Simulation results for the differential pair.

Fig-4 shows the current that flows through the load R_L (we don't have access to the current flowing through r_{dsn} so we have to use this indirect measurement). Since we are interested in the total output current, we manipulate the current divider formed by r_{ds} and R_L so that:

$$I_{ds} = I_{load} \cdot (r_{ds} + R_L)/rds \tag{4}$$
$$I_{ds} = 1.78m \cdot (2.2k + 5k)/2.2k \tag{5}$$
$$I_{ds} = 1.78m \cdot (2.2k + 5k)/2.2k \tag{6}$$
$$g_{m,diff} = I_{ds}/V_{in}, V_{in} = 1 \tag{7}$$
$$g_{m,diff} = 5.84mS, \tag{8}$$

which is close to what we expected before.

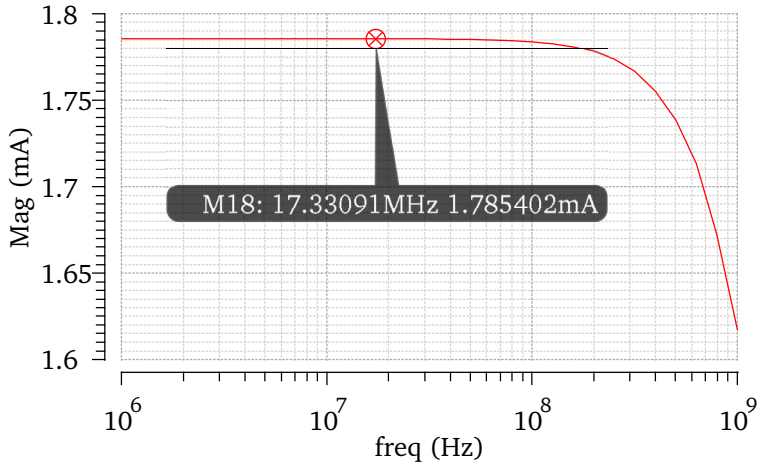

Figure 4: AC current flowing though the R_L.

For common-mode signals the differential pair behaves like a CS stage with source degeneration. The voltage at the terminals of the transistors is the same, so they behave as it were a single transistor with twice the size and twice the transconductance $g_{m,tot} = 2g_m$. The output voltage is:

$$V_{out,cm} = V_{in} \cdot [2g_m/(1 + 2g_m R_S)]R_{out}, \tag{9}$$

where $R_S = 2.2\ k\Omega$ is the output resistance of the current source that provides the DC bias. $R_{out,tot}$ is the total output resistance seen at the drain terminal, which can be calculated as:

$$R_{out,tot} = (R_L||R_L)||\{(r_{dsn}||r_{dsn})(1 + 2g_m R_S)\} \tag{10}$$
$$R_{out,tot} = (R_L/2)||[r_{ds}/2(1 + 2g_m R_S)] \approx R_L/2 \tag{11}$$
$$R_{out} = 2.5k\Omega \tag{12}$$
$$Av_{cm} = [2g_m/(1 + 2g_m R_S)]R_{out} \tag{13}$$
$$Av_{cm} = 0.989\ (\text{ -0.1 dB}) \tag{14}$$

Marker 8 in Fig-3 shows that the simulated common mode gain is -0.108 dB at lower frequencies and that it starts increasing with frequency.

Frequency response of the differential pair does not differ from the CS stage. Fig-3 also shows the simulation results for a differential amplifier with PMOS loads and a current mirror. The second configuration is commonly used as a differential to single ended conversion stage. Both configurations have the same differential gain capabilities $Av = g_m(r_{dsn}||r_{dsp})$.

The noise performance of the differential pair is worse than in the CS state since now we have two transistors and resistors contributing noise for the same voltage gain. The value of the thermal noise is around -178 dBV/$\sqrt{\text{Hz}}$ as shown in Fig-5, which is approximately 3 dB larger than in the CS stage. On the other hand, the input referred noise current is halved due to the increase in the input impedance. The reader is invited to confirm this behavior.

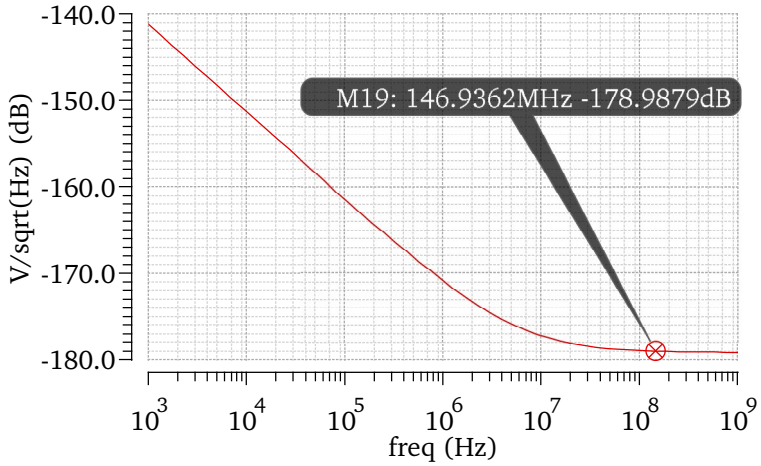

Figure 5: Input referred noise of a differential pair with resistive load.

2.2 Opamp Design

The following part of the tutorial consists of the design of a voltage amplifier with 20 dB of gain and unity gain frequency of 400 MHz. Open the schematic view in the "OPAMP TESTBENCH" cell, which is shown in Fig-6. The schematic contains four setups, as shown in Fig-6, which are: 1) the opamp signal path, 2) the amplifier prototype, 3) the biased opamp and 4) the biased amplifier prototype.

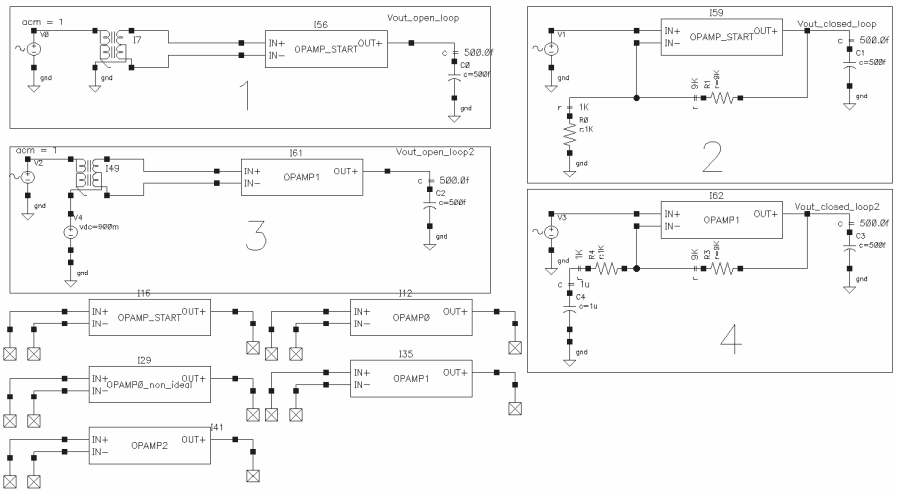

Figure 6: Schematic view in the "OPAMP TESTBENCH" cell.

One way to implement the opamp is to just use a differential pair. Before trying more sophisticated circuits, we will take a look at a simple amplifier implementation using only a differential pair and then we will draw some conclusions.

Go inside the hierarchy of "OPAMP START" symbol by pressing $\langle e \rangle$ on the

keyboard and then clicking on the symbol. You will see the schematic as shown in Fig- 7.

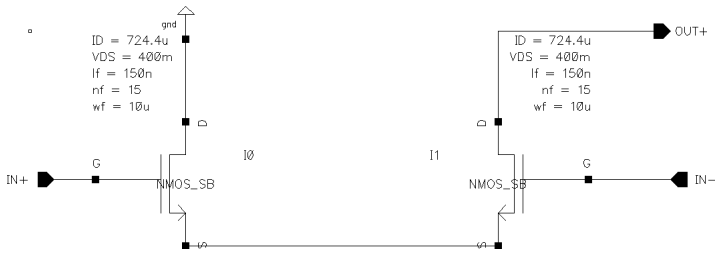

Figure 7: Schematic view in the "OPAMP START" cell.

We are still using the same 150 nm CMOS transistor that was used in the previous exercises.

The total current flowing out of the differential pair is $I_{diff} = V_{in}g_m/2$, the reader is referred to the [2] for a more detailed explanation. At this point we are going to assume ideal biasing. Accordingly, V_{out} can be expressed as:

$$V_{out} = V_{in}(g_m/2)r_{ds,n} \tag{15}$$

Return to the test bench schematic and run the simulation. The simulated voltage gain is 28 dB (25) as shown in Fig-8 . The first pole is around 60 MHz, and the unity gain bandwidth is 1.76 GHz.

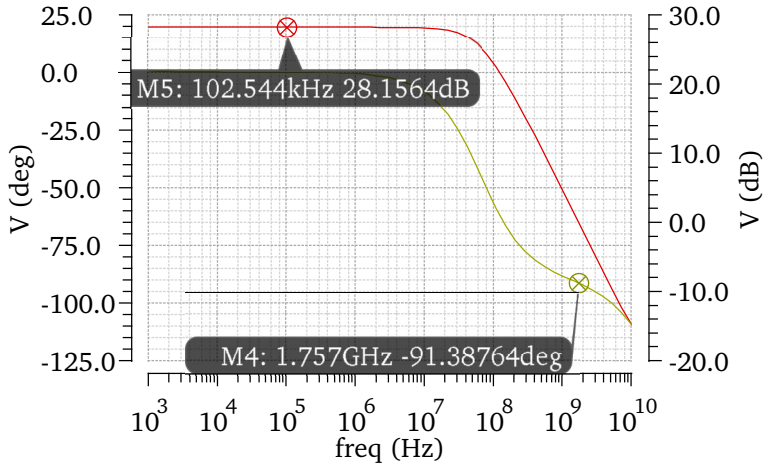

Figure 8: Bode plot of the "OPAMP START" block.

We are interested in the accuracy that this gain can provide for our 20 dB amplifier. We use the feedback network model to find the closed-loop gain.

$$Af = A_{fDC} \cdot (A\beta)/(1 + A\beta) \tag{16}$$
$$Af = 10 \cdot (25/10)/(1 + 25/10) = 7.14 \text{ (17 dB)} \tag{17}$$

The closed-loop gain of the prototype amplifier is 6.47 as shown in Fig-9. Despite that the output is loaded by the feedback, the estimation is very good. The accuracy of the voltage gain is not good. We can adjust the feedback components to compensate the low loop gain. However, process, temperature, and voltage variations will change the gain value in a random way and in practice the voltage gain will drift. Also, distortion due to nonlinearities is only partially corrected by the loop. In some cases, our application can tolerate these issues, but in general better accuracy is required. A loop factor $A\beta$ of only 2.5 is not enough and we conclude that we need to increase the open loop gain.

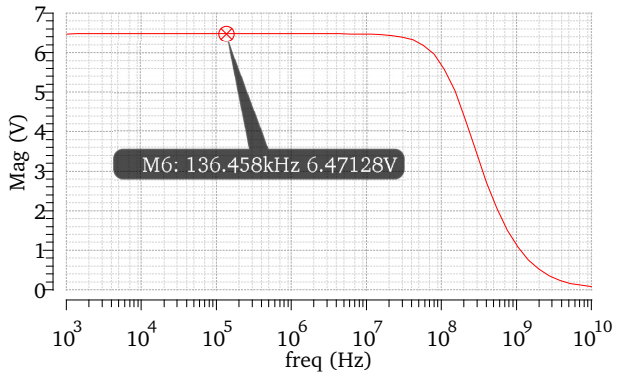

Figure 9: Closed loop gain with the "OPAMP START" block.

Now you will replace the test blocks in (1) and (2) for OPAMP0. Go inside the hierarchy of OPAMP0. You will see the schematic shown in Fig-10:

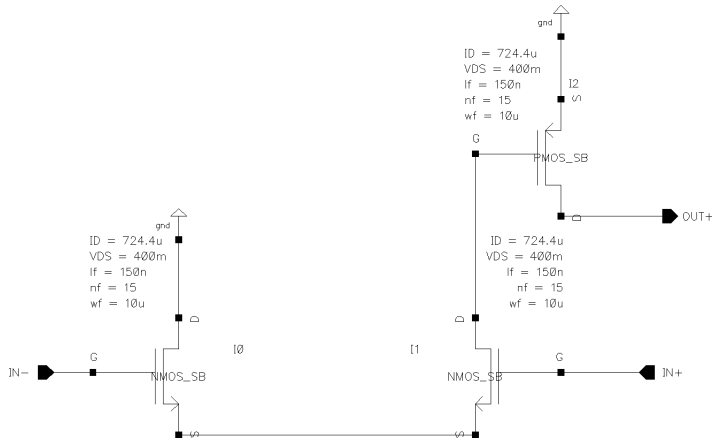

Figure 10: Schematic view in the "OPAMP0" cell.

We have added a CS stage in order to improve the open-loop gain. In this case we added a PMOS stage (we could have added an NMOS CS stage, but for biasing reasons that will be evident soon it is practical to use the PMOS). The gain of the amplifier should now increase by a factor of $g_{mp}r_{ds,p}$. Return to the test bench schematic and run the simulation.

The open loop gain is now 59 dB as can be seen from Fig-11, an improvement when compared to the previous implementation. We notice, however, that the addition of an amplifying stage added also a pole (it is possible to see a zero as well) and now the phase margin is 0 degrees when the gain is 0 dB. We are considering ideal biasing and in practice the gain will drop somewhat when we implement the additional biasing circuitry. Accordingly, we will forget for a moment this detail and continue.

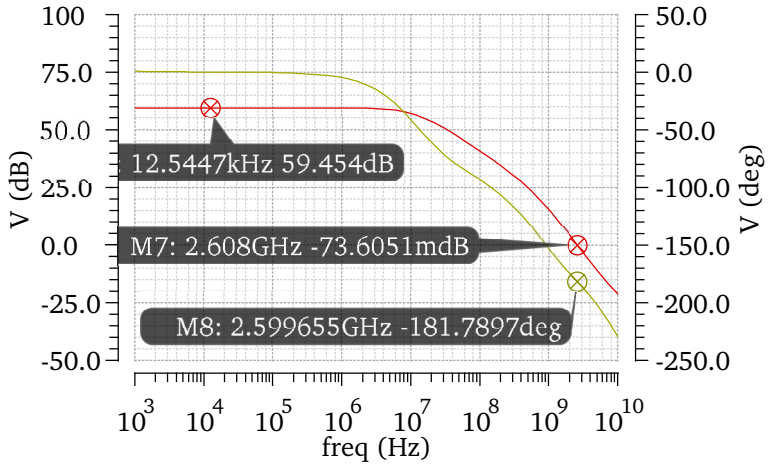

Figure 11: Bode plot of the "OPAMP0" block.

Now we check how accurate is this amplifier. The closed-loop gain of the amplifier shown in Fig-12 is 9.91, which is far better than before. We can also see a frequency peek at around 800 MHz, which is another symptom of instability.

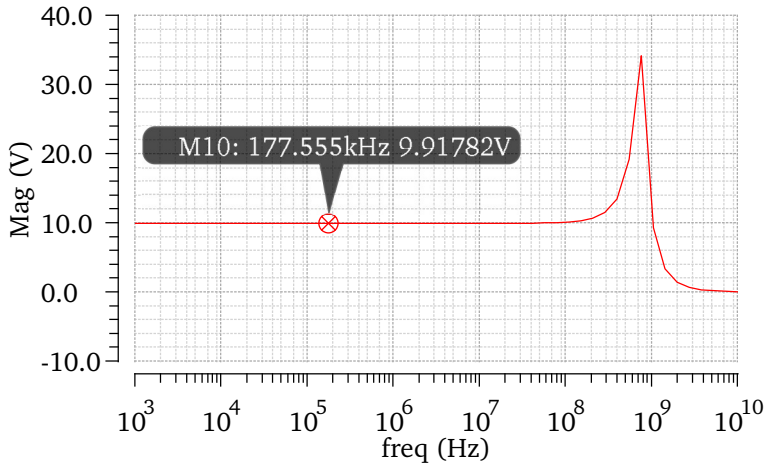

Figure 12: Closed loop gain of the "OPAMP0" block.

We are happy with the open loop gain of this configuration. Now we will add some non-idealities in order to account for the resistance of the current sources. We assume for instance that single-transistor current sources will be used and

that $r_{ds} \approx 5$ kΩ (You can be more accurate and run the PMOS BIAS template for extracting very accurate values). We will also add some Miller compensation as can be seen in Fig-13:

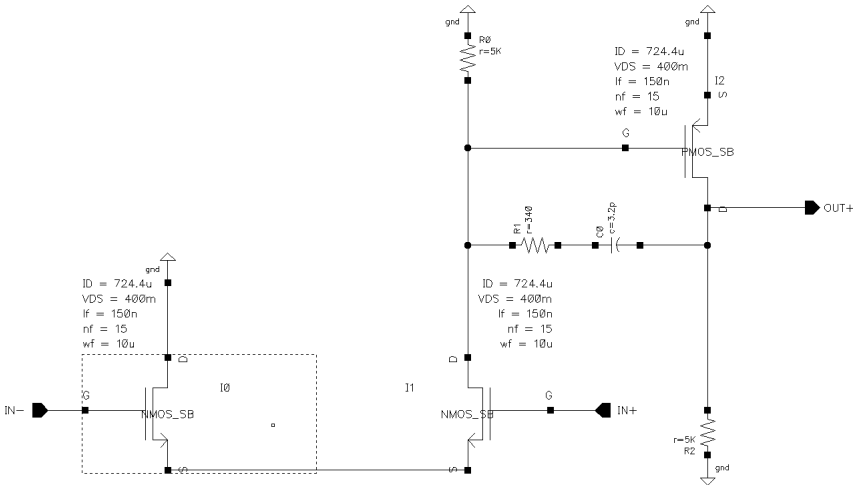

Figure 13: Schematic view in the "OPAMP0 non ideal" cell.

We return to the test bench and run the simulation. The gain dropped to 48 dB as can be seen from Fig-14 which is a bit discouraging but also expected since those resistances appear in parallel. We may use cascode current sources to improve the resistance at expenses of voltage headroom, but for now we will accept the circuit as it is. After changing the values of R1 and C2, we split the poles and obtain a phase margin of 92 degrees. Detailed procedure on how to chose the values for the compensation network are given in [1].

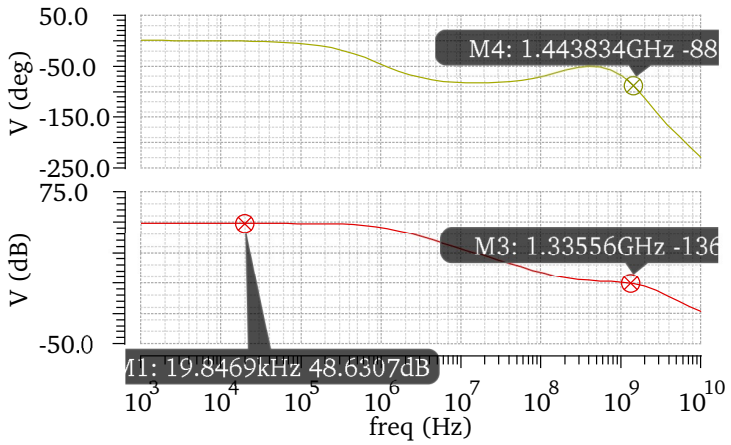

Figure 14: Bode plot of the "OPAMP0 non ideal" after the compensation.

We check the accuracy of this configuration. The closed-loop gain is 9.62 or 19.2 dB as can be seen from Fig-15, a very close value to our 20 dB target. We are content with these results and continue improving the signal path of the circuit.

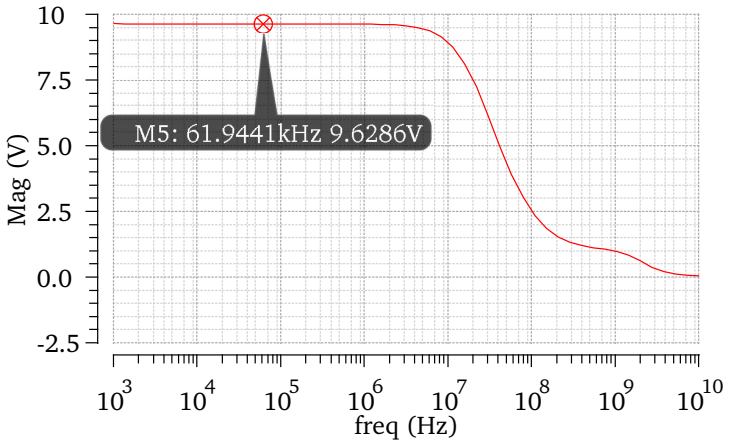

Figure 15: Closed loop gain of the "OPAMP0 non ideal" after the compensation.

Now it is time to replace the signal path with more non-idealities. Replace the block "OPAMP0 non ideal" in (1) and (2) with "OPAMP1" shown in Fig-16.

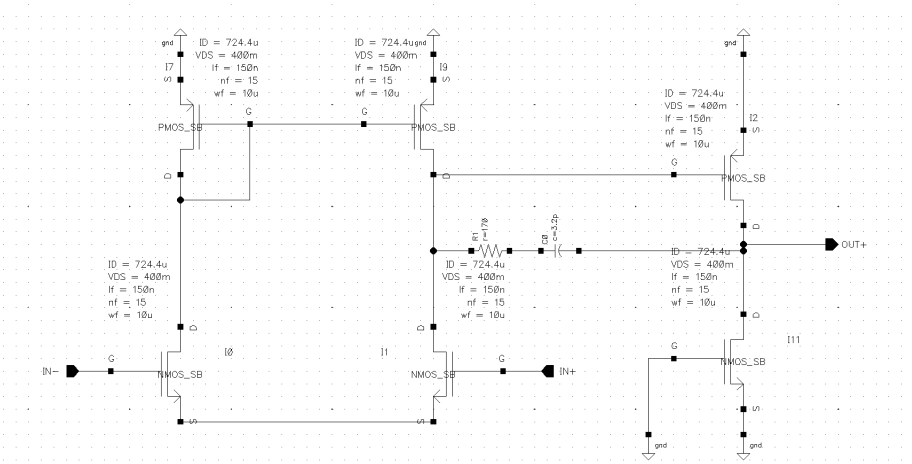

Figure 16: Schematic view in the "OPAMP1" cell.

Some of the biasing transistors that are affecting the signal path have been included. Notice that the current mirror load has been used. This is a useful configuration since it combines the AC current of the two input transistors so that the gain of the first stage is $g_m(rds_n||rds_p)$ the reader is referred to [2] for a detailed analysis. The current source of the second stage is now also modeled more accurately. Return to the test bench and run the simulation.

The open-loop gain is now 46.26 dB as can be seen from Fig-17, while the parasitic capacitances moved the position of the poles. The compensation resistor was adjusted to maintain the phase margin of 80 degrees. The closed-loop gain is 9.55 (19.6 dB) as can be seen from Fig-18. We are content with this design and decide that it is mature enough to enter in the biasing stage.

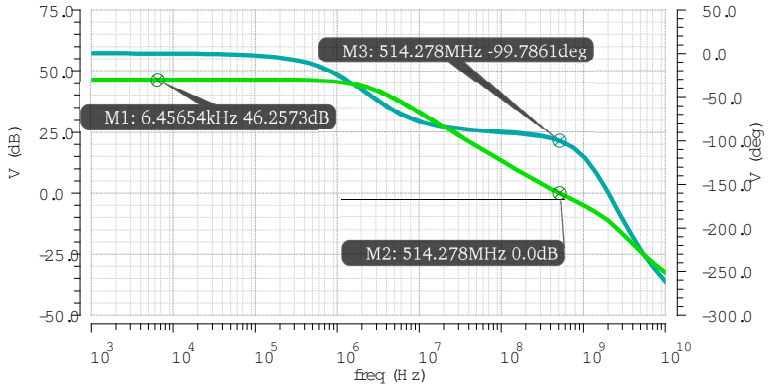

Figure 17: Bode plot of the "OPAMP1" block.

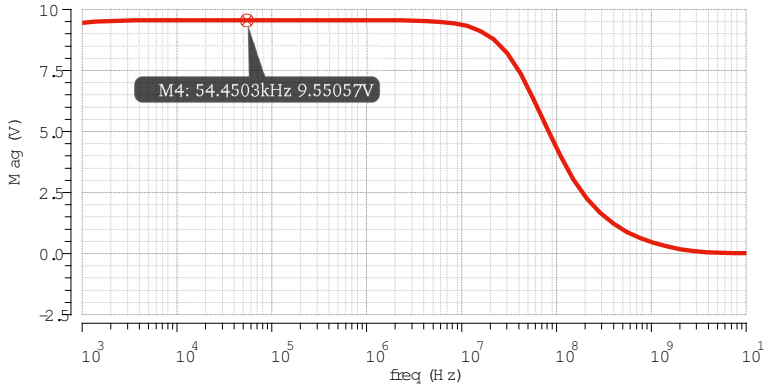

Figure 18: Closed loop gain of the "OPAMP1" block.

Replace the blocks under test by "OPAMP2" blocks. Enter in the "OPAMP2" hierarchy which is shown in Fig-19:

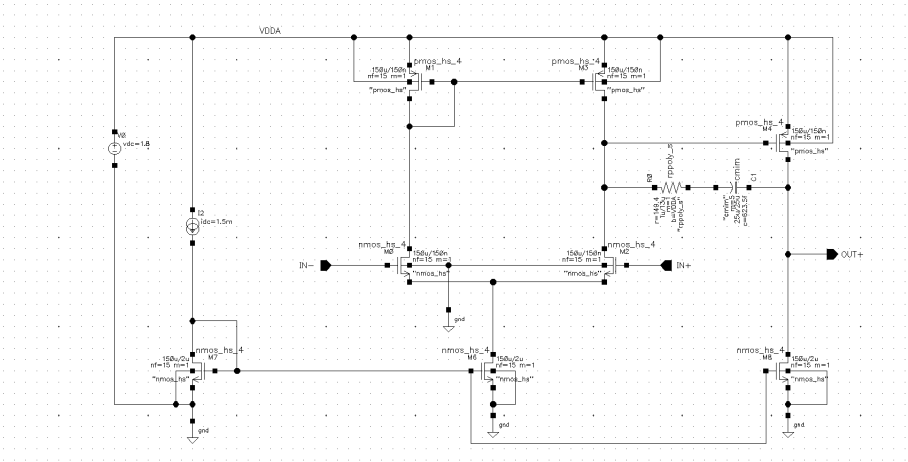

Figure 19: Schematic view in the "OPAMP2" cell.

A current reference is used to generate the biasing currents for the differential pair and the second stage. Notice that the sizes of M_7 and M_8 are equal while M_6 has double the number of fingers. Due to symmetry $V_{sd1} = V_{sd3} = V_{sg4}$. This will keep the NMOS and PMOS currents at the second stage more or less equal (the output however is floating and is only well defined when the feedback components are present).

Go back to the test bench and run the simulation. In the ADE menu bar select "Results/Annotate/DC operating point". Enter again into the OPAMP2 schematic from the closed loop configuration. You will see the voltages and currents at each node as shown in Fig-20. Check whether the values are the same as expected.

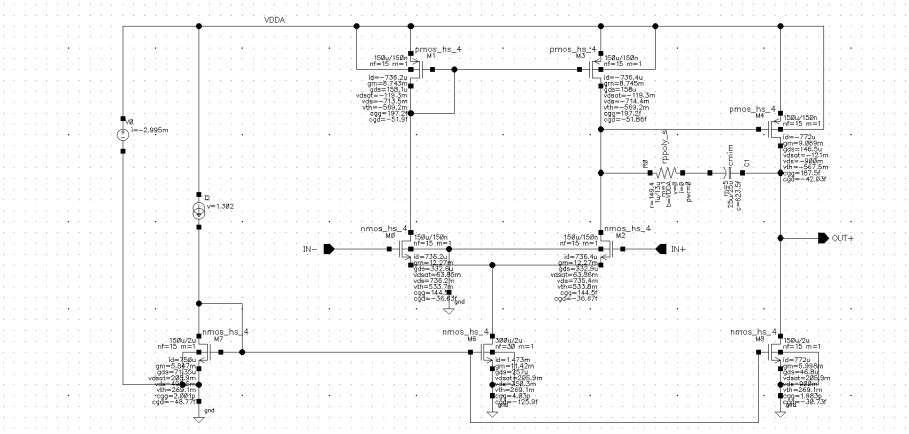

Figure 20: DC operating point of the "OPAMP2" block.

The open-loop gain has increased to 61.4 dB because the length of the current sources has been increased from 0.15 nm to 2 μm to improve the current matching accuracy by reducing the effect of channel length modulation. Note that the same can be said for the current mirror load in the differential pair, which you are welcome to try changing on your own and analyze the change in the bode plot.

The phase margin is around 74 degrees, so there was not a significant change from the signal path simulation as it can be observed in Fig-21.

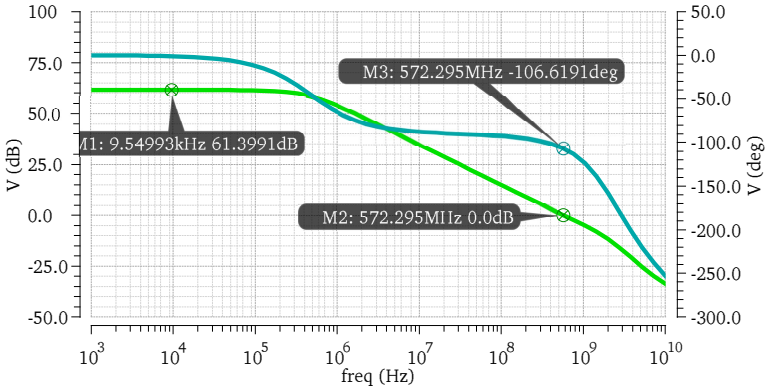

Figure 21: Bode plot of the "OPAMP2" block.

The closed loop gain is 9.87 (19.88 dB) as shown in Fig-22. Notice a zero at low frequencies coming from a coupling capacitor in the feedback. This capacitor prevents DC current flowing from the output to ground. However, it reduces the accuracy at very low frequencies. If DC is not part of our information signal (most modulation schemes are DC free), this may be acceptable.

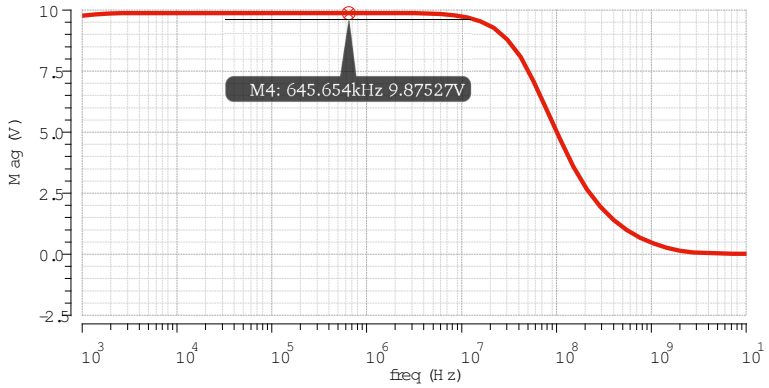

Figure 22: Closed loop gain of the "OPAMP2" block.

The amplifier is ready, but still an important stability test is missing, which is the step response. Open the schematic view in the "OPAMP TEST BENCH TRAN" cell. There are 2 simulation setups as shown in Fig-23: the 20 dB prototype amplifier (1) and a voltage follower (2). Run the simulation.

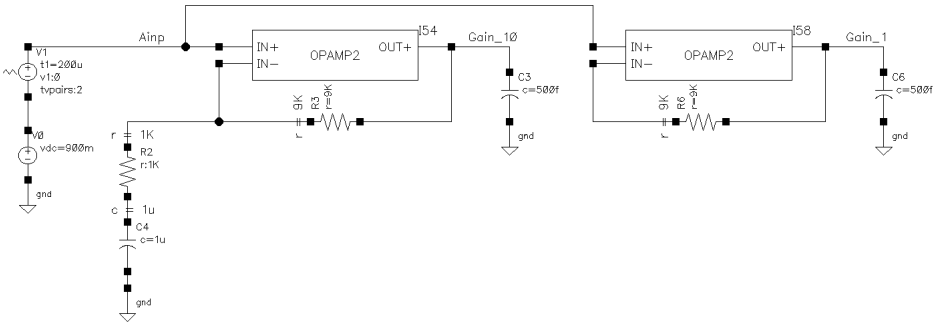

Figure 23: Schematic view in of the "OPAMP TEST BENCH TRAN" cell.

The plot in Fig-24 shows the step response of the amplifier. The step transition time has to be very quick in order to excite the very high frequency response. For the case when the voltage gain is 10 the response is an over damped exponential signal without oscillations, while for the case of unity gain the response has some ringing but it quickly settles.

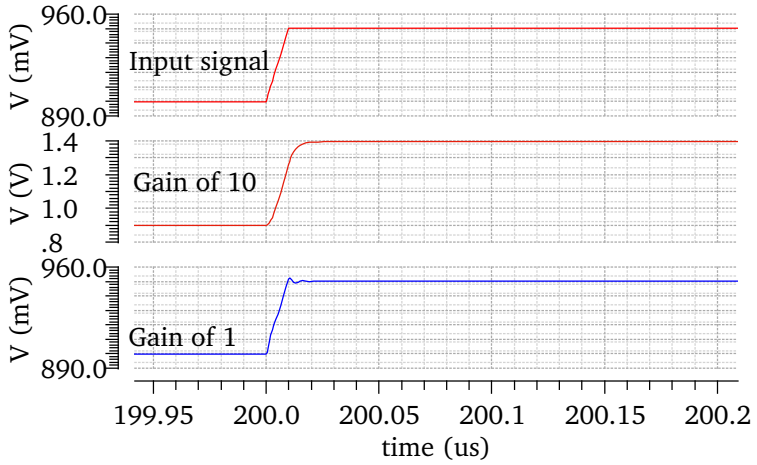

Figure 24: Step response of the "OPAMP2" for two gain configurations.

Go inside the OPAMP2 hierarchy and disconnect the compensation capacitor from the amplifier. Return to the test bench and run the simulation again. Both plots show now overshot and oscillations as seen in Fig-25.

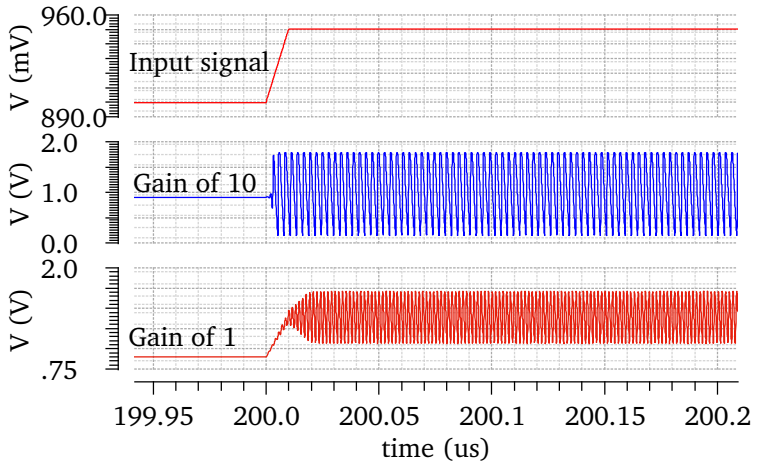

Figure 25: Step response of the "OPAMP2" for two gain configurations.

2.3 OTA Design

In the previous design we added a CS stage to our differential pair in order to increase the loop-gain. The reasoning is that the CS stage has better gain capabilities than the other stages. However we saw that it added a dominant pole that contributed to instability. Another option is to stack a CG stage at the output so that it becomes a cascode.

Open the design "OPAMP TESTBENCH2" schematic. The setup is the same as for the previous design shown in Fig-6, the only difference is that the load capacitor is now 3pF and that the feedback resistors are 90 kΩ. and 10 kΩ.

Replace the block in (1) and (2) for "OTA0". Enter the hierarchy, you should see the same circuit as shown in Fig-26.

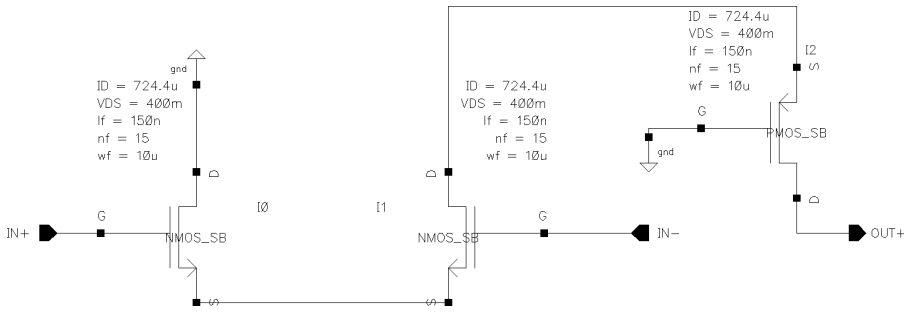

Figure 26: Schematic view in the "OTA0" cell.

The signal path now includes the differential pair and a PMOS cascode transistor (we could have used an NMOS as well, but we anticipate that stacking

it will cause problems due to limited V_{dd} and we decide to already fold it in this level of design). We decided arbitrarily that the PMOS has the same size and bias as the NMOS transistors (This will not probably give the best performance, but it is a good starting point). Return to the test bench and run the simulation.

The open-loop gain of this amplifier is 60 dB, while the dominant pole (due to the high output resistance and load capacitor) makes it very stable with more than 87 degrees phase margin as can be seen in Fig-27. The positive phase shift at low frequencies is caused by the large decoupling capacitors in the self-biased transistor that occurs in a cascode configuration. This effect will not appear when we properly bias the transistors and therefor we will ignore this effect.

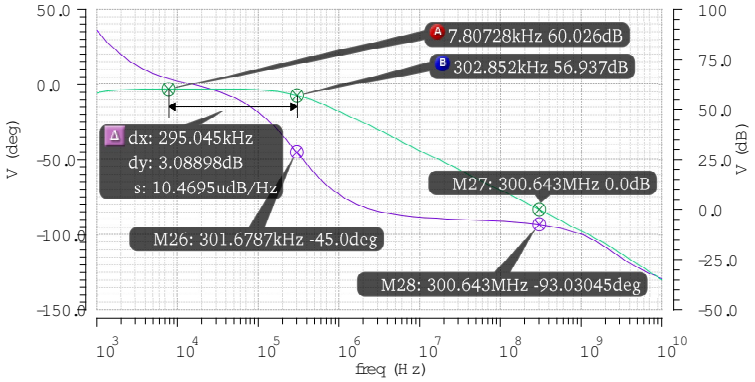

Figure 27: Bode plot of the "OTA0" block.

Now we check the prototype amplifier with the feedback components. In this case we increased the size of the feedback resistor so that they do not load the high output impedance of the cascode and degrade the loop-gain. (Notice that the price to pay for this is an increase of noise). The closed-loop gain is 10.59 or 20.49 dB as shown in Fig-28.

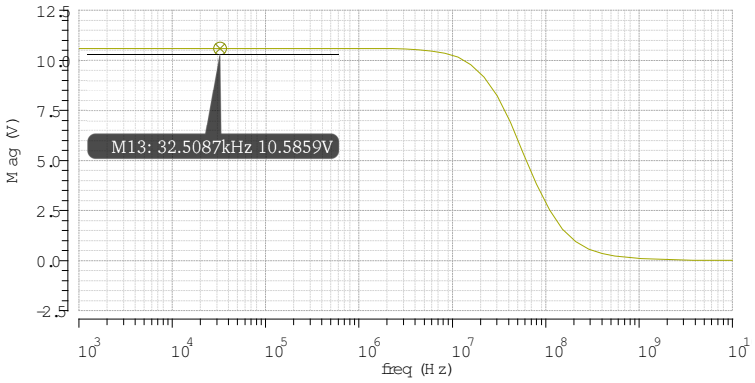

Figure 28: Closed loop gain with the "OTA0" block.

We are happy with this signal path and now we will add some of the non-idealities due to the biasing. Replace the blocks "OTA0" with "OTA1" in (1) and (2). Go inside the hierarchy, the signal path is shown in Fig-29.

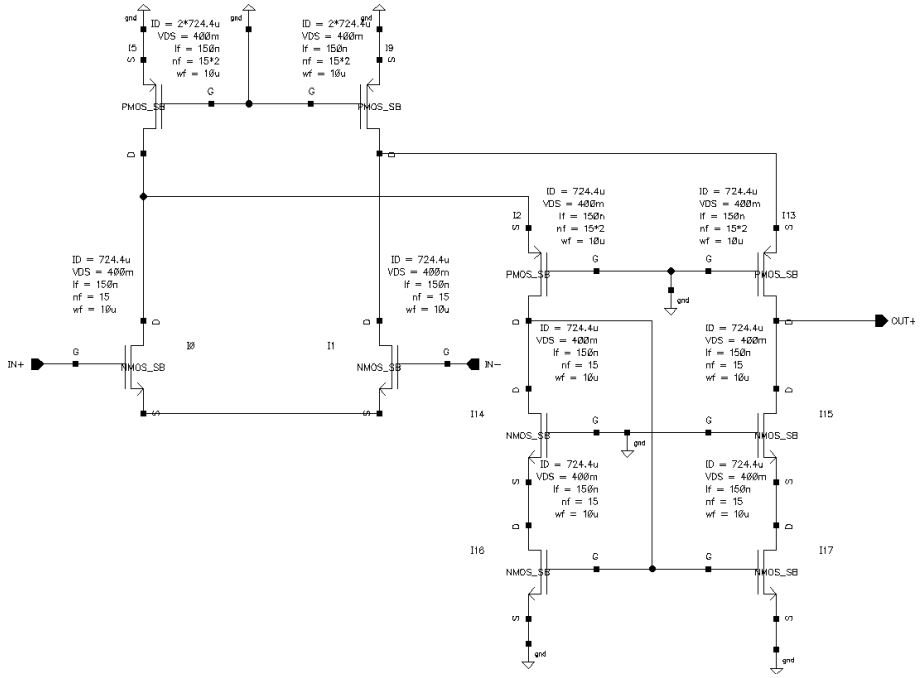

Figure 29: Schematic view in the "OTA1" cell.

We have added single-transistor PMOS current sources on the top. Notice that these sources must supply current for both the differential pair and the folded cascode structure. Also, in the same way as in the previous opamp, we are reusing the AC current of both input transistors with a current mirror. However, this time this is a wide swing cascode current mirror. Study the circuit for a moment and come back to the test bench. Run the simulation.

The open loop gain degraded to 49.78 dB as can be seen in Fig-30. The phase margin is around 73 degrees, still very good.

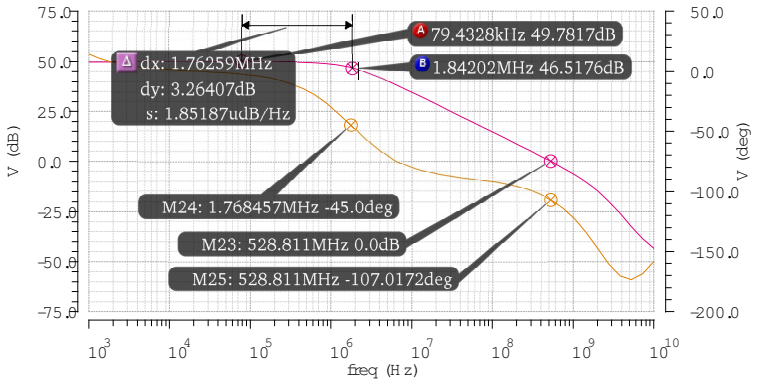

Figure 30: Bode plot of the "OTA1" block.

The closed loop gain of the prototype is 10.4 (20.3 dB). as can be seen in Fig-31. We are content with our signal path design and now we decide to bias it.

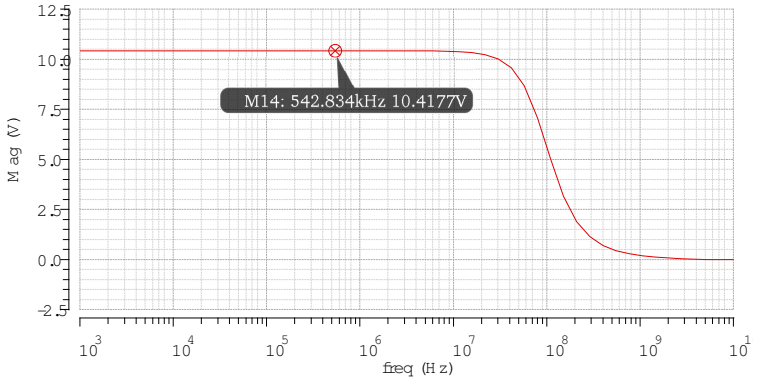

Figure 31: Closed loop gain with the "OTA1" block.

Enter the hierarchy of the "OTA2" block as shown in Fig-32. The biasing currents and voltages are derived from a single current reference. Notice how the biasing of the cascodes is implemented. We have some freedom to bias those cascode-transistors but we have to be careful. Once the currents are set, the V_{gs} of the cascodes will set the V_{ds} of the PMOS current sources M_1 and M_3 and also of M_{12} and M_{11} at the bottom of the current mirror. In this case the resistors were used to obtain these voltages, triode transistors can be used as well as diodes.

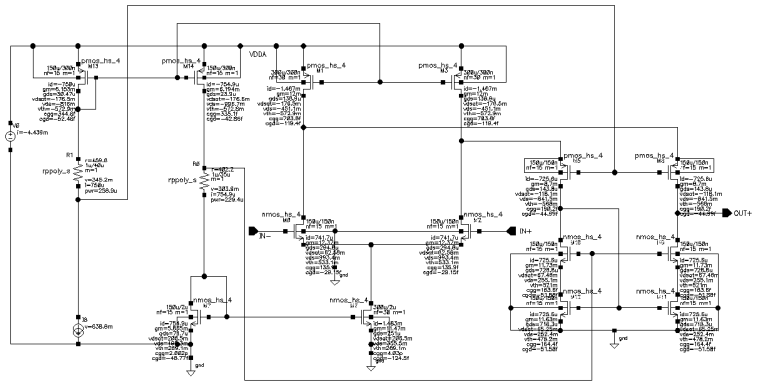

Figure 32: Schematic view in the "OTA2" cell.

Select Results/Annotate/DC operating point. Check the currents and voltages. Is there enough voltage headroom for each transistor? The open-loop gain of the biased block is 49 dB and the phase margin is 68 degrees as can be seen in Fig-33.

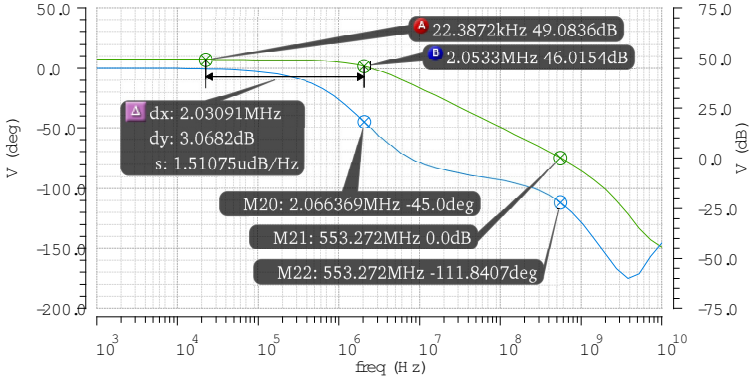

Figure 33: Bode plot of the "OTA2" block.

The gain of the biased prototype with feedback is 9.7 or 19.7 dB as can be seen in 34.

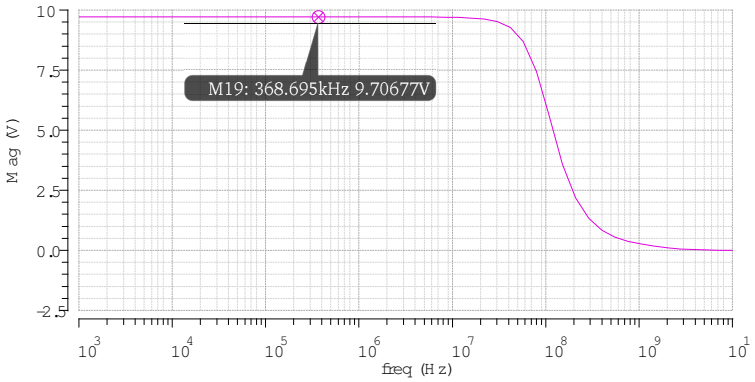

Figure 34: Closed loop gain with the "OTA2" block.

2.4 Differential OTA

Most of the RF/AMS circuits are differential and hence it is important to know how they are implemented. This example shows the implementation of the differential integrator given in Fig-35:

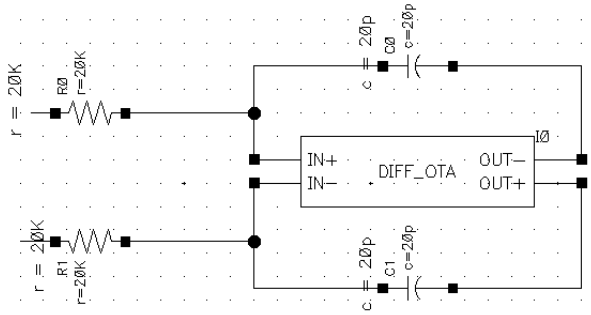

Figure 35: Block diagram of a differential integrator.

The closed-loop gain of the integrator is:

$$Av = \frac{-1}{sRC} \tag{18}$$

$$Av = \frac{2.5 \cdot 10^6}{j\omega} \tag{19}$$

At low frequencies, the closed loop gain can be very high. For instance, Av 400 (52 dB) at 1 kHz. Accordingly, we will need quite a lot of open-loop gain close to DC. Av drops when increasing the frequency at -20dB/dec rate. At 400 KHz, the gain drops to 0dB, and at 4MHz it drops to -20 dB.

Open the file "OPAMP TEST BENCH DIF2". Like the previous examples, you will see four simulation setups as shown in Fig-36.

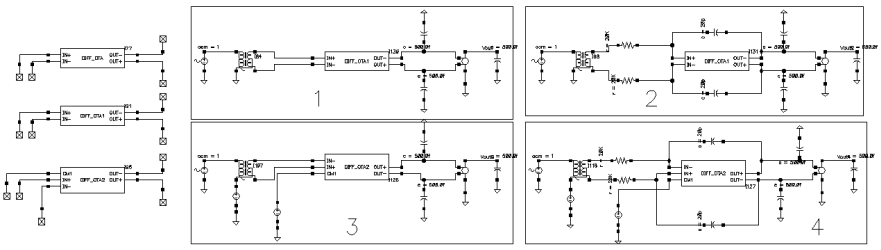

Figure 36: Schematic view in the "OPAMP TEST BENCH DIF2" cell.

Replace the blocks under test in (1) and (2) in Fig-36 with "DIFF OTA". Study the signal path of the "DIFF OTA" block shown in Fig-37. Besides the cascode stage, we have added a CS stage in order to obtain higher gain than in the previous cases. This is needed because the integrator has a large gain at low frequencies. Notice that we have already placed some compensation. Return to the test bench hierarchy and run the simulation.

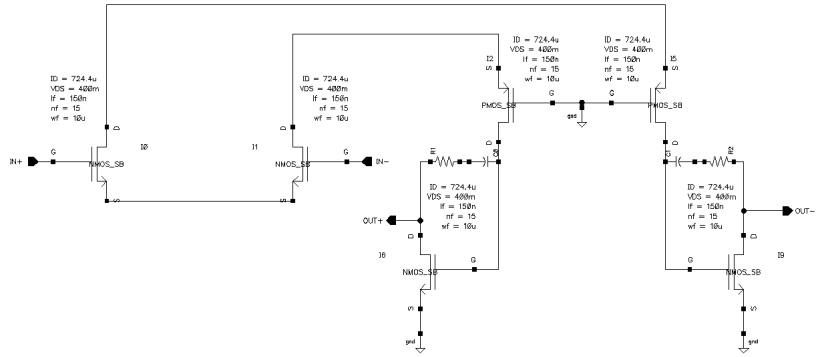

Figure 37: Schematic view in the "DIFF OTA" cell.

The open-loop gain is show in Fig-38 and is 87.8 dB, a very high value. The stability was controlled using Miller compensation. Before compensation, the first pole was located at around 400 kHz (you can disconnect the compensation capacitors and run the simulation to check the initial conditions). After compensation, the pole was moved to around 20 KHz. This was the price to pay for stabilizing this circuit with pole-splitting Miller compensation. In this case it is not so detrimental since the integrator has a $1/s$ slope and drops its gain with frequency. At 1 kHz the amplifier has a closed-loop gain of 52 dB. The open-loop gain is 87 dB at 1 kHz, so we expect the integration function to be quite accurate.

The closed-loop gain shown in Fig-39 represents the transfer function of the integrator. We can see that the magnitude of the transfer function drops at -20dB/dec for frequencies up to 100 MHz. However, we are not only interested in the magnitude. The integration function introduces exactly 90 degrees phase

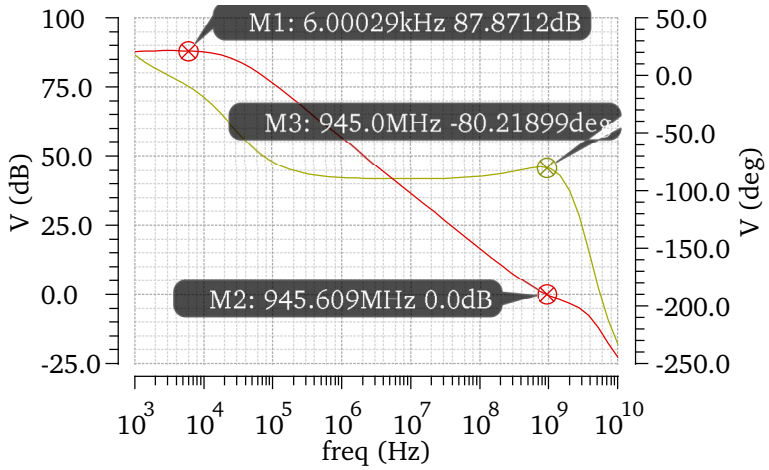

Figure 38: Bode plot of the "DIFF OTA" block.

shift, and variations on the phase will degrade our results. Additionally, we can see that there is a phase of -90 degrees from around 10 kHz Hz to around 40 MHz. The increase in phase at lower frequencies is due to the self biased transistor decoupling capacitors as mentioned earlier. We are satisfied with the precision and move forward with adding non-idealities to our signal path.

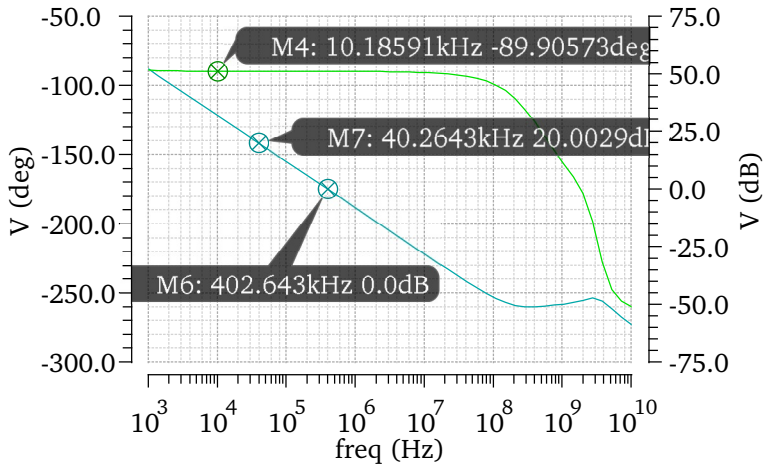

Figure 39: Closed loop gain of the "DIFF OTA" block.

Replace the blocks under test in (1) and (2) in Fig-36 with "DIFF OTA1". Go inside the hierarchy of "DIFF OTA1". We have added more non-idealities like the PMOS current sources at the first stage, the NMOS cascode current sources, and also the PMOS current source at the second stage. Notice that the PMOS current sources now have to provide current for both the input differential pair and also for the folded cascode. Therefore, their bias current is twice that of the input and cascode transistors.

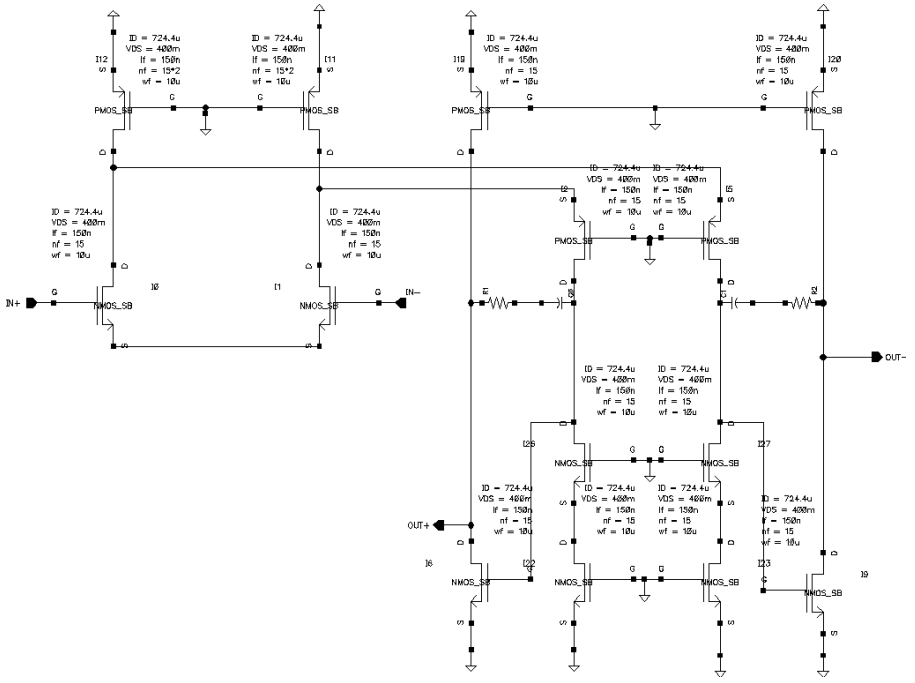

Figure 40: Schematic view in the "DIFF OTA1" cell .

Return to the test bench and run the simulation. The open loop gain dropped to 78 dB as shown in Fig-41. This result is expected since the total resistance at the cascode and second stage output will drop. Stability was not affected and neither was the closed-loop gain as shown in Fig-42. The signal path works correctly, now we move to the biasing of the circuit.

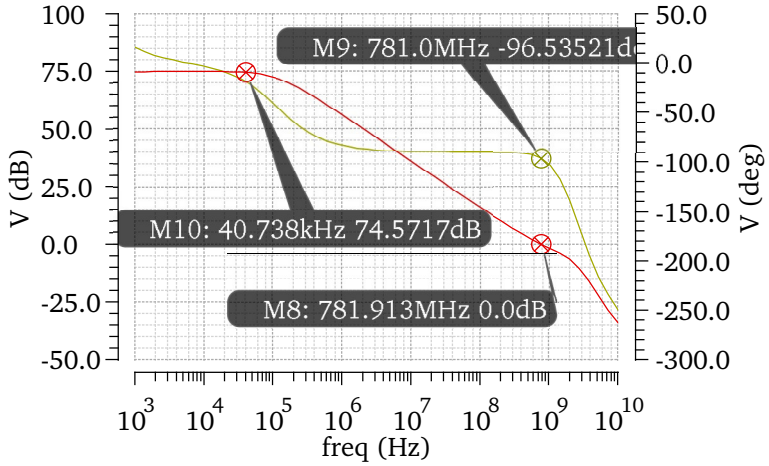

Figure 41: Bode plot of the "DIFF OTA" block with non-idealities.

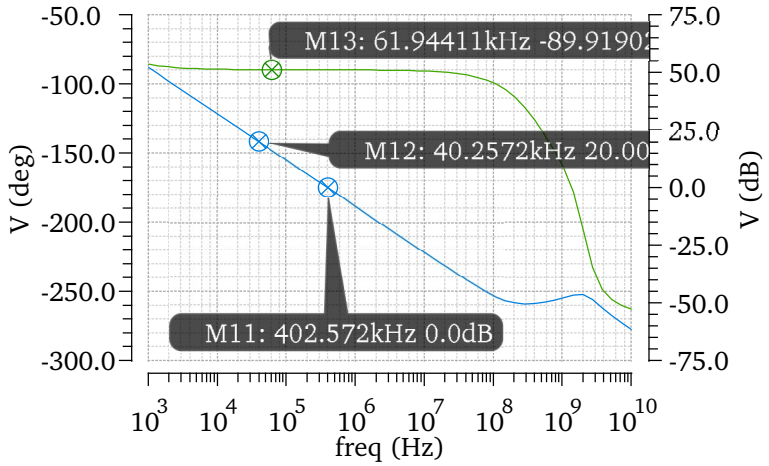

Figure 42: Closed loop gain of the "DIFF OTA" block with non-idealities.

Open the schematic of the "DIFF OTA2" block, which is given in Fig-43. There are many transistors but at this stage you should be able to identify most of the stages. Take a moment and find the signal path: the differential pair, the folded cascode, and the CS stage. Once you identify those stages, you can move to the biasing circuits that can be divided in 2 groups: bias references generation circuits, and common-mode feedback circuit.

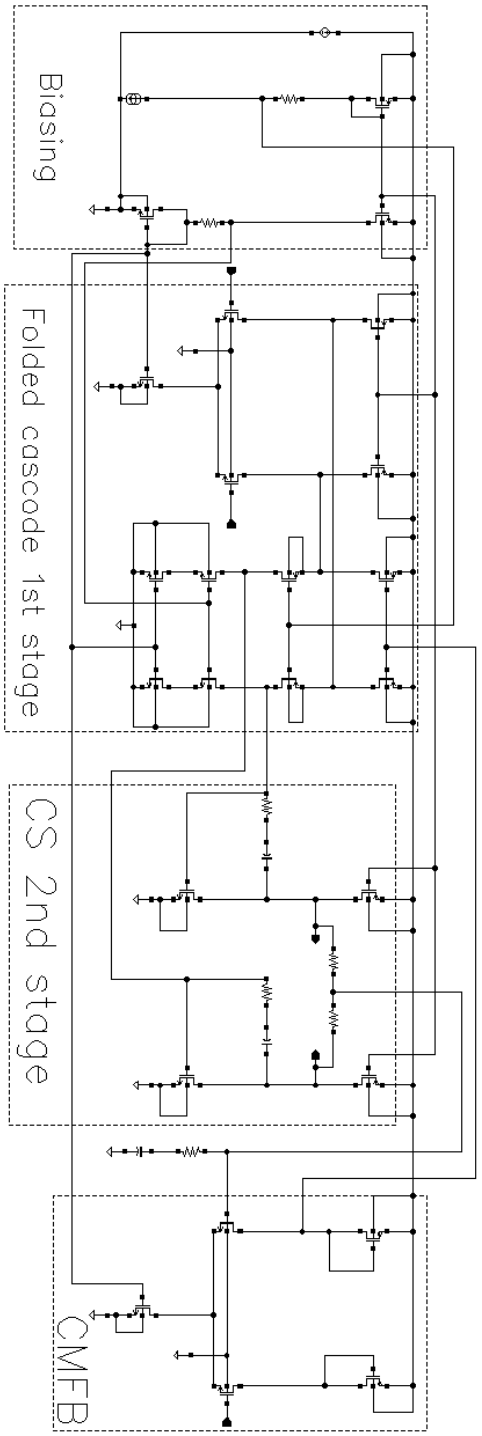

Figure 43: Schematic view in the "DIFF OTA2" cell.

The bias reference circuits are derived from a single current source as can be seen in Fig-44. Resistors are also used to generate the gate voltages for the cascode transistors. Here, the main idea is that the once the currents are set, the V_{gs} voltages of the cascodes transistors are very well known values (since they are in saturation). On the other hand, the V_{ds} voltage of the current sources transistors is not correctly defined. We can say that since they are current sources, the drain voltage can float and the current will be more or less constant as long as the transistor is in the saturation region. Accordingly, we can force the V_{ds} of the current sources to a particular value by changing the gate voltage of the cascodes. In practice we want them very low so that they do not take much overhead voltage. In this case, we decided to have Vds at least 0.25V.

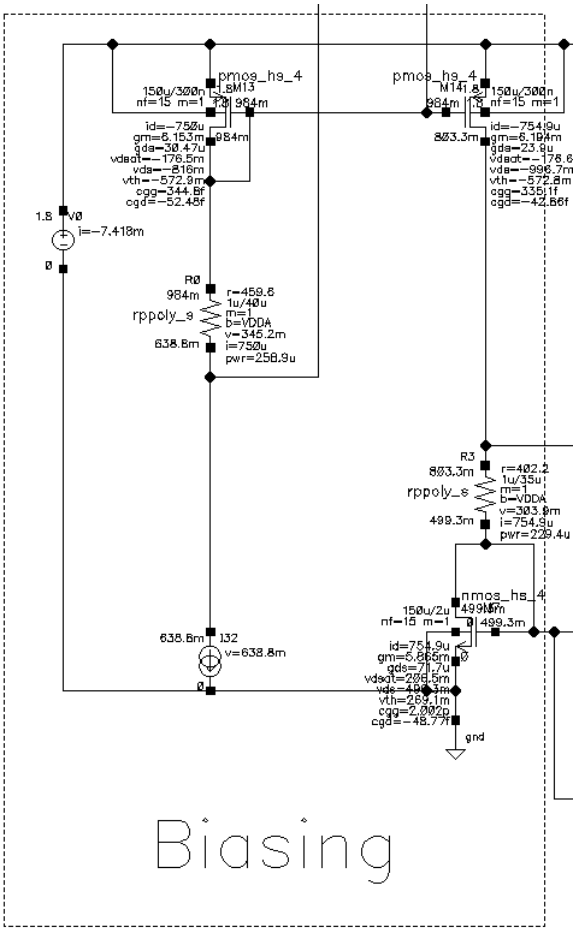

Figure 44: Biasing of the "DIFF OTA2" block.

Since we have an NMOS and PMOS current sources in the folded cascode pair, we need to have a common mode feedback (we did not have this problem in the single stage opamp since the feedback itself set the DC value at the output). For the folded cascode, we control the PMOS current sources. In order to avoid

a huge loop gain in the common- mode feedback, we decided to split the PMOS current source transistors and only use half of the current source in the common mode feedback loop. The common-mode voltage is sensed using 100 kΩ resistors at the OTA output as can be seen from Fig-45. This voltage is compared to a reference voltage using a single stage opamp with diode-connected transistors as load in order not to have to much loop gain. The output of the opamp controls the biasing of the PMOS current sources. A 1 pF capacitor was added at the input of the opamp with a 10 kΩ series resistor in order to stabilize the loop.

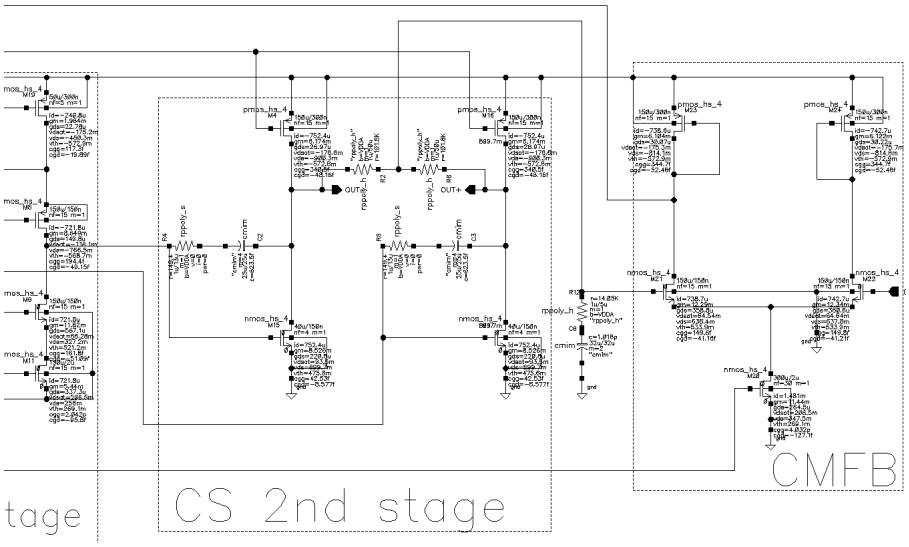

Figure 45: CMFB of the "DIFF OTA2" block.

The references for the common-mode feedback are 0.9 V ($V_{dd}/2$ is normally a good value to drive the next stage, although it should be possible to change the common mode voltage inside a range as long as the transistors are still in saturation).

The open loop gain of the biased amplifier is 75.5 dB and the phase margin is 70 degrees as can be seen in Fig-46.

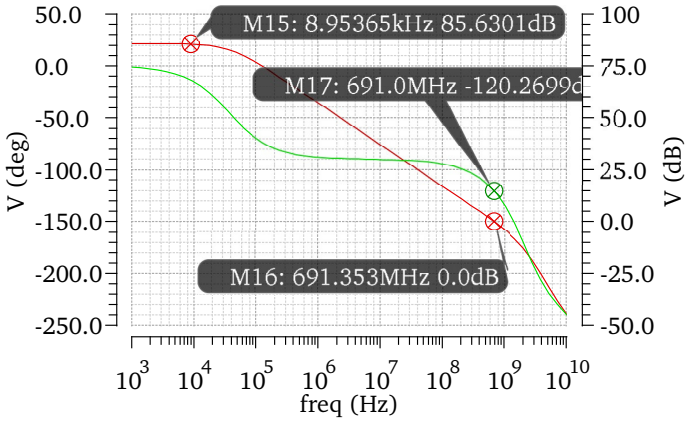

Figure 46: Bode plot of the "DIFF OTA2" block.

The closed-loop gain given in Fig-47 shows that the integrator is working with +-5 degrees error between 1 kHz - 30 MHz.

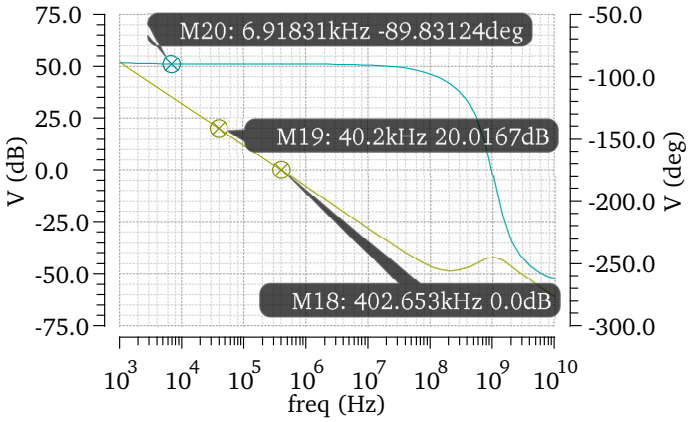

Figure 47: Closed loop gain of the "DIFF OTA2" block.

Finally, we check the stability. We have to check 2 loops: the signal path, and the common mode feedback loop. Open the schematic view in the "OPAMP TEST BENCH TRAN DIFF" cell which is shown in Fig-48. There are 2 setups with step sources. Run the simulation and check the step response. The results are shown in Fig-49 and Fig-50.

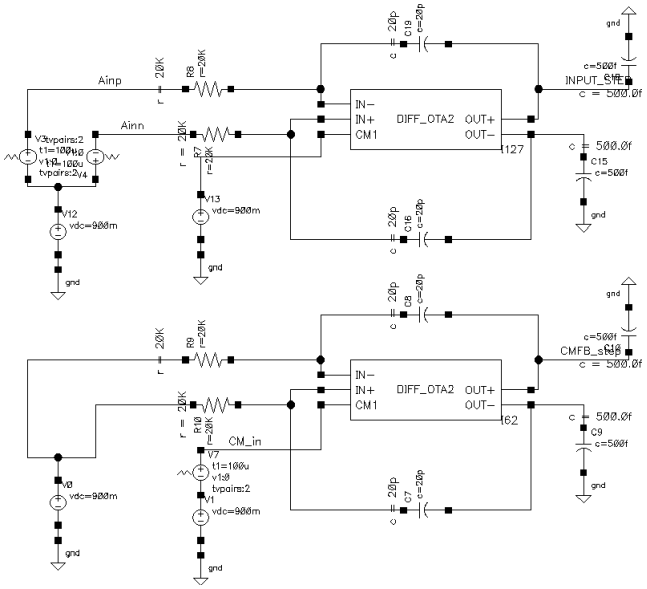

Figure 48: Schematic view in the "OPAMP TEST BENCH TRAN DIFF" cell.

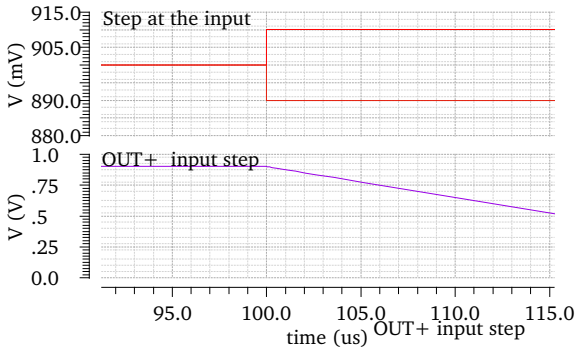

Figure 49: Step responses at the input of the "DIFF OTA2".

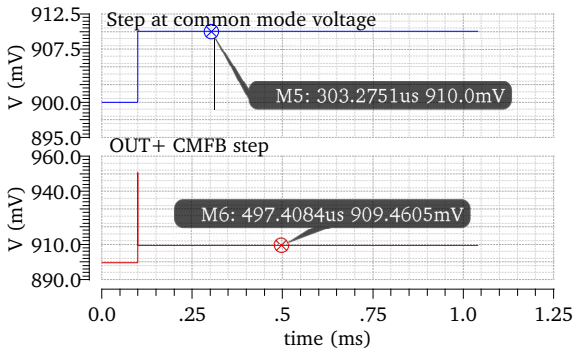

Figure 50: Step responses at the common mode reference of the "DIFF OTA2".

A Negative Feedback Amplifier Configurations and Noise Models

A.1 Negative Feedback Modeling, Loop Gain and Accuracy

The negative feedback model is very useful during the design since it relates the design parameters with the components of the negative feedback system. For example, the closed-loop gain is expressed as:

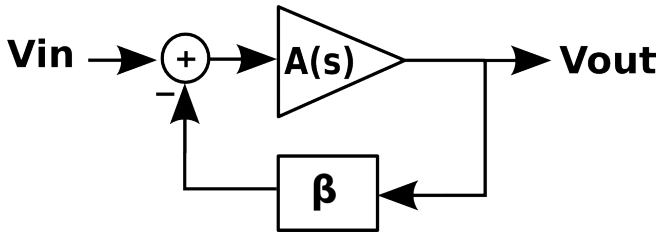

Figure 51: Block diagram of a negative feedback system.

$$Af = \frac{1}{\beta} \cdot \frac{A\beta}{1 + A\beta} \tag{20}$$

$$Af = A_{fDC} \cdot \frac{A\beta}{1 + A\beta}, \tag{21}$$

where β is the feedback factor, $A\beta$ is the loop gain and A_f is the gain variable (voltage gain Av, transconductance G, transimpedance T, current gain Ai). The accuracy of the amplification depends on how these variables are set during the design. The following example will clarify how this model is used.

Exercise: A negative feedback amplifier has a target gain of 10. Find the required open loop gain A so that the amplification error is less than 5%:

$$A_{fDC} = 10 \tag{22}$$

$$\beta = 1/A_{fDC} = 1/10 \tag{23}$$

$$9.5 = 10 \cdot \frac{A/10}{1 + A/10} \tag{24}$$

$$A = 190 \tag{25}$$

Repeat the exercise for an accuracy of 1%.

This simple tool can give us a very quick estimation of the open-loop gain that is required from the amplifier. After knowing this estimation, it is possible to make some crucial decisions regarding the kind of amplifier that can fit this specification, the number of stages, etc.

A.2 Negative Feedback Configurations and Noise models

A.2.1 Voltage Amplifier

$$A_{fDC} = (Z_1 + Z_2)/Z_1 \tag{26}$$
$$S(Vpar) = Re\{4kT(Z1||Z2)\}\,[V^2/Hz] \tag{27}$$
$$\beta = Z_1/(Z_1 + Z_2) \tag{28}$$

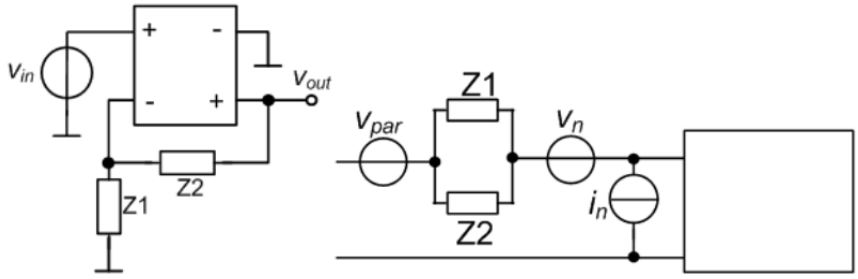

Figure 52: Voltage amplifier configuration and the equivalent input referred noise model.

A.2.2 Transimpedance Amplifier

$$A_{fDC} = Z_1 \tag{29}$$
$$S(i_1) = Re\{4kT(1/Z_1)\}\,[A^2/Hz] \tag{30}$$
$$\beta = 1/Z_1 \tag{31}$$

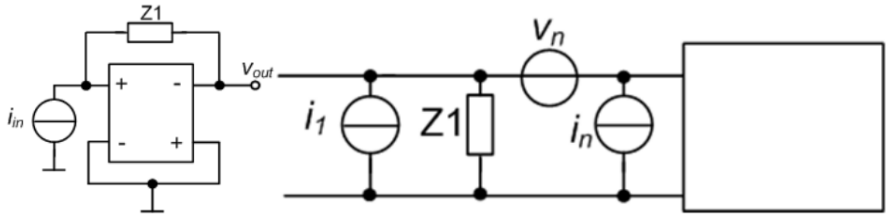

Figure 53: Transimpedance amplifier configuration and the equivalent input referred noise model.

A.2.3 Current Amplifier

$$A_{fDC} = (Z_1 + Z_2)/Z_2 \tag{32}$$
$$S(i_{SER}) = Re\{4kT(1/(Z_1 + Z_2)\}\,[A^2/Hz] \tag{33}$$
$$\beta = Z_2/(Z_1 + Z_2) \tag{34}$$

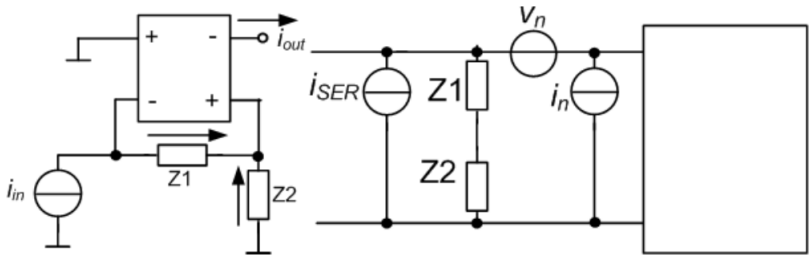

Figure 54: Current amplifier configuration and the equivalent input referred noise model.

A.2.4 Transconductance Amplifier

$$A_{fDC} = 1/Z_1 \tag{35}$$
$$S(V_1) = Re\{4kT(Z_1)\}\,[V^2/Hz] \tag{36}$$
$$\beta = Z_1 \tag{37}$$

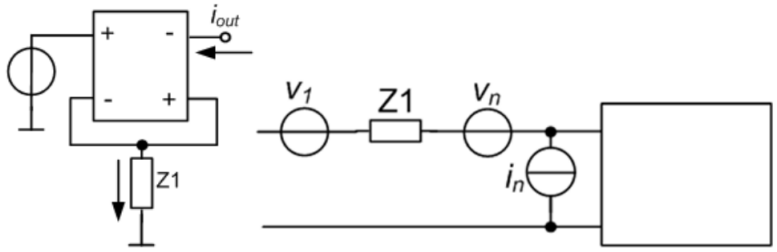

Figure 55: Transconductance amplifier configuration and the equivalent input referred noise model.

References

[1] D.A. Johns and K. Martin, "Analog integrated circuit design", *John Wiley and Sons*, 2008.

[2] B. Razavi, "Design of analog CMOS integrated circuits", *McGraw-Hill Education*, 2000.