Appendix to Tutorial 5
Stability analysis

October 31, 2017

1 Problem with the DC operating point

The objective of the following appendix is to explain the use of STB analysis. At an early stage of your design, you choose the dimensions and the biasing currents for the self-biased transistors in the signal path of your amplifier, to meet the project requirements. Afterwards, you had to replace the ideal biasing network with real devices like transistors and/or resistors to set the biasing conditions. This can cause the circuit to converge to a different DC operating point. As a result, some or all of the CMOS transistors can operate in the linear region. You can notice this problem by inspecting the annotated DC voltages of your circuit and even in the Bode-plot as a significant drop in the open-loop gain. In Tutorial 5 we did not encounter this problem because the real biasing network matched closely with the ideal conditions. However, we can demonstrate this problem by modifying a circuit from Tutorial 5 (OPAMP2 into OPAMP2stb) that gave the DC operating point shown in Fig. 1 and the Bode plot from Fig. 2. If we change the width of the common-source PMOS transistor in the second stage (circled in red in Fig. 1 and 3) from 150 μm to 70 μm width, the circuit will have a different DC operating point as shown in Fig. 3. Note that the biasing current source of the second stage, which is implemented with the NMOS transistor M8, has a drain-source voltage drop of 78.21 mV. With such a low overdrive voltage the transistor is operating in the linear region. By inspecting the Bode plot in Fig. 4 we can see that the open-loop gain also dropped to 29 dB from the starting 62 dB.

The same procedure for the STB analysis, which will be described in the following subsection, applies if you encounter this problem with the ideal biasing network.

1.1 Solution

The solution to this problem is to place your amplifier in the closed-loop configuration and to use negative feedback for setting the correct DC operating point. In order to extract the information about the stability of your closed-loop amplifier, you need to run an STB analysis instead of the AC analysis. The STB analysis is made to test the stability of closed-loop systems by calculating the phase and gain margin. The algorithm behind the analysis breaks the loop while preserving all of the loading effects.

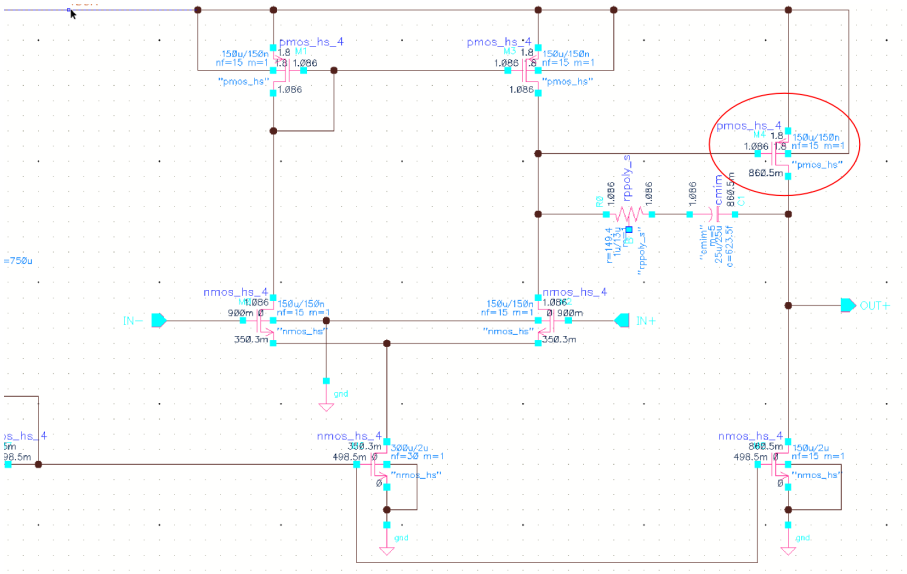

Figure 1: DC operating point of the OPAMP2.

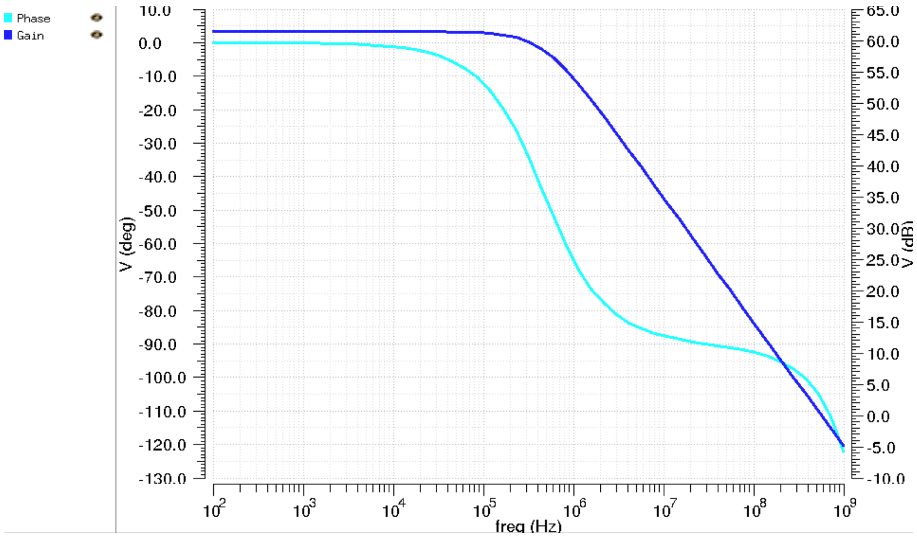

Figure 2: Bode plot of OPAMP2.

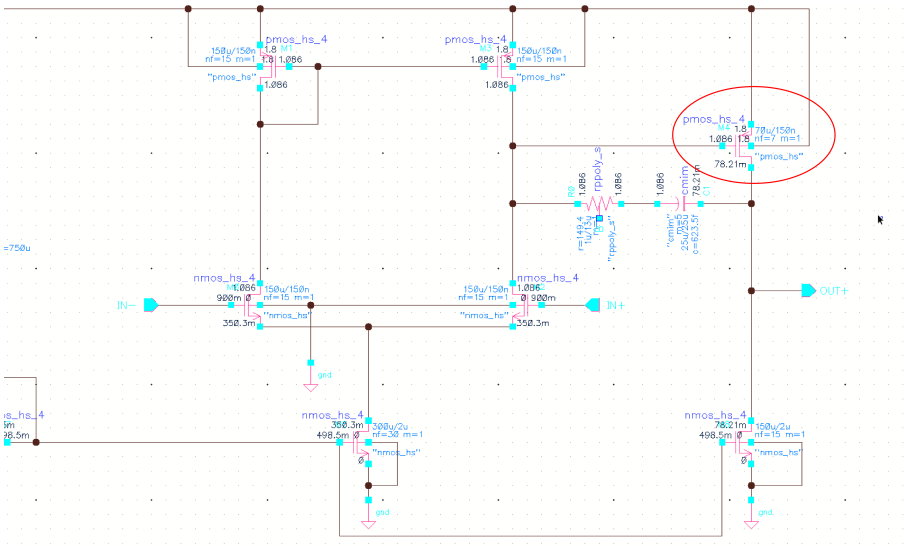

Figure 3: DC operating point of the **modified** OPAMP2stb.

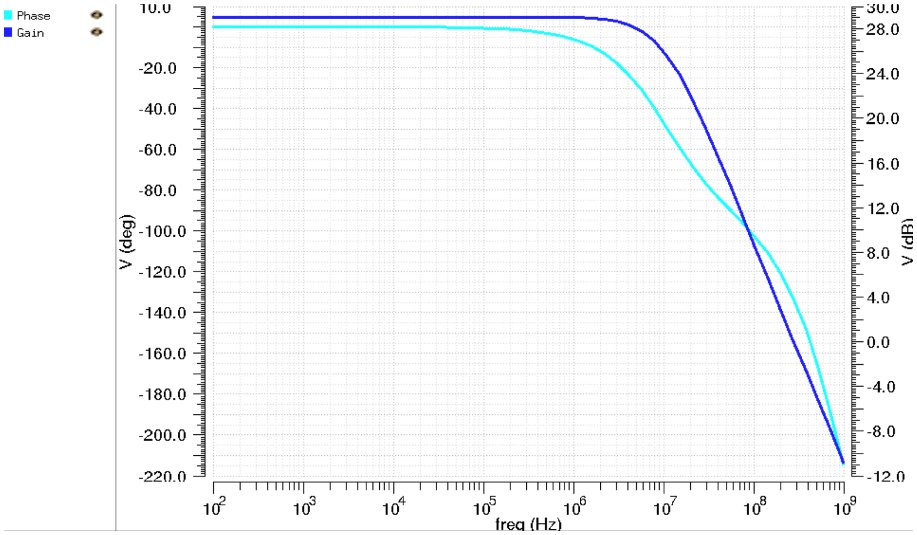

Figure 4: Bode plot of the **modified** OPAMP2stb.

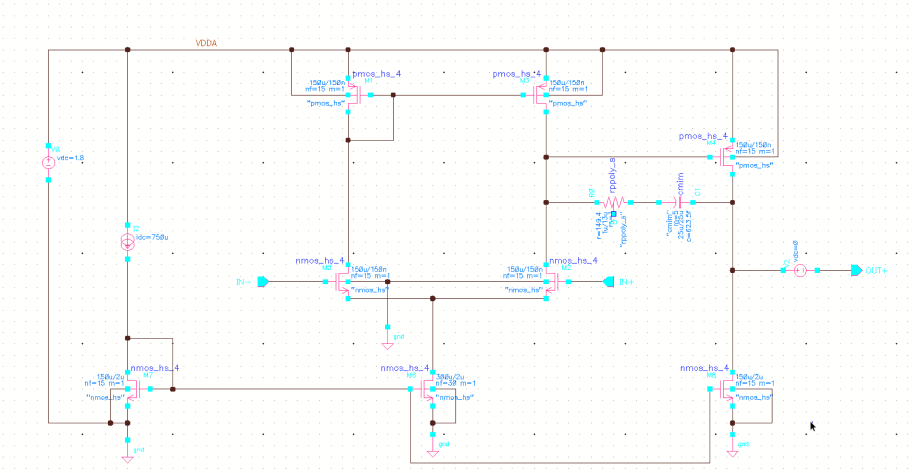

Figure 5: Addition of a voltage probe for the use in STB analysis.

To set up the STB analysis you have to do the following steps:

- First, insert a DC voltage source at the very output of your amplifier but before the output pin as shown in Fig. 5. This source should have 0 V DC voltage so as not to affect the DC operating point of the circuit.
- Second, place your amplifier in the closed-loop configuration specified in your project description. In this appendix the non-inverting configuration from Tutorial 5 is used.
- Similarly to the AC analysis, you first need to run the DC analysis and save the operating point.
- Open the STB analysis window and fill in the frequency range and the probe name according to Fig. 6. Note that your amplifier may have a different instance name then the $/I52/V2$ from Fig. 6. You can either manually enter the probe name or click the $<Select>$ button which will take you back to the schematic. There you will have to enter in hierarchy of the amplifier symbol. To do so, first select the amplifier symbol and then press $<e>$ to enter in hierarchy. When the amplifier schematic is open you need to left-click on the probing voltage source. The probe name in the STB analysis will then automatically be filled in. If you set everything correctly you can click the $<OK>$ button which will close the STB window.
- Check the log to see if the simulation completed successfully. To plot the results go to the ADE window and select **Results** ⇒ **Direct Plot Form**. A window similar to Fig. 7 will appear. Select the <Loop Gain> option and plot the magnitude in dB and the phase in degrees.

Figure 6: Window of the STB analysis settings.

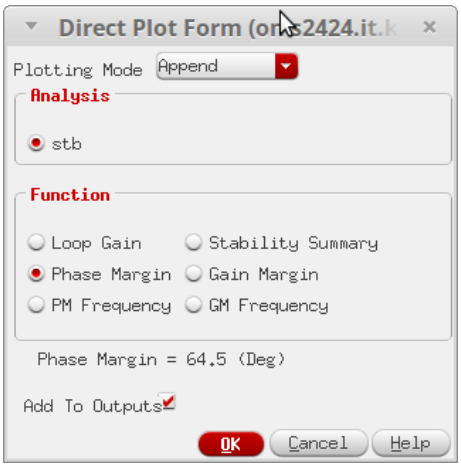

Figure 7: Direct plot form for the STB results.

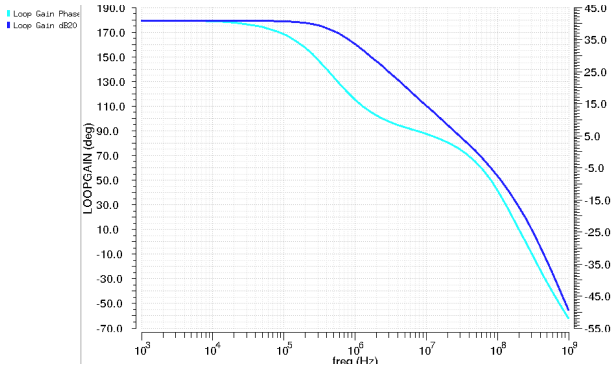

Figure 8: Bode plot obtained with STB analysis.

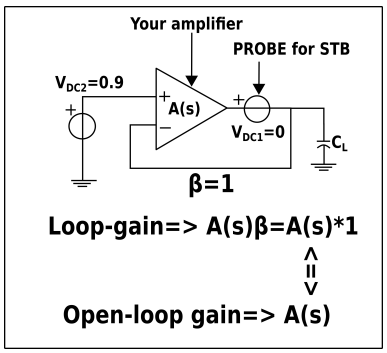

Figure 9: Bode plot obtained with STB analysis.

The results of the STB analysis are shown in Fig. 8. However, keep in mind that now we are plotting the **loop gain**, $\beta A(s)$, which includes the feedback network. The loop gain, which is also labeled on the axes, is approximately 42 dB at low frequencies. As mentioned in Tutorial 5, the feedback factor, β, was implemented with $R_2 = 10$ kΩ and $R_1 = 1$ kΩ connected in a non-inverting amplifier topology. The β for that case is equal to $R1/(R1 + R2) = 0.1$ or -20 dB, so for an open-loop gain of 62 dB the $\beta A(s)$ is $\approx$ 42 dB. Note that the position of the fist pole is the same as in the case of open-loop gain since it is determined by the Miller capacitance of the second stage. Moreover, the gain of the second stage remains the same because the feedback resistors are an order of magnitude larger than the equivalent output resistances of the transistors $r_{dsn,p}$. On the other hand, the position of the second pole is lower in frequency because the feedback network reduces the equivalent output transconductance of the second stage by 0.1 ($\omega_{p2} \approx \frac{g_{m2}}{C_L}$).

To plot the bode plot with STB analysis as though the amplifier was in open-loop configuration, you need to put your amplifier in the unity-gain feedback configuration to make $\beta = 1$ as shown in Fig. 9. With this workaround, when you plot the loop-gain, which is $A(s)\beta = A(s) \cdot 1$, it will be just like plotting the open loop transfer function A(s) of your amplifier.