Введение в Vitis HLS Tool CLI Flow

2021.2

Abstract

This lab introduces how to perform basic actions in the Vitis® HLS command prompt.

Objectives

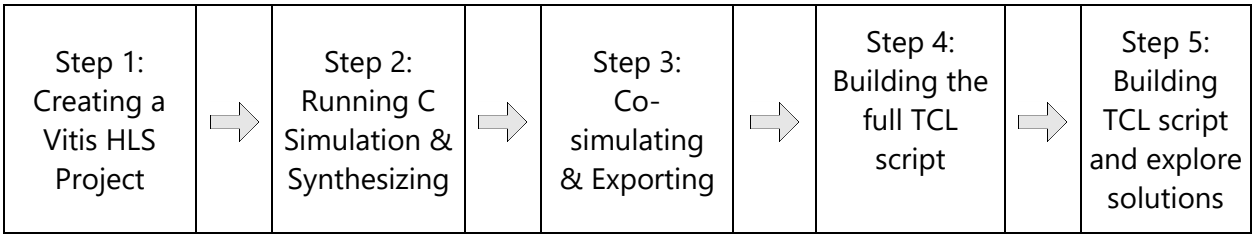
After completing this lab, you will be able to:

- Create a new project in the Vitis HLS tool CLI
- Simulate a C design by using a self-checking test bench
- Synthesize the design
- Simulate an RTL design by using a C test bench
- Implement the design

Introduction

This lab introduces the major features of the Vitis® High-Level Synthesis (HLS) tool Command Line Interface (CLI) flow. You will use the Vitis HLS tool in CLI mode to create a project. You will also simulate, synthesize, and implement the design provided.

General Flow



Before starting the lab — Step 0

Create the folders using Windows Explorer

C:\Xilinx_trn\HLS2022\lab2_z0\doc

Explore the C codes to understand algorithm and data dependencies.: **lab2_z0.h** and **lab2_z0.c** (*C:\Xilinx_trn\HLS2022\lab2_z0\source* folder).

Explore the C codes to understand algorithm and data dependencies.: **lab2_z0_test.c** file(*C:\Xilinx_trn\HLS2022\lab2_z0\source* folder).

Creating a Vitis HLS Tool Project Step 1

In this step, you will create a new Vitis HLS tool project, add source files, and provide solution settings for the default solution using the Vitis HLS tool command prompt. Later, you will open the created project in the Vitis HLS tool GUI to have a quick review of the settings were applied.

1-1. Write the commands to create a new project, associate source files, and configure solution settings.

1-1-1. Browse to the *C:\Xilinx_trn\HLS2022\lab2_z0* directory using Windows Explorer and create and open **lab2_z0.tcl** with your preferred text editor. Enter the commands pointed in the figure.

```
1  open_project -reset lab2_z0
2
3  add_files ./source/lab2_z0.c
4
5  set_top lab2_zo
6
7  add_files -tb ./source/lab2_z0_test.c
8
9  open_solution -reset "solution1"
10
11 set part {xa7a12tcsg325-1Q}
12
13 create_clock -period 6 -name clk
14 set_clock_uncertainty 1
```

Figure 1: lab2_z0.tcl with Project Information

Question 1

What does the **open_project -reset lab2_z0** do?

Question 2

What do the **add_files ./source/lab2_z0** and **set_top lab2_zo** do?

Question 3

What does the **add_files -tb ./source/lab2_z0_test.c** do?

Question 4

What does the **open_solution -reset "solution1"** do?

Question 5

What does the **set part {xa7a12tcsg325-1Q}** do?

Question 6

What do the **create_clock -period 6 -name clk** and **set_clock_uncertainty 1** do?

1-1-2. Save the **lab2_z0.tcl** file.

1-1-3. Exit the text editor to close the Tcl file.

1-2. Launch the Vitis HLS tool command prompt and change the directory to the *C:\Xilinx_trn\HLS2022\lab2_z0* working directory.

1-2-1. For Windows 10: **Start** > **Xilinx Design Tools** > **Vitis HLS 2021.2 Command Prompt**.

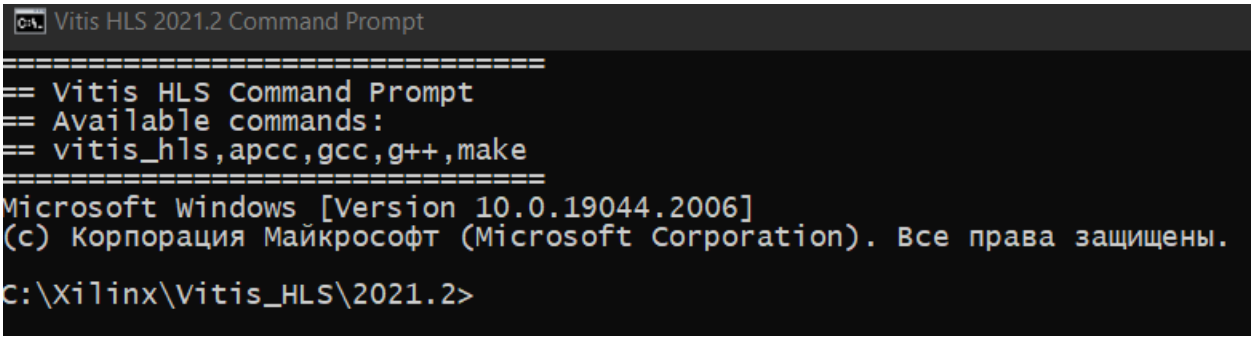


Figure 2: Vitis HLS Command Prompt

1-2-2. Enter the following command to change the directory to the current working directory:

```
cd C:\Xilinx_trn\HLS2022\lab2_z0
```

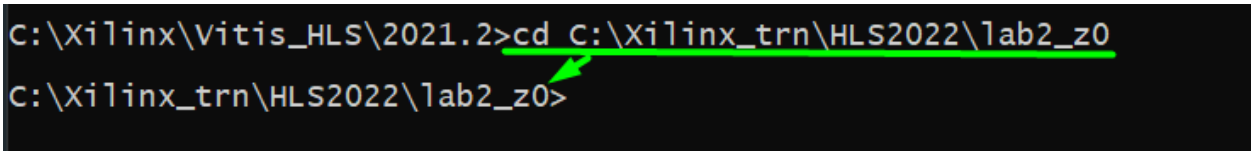


Figure 3: Changing the Directory

Run the *lab2_z0.tcl* file to create the project and open the created project in the Vitis HLS tool GUI.

1-2-1. Enter the following command in the Vitis HLS tool command prompt to run the *lab2.tcl* file:

```
Vitis_hls -f lab2_z0.tcl
```

```
C:\Xilinx_trn\HLS2022\lab2_z0>Vitis_hls -f lab2_z0.tcl
```

Figure 4: Creating the Project

1-2-2. Enter the following command to launch the GUI with the recently created project:

```
Vitis_hls -p lab2_z0
```

```
C:\Xilinx_trn\HLS2022\lab2_z0>Vitis_hls -p lab2_z0
```

Figure 5: Launching the GUI from the CLI

You should see the created project in the Explorer view.

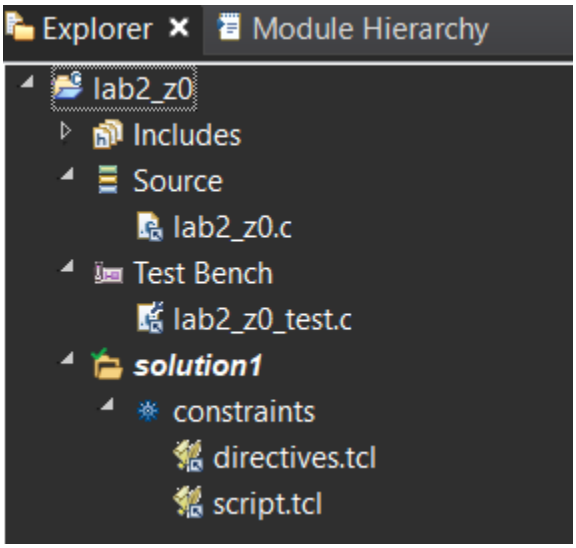


Figure 6: Vitis HLS GUI with Recently Created Project

1-2-3. Select **Project** > **Project Settings** in the Vitis HLS tool GUI.

The Project Settings dialog box opens.

1-2-3-1. Click **Synthesis** to ensure that the design source was added to the project as entered in the Tcl file.

1-2-3-2. Click **Simulation** to ensure that the test bench source was added to the project as entered in the Tcl file

1-2-4. Close the Project Settings dialog box once the source files are verified.

1-2-5. Select **Solution** > **Solution Settings** in the Vitis HLS tool GUI.

The Solution Settings dialog box for the active solution, i.e., *Solution1*, the only solution that exists in this current project, opens.

1-2-6. Select **Synthesis** to ensure that the clock frequency and part number are the ones described in the Tcl file.

1-2-7. Close the Solution Settings dialog box once the clock frequency and device settings are verified.

1-2-8. Select **File** > **Exit** in the Vitis HLS tool GUI to exit the GUI.

Running C Simulation and Synthesizing the Design Step 2

In this step, you will run C simulation and synthesize the design from the Vitis HLS tool command prompt and then open the Vitis HLS tool GUI to review the project status and Synthesis report.

2-1. Simulate the design.

2-1-1. Enter the following command in the Vitis HLS tool command prompt to run C simulation:

```
csim_design -clean
```

This command compiles and runs pre-synthesis C simulation of the design using the provided C test bench.

```
   Generating csim.exe
----------Pass!------------
INFO: [SIM 211-1] CSim done with 0 errors.
```

Figure 7: Running C Simulation from the Command Prompt

2-2. Synthesize the design.

2-2-1. Enter following command in the Vitis HLS tool command prompt to synthesize the design:

```
csynth_design
```

This will elaborate and perform high-level synthesis on the source files added to the project. This also analyzes the sources files, validates the directives if they are present, and performs some initial code transformations.

```
INFO: [HLS 200-790] **** Loop Constraint Status: All loop constraints were satisfied
.
INFO: [HLS 200-789] **** Estimated Fmax: 232.67 MHz
INFO: [HLS 200-111] Finished Command csynth_design CPU user time: 0 seconds. CPU sys
tem time: 0 seconds. Elapsed time: 5.722 seconds; current allocated memory: 0.000 MB
```

Figure 8: Performing Synthesis from the Command Prompt

2-3. Verify the Synthesis report in the Vitis HLS tool GUI.

2-3-1. Enter the following command to launch the GUI:

```
Vitis_hls -p lab2_z0
```

2-3-2. Select **Solution** > **Open Report** > **Synthesis** in the Vitis HLS tool GUI if the Synthesis report does not open automatically.

2-3-3. Analyze the report file.

Question 7

Write down the following details from the Synthesis report and Performance profile:

- Estimated clock period:
- latency (cycles):

- Loop trip count:
- Loop Iteration Latency (cycles):
- Loop Latency (cycles):
- Iteration Interval (cycles):
- Iteration Interval (time): Iteration Interval (cycles) * Estimatedë clock period =

- Number of BRAM_18K:
- Number of DSP48E used:
- Number of FFs used:
- Number of LUTs used:
- Number of URAM used:

Question 8

Explain why the Latency(cycles) is one cycle more than Loop latency (cycles).

Explain why the Iteration Interval(cycles) is one cycle more than Latency(cycles).

2-3-4. Select **File** > **Exit** in the Vitis HLS tool GUI to exit the GUI.

Co-simulating and Exporting the RTL Step 3

In this step, you will perform C/RTL co-simulation on the generated RTL files by using the C test bench from the Vitis HLS tool command prompt.

3-1. Perform C/RTL co-simulation.

3-1-1. Enter the following command in the Vitis HLS tool command prompt to execute post-synthesis co-simulation:

```
cosim_design -trace_level all -tool xsim
```

```
----------Pass!------------
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 1 seconds. CPU syst
em time: 0 seconds. Elapsed time: 30.981 seconds; current allocated memory: 0.000 MB
```

Figure 9: C/RTL Co-simulation

Notice that the message ***** C/RTL co-simulation finished: PASS ***** is displayed.

3-2. Verify the results in the Vitis HLS tool GUI.

3-2-1. Enter the following command to launch the GUI:

```
Vitis_hls -p lab2_z0
```

3-2-2. Select **Solution** > **Open Report** > **Cosimulation** in the Vitis HLS tool GUI to open the RTL Simulation report.

Question 9

Compare Iteration Interval (Avg, Max, Min), latency (Avg, Max, Min) achieved after cosimulation with the results achieved after synthesis.

3-2-3. Close the Vitis HLS tool GUI.

3-2-4. Enter the following command to close the Vitis HLS tool command prompt:

```
exit
```

```
vitis_hls> exit
INFO: [HLS 200-112] Total CPU user time: 4 seconds. Total CPU system time: 2 seconds
. Total elapsed time: 2163.63 seconds; peak allocated memory: 1.073 GB.
INFO: [Common 17-206] Exiting vitis_hls at Mon Oct  3 13:01:13 2022...

C:\Xilinx_trn\HLS2022\lab2_z0>
```

Building the full lab2_z0.tcl file — Step 4

4-1. Complete the lab2_z0.tcl file.

4-1-1. Browse to the *C:\Xilinx_trn\HLS_2022\lab2_z0* directory using Windows Explorer and open **lab2_z0.tcl** with your preferred text editor.

4-1-2. Insert the following, highlighted commands, into *lab2_z0.tcl* to complete the script:

```
1   open_project -reset lab2_z0
2
3   add_files ./source/lab2_z0.c
4
5   set_top lab2_z0
6
7   add_files -tb ./source/lab2_z0_test.c
8
9   open_solution -reset "solution1"
10
11  set_part {xa7a12tcsg325-1Q}
12
13  create_clock -period 6 -name clk
14  set_clock_uncertainty 1
15
16  csim_design -clean
17
18  csynth_design
19
20  cosim_design -trace_level all -tool xsim
21
```

Figure 10: Full lab2_z0.tcl script

4-1-3. Save the **lab2_z0.tcl** file.

4-1-4. Exit the text editor to close the Tcl file.

4-2. Run complete script.

4-2-1. Enter the following command in the Vitis HLS tool command prompt to run the *lab2_z0.tcl* file:

```
Vitis_hls -f lab2_z0.tcl
```

Full procedure from creating the project up to cosimulation will be implemented.

```
INFO: [COSIM 212-316] Starting C post checking ...
----------Pass!------------
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 1 seconds. CPU syst
em time: 0 seconds. Elapsed time: 25.284 seconds; current allocated memory: 0.000 MB
.
vitis_hls>
```

4-2-2. Enter the following command to close the Vitis HLS tool command prompt:

```
exit
```

Building the lab2_z0_ex.tcl file and conduct an exploration Step 5

5-1. Complete the lab2_z0_ex.tcl file.

5-1-1. Browse to the *C:\Xilinx_trn\HLS_2022\lab2_z0* directory using Windows Explorer create and open **lab2_z0_ex.tcl** with your preferred text editor.

5-1-2. Insert the commands into *lab2_z0_ex.tcl* to complete the script for exploration procedure:

```
# The command to create new project
    open_project -reset lab2_z0_ex
# The  command to add design file
    add_files ./source/lab2_z0.c
# The  command to specify the top-level function
    set_top lab2_z0
# The  command to add testbench file
    add_files -tb ./source/lab2_z0_test.c
# The  command to create the base solution named base
    open_solution -reset "ex_sol1"
# The  command to associate the device to the solution1
    set_part {xa7a12tcsg325-1Q}
# The  command to associate clock period to the solution1
    create_clock -period 5 -name clk
    set_clock_uncertainty 1
# The comamnd to Synthesize the design
    csynth_design
# The  comamnd to run the base C simulaiton
    csim_design -clean
# Build the lists of solution's name and target delay
    set all_solutions {ex_sol2 ex_sol3 ex_sol4 ex_sol5 ex_sol6}
    set all_period    {{6}       {7}    {8}     {9}     {10} }
# The comamnd to run the loop for the lists
foreach the_solution $all_solutions the_period $all_period {
    # The openning bracket for the loop

    # The command to create the solution named from the list
    open_solution -reset $the_solution

    # The command to associate clock period to the solution from the list
    create_clock -period $the_period -name clk
    set_clock_uncertainty 1

    # The  command to associate the device to the solution1
    set_part {xa7a12tcsg325-1Q}

    # The comamnd to Synthesize the design
    csynth_design

    # The comamnd to perform C/RTL Cosimmulation
    cosim_design -trace_level all -tool xsim
}
# The closing bracket for the loop
```

Figure 11: lab2_ex.tcl script

5-1-3. Save the **lab2_z0_ex.tcl** file.

5-1-4. Exit the text editor to close the Tcl file.

5-2. Run complete script.

5-2-1. Enter the following command in the Vitis HLS tool command prompt to run the *lab2_z0_ex.tcl* file:

```
Vitis_hls -f lab2_z0_ex.tcl
```

Full procedure from creating the project up to co-simulation for each delay in the list will be implemented.

5-2-2. Enter the following command to close the Vitis HLS tool command prompt:

```
exit
```

5-3. Verify and compare the Synthesis reports in the Vitis HLS tool GUI.

5-3-1. Enter the following command to launch the GUI:

```
Vitis_hls -p lab2_z0_ex
```

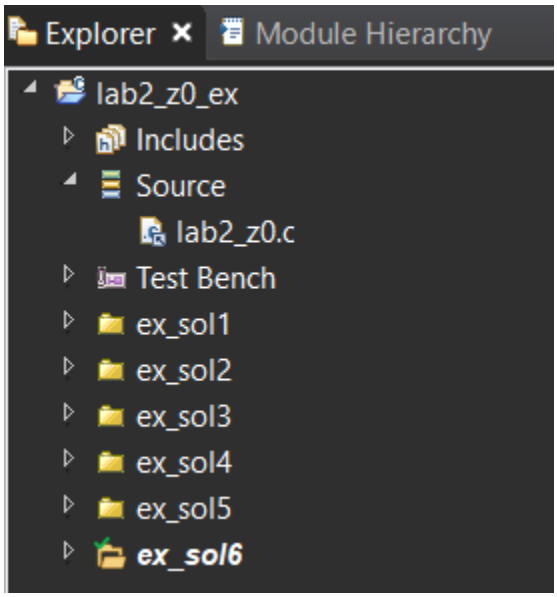


Figure 12: Vitis HLS tool GUI for lab2_explore_prj project

5-3-2. Verify that there are six solutions: *ex_sol[6:1]*.

5-3-3. Verify that *ex_sol6* is active and the target clock period is equal 10ns.

5-3-4. Select **Project** > **Compare Reports** in the Vitis HLS tool GUI.

5-3-5. In the window appeared select all solutions for comparing.

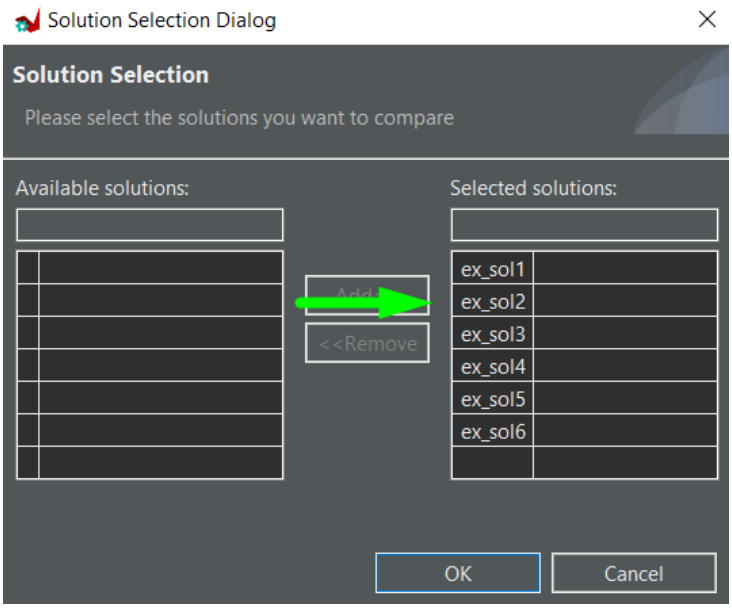


Figure 13: Solutions to compare - report

5-3-6. Use data from the *compare_report* tab to complete the spreadsheet as it done on the following figure (An example of the spreadsheet is in file ./source/lab2_z0_ex.xlsx).

Pay attention that Latency (ns) is calculated by multiplying Clock estimated (ns) on Iteration interval (cycles).

		ex_sol1	ex_sol2	ex_sol3	ex_sol4	ex_sol5	ex_sol6
Clock	Target (ns)	6	7	8	9	10	11
	Estimated (ns)	3,194	4,298	4,298	6,450	6,450	6,450
Iteration Interval	(cycles)	14	11	11	8	8	8
	(ns)	45	47	47	52	52	52
Resources	BRAM_18K	0	0	0	0	0	0
	DSP48E	1	1	1	1	1	1
	FF	58	25	25	7	7	7
	LUT	76	72	72	68	68	68
	URAM	0	0	0	0	0	0

Figure 14: Solutions to compare - spreadsheet

5-3-7. Construct the diagram by using Iteration Interval (ns) and FF, LUT resources (DSP, BRAM18, URAM have constant values and can be omitted). (An example of the spreadsheet with the diagram is in file ./source/lab2_z0_ex.xlsx).

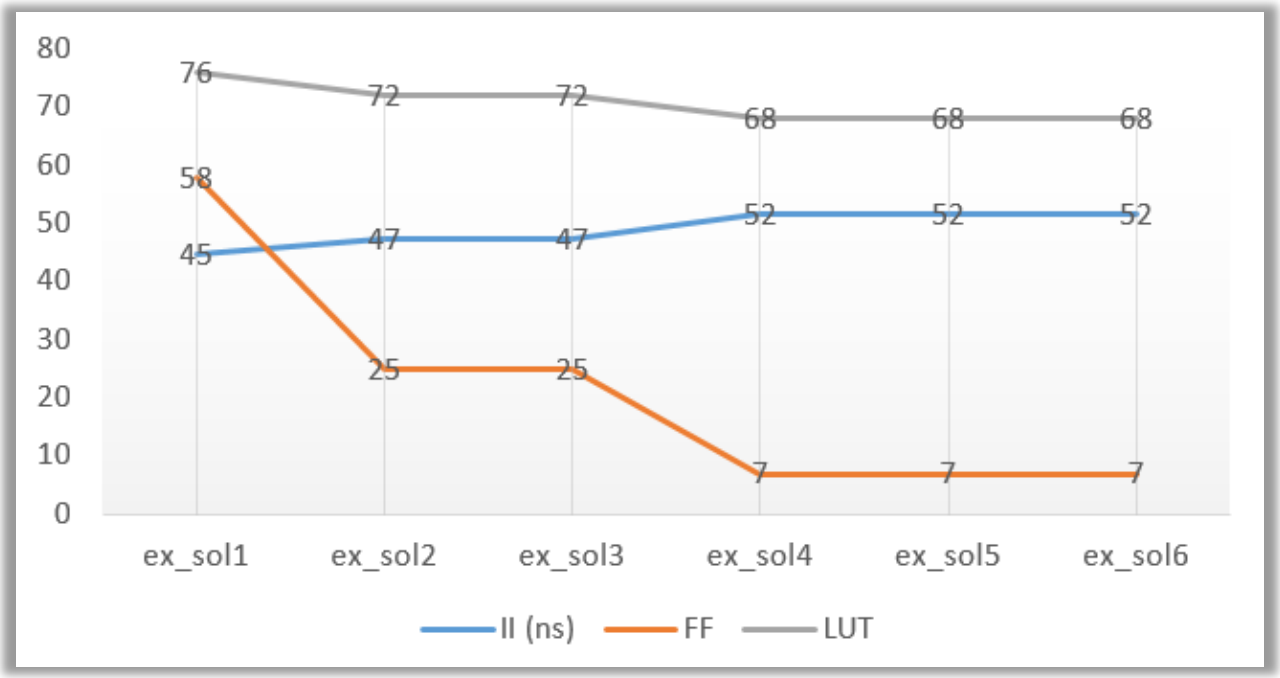


Figure 15: Solutions to compare - diagram

Question 10

Explain which solution, in your opinion, is the best (criteria are max performance and min resources) and why do you think so.

Summary

In this lab, you learned how to use the Vitis HLS tool command prompt to:

- Create the Vitis HLS tool project
- Create a solution with the desired settings
- Execute major actions in the Vitis HLS (simulate, synthesize, cosimulate and export the RTL of the design) design flow