Project part I: Design of an audio amplifier

(CSC-CDC-AB configuration)

***Abstract*—An audio amplifier is presented and designed to drive a 4Ω-loudspeaker using an input signal of max 100mV$_{RMS}$ and power supply 10V. A three-stage-amplifier is used, starting with a common source circuit, next a common drain circuit, and ending with a class AB amplifier. This cascade is needed in order to get high input impedance, low output impedance, and efficient voltage transfer between stages. The distortion of the amplifier must be as low as possible. This is done by avoiding clipping and cross-over distortion.**

I. INTRODUCTION

For the third module of Electrical Engineering at University of Twente, the task given was to design an audio amplifier. The required operating conditions are $100mV_{RMS}$ input signal and a power supply of $10V$. The audio amplifier is designed to drive a 4Ω loudspeaker. In order to accomplish this, first a common source circuit is used. This circuit has a high input impedance and is responsible for the voltage gain. Given the mentioned constrains to satisfy the requirements of a typical audio amplifier, the voltage gain must be around 30. Next, a source follower is implemented. This sub-circuit is used to achieve an efficient voltage transfer between the first and the last stage. Lastly, a class AB is used to deliver the current needed for the loudspeaker. This report will discuss the design process and the highlights of the audio amplifier. Experimental proof will be shown, and finally the issues faced while achieving this task will be discussed.

II. ANALYSIS AND DESIGN

A step by step explanation for the design process of the circuit stages will be done in this section. The schematics in the figures are from the final circuit itself.

A. STAGE 1: COMMON SOURCE CIRCUIT

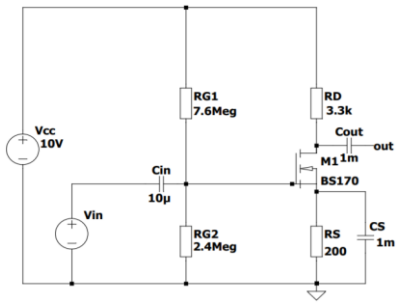

Figure 1 Input stage; common source circuit

The input impedance of the common source circuit is relatively high. This is needed for maximum transfer from the input source (e.g. laptop audio port) to this first stage. The circuit behaves as a voltage divider: in order to get most of the voltage to the first stage its input impedance needs to be high in comparison to the impedance of the signal source. This stage also delivers the voltage gain, given by the following equation: $A_V = -g_m \cdot R_D$ [1] (the minus is not included in the rest of the calculations, because this does not affect the performance of the audio amplifier). In order to get enough gain, the resistor values are calculated using the equations for the given stage which were fitted for biasing. Also, the bias settings need to be in such a way, that the output voltage can get maximum swing. This means that the bias voltage at the output of this stage needs to be approximately 6V. The positive peak can then reach the supply voltage V_{CC}, (the amplitude of the output signal of this stage is 4V, and the minimum value is 2V), which is just above the threshold voltage of the MOSFET. A gain of 30 is the maximum possible, because 0.141·30 = 4.23V, which is about the maximum voltage swing. The output impedance is approximately the same as R_D, which is relatively high, so a buffer stage is needed.

The resistor values need to be calculated. Firstly, the gain needs to be 30. But it is known that there will be some loss in the source follower, so for the calculations 32 is chosen. The output bias voltage of this stage is chosen to be 6V, because then maximum swing is possible (not 5V, because of the threshold voltage).

$$I_D = \frac{V_{CC}-V_{out}}{R_D} \rightarrow I_D R_D = 4 \quad (1)$$

Also, the voltage gain equation is known K =0.04 A/V^2 and V_T =1.9V (same value as discussed in the measurement section.)

$$A_V = g_m R_D = \sqrt{2KI_D}R_D = 32 \rightarrow R_D = 3.2k\Omega \quad (2)$$

An available resistor value will be chosen: 3.3kΩ Then, the other resistances will be calculated. The equation $I_D = \frac{1}{2}K(V_{GS}-V_T)^2$ is known. Then:

$$V_G - V_S = \sqrt{\frac{2I_D}{K}} + V_T = V_G - I_D R_S \quad (3)$$

The value for R_S may not be too high, because clipping at the negative side of the signal can occur. Therefore, R_S = 200Ω is chosen to avoid this issue. Thus:

$$V_G = \sqrt{\frac{2I_D}{K}} + V_T + I_D R_S \approx 2.4V \quad (4)$$

Then the bias values for the gate are quite easy: R_{G2} = 2.4MΩ and then R_{G1} = 7.6MΩ.

B. STAGE 2: COMMON DRAIN CIRCUIT

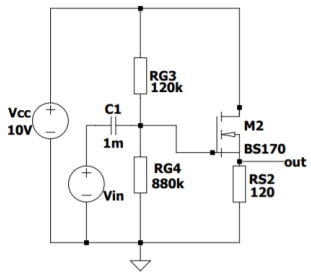

Figure 2 The common drain circuit

The second stage is a common drain circuit, which has a high input impedance and a low output impedance, perfectly fitting between the first and last stage. The gain will

be always lower than 1 (see the equation in Table I), but there will not be a significant loss if it is close enough to 1. Therefore, this gain is calculated and set at least 0.90, because then the loss is acceptable. Moreover, the output impedance may not be too high. Therefore, R_S cannot be too big or too small. Choosing a value of 120Ω, R_{G3} and R_{G4} can be calculated, using equation 4 again. Choosing $I_D = 50\,mA$, results in $R_{G3} = 120k\Omega$ and $R_{G4} = 880k\Omega$. These resistor values result in r_{out}=9Ω and A_V = 0.93. The equations used for calculating this are shown in Table I.

Table 1 SMALL SIGNAL PROPERTIES OF THE SOURCE FOLLOWER [1]

Voltage gain	$A_V = \frac{g_m R_S}{g_m R_S + 1}$
r_{out}	$\frac{1}{g_m}$
r_{in}	$R_{G1} // R_{G2}$

C. STAGE 3: CLASS AB AMPLIFIER [2]

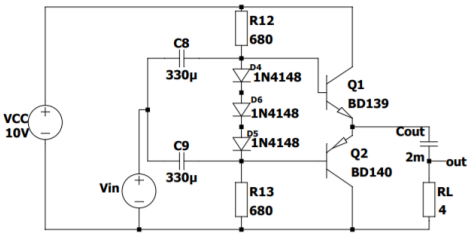

Figure 3 The class AB-amplifier

Up until now the two stages previously discussed will deliver an amplified input signal. The next step is used to ensure a maximum current driving to the load. This would have not been possible with the first two stages. Their transistors always consume power even if there is no input signal, therefore, providing less current and less power. A solution for this is to implement a class AB amplifier. They not only have a low output impedance but also low distortion when properly biased.

Thus, in order to accomplish this, the following considerations are taken:

a) The use of a fixed biasing voltage allows each transistor conduct one-half of the input cycle.
b) To put the transistors in active operation a voltage difference between the base and emitter of each BJT must be higher than 0.6V.
c) The current seen at the load depends on the output impedance of the power transistor.
d) Since the circuit acts as a pull and push amplifier one of the transistors will take charge of the positive half input signal. Thus, reducing the analysis to only one transistor. Such one being a common collector circuit.
e) Lastly, because power dissipation is avoided a cascade of diodes (instead of resistors) meeting the condition of literal b) is required.

All things considered, Figure 3 can be treated as a common collector circuit, when the input signal is at its positive side. But when the negative part of the signal, the other transistor is working. First, the diodes between the pair of transistors is shorted. Their resistance is negligible and make calculations easy. Secondly, the PNP transistor is seen as an open loop until the negative part of the input signal is reached. Then, the 4Ω resistance is placed as the load of this new configuration. Calculating the transfer function of this set up, the following equation is obtained:

$$\frac{V_{out}}{V_{in}} = \frac{g_m R_L}{1 + g_m R_L}$$

Now, since a common collector circuit acts a voltage buffer a gain of 0.99 is chosen. Thus

$$\frac{100}{1 + 100} = \frac{g_m R_L}{1 + g_m R_L}$$

Equating both sides and solving for I_C:

$$I_C = \frac{100}{40 \cdot R_L} = 625mA$$

Where $g_m \approx 40 I_C$ stands for the transconductance of the BJT power transistor. The next step is to calculate the resistor values with the current obtained in the above equation. This is done by realizing that the node where both transistors meet each other is at 5V. Thus, for the common collector circuit of this analysis, the voltage over resistor R_{12} should be 4.4V. Looking at the datasheet of the transistor used in the real circuit it is found that the current gain is around 100 when I_C is 625mA. Applying Ohm's law this results in 700Ω. During measurements the available resistor value of 680Ω was chosen as it did not affect the biasing.

Table 2 SMALL SIGNAL PROPERTIES OF AB AMPLIFIER

Voltage gain	$A_V = \frac{g_m(1+\propto)R_L}{\propto + g_m(1+\propto)R_L}$
r_{out}	$\frac{R_L // \frac{\propto}{g_m}}{1 + g_m\left(R_L // \frac{\propto}{g_m}\right)}$
r_{in}	$R_L(1+\propto) // (R_{B1} // R_{B2})$

D. WHOLE CIRCUIT

When connecting the three stages to each other, the complete amplifier is the result. This circuit can be seen in Figure 4. The gain for this circuit is not exactly the same as the gain of the common source circuit, because the gain of the source follower and the AB amplifier is less than 1. When multiplying those two voltages gain equations, the result is: $A_V = 0.99 \cdot 0.93 \cdot 32 \approx 29$.

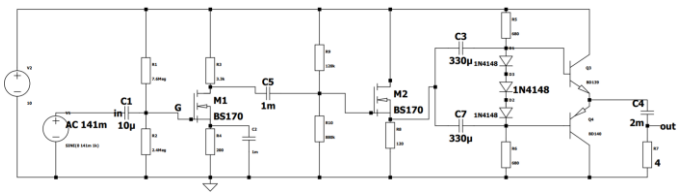

Figure 4 The complete amplifier circuit

III. RESULTS

A. Simulations

In this section, the simulations of the total amplifier circuit are presented:

Voltage Gain

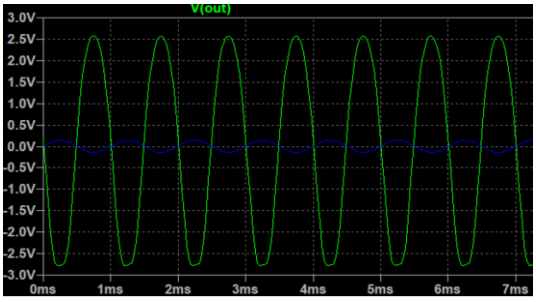

Figure 5 Simulation Voltage Gain

Starting with the voltage gain. A proper biasing for the different stages resulted in Figure 5. There, in green colour the output signal is shown. A close analysis reveals an amplitude of 2.7 volts. This corresponds to a voltage gain of around 20.

Bode plot

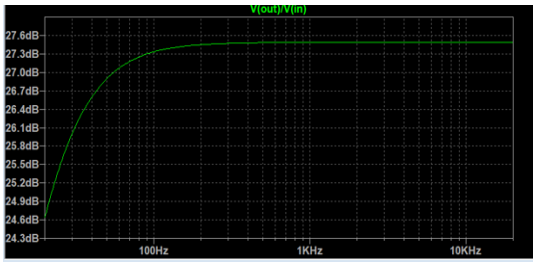

Figure 6 Simulation Bode plot

Figure 6 presents a Bode plot obtained in LTSpice. Looking at the top part in the y axis, a voltage gain of 23 is calculated. This corresponds to 27,4 dB within a bandwidth of 20Hz to 20kHz.

Distortion

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]
1	1.000e+03	3.081e+00	1.000e+00	-178.59°
2	2.000e+03	2.168e-01	7.038e-02	91.06°
3	3.000e+03	1.603e-01	5.204e-02	-178.36°
4	4.000e+03	8.250e-02	2.678e-02	92.45°
5	5.000e+03	4.975e-02	1.615e-02	2.40°
6	6.000e+03	2.441e-02	7.924e-03	-88.04°
7	7.000e+03	1.334e-02	4.331e-03	-177.33°
8	8.000e+03	2.810e-03	9.121e-04	97.77°
9	9.000e+03	1.668e-03	5.414e-04	-175.49°

Total Harmonic Distortion: 9.339122% (9.343983%)

Figure 7 Screenshot of THD simulation

Accounting to the fact of a slightly distorted signal at the negative peaks where it is not perfectly rounded, an analysis to measure the distortion of the audio amplifier was carried out. [3]. This resulted in a THD of 9.33% as it can be seen in Figure 7.

Input impedance

The input impedance in the simulation is calculated using the values of the current passing through the input terminal and the voltage across it. Using Ohm's Law, the result is 2,02MΩ

Output impedance

In a similar manner, the impedance as seen at the output terminals of the audio amplifier is 0.031Ω

B. Measurements and Performance

Before collecting measurements, in order to match the K parameter of the MOSFET used in the first two stages and the one in simulations, a test with my-DAQ is run. A set of instructions is followed. MATLAB is used and the transistor analyser studied during Lab sessions is put into practice [4]. It is found that the K-value is 0.04 A/V^2 and the threshold voltage is 1.9V. Marginally different, reason for which these parameters were changed during simulations. With this set up the biasing is readjusted, and the measurements are taken.

Voltage Gain

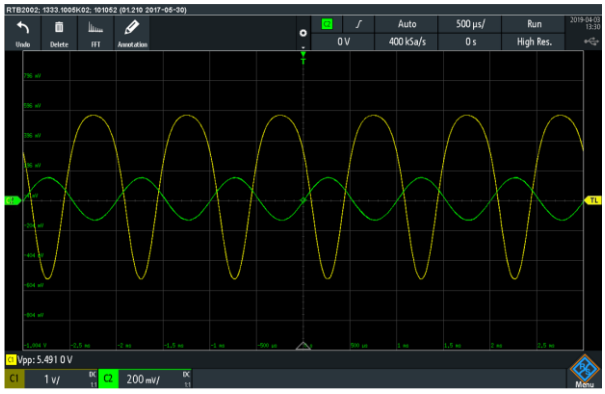

Figure 8 Real amplifier voltage gain; green: input, yellow: output

Figure 8 shows the output signal in the real circuit. The yellow line corresponds to the output signal whereas the green one to the input. A voltage of 5.49 peak to peak is observed, thus, calculating an amplitude which produces a gain of 19 times.

Bode plot

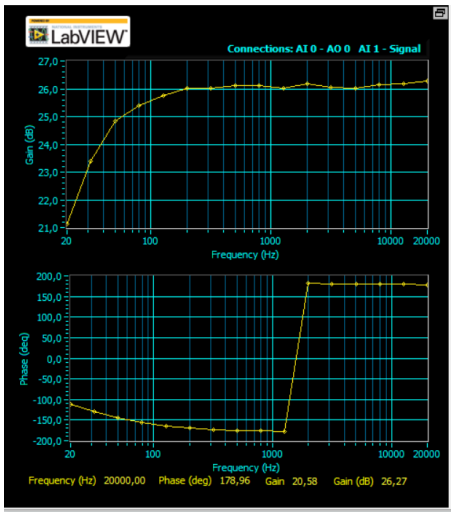

Figure 9 The measured Bode Plot

In figure 9 the analysis done with the Bode Analyser of my-DAQ is shown. In the window one can see that the cut-off frequency is rounding the 30Hz. This can be explained due to a relatively small (330µF) output capacitor which was used when doing this measurement. When a bigger capacitor (2mF) was used instead of the previous one, the cut-off frequency would have been lower than 20Hz, just as in the simulation. The gain in this figure is 26dB (20 times).

Distortion

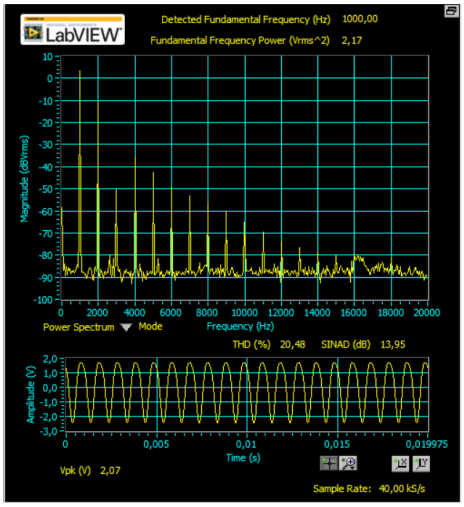

Figure 10 Measured Fourier transform

In Figure 10, the Dynamic Signal Analyzer was used to analyse the real circuit. As shown, the level of distortion THD is approximately 20%. This value, however, can be observed when looking to the output wave, in Figure 8. There, the yellow sinusoidal wave being the output presents positive peaks that are significantly wider than the negative ones. The green line is the input of 100mV$_{RMS}$, and it used as a point of reference.

Input impedance

The value for the impedance is determined by measuring the current and the voltage seen at the input ports of the audio amplifier; 1.28 MΩ is obtained. The multimeter used for this purpose was the Agilent 34401A Multimeter and the calculation was done using Ohm's law.

Output impedance

Applying the same concept to measure the input impedance the value obtained during real experimentation resulted in 0.062Ω. This time, the current measured was at the node of the emitter between the two power transistors and the load. Similarly, the voltage used in this case was the output voltage gain.

Table 3 Performance summary

Characteristics	Simulated	Measured
r_{in}	$2.02M\Omega$	$1.28M\Omega$
r_{out}	0.031Ω	0.062Ω
A_V	23	19
THD	9.33%	20%
Bandwidth	20-20kHz	30-20kHz

IV. DISCUSSION AND CONCLUSION

Throughout the process of design, simulation, and testing, some issues became apparent which needed to be resolved.

One of the issues faced was the unknown k-factor. Thus, the first trial was done using the value of the k-factor from LTSpice, however this resulted in distortion. This was resolved by implementing a proper method to derive the value for the used MOSFET, namely the method used in one of the labs of the third module.

In the pitch, the circuit design was slightly different than it is now. Some changes have been made, listed down here:

1. Capacitor values changed. Some capacitor values were chosen too big (1 mF for most of them). This would result in a high time constant τ (around 4s). This is avoided by choosing lower capacitances.
2. The resistor values have changed. Biasing was not done very properly. Also, the biasing was done using the simulation K and V_T, which are not the true values.
3. The input of the class AB was placed between the two diodes during the pitch. Because crossover distortion was happening, another diode was added to ensure the required bias voltages at the bases of the transistors. Therefore, the input was split into two different inputs, otherwise it could not be in the middle of the diodes.
4. The biasing of the source follower was first done by using the bias voltage of the input stage, but because this one was changed, also this bias changed. That is not wanted, so two biasing resistors were added to this stage.
5. For the transistors at the output stage, first the BC550 and the BC560 were chosen, however these transistors cannot handle the required current. Therefore, they are replaced by high current transistors (BD139 and BD140).

The aim of this project was to design an audio amplifier circuit which fits the requirements and restrictions given. The final circuit design was able to drive the 4-ohm loudspeaker with the limitation of 10V supply, however distortion was clearly audible. This was seen through the distortion levels of the output signal (Figure 10). Taking this into consideration, the design of the amplifier circuit could be improved in some areas. For example, the bias settings could be improved even more. Also, by boosting the supply voltage (e.g. using a step-up-converter) the amplification could have been higher while clipping and other kinds of distortion would be avoided more.

Another improvement that can be made, is to add a heatsink to the power transistors in the class AB amplifier, because they were heating up significantly.

V. REFERENCES

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