On the role of interface states in low-voltage leakage currents of metal–oxide–semiconductor structures

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This work investigates the additional gate current component with respect to the direct tunneling of electrons between the conduction bands measured in ultrathin oxide metal–oxide–semiconductor field-effect transistors at low voltages, before and after the application of a high field stress. We discuss several possible conduction mechanisms on the basis of the band diagram profiles obtained by means of a one-dimensional self-consistent Poisson–Schrodinger solver and we explain why this additional leakage current is mainly due to electron tunneling involving the native and stress-induced interface states in the silicon band gap either at the cathode or at the anode. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1487450]

Understanding the charge transport mechanisms at low voltages (smaller than 2 V) in metal–oxide–semiconductor (MOS) structures with ultrathin oxides (less than 3 nm) is mandatory in order to develop reliable ultra-large-scale-integration circuits. In 1999, Nicollian *et al.* first showed that the relative increase of the current after an electrical stress in ultrathin oxides is significantly larger for gate voltages between $V_{FB}-1$ V and $V_{FB}+1$ V for both n-metal–oxide–semiconductor field-effect-transitors (MOSFETs) and p-MOSFETs, where V_{FB} is the flatband voltage.[1] They suggested that this additional leakage component is due to the tunneling between the interface states generated during the stress on both sides of the MOS structure. Ghetti *et al.* analyzed this low voltage leakage current in a smaller gate voltage window (between 0 V and V_{FB}) in fresh and stressed oxides and proposed a different conduction mechanism involving the interface states (native and stress induced) only at the anode side.[2] They suggested that electrons at the cathode come from the silicon conduction band and not from the interface states. In this letter, we report the results of a study on the role of native and stress-induced interface states on the low voltage leakage currents in MOS structures.

The samples used in this work were n-MOSFETs with a n^+ polycrystalline silicon (polysilicon) gate, a p-type substrate ($N_A=10^{18}$ cm^{-3}) and an oxide thickness of 2.15 nm. The substrate doping and the oxide thickness were extracted by the comparison of the capacitance–voltage ($C-V$) measurements with the simulated $C-V$ curves. All the simulations reported in this work have been obtained by means of a one-dimensional self-consistent Poisson–Schrodinger solver, that has been already validated in thicker oxides biased in the Fowler–Nordheim regime.[3] We have used $0.5m_0$ for the electron effective mass (where m_0 is the mass of free electron at rest) and 3.1 eV for the barrier height in the conduction band at the Si/SiO_2 interface. These values are in substantial agreement with those used in the literature.[4–8]

Initially, we compute the gate current as a function of the gate voltage (with drain and source grounded) for a fresh oxide taking in account only the direct tunneling of electrons between the conduction bands at the gate and at the substrate (DT). The results are plotted in Fig. 1 together with the experimental measurements: a perfect agreement can be ob-

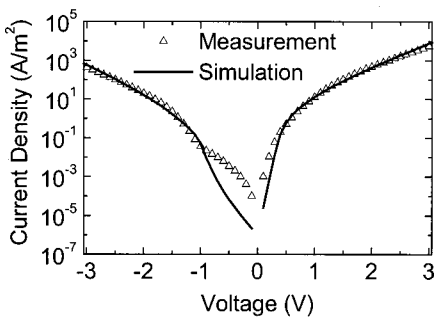

FIG. 1. Comparison between the $J-V$ curves measured and simulated in an ultrathin oxide n-MOSFETs. A perfect agreement is observed except at low negative voltages.

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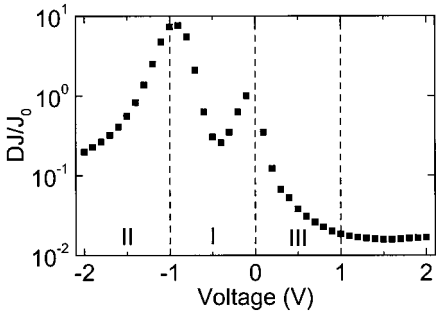

FIG. 2. Relative increase of the current density, DJ/J_0, after a high field stress as a function of the gate voltage in an ultrathin oxide *n*-MOSFETs. At voltages lower than about 1 V, DJ/J_0 is higher and voltage dependent.

served in all the voltage range except in the region between 0 V and $V_{\mathrm{FB}}(\approx -1\,\mathrm{V})$, where an additional conduction mechanism has to be considered, as will be discussed in the following.

After a high voltage stress, 300 C/cm^2 at a constant gate voltage of 4 V, we observed an increase of the current through the oxide. In Fig. 2 we plot as a function of the sensing voltage the relative increase of the current, DJ/J_0, with $DJ=J-J_0$, where J_0 and J are the current density measured before and after the electrical stress, respectively.

For voltages higher than about 1 V, DJ/J_0 is practically independent of the voltage, in agreement with the results reported by DiMaria *et al.*[9] This stress-induced leakage current (SILC) has been ascribed to the tunneling assisted by traps (TAT) inside the oxide and therefore it has been used as a monitor of the trap buildup during the stress up to the oxide breakdown.[10] For voltages lower than about 1 V, the SILC level is voltage dependent and is much larger than the plateau level. Although in the case of SILC due to TAT a few authors have proposed that the tunneling is inelastic (with an energy loss of 1.5 eV),[4,11,12] we think that this low voltage SILC is due to elastic tunneling, because we observe it at voltages as low as a few millivolts and if tunneling electrons lost an energy amount significantly higher than the energy corresponding to the applied voltage (a few millielectronvolts), they would not find available states at the anode.

This low voltage SILC can be explained by the presence of stress-induced interface states in the silicon band gap at both interfaces, gate and substrate, whose effect is clearly more pronounced at low voltages. We distinguish three regions on the basis of the dominant SILC mechanism, evaluated in terms of DJ/J_0, referred to as region I, $V_{\mathrm{FB}}<V_G<0$ V, region II, $V_G<V_{\mathrm{FB}}$, and region III, $0\,\mathrm{V}<V_G<1$ V. In the following discussion we will discard, in the evaluation of DJ/J_0, the contribution due to the direct and the oxide trap assisted tunneling of electrons between the silicon conduction bands, because the former does not change after stress and the latter gives a lower, voltage independent contribution, as observed for voltages larger than 1 V. In each region, we will discuss all the possible conduction mechanisms involving the interface states at least at one of the interfaces.

Figure 3(a) shows the simulated band diagram corresponding to a generic voltage ($V_G=-0.5$ V) in region I. The three plausible different conduction mechanisms involving the interface states are:

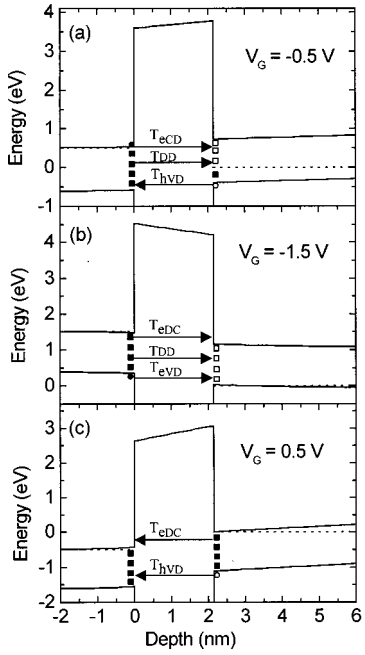

FIG. 3. Band diagram corresponding to a generic voltage in the region I (a), II (b), and III (c). Sketches of the conduction mechanisms involving the interfaces states in the three regions are also drawn.

(1) the tunneling of electrons from the gate conduction band to the substrate empty interface states, T_{eCD};
(2) the tunneling of electrons from the gate occupied interface states to the substrate empty interface states, T_{DD}; and
(3) the tunneling of holes from the substrate valence band to the gate occupied interface states, T_{hVD}.

The T_{eCD} mechanism should be the dominant one because the potential barrier is lower with respect to the other two cases and because at the cathode the electron concentration in the conduction band is larger than the concentration of occupied interface states necessary for the T_{DD} mechanism. It is worth noticing that this T_{eCD} mechanism can also explain the additional current component observed in fresh oxides in the region I, as indicated by the comparison with the simulation shown in Fig. 1. The analysis of the DJ/J_0 data in this region can be used as a monitor of the substrate interface states, because varying V_G between the V_{FB} and 0 V, the emitter in the T_{eCD} mechanism (conduction band electron) scans the substrate interface states between E_c and $\sim E_c-1/3E_G$. As DJ/J_0 should be increase as the relative increase of the interface states, DD_{it}/D_{it0}, this observation indicates that, at least in our case, at the energies close to edge of the conduction band where the D_{it} is higher also its relative increase results higher. Moreover the concavity in the DJ/J_0 centered at $V_G=-0.4$ V (emitter aligned at the interface states at $E_c-0.22$ V) corresponds to the similar concavity observed in the D_{it} at $\sim E_c-0.2$ V in another work.[2] It can be observed that DD_{it}/D_{it0} close to the conduction band edge results a factor 30 higher than the minimum at $E_c-0.2$ V.

Figure 3(b) reports the band diagram corresponding to a generic voltage ($V_G=-1.5$ V) in the region II. The three

plausible different conduction mechanisms involving the interface states are:

(1) the tunneling of electrons from the gate occupied interface states to the empty states in the substrate conduction band, $\dot{T}_{eDC}$;
(2) the tunneling of electrons from the gate occupied interface states to the substrate empty interface states, T_{DD}; and
(3) the tunneling of electrons from the gate valence band to the substrate empty interface states, T_{eVD}.

The T_{eDC} mechanism should be dominant because the potential barrier is lower with respect to the other two cases and because at the anode the concentration of empty states in the conduction band is larger than the concentration of empty interface states required for the T_{DD} and the T_{eVD} mechanism. It should be noted that in this region the T_{eCD} mechanism is not active, because the conduction band electrons in the gate are not aligned to the energy states in the substrate silicon gap. The sharp decrease of DJ/J_0 for voltages slightly smaller than V_{FB} is due to the turn-off of the T_{eCD} mechanism, whereas for lower voltages it is due to the steep increase of the DT and the TAT mechanisms, that, as discussed before, give no (DT) or much lower (TAT) contribution.

Figure 3(c) reports the band diagram corresponding to a generic voltage ($V_G = 0.5$ V) in the region III. The two plausible conduction mechanisms involving the interfaces states are:

(1) the tunneling of electrons from the substrate occupied interface states to the empty states in the gate conduction band, T_{eDC}; and
(2) the tunneling of holes from the substrate valence band to the gate occupied interface states, T_{hVD}.

Note that the current fluxes associated with the two mechanisms are opposite and therefore the T_{eDC} is clearly the dominant mechanism because we observe an increase in the current after the stress and not a decrease. The sharp decrease of DJ/J_0 for voltages slightly larger than 0 V is due to the turn-off of the T_{eCD} mechanism, whereas for larger voltages it is due to the steep increase of the DT and the TAT mechanisms, that, as discussed before, give no (DT) or much lower (TAT) contribution.

A more quantitative discussion of Fig. 2 would require the knowledge of important unknown parameters, such as the capture cross section and the density of interface states per unit energy. The determination of such parameters, both by fitting with numerical simulation or by independent measurement, is beyond the scope of the present work.

Another mechanism that introduces an additional component to the leakage current at low voltages after a high field stress is the boron passivation at the substrate by means of mobile hydrogen released at the anode by injected electrons.[9] The lowering of the doping at the substrate results in a strong increase of the leakage current in the region I, due to the lowering of the thermionic barrier associated with the silicon energy gap at the substrate.[2] Results from simulations indicate that if only this mechanism were present, the increase of DJ/J_0 at voltages close to 0 V should be much higher with respect to the increase of DJ/J_0 at voltages close to V_{FB}, thus excluding that the boron deactivation can be the dominant effect in all the region I. In conclusion, we have studied the leakage current in ultrathin MOS devices at low voltages. We propose that the additional current component with respect to the direct tunneling between the conduction bands measured before and after the application of an electrical stress is mainly due to electron tunneling involving the native and stress-induced interface states in the silicon band gap either at the cathode or at the anode.

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