Twenty-four percent efficient silicon solar cells with double layer antireflection coatings and reduced resistance loss

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Significant performance increase for silicon solar cells is reported. This has been achieved by a combination of several mechanisms. One is the reduction of recombination at cell surfaces using atomic hydrogen passivation of silicon/silicon dioxide interfaces. Joule resistive losses in the cell have been reduced by a process which allows different thickness for fine and coarse features in the top cell metallization. Finally, reflection losses have been reduced by the use of a double layer antireflection coating. For successful incorporation, this required the development of techniques for growing the surface passivating oxide very thin, without reducing its passivation qualities. The cells display a monochromatic light energy conversion efficiency of 46.3% for 1.04 μm wavelength light, also the highest ever for a silicon devices. © *1995 American Institute of Physics.*

Despite the maturity of silicon cell technology, with the first modern devices reported in 1954,[1] the last 10 years have seen a massive improvement in silicon cell energy conversion efficiency.[2] Between 1983 and 1991, cell efficiency increased from 17% to 23%.[2] This letter reports the first major improvement beyond the latter figure obtained by a combination of improved passivation of the cell surfaces and reduced optical and Joule resistive losses.

The cell structure used in this work is the passivated emitter, rear locally-diffused (PERL) cell of Fig. 1. Key features include the almost complete enshroudment of the cell in a layer of SiO$_2$. The well-known passivation properties of this interface[3] allow recombination losses in oxide covered areas to be kept very low. Metal contact to the cell rear is made through small holes in this oxide (10 μm×10 μm) to keep the contact area as small as possible due to the inferior recombination properties of this region. Immediately beneath these rear contact areas, the silicon is heavily doped (with boron) to further suppress contact recombination by suppressing minority carrier concentrations. For the present devices, the top surface contact was made via a contact stripe through the oxide of 2 μm width, slightly narrower than in earlier devices[4] to further reduce the recombination loss at this contact.

Other features include the incorporation of an efficient rear reflector formed by the rear Al layer displaced from the silicon surface by the intervening oxide. This configuration gives high internal surface reflectance for all internal angles of incidence of light onto this stack, particularly once this angle exceeds the critical angle of the Si/SiO$_2$ interface (24.7°).[5] The "inverted pyramid" texture on the top surface, formed by anisotropic etching of the originally (100) orientated surface serves two functions. One is to reduce reflection of externally incident light. A second is to give a high reflection of internally incident light reflected from the back surface.[5] In this way, weakly absorbed light can be trapped in the cell for an average path length enhancement of about 40 times for the present devices. This contributes to their outstanding responsivity to weakly absorbed infrared light with a value of 0.786 A/W independently measured at Sandia National Laboratories at a wavelength of 1.04 μm. This is the highest value ever for a silicon cell, well in excess of the previously highest value of 0.75 A/W.[6] This contributes to the record conversion efficiency of 46.3% of light of this wavelength at an incident light intensity of 51.8 mW/cm^2, for any photovoltaic device.

In the present devices, top surface reflection of externally incident light was further reduced by the application of a MgF$_2$/ZnS double layer antireflection (DLAR) coating. The challenge here arises from the fact that the underlying oxide must be kept less than about 250 Å for this coating to be effective.[7] However, our earlier work had shown that good surface passivation was only obtained if the oxide was grown much thicker than this. Table I compares the performance of cells with different thickness of oxide grown in oxygen in the presence of trichloroethane (TCA) and annealed in forming gas. The lower voltages of the cells with thinner oxides result from the poorer surface passivation quality of these oxides. Attempts to etch thick oxides back to the required thickness for DLAR coating were only partially successful,[8] attributed to nonuniform etching on a microscopic scale.
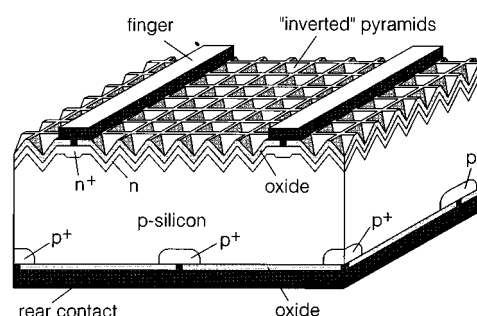
The solution was found by introducing an "alneal" (Al

FIG. 1. The passivated emitter, rear locally-diffused cell.

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TABLE I. Measured cell performance with different oxide thicknesses.

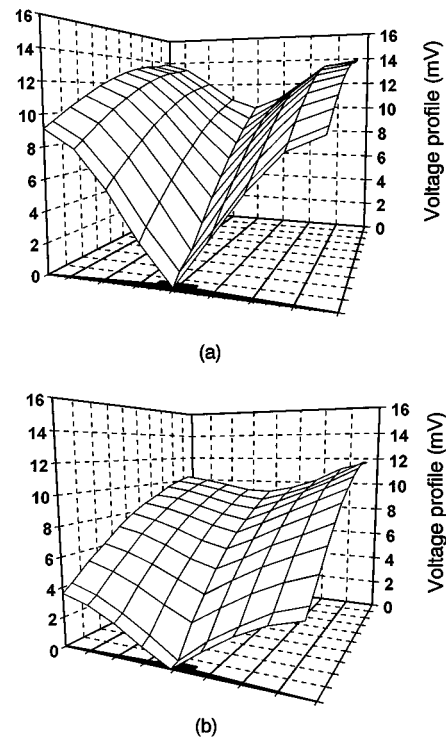| Cell ID	Oxide thickness (Å)	J_{sc} (mA/cm^2)	V_{oc} (mV)
W4-19-2E	200	36.5	682
Z4-16-2E	600	37.5	697
W4-6-1H	1100	40.7	703

FIG. 2. The measured voltage distribution over the cell metal grid at the maximum power point of (a) an earlier PERL cell (cell W413E); (b) a cell with double busbar metal plating (cell ZT11E). The voltage drop along the grid is significantly reduced in case (b).

anneal)[3] step into the top oxide processing sequence. A layer of Al is evaporated onto the oxide on the top surface. The cells are then annealed in forming gas at 370 °C for 30 min. The Al covering the cell aperture is then etched off in phosphoric acid. The rest of the Al around the cell periphery is left on to act as an aperture mask to accurately define the cell area. During the annealing step, it is believed that the Al reacts with hydroxyl ions within the oxide to generate atomic hydrogen. The atomic hydrogen then migrates to the Si/SiO$_2$ interface and passivates defects such as dangling bounds. Repeating the experiment of Table I with this "alneal" processing improvement produced devices with improved open-circuit voltage of close to 709 mV after AR coating regardless of oxide thickness over the range shown. This is about 7 mV higher than the best earlier PERL cells without this feature.[9]

The "alnealing" step was automatically included in earlier processing of the rear surface, since Al is used as the rear contact metal. The "alnealing" which occurs at peripheral areas of the top surface is also thought very important. Surface recombination can be much higher in these nonilluminated areas exacerbating the reduction in current and voltage output caused by these regions.

Relatively low fill factors of around 81% had been another limiting factor for PERL cells in the past.[4,9] Voltage dependence of the rear surface recombination velocity was thought a major contributor.[10] However, careful measurement of cell losses, excluding nonlinear effects due to the previous mechanism, showed significant Joule resistive loss.[11] Cell series resistance was measured as 0.5 Ω cm^2, with a contribution from the front metal grid of 0.3 Ω cm^2.[11]

The plating process used to increase the metallization grid conductivity also broadens these metallization features as it increases their thickness. Since the cells are illuminated in the plating solution, the lower densities of light-generated current near coarse features result in less metal plating in the areas. This was producing excessive voltage drop along coarse features, such as the cell busbar. This is demonstrated by Fig. 2(a), which shows the measured voltage distribution along the cell metallization for a cell at the maximum power

point (not all the metallization fingers are shown). Even though the large voltage drop along the metal grid, the particular cell has a fill factor of 81.2%, which is a relatively high fill factor among the earlier PERL cells.

A two-step plating sequence was developed to correct for this deficiency. Az4620 photoresist is used to protect most of the fine metallization fingers during the second plating step, where the coarse busbar is further plated. This has significantly reduced Joule resistive losses as shown by the voltage profile of Fig. 2(b). The total series resistance of the cell is reduced to 0.3 Ω cm^2 in this way.

Cells with 200 Å oxide and MgF$_2$/ZnS DLAR coatings were processed with these improvements on 1.0 and 1.5 Ω cm float zone substrates and independently tested at Sandia National Laboratories. The results are shown in Table II. The main improvements over earlier devices[4,9] are in open-circuit voltage and fill factor due to the "alnealing" and two-step plating processes, as previously explained. Current output was slightly lower than possible due to a marginally nonoptimal top surface diffusion. The ZnS layer in the DLAR coating also becomes strongly absorbing at wave-

TABLE II. Output parameters of high-performance 4 cm^2 PERL silicon solar cells as measured by Sandia National Laboratories under the global AM1.5 spectrum (100 mW/cm^2) at 25 °C.

Cell ID	Resistivity (Ω cm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill factor (%)	Efficiency (%)
ZT-1-3E	1.0	707	40.7	83.0	23.9
ZT-1-4E	1.5	708	40.8	83.1	24.0
ZT-1-5E	1.0	709	40.9	82.7	24.0

lengths below 390 nm, reducing current density by between $0.5 - 1.0$ mA/cm^2. Further improvements seem likely to produce cell efficiency above 25%.

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