1.5 nm Direct-Tunneling Gate Oxide Si MOSFET's

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Abstract—**In this paper, normal operation of a MOSFET with an ultra-thin direct-tunneling gate oxide is reported for the first time. These high current drive n-MOSFET's were fabricated with a 1.5 nm direct-tunneling gate oxide. They operate well at gate lengths of around 0.1 μm, because the gate leakage current falls in proportional to the gate length, while the drain current increases in inverse proportion. A current drive of more than 1.0 mA/μm and a transconductance of more than 1,000 mS/mm were obtained at a gate length of 0.09 μm at room temperature. These are the highest values ever obtained with Si MOSFET's at room temperature. Further, hot-carrier reliability is shown to improve as the thickness of the gate oxide is reduced, even in the 1.5 nm case.**

This work clarifies that excellent performance—a transconductance of over 1,000 mS/mm at room temperature—can be obtained with Si MOSFET's if a high-capacitance gate insulator is used.

I. Introduction

CONTINUING improvements in integrated circuit fabrication technology have enabled the internal dimensions of semiconductor devices to be steadily reduced. Much progress in MOSFET down-sizing has been accomplished using the scaling method [1] proposed by R. H. Dennard *et al.* in [1] and its modifications. Recently, however, it has proven difficult to reduce MOSFET gate lengths below 0.1 μm using this scaling method, since there are certain limitations in the scaling of the parameters. For example, in 0.1 μm devices, a gate oxide thickness of 3–4 nm [2]–[4] and a channel impurity concentration of $5 \times 10^{17} - 1 \times 10^{18}$ cm^{-3} [2]–[4] are usually adopted. Reducing the gate oxide below 3 nm appears to be difficult because current leaks through the oxide by direct-tunneling. Increasing the channel concentration above 1×10^{18} cm^{-3} is also likely to be difficult, since this will lead to problems of tunneling leakage current through the source/drain and channel (substrate) junction.

It has been reported that 0.04 μm gate length n-MOSFET's can be fabricated by reducing the source and drain junction depths to 10 nm [5]. This type of MOSFET is illustrated in Fig. 1(a). These shallow junctions were successfully produced by solid-phase diffusion from a PSG film, achieving a sheet resistance of less than 10 kohm/sq. The current drive and transconductance of these devices showed a 30% improvement over the figures for 0.1 μm MOSFET's. Although not very large, this increment can be considered reasonable considering the technological difficulties faced in increasing current drive beyond the 0.1 μm regime. The rather limited improvement can be partially attributed to the fact that the sheet resistance of the ultra-shallow source and drain layers is not very low and partially to the fact that the carrier velocity reaches saturation in 0.04 μm devices. Efforts to reduce the sheet resistance still further are continuing, with the aim of further improving current drive [6].

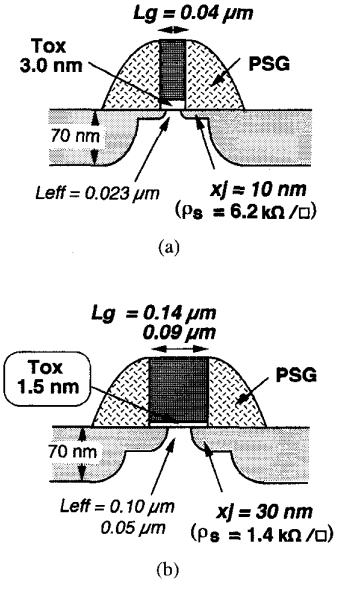

Fig. 1. Different approaches to MOSFET scaling: (a) Reducing junction depth, and (b) reducing gate oxide thickness beyond the tunneling limit.

In this paper, we describe a somewhat different approach. We retain slightly deeper junctions—around 30 nm—so as to keep resistance low, while slightly increasing the gate length to 0.09 μm to achieve MOSFET operation with the deeper junctions and reducing the gate oxide thickness beyond the direct-tunneling limit (3 nm) so as to increase the current drive [7]. This approach is illustrated in Fig. 1(b). Previously, MOSFET's of this type with a direct-tunneling gate insulator had been reported with 2.5 nm gate oxides [8]–[11]. The main question raised by this approach is how well the gate leakage current can be suppressed with such an ultra-thin (1.5 nm) gate oxide film. We have found that the direct-tunneling component of gate leakage is suppressed well in MOSFET's with a deep-submicron gate length. This paper represents an attempt to apply a 1.5 nm gate oxide to 0.1 μm n-MOSFET's. We have succeeded in achieving good transistor operation with

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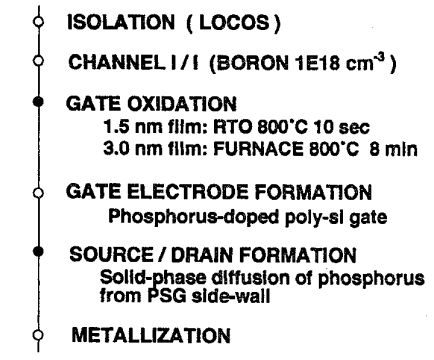
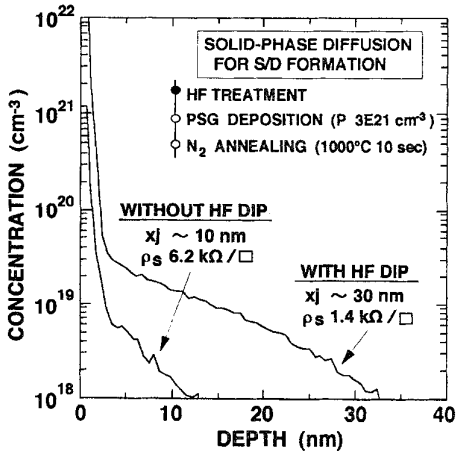


(a)



(b)

Fig. 2. Fabrication of tunneling gateoxide n-MOSFETs: (a) Process, and (b) SIMS profiles of phosphorus distribution in source and drain layers.

such thin direct-tunneling gate oxide MOSFET's for the first time.

II. Experimental

A. Sample Fabrication

Sample n-MOSFET's with a direct-tunneling gate oxide were fabricated for use in our experiments. Fig. 2(a) shows the fabrication procedure used for these MOSFET's. A $P(100)$ Si substrate was used as the starting material. After LOCOS isolation, channel doping was carried out using a 12 nm sacrificed oxide film by implantations with boron ($3.6 \times 10^{13}\text{cm}^{-2}$; 50 keV). The channel concentration was approximately $1 \times 10^{18}\text{cm}^{-3}$. After removing the oxide film, the ultra-thin gate oxide films were formed. The forming conditions are described in the next section (Section II-B). After gate oxidation, polysilicon doped in situ with phosphorus was deposited for the gate electrode. The film thickness was 100 nm. Gate lithography was carried out using an excimer stepper, and then the resist pattern was thinned to below 0.1 μm by a resist ashing technique using an isotropic oxygen plasma [5], [12].

The n^+ source and drain were formed by solid phase diffusion from the PSG gate side wall; this was achieved with rapid thermal annealing (RTA) at 1,000 °C for 10 s. The phosphorus concentration in the PSG film was 3×10^{21} cm^{-3}. In fabricating these samples, the PSG film was deposited after a diluted HF dip, in contrast with the process used for the 0.04 μm gate length MOSFET's previously published [5]. Low sheet resistance with relatively deep junctions was obtained by this method, as shown in Fig. 2(b). The junction depth of the source/drain diffusion layer was 30 nm, deeper than that in the case of the 0.04 μm gate length MOSFET's (10 nm). However, the sheet resistance was as low as 1.4 kΩ/□, which is one quarter of that in the case of 0.04 μm gate length MOSFET's. As a result, the source-drain series resistance of MOSFET's with deeper junctions, 30 nm, are about 150 Ω μm, while that of the MOSFET's with shallower junctions, 10 nm, are about 800 Ω μm.

After metallization, sintering was carried out at 450 °C in forming gas.

B. Ultra-Thin Gate Oxide Formation

An ultra-thin gate oxide film of 1.5 nm was grown by rapid thermal oxidation (RTO) at 800 °C for 10 s after removing native oxide by a conventional diluted HF treatment, which was followed by a water rinse. Samples with a 3 nm gate oxide were also fabricated as a control. The 3 nm thick gate oxide film was grown by conventional furnace oxidation at 800 °C for 8 min. Fig. 3(a) shows a TEM cross section of a MOSFET with a 1.5 nm gate film. Fig. 3(b) is a magnified view of the gate oxide. The oxide film thickness was determined by TEM observations. It is worth noting that the resulting oxide film is quite uniform and very smooth at the Si/SiO_2 interface. Uniformity is important, since it reduces anomalously large gate leakage currents through weak points where the oxide is thinner. Smoothness is also crucial to higher carrier mobilities.

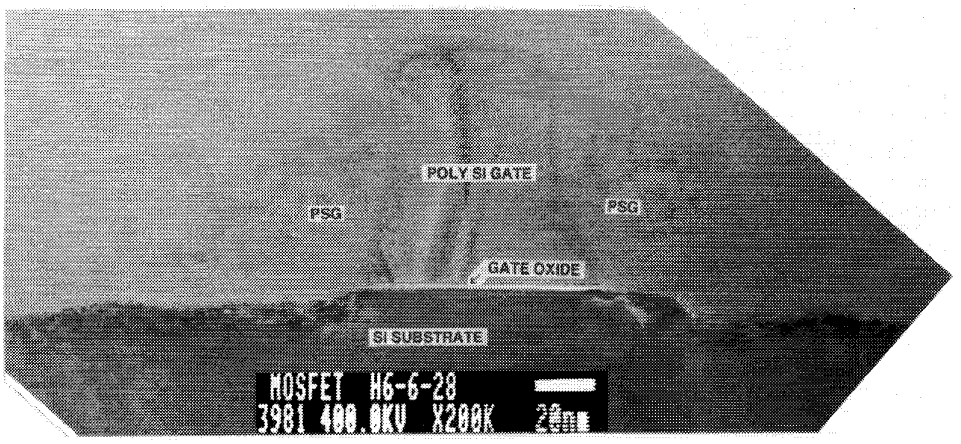
III. Electrical Characteristics

A. I-V Characteristics of MOS Diodes with Direct-Tunneling Gate Oxide

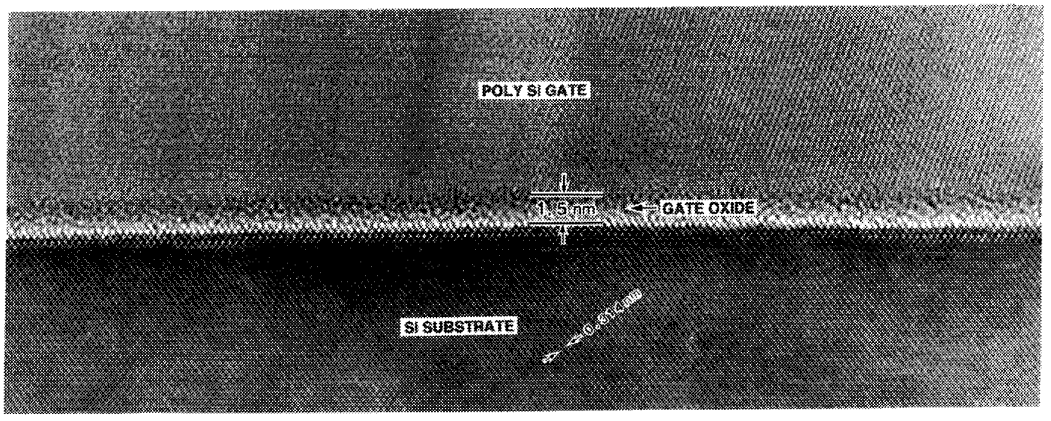
The I-V characteristics of MOS diodes with the 1.5 nm gate oxide are shown in Fig. 4. The diodes are 100×110 μm^2 in area. The characteristics of MOS diodes with thicker gate oxides, ranging up to 12 nm in thickness, are also plotted for reference. Diodes with gate oxides of 2.5 nm and below have a significant leakage component in the region of low gate bias. This is due to direct-tunneling. The gate current in the case of 1.5 nm oxide is of the order of 0.1 μA/μm^2 when the supply voltage is 1.5 V.

B. Current Flow in Direct-Tunneling Gate Oxide MOSFET's

Fig. 5 shows I_d-V_d characteristics for 1.5 nm gate oxide MOSFET's with 10 μm, 5 μm, and 1.0 μm gate lengths. In the long channel case, unusual electrical characteristics are exhibited because of the significant direct-tunneling leakage current through the gate oxide, as shown in Fig. 5(a) and (b).



(a)



(b)

Fig. 3. TEM cross sections of a 1.5 nm gate oxide MOSFET: (a) Cross section through the gate electrode, and (b) Magnified view of 1.5 nm gate oxide.

Large leakage currents are observed even at $V_d = 0$ V, when the gate is biased. However, the characteristics become quite normal as the gate length is reduced below around 1.0 μm, as shown in Fig. 5(c). This is because the gate leakage current is then smaller in comparison with the gate length, and the drain current increases in inverse proportion to the gate length. This is explained in more detail below.

In a direct-tunneling gate oxide MOSFET, there is also a gate leakage current component, $I_g\,(=\, I_{gd} + I_{gs} + I_{gb})$ in addition to the channel current component, I_{ch}. Roughly speaking, as the gate length L_g is decreased, the channel current, I_{ch}, increases in inverse proportion to the gate length. Conversely, the gate leakage component, I_g, decreases in proportion. Thus, the ratio of gate leakage current to channel current, $\frac{I_g}{I_{ch}}$, falls approximately in proportion to the square of gate length, L_g^2.

Figs. 6 and 7 show the dependence of the current flows into each terminal on drain voltage, V_d. The gate voltage, V_g, is the parameter. Long- and short-channel cases are shown in these figures. In the long-channel case, a significant amount of gate terminal current, I_g, is observed (Fig. 6(c)), while in the short-channel case, no such gate current component appears on the plot (Fig. 7(c)). Here, I_g is the sum of I_{gd}, I_{gs}, and I_{gb}. It should be noted that I_{gb} is very small compared with I_{gd} and I_{gs}, because in the case of positive gate bias, an inversion layer forms, shielding the substrate almost completely from

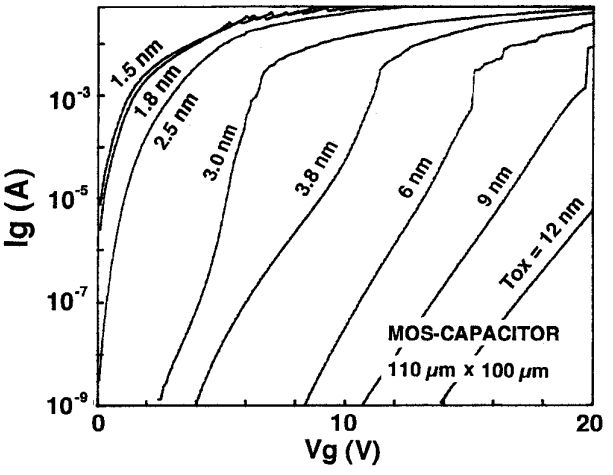
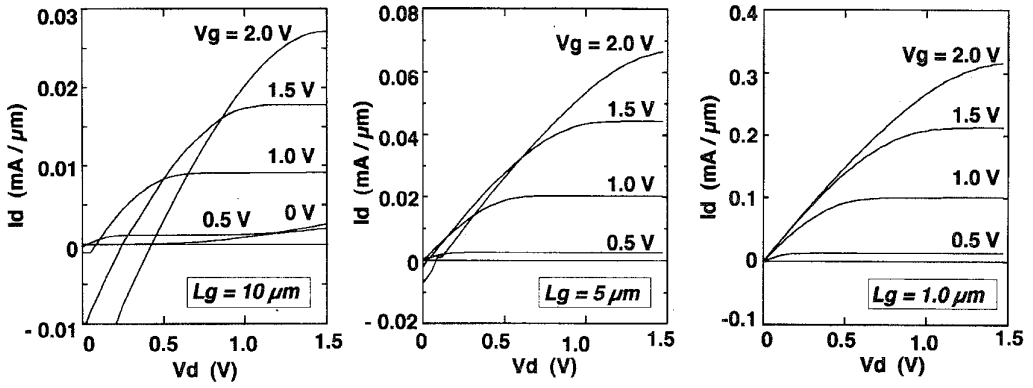
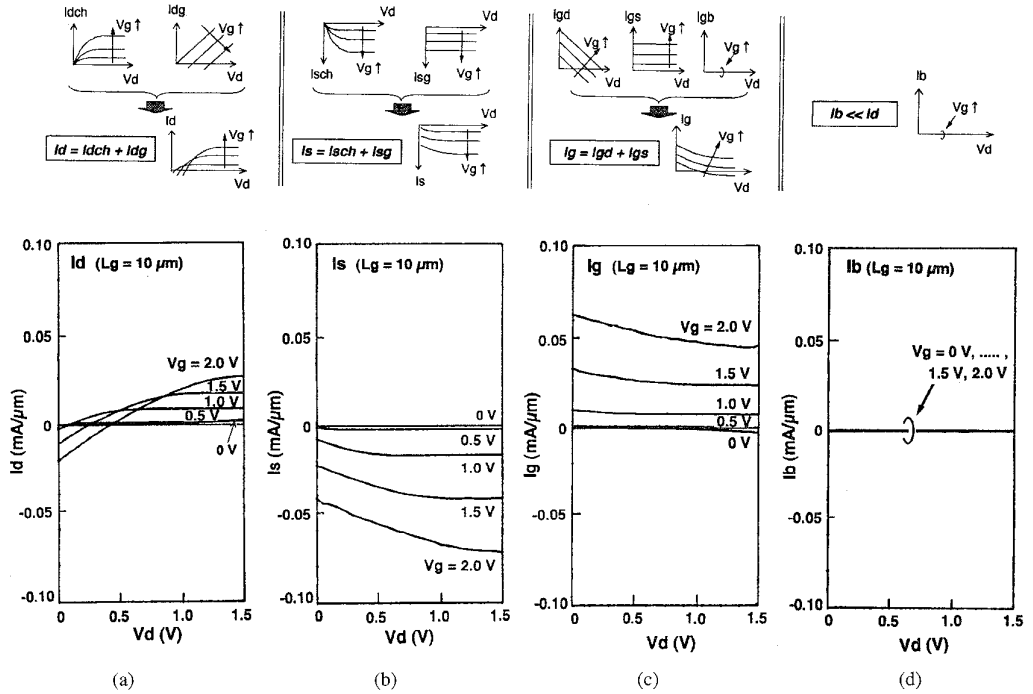


Fig. 4. Dependence of I-V characteristics on gate oxide film thickness for various MOS capacitors. Capacitor area is 100 × 110 μm^2. Film thicknesses 3.8 nm and below were determined by TEM.



(a) (b) (c)

Fig. 5. I_d-V_d characteristics of 1.5 nm gate oxide MOSFET's with 10, 5, and 1.0 μm gate lengths: (a) 10 μm gate length, (b) 5 μm gate length, and (c) 1.0 μm gate length.



(a) (b) (c) (d)

Fig. 6. I-V characteristics of 1.5 nm gate oxide MOSFET with 10 μm gate length: (a) Current at drain terminal, (b) current at source terminal, (c) current at gate terminal, and (d) current at substrate terminal.

the gate, and electrons flowing from the gate into the channel migrate to the drain/source through the inversion layer. In fact, I_b at the terminal is so small as to not appear in the plot even in the long channel case (Fig. 6(d)). The dependences of I_{gd} and I_{gs} on V_d with V_g as a parameter is illustrated at the top of Fig. 6(c). It is easy to see that the measured I_g curves for the long channel MOSFET (Fig. 6(c)) are the sum of the I_{gd} and I_{gs} curves.

In a similar way, the irregular I_d and I_s curves (Fig. 6(a) and (b)) and the asymmetry between the I_d and I_s curves can be seen as the sum of the I_{dch} and I_{dg} curves, and the sum of the I_{sch} and I_{sg} curves, respectively.

In the short channel case, all the gate leakage current components, I_{gd}, I_{gs}, and I_{gb} (Fig. 7(c)) are at least a few orders of magnitude smaller than the channel current components, I_{ch}. Thus, the I_d and I_s curves reflect typical MOSFET characteristics and there is a symmetry between the I_d and I_s curves. Because of the small gate leakage components, I_g and I_b cannot be seen in these plots (Fig. 7(c) and (d)).

C. Current Drive and Transconductance

Fig. 8 shows the I_d-V_d and $g_m - V_g$ characteristics of 0.14 μm and 0.09 μm n-MOSFET's. The effective channel lengths of these devices were estimated to be about 0.10 μm and 0.05 μm, respectively, from the source/drain junction depth of 30 nm. Very high current drive was achieved. For example, the drain current at $V_d = V_g$ =1.5 V was 1.1 mA/μm in

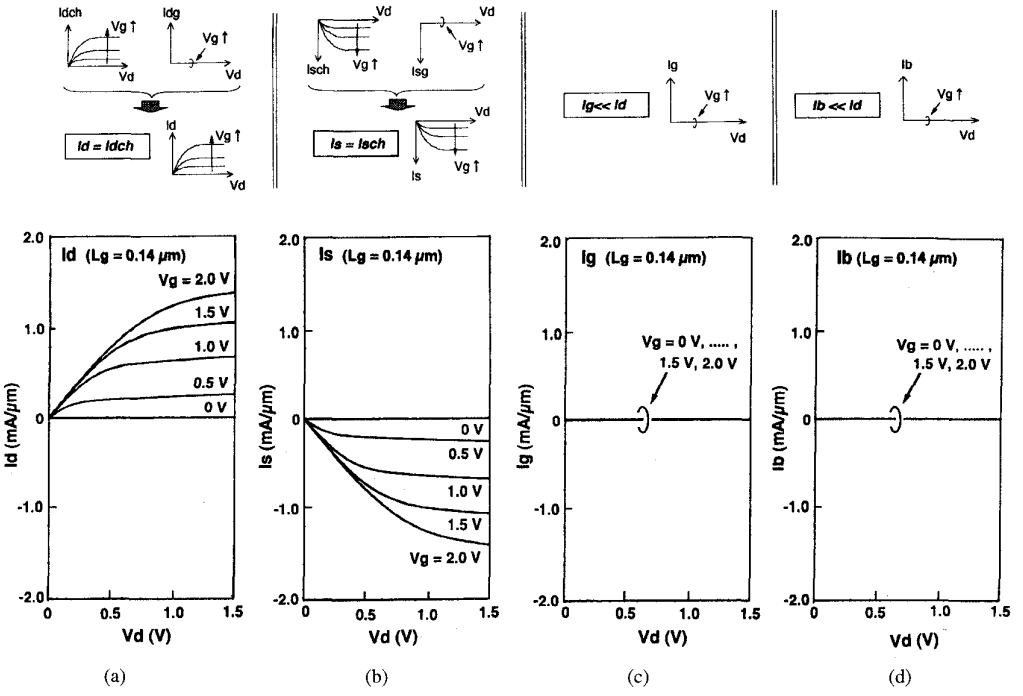


Fig. 7. I-V characteristics of 1.5 nm gate oxide MOSFET with 0.14 μm gate length: (a) Current at drain terminal, (b) current at source terminal, (c) current at gate terminal, and (d) current at substrate terminal.

the case of $L_g = 0.14$ μm and 1.6 mA/μm for $L_g = 0.09$ μm, as shown in Fig. 8(a) and (b), respectively. However, the threshold voltages of these transistors were low—0.00 V for $L_g = 0.14$ μm and -0.21 V for $L_g = 0.09$ μm—because of the short channel effects arising from the relatively deep source and drain junctions of 30 nm. This will tend to cause overestimation of the current drivability. In addition, the bipolar action of the device caused by the injection of the gate leakage current into the substrate would further increase the channel current. The drain currents at $V_d = V_g = 1.5$ V should thus be normalized by the threshold voltage. Assuming $V_{th} = 0.3$ V for $V_d = 1.5$ V, the normalized values for I_d are 0.85 mA/μm for $L_g = 0.14$ μm, and 1.2 mA/μm for $L_g = 0.09$ μm, respectively. This very high drive current of 1.2 mA/μm is more than 1.8 times greater than the maximum measured for a conventional n-MOSFET at room temperature [2], [13]–[15].

Extremely high transconductance was also obtained. The values are 857 mS/mm for $L_g = 0.14$ μm and 1,010 mS/mm for $L_g = 0.09$ 0.14 μm. This value of 1,010 mS/mm is 1.4 times larger than the conventional maximum for n-MOSFET's with a supply voltage of 1.5 V at room temperature—given as 740 mS/mm [13] and 620 mS/mm [2]. These ultra-high performance figures can be attributed to the high capacitance of the ultra-thin gate oxide. In addition, in the $L_g = 0.09$ μm case, there may be some overestimation of transconductance due to the short channel effects [16], similarly as the drive current case explained in the previous paragraph.

The effect of the thin gate oxide on MOSFET characteristics was further investigated. Fig. 9(a)–(c) shows the dependence of drain current, transconductance, and threshold voltage on the gate length when the supply voltage is 1.5 V. These figures compare the results with those for MOSFET's with a 3 nm gate oxide and 10 nm and 30 nm source/drain junction depths, x_j. Certainly the effective channel lengths, L_{eff}, of samples with the same gate length, L_g, differ in the 10 nm x_j and 30 nm x_j cases.

In the case of 10 nm x_j, increases in drain current and transconductance values start to saturate in the deep-submicron region due to relatively higher source/drain extension resistance and velocity saturation. In the cases of 30 nm x_j with both 1.5 nm and 3.0 nm gate oxides, the increase continues down to the deep-sub-0.1 μm range due to relatively lower source/drain extension resistance and short channel effect resulting from the deeper junctions. As shown in Fig. 9(c), the short channel effect starts in the deep-sub micron region in the cases of 30 nm x_j, while it becomes notable in the deep-sub-0.1 μm region in the case of 10 nm x_j.

In the short channel region at around $L_g = 0.1$ μm or below, drain current and transconductance are very much affected by small-geometry effects such as enhanced drain current and transconductance, velocity saturation, and the series resistance of the source/drain extension. Thus, the contribution of gate oxide thinning to performance has been compared over a relatively wide range of gate lengths from sub-micron gates to 1.0 μm. Throughout this region, short channel effects appear in none of the samples and the gate leakage current remains at least one order of magnitude lower than the channel current. Thus, it is fair to compare the effects of gate oxide thickness in this region. The figure shows that I_d and g_m values for 1.5 nm gate oxide MOSFET's are 1.5–1.6 times larger than those for 3 nm oxide MOSFET's in this region. This increase is smaller than the ratio of gate film thickness $(3/1.5 = 2)$, presumably because of the effect of the higher normal electric field in the 1.5 nm sample on the degradation of carrier conduction, and

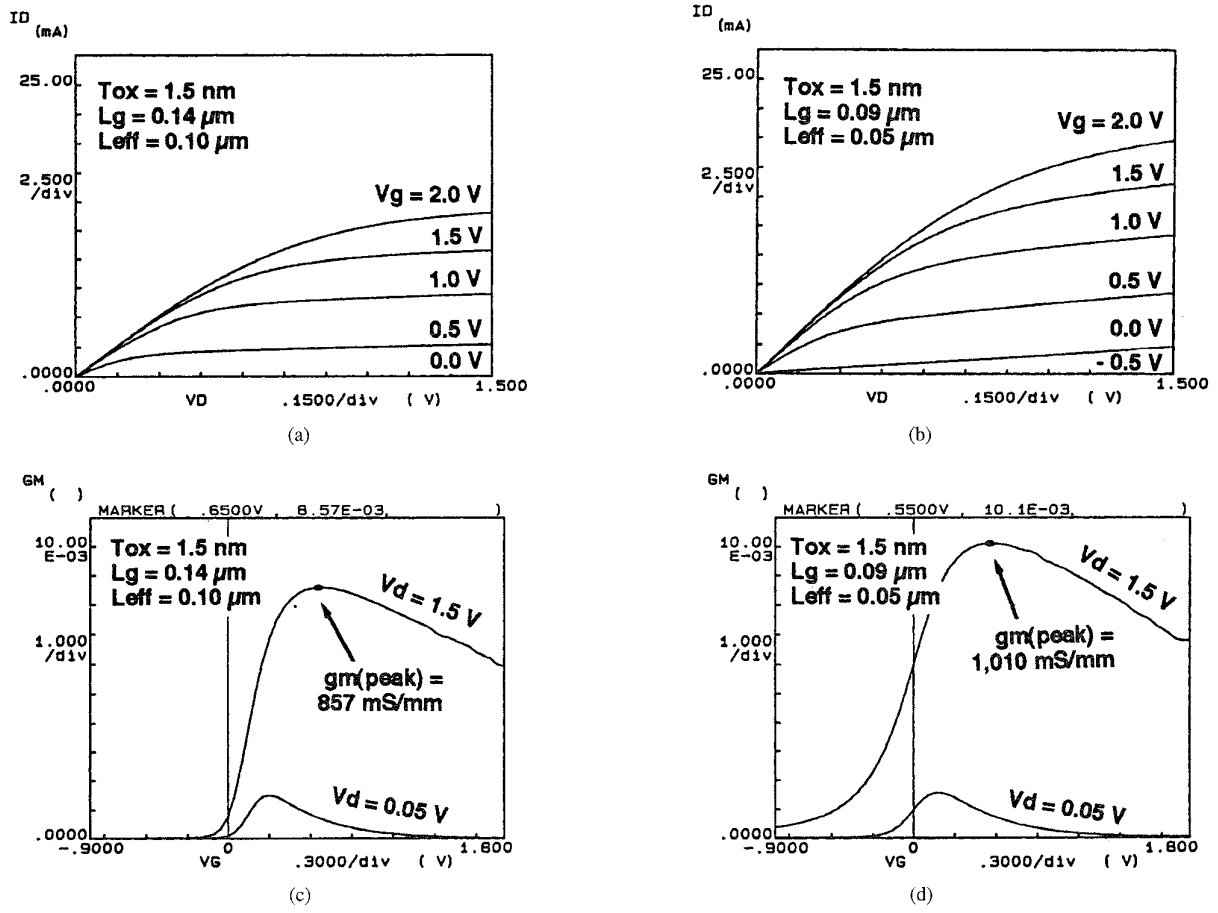


Fig. 8. I_d-V_d and g_m-V_g characteristics of 1.5 nm gate oxide MOSFET's with 0.14 μm and 0.09 μm gate lengths. Gate width is 10 μm:(a) I_d-V_d characteristics for 0.14 μm gate MOSFET, (b) I_d-V_d characteristics for 0.09 μm gate MOSFET, (c) g_m-V_g characteristics for 0.14 μm gate MOSFET, and (d) g_m-V_g characteristics for 0.09 μm gate MOSFET.

also due to the effect of inversion layer capacitance on the reduction of total gate capacitance.

D. Gate Leakage Current

Fig. 10(a) shows the dependence of gate leakage current on gate length in 1.5 nm gate oxide MOSFET's. Drain and gate voltages are 1.5 V. Leakage is 3×10^{-7} A/μm^2 for the 1.5 nm gate oxide. This corresponds to the gate oxide leakage current measured in large MOS capacitors described in Section III-A, 1×10^{-7} A/μm^2 at 1.5 nm. The measured gate leakage current decreases in proportion to L_g. The slope is about 1.8, which is more significant than the simple estimate previously given in Section III-B. A more accurate two-dimensional simulation is required to explain the gate length dependence of the gate leakage current, but this has not been done.

Fig. 10(b) shows the dependence of the ratio $\frac{I_g}{I_d}$ on the gate length of 1.5 nm direct-tunneling gate oxide MOSFET's. The measured ratio decreases as L_g falls, in proportion to $L_g^{2.6}$. This is also more significant than the simple estimate previously given in Section III-B. For example, the ratio was found to be 1.3 at $L_g = 10$ μm, while it was be 3.0×10^{-6} at $L_g = 0.1$ μm. By the earlier estimate, the ratio falls by 10 000 as the gate length is reduced from 10 to 0.1 μm, while in the experiment the actual reduction was 430 000.

IV. Hot-Carrier Reliability

A. Hot-Carrier Generation

It is known that the hot-carrier generation becomes more significant as the gate oxide is reduced in thickness. Fig. 11(a) shows the I_{SUB} (substrate current)—V_g curve for the 1.5 nm and 3.0 nm gate oxide MOSFET's with the same source/drain junction depth of 30 nm. The drain voltage was 1.5 V. As expected, a very large substrate current (3×10^{-8} A/μm) was observed in the 1.5 nm gate oxide case, even at this low drain voltage.

Fig. 11(b) shows the corresponding $\frac{I_{sub}}{I_d}$ (impact ionization ratio)—V_g curve for 1.5 nm and 3.0 nm gate oxide MOSFET's with the same source/drain junction depth of 30 nm. The impact ionization rate is also significant in the 1.5 nm gate oxide MOSFET's.

B. Hot-Carrier Stress Induced Degradation

The hot-carrier degradation of direct-tunneling oxide gate n-MOSFET's was investigated. Stress was applied at the maximum substrate current for 100 s. The drain voltage during stress was 2.5 V.

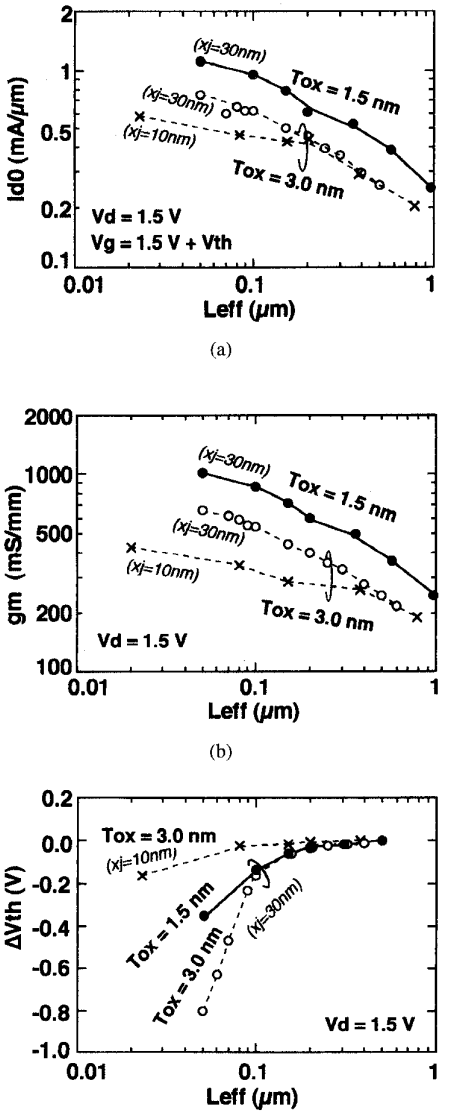


Fig. 9. Dependence of drain current, transconductance, and threshold voltage shift on effective channel length: (a) Drain current, (b) transconductance, and (c) threshold voltage shift.

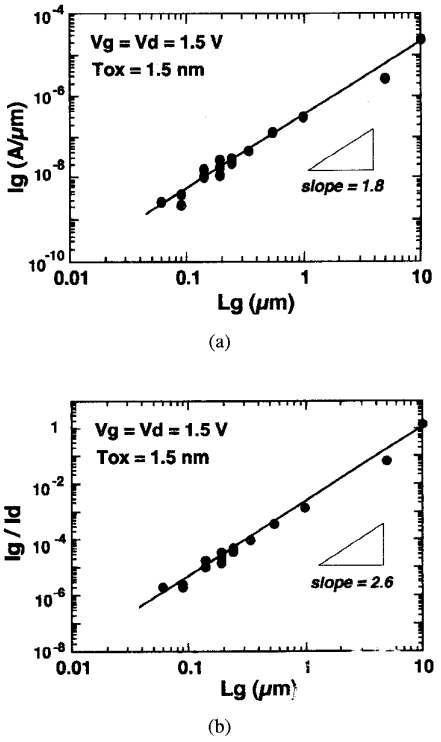


Fig. 10. Dependence of gate leakage current on gate length: (a) Gate leakage current, and (b) ratio of gate leakage current to drain current.

Fig. 12 shows the dependence of transconductance on initial substrate current. Despite the high substrate current and impact ionization rate, the 1.5 nm oxide MOSFET's have better hot-carrier reliability than the 3.0 nm samples. The findings of Toyoshima *et al* [17] that n-MOSFET's with thinner gate oxides have better hot-carrier reliability still appear to hold true for gate oxides down to 1.5 nm. Fig. 13 schematically shows the dependence of effective channel mobility on effective electric field. In thin gate oxide devices, mobility degradation due to interface state generation has a less significant effect on drain current. This is because mobility is governed mainly by surface roughness effects under the extremely high vertical electric field of the channel, while Coulomb scattering by interface states has little influence on mobility.

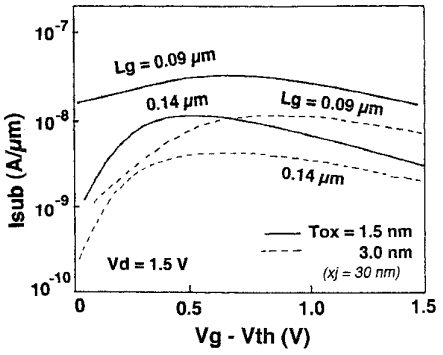
It is known that there is very little threshold voltage shift after hot-carrier stress in MOSFET's with an ultra-thin gate oxide, because charges trapped in the ultra-thin gate oxide are simultaneously detrapped by direct-tunneling [18]. In our experiment, also, no threshold voltage shift at all was seen in the case of 1.5 nm gate oxide MOSFET's.

To summarize these results, we have confirmed that hot-carrier reliability improves as the gate oxide thickness is reduced, even in the 1.5 nm case. Not only does a very thin oxide film of less than about 3 nm contain no trapped charges after hot-carrier stress, but interface state generation also affects mobility degradation less as the gate oxide thickness falls.

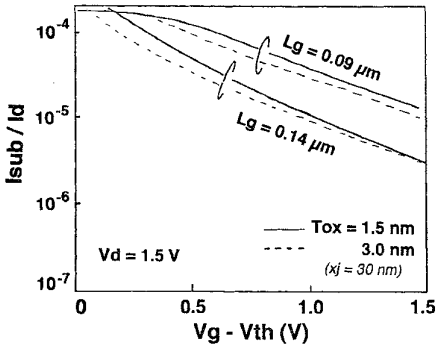
V. Summary and Conclusion

We have found for the first time that 1.5 nm gate oxide n-MOSFET's operate well when the gate length is around 0.1 μm. This is because gate leakage current due to direct-tunneling falls in proportional to the gate length, while drain current increases in inverse proportion. In MOSFET's with this thin gate oxide and with relatively deep source and drain junctions of 30 nm, the drain current drive and transconductance were the largest ever observed at room temperature with a 1.5 V supply.

We have also confirmed that hot-carrier reliability improves as the gate oxide thickness is reduced, even down to the 1.5 nm case. In our experiments, short channel effects were not very satisfactory for n-MOSFET's in the sub 0.1 μm region because of the relatively deep junction needed to ensure there



(a)



(b)

Fig. 11. Dependence of substrate current and impact ionization rate on gate voltage: (a) Substrate current, and (b) impact ionization rate.

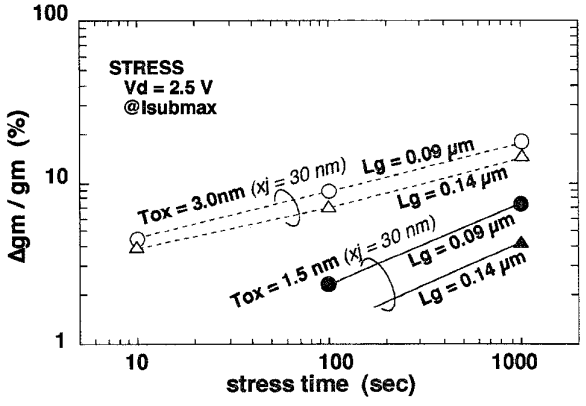


Fig. 12. Dependence of transconductance degradation on stress time. Gate width is 10 μm. Stress applied under $I_{SUB,MAX}$ conditions. Stress drain voltage is 2.5 V.

is no suppression of the high current drive. However, it should be possible to solve this problem in the future using technology which achieves ultra-low resistance in shallower junctions, such as S^4D (silicided silicon source and drain structure [6]; an elevated source and drain structure).

There still remains the question of the reliability of the direct-tunneling gate oxide after long-term low-level bias stress, but at least it can now be said that direct-tunneling gate oxide MOSFET's are worthy of study for use in low-

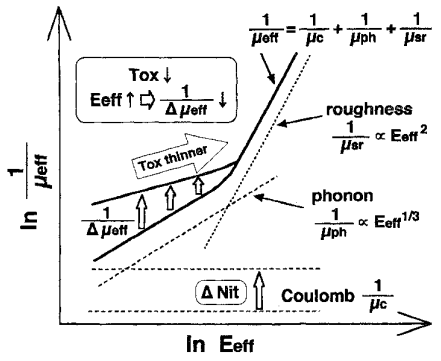


Fig. 13. Effective electric field dependence of effective mobility.

voltage, high-speed devices because of their extremely high current drivability.

This work demonstrates that transconductance of over 1,000 mS/mm is possible in Si devices, as long as a very-high-capacitance gate insulator is used. As one candidate for such a gate film, we have investigated the possibility of reducing the gate oxide thickness below the direct-tunneling limit in small gate length MOSFET's, thus achieving better current drive and transconductance.

Our results suggest that the development of high-ε gate insulators for MOSFET's is important—with thickness equivalent to the direct-tunneling oxide in terms of capacitance, and with considerably higher barrier height to suppress direct-tunneling—as a future replacement for the direct-tunneling oxide.

We can conclude that there is great potential in silicon MOSFET's for much higher current drive than in present devices. We look forward to more progress in silicon MOSFET performance through the development of new technologies such as the ultra-high ε gate insulator described here.

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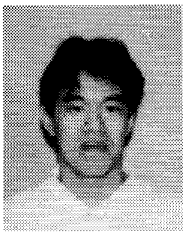

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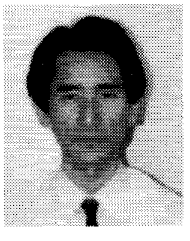

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