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Study of the properties of SiO_x layers prepared by different techniques for rear side passivation in TOPCon solar cells

Nabin Chandra Mandal, Susmita Biswas, Shiladitya Acharya, Tamalika Panda, Sourav Sadhukhan, Jayasree Roy Sharma, Anupam Nandi, Sukanta Bose, Arindam Kole, Gourab Das *, Santanu Maity, Partha Chaudhuri, Hiranmay Saha

Centre of Excellence for Green Energy and Sensor Systems, Indian Institute of Engineering Science and Technology, Shibpur, India

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ABSTRACT

Passivation of n-type and p-type monocrystalline CZ Si wafers (both polished and textured) with silicon oxide layers prepared by thermal (TO), chemical (CO) and plasma (PO) techniques have been extensively investigated from the measurement of minority carrier lifetime (τ) by transient electrical photoresponse method, density of interface states (N_{SS}) measurement by capacitance – voltage study and silicon oxidation states by X-ray photoelectron spectroscopy (XPS) study of the SiO_2/Si interface. It has been observed that N_{SS} and τ have an inverse relation but the dependence is not linear. The method (TO, CO or PO) of oxide layer development has been found to play a crucial role to control the passivation of the c-Si wafer surface. It has been observed that the thermally grown oxide layer (TO) is superior among three oxide layers for all the different c-Si surfaces. Very low density of interface states ($<5 \times 10^{11}$) were found in both p-type and n-type polished wafer passivated with TO layer. Highest lifetimes of 170 μs for n-type polished wafer and 102.74 μs for p-type polished wafer were obtained with TO. The amount of sub oxide formed at the interface of both n- and p-type of wafers during different oxidation process, may have some correlation with N_{ss} which in turn determines the passivation quality of the wafers. Improvement of implied V_{oc} for both polished and textured wafers (n-type and p-type) was found using thermally grown oxide with respect to others.

1. Introduction

Crystalline silicon based solar cell technologies are dominating the photovoltaic (PV) industry for a while and this trend will be sustained for another few decades. There is steady improvement in c-Si based solar cell performance but an Aluminum-Back surface field (Al-BSF) solar cell is still the leading commercialized technology [1–3]. But in last few years there is a swing to enhance the performance of c-Si based solar cell and move forward for the better technologies. Particularly high level of surface passivation is the new trend. Surface passivation of c-Si wafer reduces the recombination occurs at the defects on the surface which causes to enhance the open circuit voltage (V_{oc}) leads to improve the performance of the solar cell.

Many groups have developed different kind of high efficiency solar cells i.e. PERC [4–6]; PERL [7–9]; HIT [10–12]; TOPCon [13–16] mainly on the ground of appropriate surface passivation [4–13]. PERC solar cell technology has been recently industrialized in large scale for its higher efficiency as compared to Al-BSF but it needs high cost laser ablations for making contact and ALD process for rear surface passivation. From the point of view of cost effectiveness Tunnel Oxide Passivated Contact (TOPCon) solar cell technology has the potential and promising candidate to be industrialized in large scale for its high efficiency and minimal process hazardous (simple process steps); moreover it can be fabricated with the existing facilities required for fabrication of Al-BSF solar cells though small modification is necessary. Recently Jinko Solar and Trina Solar has started production of n-TOPCon solar cells with cell efficiency ~24% [17,18]. Excellent surface passivation and selective carrier transport phenomena are involved in TOPCon solar cells [19]. Studies reveal that c-Si surfaces need to be prepared with extreme care in order to get a low surface recombination velocity at the interface [20]. Recently many research groups are trying to optimize the rear-passivation layer by reducing the interface defects and contamination through different types of passivating layers (SiO_2, SiO_x, SiN_x, Al_2O_3 and a-Si:H) [21–23]. But there is very limited work on the basic

* Corresponding author.
E-mail address: gourab_electron@hotmail.com (G. Das).

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understanding about the growth and characteristics of passivating cum tunnelling layer on both n-type and p-type c-Si wafers.

In order to improve the passivating properties, study of the dependency of the minority carrier lifetime on quality and thickness of the passivating layer is immensely essential. Although a number of materials can be chosen as passivation layer for c-Si surface (a-Si, SiN_x, SiO_x), silicon oxide (SiO_x) is the common passivation cum tunnelling layer used in TOPCon solar cells [24].

Tong et al. reported a method to grow high-quality tunnel silicon oxide layer by using acid mixture of HNO_3 and H_2SO_4 in a ratio 3:1 and applied in n-TOPCon solar cell as passivating tunnelling contact [25]. Whereas Huang et al. developed a plasma-assisted N_2O gas oxidation method to prepare the ultrathin SiO_x layer which showed good surface passivation on n-type c-Si wafer for n-TOPCon solar cell [26]. Vossen et al. have done a comparative analysis of differently grown tunnel oxide layers and studied the contact resistivity and surface passivation in details [27]. Substantial reports are presented on the passivation and tunnelling properties of the thin silicon oxide layer in n-type TOPCon solar cell but a very few reports are available regarding p-type TOPCon solar cell. This motivated us to further investigate the surface passivation properties of thin SiO_x layer developed by different means (wet chemically, thermally & plasma assisted) in both n-type & p-type textured as well as polished c-Si wafer surfaces. Here, chemically grown ultrathin (~1.5 nm) silicon oxides referred to as chemical oxide (CO) were prepared on Si by oxidizing the Si wafers with hot concentrated HNO_3, thermally grown oxides of 1.5–2 nm thickness called thermal oxide (TO) were grown by dry oxidation of Si wafers at high temperatures and silicon oxides with thickness ~1.8 nm named plasma oxide (PO) were grown by plasma enhanced chemical vapour deposition (PECVD) method.

In this paper, a study of density of the interface states (N_{ss}) for different SiO_x layers on both n-type and p-type monocrystalline Si wafers has been done from C–V measurements at different frequencies of the metal insulator semiconductor (MIS) devices formed on n-type and p-type Si wafers [28]. The N_{ss} values are then compared with the minority carrier lifetimes determined by quasi steady state photoconductance (QSSPC) technique. We have also tried to find out the information about the insights of the SiO_2/Si interface and stoichiometry by the X-ray photoelectron spectroscopy (XPS). The SiO_x layers were grown by three different techniques and with various thicknesses for optimization. Thickness of the oxide layers is to be limited within a few nanometers as the carriers has to be tunnelled through the passivating oxide layer.

2. Experimental details

2.1. Sample preparation

2.1.1. Development of passivating layer on both side of n-type and p-type monocrystalline silicon wafer

All the process steps for developing oxide based passivating cum tunnelling layer is given below in details.

a) **Starting material:** 180 μm thick p-type and n-type CZ wafers (<100>) were taken having resistivity of 1–3 Ω-cm and 4–4.5 Ω-cm, respectively. Some of the wafers (both p-type and n-type) are taken for texturization and some are kept for polishing.
b) **Texturization:** p-type & n-type CZ as-cut crystalline silicon wafers with plane orientation of <100> has been considered as the substrate on which texturization has been carried out in a chemical bath using 1.8% KOH solution in presence of 5% isopropyl alcohol (IPA) at 80 °C temperature for 35 min for the formation of 4–5 μm size pyramids on both side of the wafers and finally rinsed with DI water.
c) **Polishing:** Polishing of wafers have been done by dipping them in 10% KOH solution at 80 °C for ~4 min and followed by rinsed with DI water.
d) **Cleaning**:
RCA-1 cleaning of wafers: This process has been done by dipping wafers in a solution containing DI water: NH_4OH: H_2O_2 (5:1:1) at (70 ± 5 °C) for 15–20 min.
RCA-2 cleaning of wafers: This process has been done by dipping wafers in a solution containing DI water: HCl: H_2O_2 (4:1:1) at (70 ± 5 °C) for 15–20 min.
Piranha treatment: This process has been done by dipping the wafers in H_2SO_2: H_2O_2 (4:1) solution for 15–20 min.
Removal of native oxide of cleaned silicon wafers: This process has been done by dipping the wafers in 1% HF solution for 1–2 min.

After that cleaned wafers are divided in four groups for different type of oxide layer growth i.e. thermal oxide (TO), chemical oxide (CO), Plasma Enhanced Chemical Vapour Deposited oxide (PO).

e) Different oxide formation on both sides of n-type and p-type silicon wafer *for passivation study by lifetime measurement:*
Chemical oxidation (CO): Chemical oxide was grown on both sides of p-type wafers and n-type wafers by fuming process in boiling HNO_3 (68%) at 100 °C–110 °C for 30 min.
Thermal oxidation (TO): Dry thermal oxidation of p- and n-type silicon wafers were carried out in a tubular type furnace at 850 °C having oxygen flow rate of 8 L/min with oxide growth rate being 0.6 Å/min approximately. The thicknesses of the TO grown on both p-type and n-type wafers were ~1.5 nm.
PECVD oxidation (PO): PECVD oxide (PO) was grown on both sides of p-type and n-type wafers at 250 °C with the help of CO_2 gas with RF plasma (13 MHz) at 60 mW/cm^2 power density and 1 torr pressure.
f) **Annealing of fabricated oxide layers:** CO and PO grown samples prepared by the process mentioned above were further annealed at a temperature of 800 °C in N_2 environment for 30 min. Thicknesses of all the films are verified by XRR and Ellipsometric study.

2.2. Fabrication of Metal Insulator Semiconductor (MIS) devices for Capacitance-Voltage (C–V) measurements

MIS devices were next fabricated by forming an ohmic contact on the back surface and a metal-oxide barrier contact on the front surface. Back surface screen printing was done with aluminum for p-type samples and with silver for n-type samples followed by standard optimized firing process in a three zone belt furnace for the formation of the ohmic contact. Ohmic nature of the contact made by the screen printing method has also been assured independently.

For metal-oxide barrier in the front surface dot like (dot diameter: 2 mm) metal contacts (aluminum for p-type samples and silver for n-type samples) have been vacuum evaporated at room temperature. Thus, a number of metal-insulator-semiconductor (MIS) devices have been fabricated (Fig. 1) on the same wafer for the studies. Different sample specifications have been given in Table 1.

3. Results and discussion

A. ***Lifetime measurement*:** The minority carrier lifetime with the implied open circuit voltages (V_{oc}) for both p-type and n-type oxide passivated silicon wafers have been measured by quasi steady state photoconductance (QSSPC) technique using a Sinton WCT-120 instrument.
B. ***Capacitance vs. Voltage measurement*:** The quality of the diode formed by MIS structure shown in Fig. 1 is fairly good showing very low leakage current as shown in Fig. 2 which indicates that the CV measurement would be a reliable study for evaluating the quality of ultra-thin SiO_x (1.5–2 nm). Energy band diagram of the MIS diodes

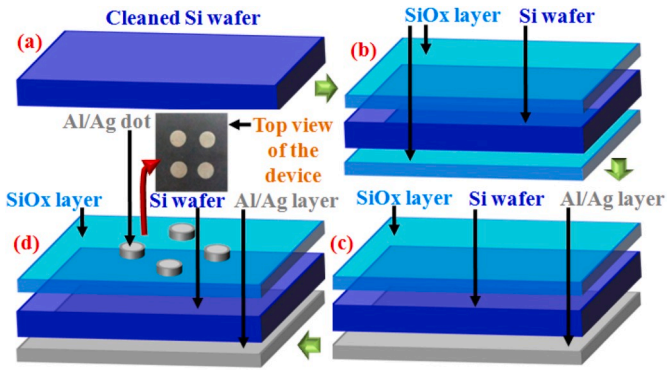

Fig. 1. Schematic diagram of the MIS structure for all samples as well as real image of the top surface of the device (not to be scaled).

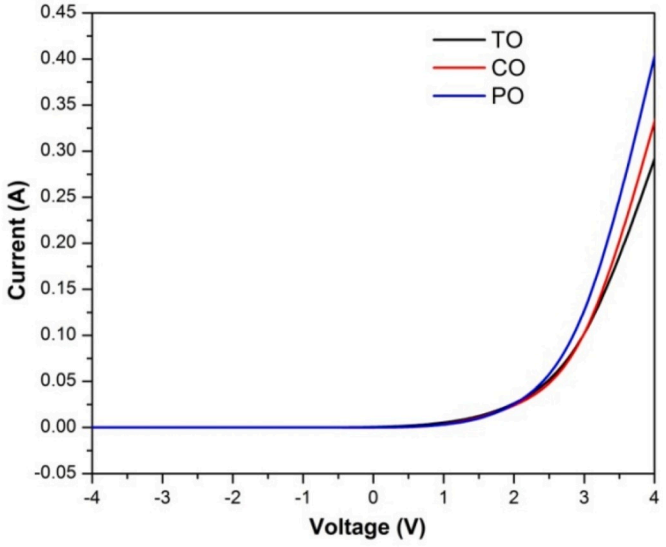

Fig. 2. I–V study of the MIS diode formed with ultrathin SiO_x layers.

formed by metal/oxide/p-type Si and metal/oxide/n-type Si combination are shown in Fig. 3(a) and (b) respectively.

Capacitance vs. Voltage (C–V) and current vs. voltage (I–V) measurements have been carried out on all MIS devices varying voltage from −4 V to +4 V at frequency 5 kHz. C–V measurements were done using Keithley-PCT-CVU-Multi-frequency CV meter. Capacitance-voltage (C–V) plots (at 5 kHz) and respective $1/C^2$ vs. Voltage plot for sample S1 to S12 have been shown in Fig. 4 and Fig. 5 respectively. C–V plots for MIS devices have been analyzed to get the interface state densities Nss.

From the intercept of $1/C^2$ curve with voltage (V) axis the built in potential (V_0) has been obtained and, the barrier height (Φ_b) has been calculated using a well-known equation as follows [29];

$$\Phi_b = V_0 + \Phi_n + \frac{kT}{q} - \Delta\Phi_b \quad (1)$$

Where kT/q is a correction factor due to reserve layer in the semiconductor [29], Φ_n is the energy difference between the Fermi level and the valence band edge for p-type semiconductor and difference between the Fermi level and the conduction band edge for n-type semiconductor; $\Delta\Phi_b$ is the image force barrier lowering being calculated from V_0 [28].

Table 1
Different sample specifications.

Wafer type	Name of sample	Oxidation Process	Back Contact	Front Contact
p-type textured	**S1**	TO	Al	Al
	S2	CO		
	S3	PO		
p-type polished	**S4**	TO		
	S5	CO		
	S6	PO		
n-type textured	**S7**	TO	Ag	Ag
	S8	CO		
	S9	PO		
n-type polished	**S10**	TO		
	S11	CO		
	S12	PO		

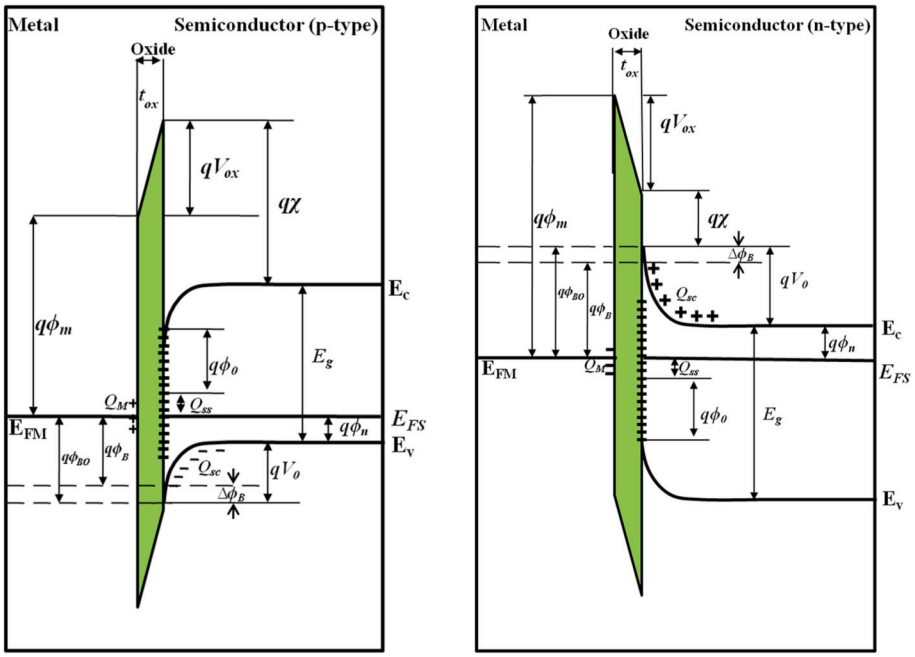

Fig. 3. Energy band diagram of MIS structure (a) melal/SiOx/p-type Si (b) melal/SiOx/n-type Si.
Where E_c = Conduction band edge; E_v = Valance band edge; E_g = Band gap of the semiconductor; E_{FS} = Fermi level of semiconductor; E_{FM} = Fermi level of metal; V_o = Built in potential; t_{ox} = Oxide layer thickness; V_{ox} = Potential across oxide layer; χ = Electron affinity of the semiconductor; φ_m = Work function of the metal; $\Delta\varphi_B$ = Image force barrier lowering; φ_{B0} = Barrier height (without image force lowering); φ_B = Barrier height (with image force lowering); φ_0 = Neutral level of interface states; Q_{sc} = Space-charge density in semiconductor; Q_{ss} = Interface trap charge; Q_M = Surface charge density on metal.

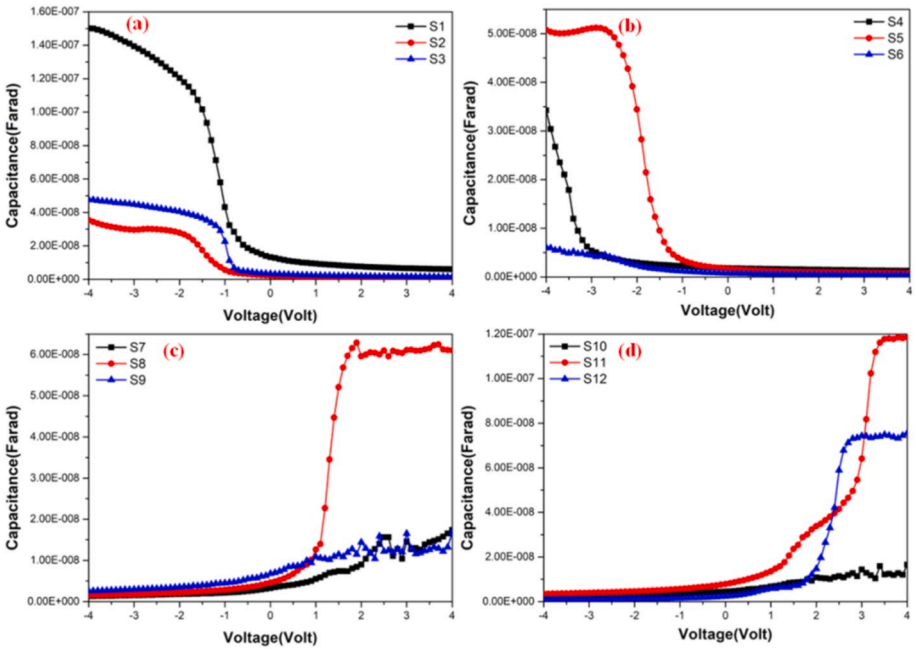

Fig. 4. **(a)** CV characteristics of sample S1, S2, and S3, **(b)** CV characteristics of sample S4, S5, and S6, **(c)** CV characteristics of sample S7, S8, and S9, **(d)** CV characteristics of sample S10, S11, and S12.

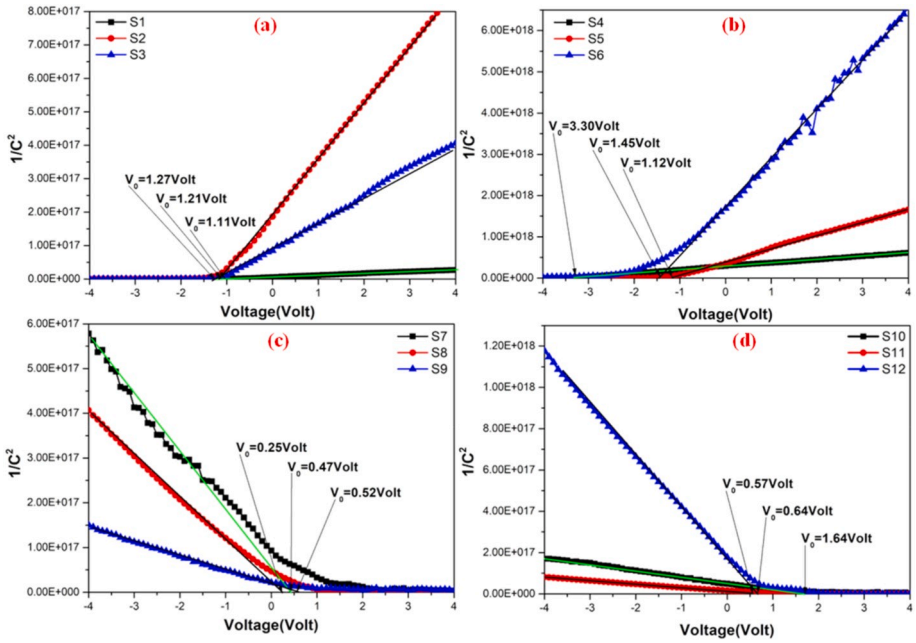

Fig. 5. **(a)** $1/C^2$ vs. Voltage plot of sample S1, S2, and S3, **(b)** $1/C^2$ vs. Voltage plot of sample S4, S5, and S6, **(c)** $1/C^2$ vs. Voltage plot of sample S7, S8, and S9, **(d)** $1/C^2$ vs. Voltage plot of sample S10, S11, and S12.

$$\Delta\Phi_b = \left(\frac{qE_m}{4\pi\varepsilon_S\varepsilon_0}\right)^{\frac{1}{2}} \tag{2}$$

Where q is the electronic charge, ε_S is the dielectric constant of semiconductor, ε_0 is the absolute value of permittivity, E_m is the maximum electric field.

$$E_m = \left(\frac{2qNV_0}{\varepsilon_S\varepsilon_0}\right)^{\frac{1}{2}} \tag{3}$$

Where N is the doping concentration.

The capacitance of insulator layer is given by

$$C_{ox} = C_a\left[1 + \frac{G_a^2}{(\omega C_a)^2}\right] \tag{4}$$

Where C_a and G_a are the value of capacitance and conductance in accumulation region and ω is the angular frequency of CV measurement respectively.

The interface states density (N_{SS}) between silicon and silicon oxide layer is calculated [27] at frequency 5 kHz for all the samples using equation (5).

$$N_{ss} = \frac{2}{qA} \frac{\left(\frac{G_C}{\omega}\right)_{max}}{\left[\left(\left(\frac{G_C}{\omega}\right)_{max} C_{ox}\right)^2 + \left(1 - \left(\frac{(C_C)_{max}}{C_{ox}}\right)\right)^2\right]} \quad (5)$$

Where q is the electronic charge, A is the area of the single top contact, G_C is the corrected value of conductance and C_C is the corrected value of capacitance (correcting factor is a $= G_m - \{(G_m)^2 + (\omega C_m)^2 \times R_S\}$). Where ω is the value of angular frequency corresponding to the frequency 5 kHz, G_m is the measured value of conductance and C_m is the measured value of capacitance and R_S is the series resistance.

We have calculated barrier height (φ_b) and interface state density (N_{ss}) of the respective MIS structure using CV analysis and also obtained minority carrier lifetime (τ) and implied Voc (iV_{oc}) with different SiO_x layer passivation for p-type and n-type textured and polished Si wafer which were shown graphically in Fig. 6.

Fig. 7 represents the non-linear inverse relation between the interface trap state density and minority carrier lifetime. The label of the corresponding samples is also shown. From Fig. 6 it can be observed that for p-type textured silicon wafer PO gives maximum barrier height (1.0311 eV) as compared to other oxides (PO > CO > TO). At the same time TO gives maximum minority carrier lifetime (56.75 μs) as compared to other oxides (TO > PO > CO) and minimum interface state density (9.9203×10^{12}) as compared to other oxides (TO < PO < CO).

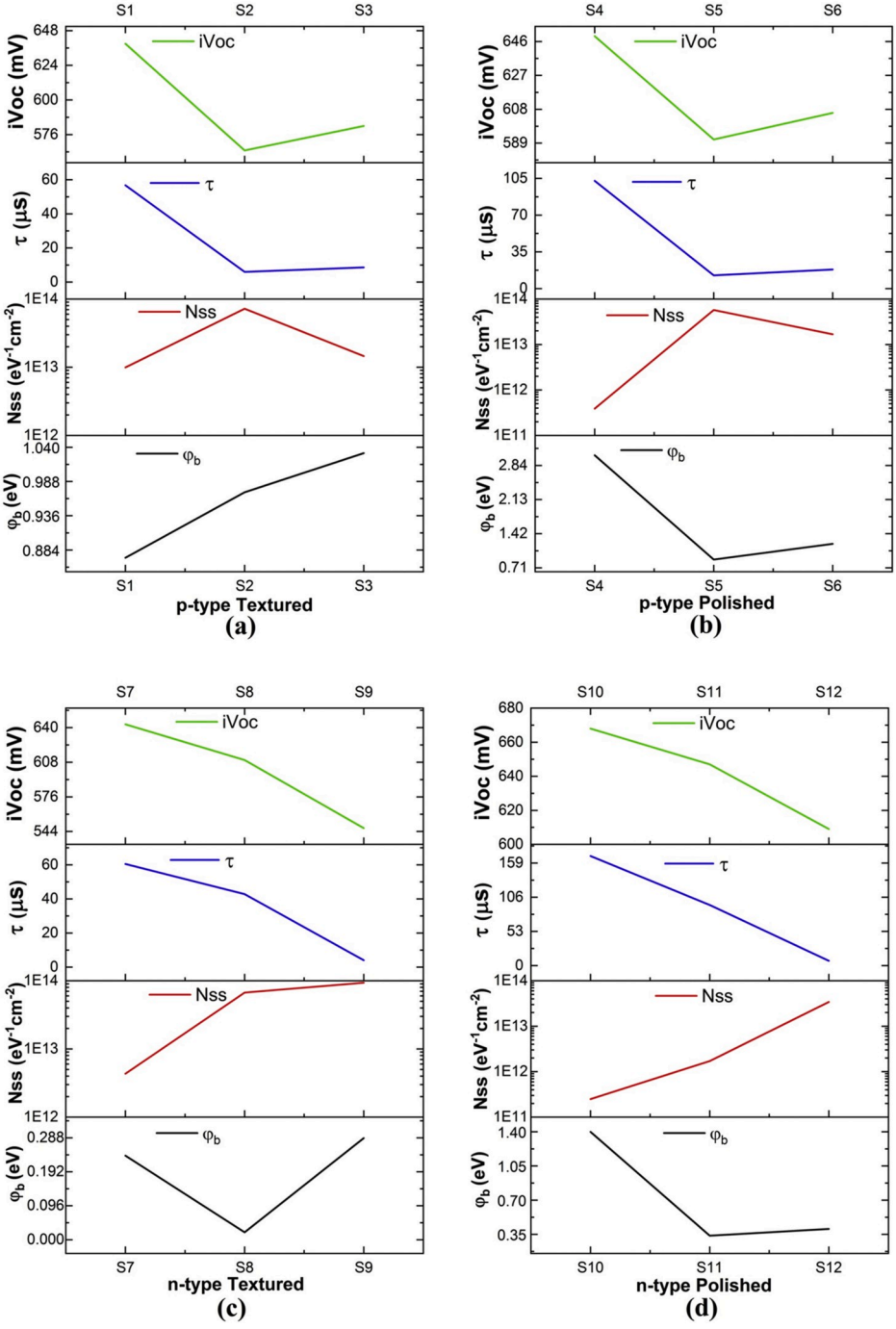

Fig. 6. Variation of barrier height (φ_b), Interface state density (N_{ss}), Minority carrier lifetime (τ) and Implied V_{oc} (iV_{oc}) with different SiO_x layer passivation of (a) p-type textured Si wafer (b) p-type polished Si wafer (c) n-type textured Si wafer and (d) n-type polished Si wafer.

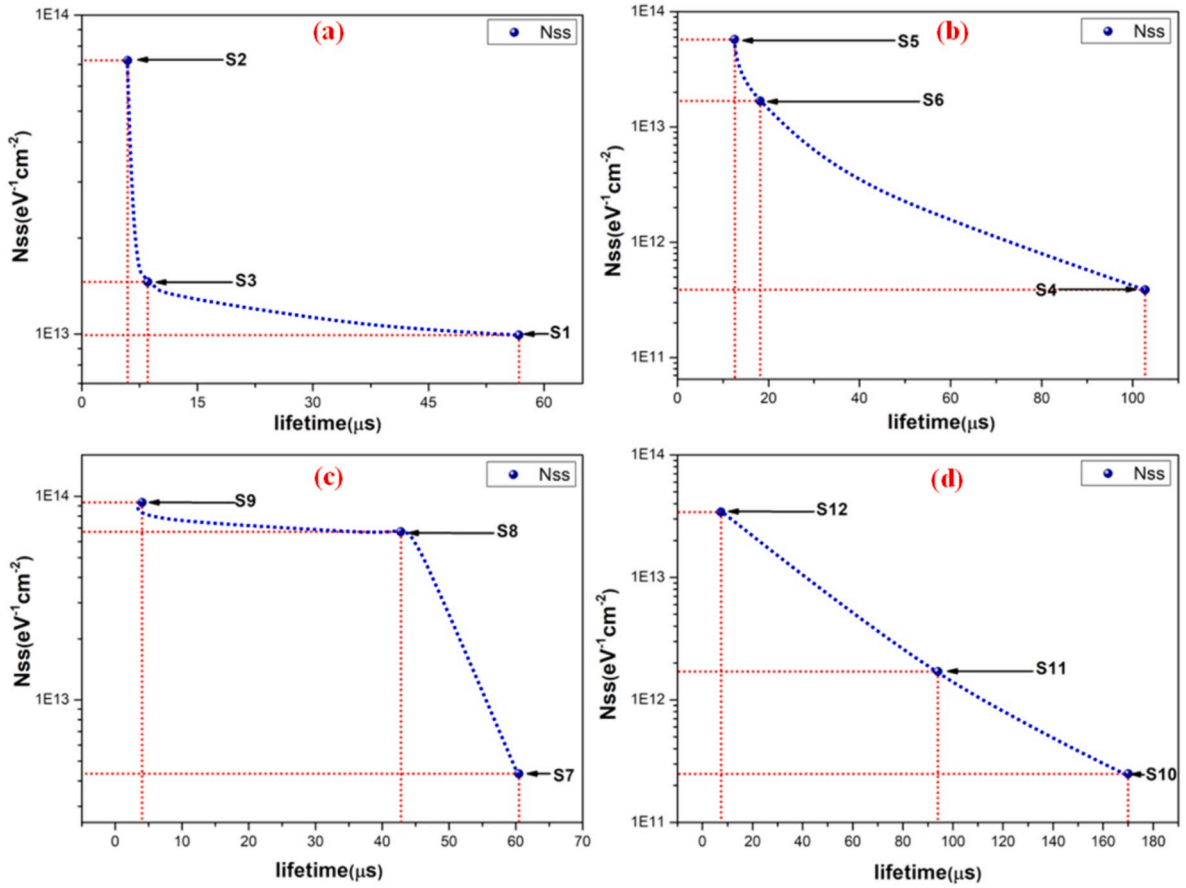

Fig. 7. **(a)** Interface trap state density vs. lifetime curve of sample S1, S2, and S3, **(b)** Interface trap state density vs. lifetime curve of sample S4, S5, and S6, **(c)** Interface trap state density vs. lifetime curve of sample S7, S8, and S9, **(d)** Interface trap state density vs. lifetime curve of sample S10, S11, and S12.

For p-type textured silicon wafer TO provide maximum passivation also. Due to the interface state density of the order 10^{13}, PO and CO gives very poor passivation for p-type wafers. For p-type polished silicon wafer, TO gives maximum barrier height (3.0530 eV) as compared to other oxides (TO > PO > CO). At the same time TO gives maximum minority carrier lifetime (102.74 μs) as compared to other oxides (TO > PO > CO) and minimum interface state density (4.1182×10^{11}) as compared to other oxides (TO < PO < CO). Overall for p-type polished silicon wafer TO offers good passivation as compared to PO and CO. For n-type textured silicon wafer PO gives maximum barrier height (0.2871 eV) as compared to other oxides (PO > TO > CO). At the same time TO gives maximum minority carrier lifetime (60.48 μs) as compared to other oxides (TO > CO > PO) and minimum interface state density (4.3359×10^{12} respectively) as compared to other oxides (TO < CO < PO). For n-type textured silicon wafer TO gives maximum passivation as compared to CO and PO (having interface state density of the order of 10^{13}). For n-type polished silicon wafer, maximum barrier height (1.3991 eV) was perceived in case of TO as compared to other oxides (TO > PO > CO). At the same time TO provides maximum minority carrier lifetime (170 μs) as compared to other oxides (TO > CO > PO) and minimum interface state density (2.4906×10^{11}) as compared to other oxides (TO < CO < PO). Overall for n-type polished silicon wafer, TO and CO offer better passivation as compared to PO. Reduction in interface state density (N_{ss}) reduces the probability of carrier recombination which in turns influences the implied V_{oc} to improve. It is evident from Fig. 6 that samples having higher carrier lifetime shows higher implied V_{oc}. Significant improvement in implied V_{oc} has been observed by using thermally grown oxide (TO) as passivating layer for both textured and polished wafers (p-type and n-type) as compared to other oxides. For n-type polished wafer, implied V_{oc} value for different oxides are as follows: TO (668 mV) > CO (647 mV) > PO (609 mV) and the value for n-type textured wafer are TO (643 mV) > CO (610 mV) > PO (547 mV). Same trend was also noticed for p-type polished: TO (649 mV) > PO (606 mV) > CO (591 mV) and p-type textured wafer: TO (639 mV) > CO (582 mV) > PO (565 mV).

It is noticed from Fig. 7 that the relationship between N_{ss} and lifetime is not linear. Lifetime (τ) is related to N_{ss} by the following equation,

$$\tau = \frac{d}{2S} = \frac{d}{2\sigma V_{th} N_{ss}} \tag{6}$$

Where S is the surface recombination velocity, d is the thickness of the sample, σ is the capture cross-section and V_{th} is the thermal velocity. A linear relationship will not hold if σ is not constant for the various interfaces. In fact there is evidence in the literature that σ can vary by as much as a factor of 10 for different silicon/insulator interfaces [30]. A recent study by Madoudj et al. [31] show only a nominal change in τ from 32 μs to 23 μs for KOH treated and NaOH treated silicon surface whereas N_{ss} changes by a factor of 40.

3.1. XPS study

In order to study the structural modification occurred at the (p-Si or n-Si)/SiO_x interface and quantitatively analyze the contribution of different bonding of O with Si during different oxidation process of PO, CO and TO, we have characterized the samples by means of X-ray photoelectron spectroscopy (XPS) measurements. Fig. 8 shows the full scan XPS spectra in the range of binding energy from 50 to 800 eV for (a) S6: PO on p-type wafer (Curve-1), (b) S12: PO on n-type wafer (Curve-2), (c) S5: CO on p-type wafer (Curve-3), (d) S11: CO on n-type wafer (Curve-4), (e) S4:TO on p-type wafer (Curve-5) and (f) S10: TO on n-type

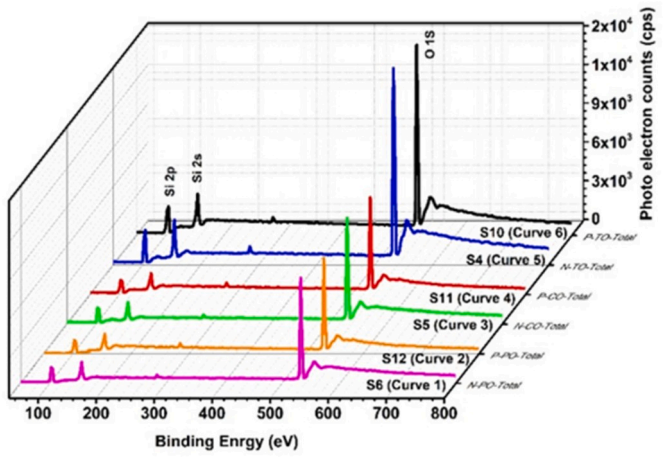

Fig. 8. XPS spectra of different samples in the range of binding energy between 50 eV and 800 eV. Curve-1: PO on p-type wafer (S6), Curve-2: PO on n-type wafer (S12), Curve-3: CO on p-type wafer (S5), Curve-4: CO on n-type wafer (S11), Curve-5: TO on p-type wafer (S4) and Curve-6: TO on n-type wafer (S10).

wafer (Curve-6) samples.

We have observed the clear signature of Si 2P, Si 2S and O 1S band for all the samples. For detail analysis of various oxidation states formed during TO, CO and PO we have deconvoluted the Si 2P band (98 to 107eV) into relevant peaks using Shirley background correction. The structure of the interface of silicon/silicon oxide consists mainly of three regions (1) the bulk Si (Si^0), (2) the near interface: contains few atomic layers of Si atoms in intermediate oxidation states i.e. $Si^{1+}(Si_2O)$, $Si^{2+}(SiO)$ and $Si^{3+}(Si_2O_3)$ and (3) a region extends into SiO_2 (Si^{4+}) overlayer [32]. The percentage contribution (X%) of the element X in different bonding configuration can be calculated from the following equation,

$$X\% = \frac{\frac{A_X}{S_X}}{\sum_{i=1}^{N}\frac{A_i}{S_i}} \tag{7}$$

where A_X and S_X are the area under the curve and the sensitivity factor for the element X respectively [33]. The sensitivity factor for Si and O is 0.37 and 0.72 respectively. The binding energies corresponding to bulk Si and different Si oxides with percentage contributions as calculated from equation (7) are listed in Table- 2.

Fig. 9 (a) and (b) shows the deconvolution of the Si 2P spectra for S4 and S10 samples respectively. Mainly three peaks corresponding to Si^0, Si^{3+} and Si^{4+} and four peaks related to Si^0, Si^{2+}, Si^{3+} and Si^{4+} appear in

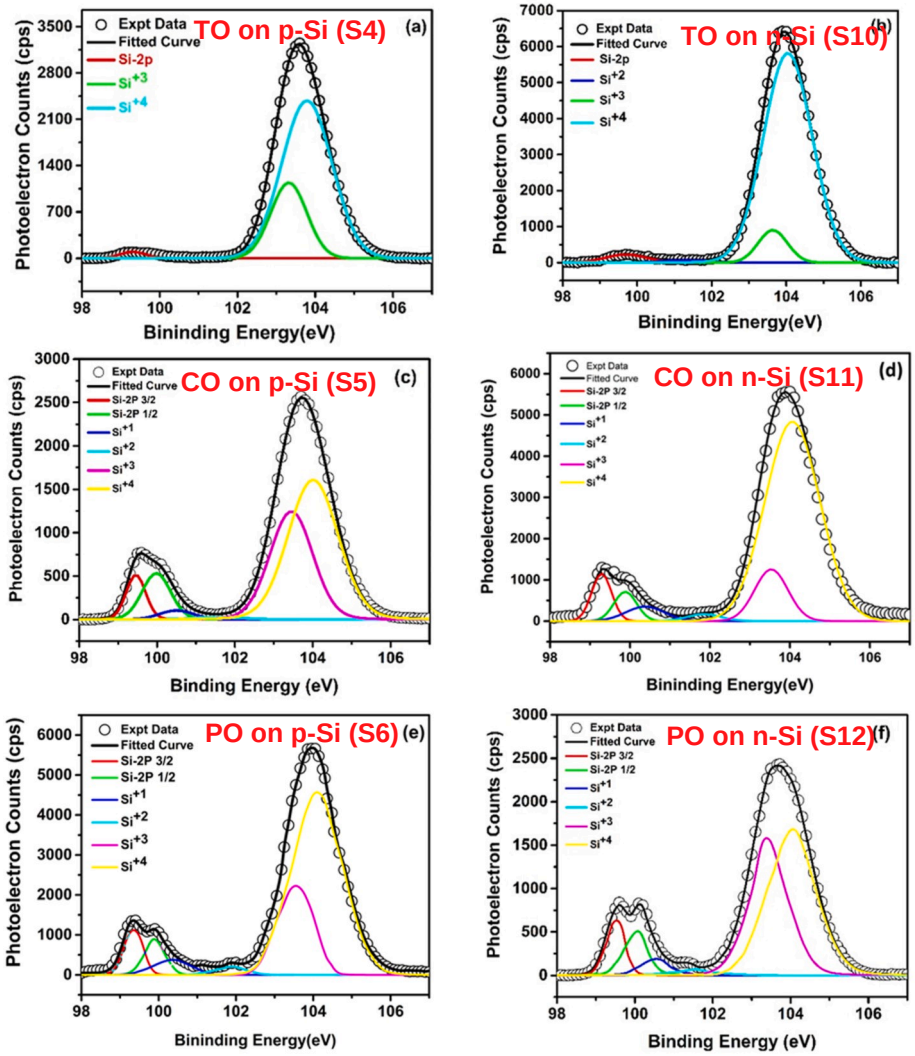

Fig. 9. XPS spectra of Si-2p band (98–107 eV) showing the deconvolution of various samples. (a) TO on p-type wafer (S4), (b) TO on n-type wafer (S10), (c) CO on p-type wafer (S5), (d) CO on n-type wafer (S11), (e) PO on p-type wafer (S6) and (f) PO on n-type wafer (S12).

Table 2
Comparative contribution for bulk Si and silicon oxide obtained from XPS analysis.

Type of wafer	Type of oxide	Si or SiO	Binding Energy	% Contribution
p-type	(S4) Thermal Oxide (TO)	Si^{0}	99.3	1.5
		Si^{3+}	103.3	25.2
		Si^{4+}	103.9	73.3
	(S5) Chemical Oxide (CO)	Si $2P^{3/2}$	99.4	6.1
		Si $2P^{1/2}$	99.9	9.3
		Si^{+1}	100.4	2.2
		Si^{+2}	101.5	0.8
		Si^{+3}	103.4	32.5
		Si^{+4}	104	49.1
	(S6) PECVD Oxide (PO)	Si $2P^{3/2}$	99.3	7.1
		Si $2P^{1/2}$	99.9	6.5
		Si^{+1}	100.3	4.6
		Si^{+2}	101.8	1.9
		Si^{+3}	103.5	24.8
		Si^{+4}	104	55.1
n-type	(S10) Thermal Oxide (TO)	Si^{0}	99.6	2.9
		Si^{2+}	101.3	0.9
		Si^{3+}	103.6	8.3
		Si^{4+}	104	87.9
	(S11) Chemical Oxide (CO)	Si $2P^{3/2}$	99.3	6.3
		Si $2P^{1/2}$	99.8	4.4
		Si^{+1}	100.3	3.7
		Si^{+2}	101.84	1.6
		Si^{+3}	103.5	11.4
		Si^{+4}	104	72.6
	(S12) PECVD Oxide (PO)	Si $2P^{3/2}$	99.5	7.8
		Si $2P^{1/2}$	99.8	10.1
		Si^{+1}	100.5	3.6
		Si^{+2}	101.5	2.1
		Si^{+3}	103.6	35.5
		Si^{+4}	104.1	40.9

case of p-type TO samples and n-type TO samples respectively. As seen from Table 2 that the contributions from bulk silicon Si^{0} was very small and takes a value of only 1.5% and 2.9% whereas the stable oxide (SiO_2) formation was large and contributed to 73.3% and 87.9% for S4 and S10 samples respectively. On the other hand, the percentage of sub oxide for S4 was 25.2% that of S10 samples was 9.2%.

Fig. 9 (c) and (d) represents the deconvolution of the Si 2P band for S5 and S11 samples respectively. It was observed from the deconvolution that two distinguishable peaks for bulk Si (Si $2P^{3/2}$ and Si $2P^{1/2}$) including all three sub oxides and stable oxides were contributing to the Si 2P spectra. The contributions from bulk Si for S5 and S11 samples were 15.4% and 10.7% respectively. The SiO_2 formation was greater for S11 samples (72.6%) compared to the S5 samples (49.1%). The total sub oxide (Si^{1+}+Si^{2+}+Si^{3+}) formed for S5 samples was 35.5% which is greater than that formed for S11 samples (15.7%).

The Si 2P spectra was deconvoluted into six peaks same as CO samples and shown in Fig. 9 (e) and (f) for the S6 and S12 samples respectively. It was observed from Table 2 the percentage contribution from bulk Si (Si 2P 3/2 and 1/2) for S6 and S12 samples are 13.6% and 17.9% respectively. The formation of the stable oxide i.e. $SiO_2$was greater for S6 (55.1%) compared to the S12 samples (49.1%). On the other hand, the total sub oxide (Si^{1+}+Si^{2+}+Si^{3+}) formed for S6 samples was 31.3% which is lower than that formed for S12 samples (41.2%).

It was observed from Si 2P band that in case of TO for both n-type and p-type Si the contribution from the bulk Si was minimum as compared to both the PO and CO. The main reason was that the self-limiting CO process as well as PECVD grown PO has lower oxide thickness as compared to TO. The higher value of the stable oxide and lower value of the sub-oxide gives rises to the better passivation for thermally grown oxide (TO) for both type of Si than that of CO and PO. Bert Stegemann et al. studied the correlation between the interface defect states with the sub-oxide formed during oxidation [34]. They showed that with the increase in the amount of sub-oxide the interface defect states increase. Due to the presence of larger amount of sub-oxide for S5 sample (p-type CO) give rise to increase in N_{ss} which in turn lower the passivation of S5 sample compared to that of S11 (n-type CO) samples. In case of PO the amount of sub-oxide for both S6 and S12 samples were comparably higher results in higher N_{ss} which degrades the passivation quality of the wafer.

4. Conclusion

Passivation of n-type and p-type monocrystalline Si wafers (both polished and textured) with different oxide layers prepared by chemical, thermal and PECVD methods has been studied by the measurement of minority carrier lifetime (τ) and density of interface states (N_{SS}). Results show that TO provides the highest lifetime and implied V_{oc} for both polished and textured p-type and n-type wafers due to generation of less number of defect states (N_{ss}) at the interface of the SiO_x/Si as compared to the other oxides. It is confirmed from the XPS results that formation of stable oxide i.e. SiO_2 is higher for TO in both p-type and n-type as compared to others oxides. It is also perceived that the amount of sub oxide formed at the interface of both n-type and p-type of wafers during different oxidation process have direct correlation with N_{ss} which in turn influences the passivation quality of the wafers.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Nabin Chandra Mandal: Investigation, Formal analysis. **Susmita Biswas:** Investigation, Formal analysis. **Shiladitya Acharya:** Investigation. **Tamalika Panda:** Validation. **Sourav Sadhukhan:** Validation. **Jayasree Roy Sharma:** Writing - review & editing. **Anupam Nandi:** Formal analysis. **Sukanta Bose:** Writing - original draft. **Arindam Kole:** Formal analysis, Writing - original draft. **Gourab Das:** Conceptualization, Investigation, Writing - review & editing. **Santanu Maity:** Visualization. **Partha Chaudhuri:** Supervision, Project administration. **Hiranmay Saha:** Supervision, Project administration.

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Appendix A. Supplementary data

Supplementary data related to this article can be found at https://doi.org/10.1016/j.mssp.2020.105163.

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