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Carrier selective, passivated contacts for high efficiency silicon solar cells based on transparent conducting oxides

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Abstract

We describe the design, fabrication and results of passivated contacts to n-type silicon utilizing thin SiO_2 and transparent conducting oxide layers. High temperature silicon dioxide is grown on both surfaces of an n-type wafer to a thickness <50 Å, followed by deposition of tin-doped indium oxide (ITO) and a patterned metal contacting layer. As deposited, the thin-film stack has a very high $J_{0,contact}$, and a non-ohmic, high contact resistance. However, after a forming gas anneal, the passivation quality and the contact resistivity improve significantly. The contacts are characterized by measuring the recombination parameter of the contact ($J_{0,contact}$) and the specific contact resistivity ($\rho_{contact}$) using a TLM pattern. The best ITO/SiO_2 passivated contact in this study has $J_{0,contact}$ = 92.5 fA/cm^2 and $\rho_{contact}$ = 11.5 mOhm-cm^2. These values are placed in context with other passivating contacts using an analysis that determines the ultimate efficiency and the optimal area fraction for contacts for a given set of ($J_{0,contact}$, $\rho_{contact}$) values. The ITO/SiO_2 contacts are found to have a higher $J_{0,contact}$, but a similar $\rho_{contact}$ compared to the best reported passivated contacts.

Keywords: Silicon solar cells, passivated contacts, SiO₂, ITO

1. Introduction

As bulk silicon PV wafer lifetimes progressively improve, the need for low recombination, passivated contacts to high efficiency solar cells increases. Contacts can be characterized by their ability to passivate the surface of the Si wafer through their recombination parameter ($J_{0,contact}$) and by their contact resistivity ($\rho_{contact}$). As other recombination pathways are reduced these two contact parameters can greatly influence the efficiency of the device and set the optimum contact area fraction coverage. One of the best examples of a passivated contact solar cell is the Si/a-Si/ITO heterojunction device which reached an impressive V_{oc} of 750 mV due to extremely low

recombination at the passivated contacts.[1] Recently Si/SiO$_2$/polycrystalline silicon (pc-Si) passivating contacts have also given excellent results.[2-4] Si/a-Si/ITO contacts have very low $J_{0,contact}$ ~5 fA/cm^2, but relatively high contact resistivity $\rho_{contact}$ ~0.3 ohm-cm^2 which may limit them to unity contact area fractions to avoid high series resistance. The Si/SiO$_2$/pc-Si contacts have very good $J_{0,contact}$ ~9 fA/cm^2 and low $\rho_{contact}$ ~10 mOhm-cm^2 allowing contact area fractions less than one. Some of the drawbacks of the Si/a-Si/ITO contacts are the parasitic optical absorption loss in the doped a-Si layers, a narrow processing window including temperatures < 250 ˚C, and the need for ultra-clean wafer surfaces before the deposition of the a-Si layer. This contact has proven to be difficult to reproduce between laboratories. The Si/SiO$_2$/pc-Si contact of Feldmann et al.[4] also has excellent passivation, but requires a high temperature anneal (~850 ˚C) for optimum performance. This paper explores the use of a thin silicon oxide layer and a transparent conducting oxide (TCO) contact layer to form a passivated contact to n-type silicon. The thin silicon oxide layer provides good chemical passivation, yet allows electrons in the silicon to tunnel to available energy states in the TCO. Figure 1a shows the band alignments, bandgaps and Fermi level positions for the Si/SiO$_2$/ITO contact discussed here. The diagram was constructed using measured carrier densities (from Hall effect) and a density-of-states effective mass value for degenerate ITO along with measured work function values.[5-7] Though the conduction band minimum levels do not align between the Si and ITO, the Fermi levels do align when the ITO is heavily degenerate. Figure 1b illustrates that transport of electrons between the Si and the ITO is favourable, but transport of holes is not, due to a large valence band offset. These band alignments should make the contacts selective to electrons due to the lack of available receiving states for minority carriers tunnelling across the thin silicon oxide. The advantages of these band-offset, carrier-selective contacts are three fold:

> 1) Band offsets provide majority carrier selectivity, without the use of heavy majority carrier doping in the silicon to reflect minority carriers. Lower doping in the silicon lowers Auger recombination at the contact.
> 2) Less optical absorption in the TCO layer due to a higher bandgap than polysilicon and a-Si if used on the sunny-side surface of the cell. An index of refraction of n~2 for most TCOs may also be beneficial for antireflective coatings and photon management within the Si cell.
> 3) Lower processing temperatures, compared with polysilicon,[4] but higher processing temperatures than a-Si contacts.[1] The former may help to preserve bulk wafer lifetime, while the latter may allow for more traditional ink-based contact processing and other passivated surfaces needing moderately high annealing steps (e.g. SiNx).

These advantages make TCO based, passivating contacts worth exploring for high efficiency solar cells. We will describe in this paper Si/SiO$_2$/ITO passivating contacts to both n and n+ wafer surfaces. We will then compare these contacts to the best reported Si/a-Si and Si/SiO$_2$/pc-Si contacts by using an analytical model to optimize device
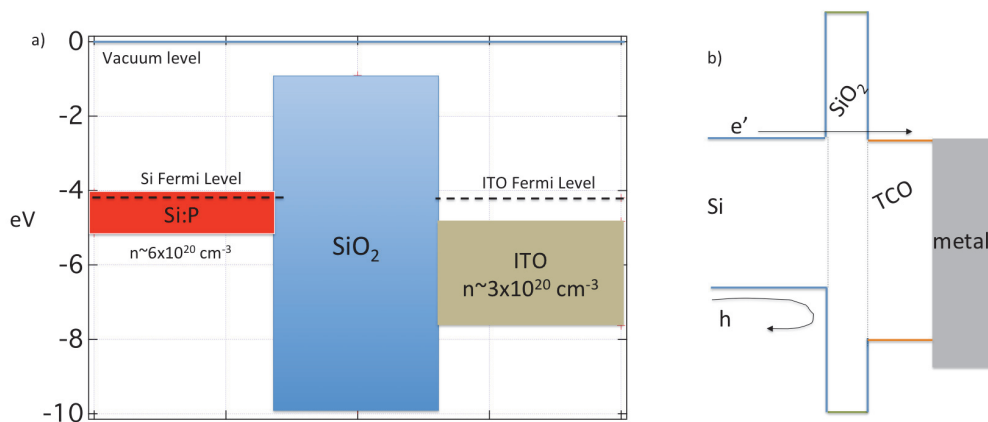

Fig. 1. a) Band alignment diagram for Si/SiO$_2$/ITO contact. b) Simplified band alignment diagram illustrating electron and hole transport at the Si/SiO$_2$/ITO interface.

efficiency and contact area fraction as a function of $J_{0,contact}$, $\rho_{contact}$.

2. Experiment

To test Si/SiO$_2$/ITO passivated contacts we grew thick SiO$_2$ layers on both n+ (P-diffused) and undiffused surfaces of n-type 1-10 ohm-cm CZ wafers. The SiO$_2$ layers were then thinned to below 50 Å using a 2% HF etchant solution. The thickness of the SiO$_2$ layers were monitored by ellipsometry between etch times. After each thickness measurement the wafers were also measured with a Sinton lifetime tester to extract the implied open circuit voltage (iV_{oc}) values. Fig. 2 shows how iV_{oc} varies as a function of SiO$_2$ thickness. Note that iV_{oc} does not start to be affected until the thickness of the SiO$_2$ is below about 30Å. This is approximately the same thickness where tunneling begins to be allowed across SiO$_2$. [8]
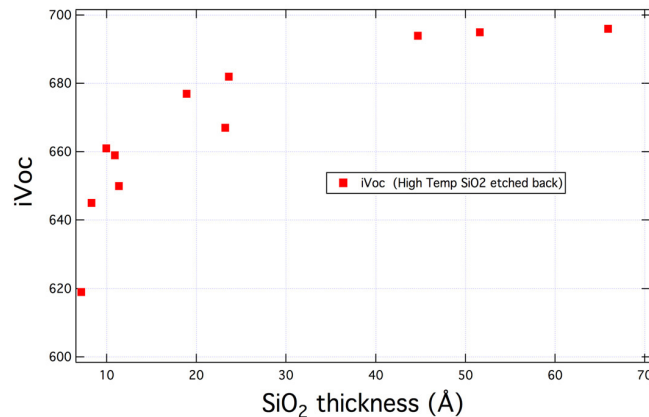

Fig. 2. iV_{oc} as a function of etched SiO$_2$ thickness.

Using the thinned oxide we next sputter deposited ITO layers (70-80 nm) on both sides of the wafer at a deposition temperature of approximately 200 ˚C. The sputtering conditions were 5 mT of Ar and O$_2$ using a 13.56 MHz RF source on a 10% Sn doped indium oxide target. A series of forming gas anneals were used to help improve the passivation quality. Sinton lifetime testing was done after each process step.

2.1. n+ surface passivation

n-type, 1-10 ohm-cm Cz, single-side polished wafers were ion implanted with P (10 keV, 3e14 cm^{-2} on the polished side) and then annealed to heal implant damage and form a 102 Å thick SiO$_2$ passivation layers on both sides. Following the implant anneal, the sheet resistance of the n+ layer was 116 Ohm/square. The emitter saturation current density, J_0, and iV_{oc} were measured on the wafers using a Sinton lifetime tester in the transient or generalized mode. Line 1 of Table 1 shows these values for a wafer following the post-implant anneal. Next, the rough surface of the wafer was protected with photoresist while the polished surface was exposed to a 2% HF etch to thin only the oxide on the smooth side to ~17Å. The protected rough surface maintained its as-deposited passivation level. The passivation quality of the contact decreases only slightly for this thin layer (lower iV_{oc} on line 2, Table 1). Next, the photoresist was removed from the rough side of the wafer and a 70 nm thick ITO layer was deposited by RF magnetron sputtering onto both sides of the wafer. This time, the passivation quality of the wafer was severely diminished (line 3, Table 1) most likely due to H effusion in the heated, vacuum sputtering environment or due to sputter damage of the SiO$_2$ layer. A metal (Ti/Pd/Ag/Pd) TLM pattern, deposited onto the ITO and isolated by etching down to the SiO$_2$ between the contacts, gave a contact resistivity value of 540 milliOhm-cm^2 and a non-ohmic IV curve. Next, the sample was annealed for 30 minutes at 400 ˚C in forming gas. Following this anneal the passivation quality of the contact increased significantly (lower J_0, higher iV_{oc}) and the

Table 1. Passivation parameters for an Si/SiO$_2$/ITO contact on an n+ surface.

Sample state	J_{oTotal} (fA/cm^2)	iV_{oc} (mV)	Contact resistivity (mOhm-cm^2)
1- Post implant anneal + SiO$_2$ (102 Å)	230	636	N/A
2- Thinned SiO$_2$ (17Å)	200	634	N/A
3- ITO (70 nm)	1700	555	Si/SiO2/ITO/Metal 537 (non-ohmic)
4- FGA (30 mins, 400C)	553	614	2.5 (ohmic)
5- FGA (50 mins, 400 c)	213	637	1.8 (ohmic)

contact became ohmic with a low contact resistivity of 2.5 milliOhms-cm^2 (line 4, Table 1). A second forming gas anneal at 400 ˚C for 50 mins continued to improve the passivation quality of the contact (line 5, Table 1) almost back to the original level of passivation (line 2, Table 1), and reduced the contact resistivity even lower. The contact is about five-times lower in $J_{0,total}$ than a direct metal-to-Si contact, and has an excellent $\rho_{contact}$ that is comparable to a metal/Si contact.[9] Temperature dependent IV data revealed that the contact is ohmic down to 125 K with an activation energy of the resistance equal to 17 meV. It is interesting to note that both the passivation quality and the transport across the SiO$_2$ improved significantly following the forming gas anneals. Experiments are on-going to understand the passivation and the electron transport mechanisms affected by the anneals and to reveal if the ITO/SiO$_2$/Si contact is truly hole blocking, as predicted.

2.2. n- surface passivation

In a second experiment a high lifetime (1-10 ohm-cm) single-side polished FZ wafer was used to grow a Si/SiO$_2$/ITO contact to an undoped n-type surface. A thick SiO$_2$ layer (900 Å) was grown on both sides of the wafer at high temperatures to achieve excellent passivation (Table 2, line 1). The SiO$_2$ layers were both systematically thinned with the 2% HF solution followed by Sinton lifetime tester measurements to record the passivation quality (Table 2, lines 2-4). Once the SiO$_2$ layer achieved a thickness of less than 50 Å an 80 nm ITO layer was sputtered

Table 2. Passivation parameters for a Si/SiO$_2$/ITO contact on an n- surface.

Process	SiO$_2$ thickness (Å)	$J_{o,contact}$ – one side (fA/cm^2)	iV_{oc} (mV)
1- As-grown	900	2.2	691
2- HF Etch 1	194	8.6	676
3- HF Etch 2	45.2	8.2	650
4- HF Etch 3	43.6	10.75	625
5- ITO as-grown	43.6	1865	504
6- FGA #1	43.6	55.5	633
7- FGA #2	43.6	92.5	635

deposited onto both sides of the wafer following the same deposition parameters described above. The passivation quality was severely decreased (Table 2, line 5) presumably for the same reasons as with the n+ surface. The passivation was improved by annealing the sample in forming gas for 45 mins at 450 ˚C (Table 2, line 6). Another forming gas anneal had little effect on the passivation quality (Table 2, line 7). The final passivation quality was characterized by a $J_{0,contact}$ of 92.5 fA/cm^2 with an iV_{oc} of 635 mV. For the n- surface the passivation quality ($J_{0,contact}$) was not fully restored after the ITO layer was deposited in contrast to the n+ surface. Next, a metal (Ti/Pd/Ag/Pd) patterned TLM contact was e-beamed deposited onto the polished-side ITO layer. The ITO was then etched away between the contacts down to the SiO$_2$ layer to provide electrical isolation between the contacts. The contact was found to be ohmic with a contact resistivity of 11.5 mOhms-cm^2. Overall, the ITO/SiO$_2$ contact to low doped n$^-$ c-Si surfaces showed excellent contact resistivity, but was about 10-20x higher in $J_{0,contact}$ compared with a-Si/Si or pc-Si/SiO$_2$ passivated contacts, but over an order of magnitude better than a metal/Si contact.[9]

3. Optimized contact area for passivated contacts.

As mentioned above, contacts can be characterized by their ability to passivate ($J_{0,contact}$) and conduct ($\rho_{contact}$). This pair of contact parameters greatly influence high efficiency devices and set an optimum contact area fraction coverage. For solar cells, J_{0_total} and r_{series_total}, along with an assumed J_{sc}, fully describe the cell output characteristics (ignoring R$_{shunt}$). The efficiency is given by

$$\eta = FF * J_{sc} * V_{oc} = FF(r_s, J_{sc}, J_o) * J_{sc} * kT * Ln\left(\frac{J_{sc}}{J_o}\right) \tag{1}$$

where the fill factor, FF, is a function of r_{s_total}, J_{0_total} and J_{sc} through the Lambert W-Function.[10] Fig. 3 describes the many regions of a solar cell that individually contribute to J_{0_total} and r_{s_total}. We define J_{0_total} by

$$J_{o\_total} = J_{o\_back\_contact} * Af_{back\_contact} + J_{o\_back\_surface}(1 - Af_{back\_contact}) + J_{o\_everything\_else} \tag{2}$$

where $J_{0\_everything\_else}$ includes contributions from the emitter, front contacts and the bulk and A_f is the contact area fraction. In a similar fashion r_{s_total} is defined by

$$r_{s\_total} = \frac{\rho_{back\_contact}}{Af_{back\_contact}} + r_{s\_everything\_else} \tag{3}$$

A_f = back contact area fraction
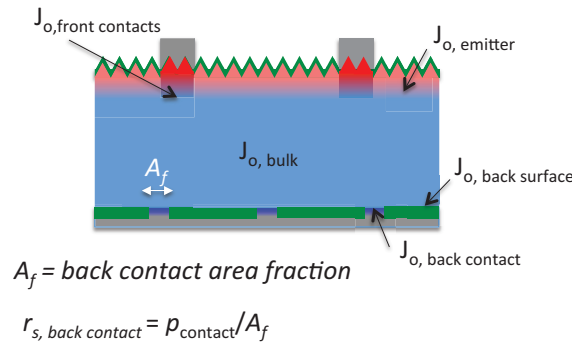
$r_{s,\ back\ contact} = \rho_{contact}/A_f$

Fig. 3. Cell diagram showing regions of recombination.

Substituting equations (2) and (3) into equation (1), the efficiency can be optimized as a function of $J_{0\_back\_contact}$ and $\rho_{\_back\_contact}$ with respect to the back contact area fraction. Figures 4 and 5 show iso-efficiency contours and optimum contact area contours as functions of $J_{0\_back\_contact}$ and $\rho_{\_back\_contact}$. $J_{0\_back\_surface} = 1$ fA/cm^2 which is a reasonably low value attainable by thermal SiO$_2$ passivation. For Fig. 4 the J_{sc}, $J_{0\_everything\_else}$ and $r_{\_everything\_else}$ were taken from the record HIT cell developed by Panasonic.[1] The Figures easily identify the necessary passivation and contact resistivity needed for a given efficiency along with an optimized contact area. Note that there is an upper limit to the contact resistivity that will give high efficiency devices (~0.6 ohm-cm^2). The blue diamond placed on Fig. 4 shows the $J_{0\_back\_contact}$ and the $\rho_{back\_contact}$ values of the Si/a-Si passivated contact for the
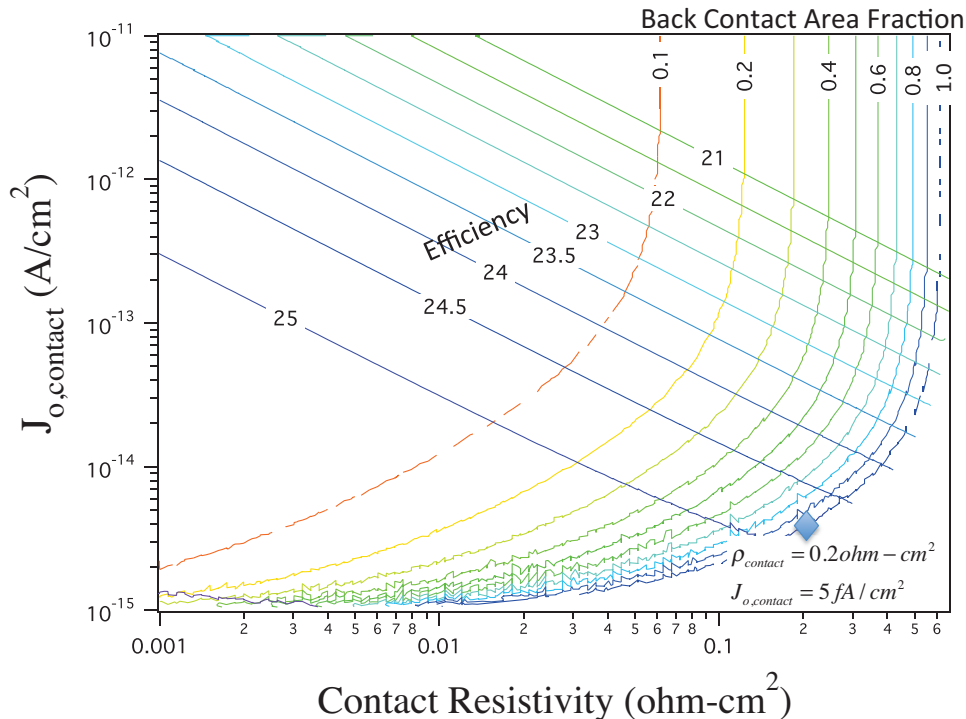

Fig. 4. Iso-efficiency and back contact area fractions as a function of J$_{0,contact}$ and back contact resistivity for a device similar to the Panasonic HIT device.

HIT cell. Note that the diagram correctly predicts the efficiency of the 24.7% device and the necessity of the full area contact due to the relatively high contact resistivity. The $\rho_{\_back\_contact}$ of 0.2 ohm-cm^2 would limit the use of this contact in a very efficient interdigitated back contact configuration due to a high series resistance for a contact area fraction less than one. Fig. 5 shows a similar diagram as Fig. 4 but calculated using the values of a recently published cell with a full area Si/SiO$_2$/pc-Si passivated contact.[4] The open red square in this diagram
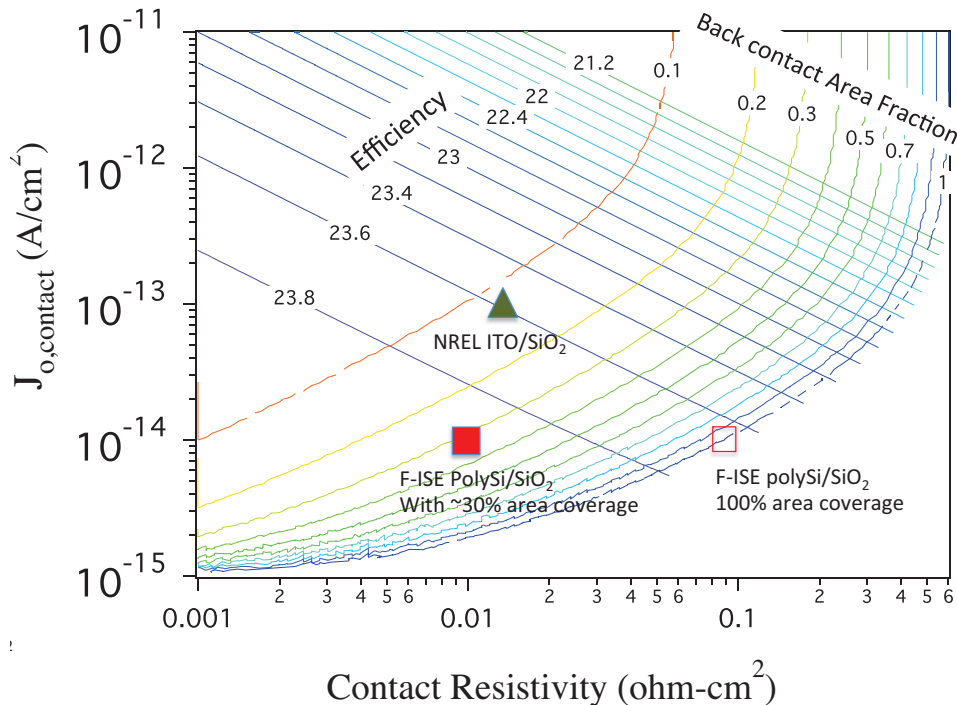
Fig. 5. Iso-efficiency and back contact area fraction contours as a function of $J_{0,contact}$ and back contact resistivity. The input parameters are similar to the device by Feldmann et al. The symbols are described in the text.

shows the placement of their full area contact on the diagram and correctly gives their excellent efficiency of 23.7%. Careful observation shows that this device could actually increase in efficiency by *decreasing* the back contact area coverage to about 30% (solid red square) and instead passivate the uncontacted back surface with a thick, high temperature oxide (assumed to give a $J_0 = 1$ fA/cm^2). This highlights one of the utilities of this diagram.

We can use Fig. 5 to compare our Si/SiO$_2$/ITO contacts with the Si/SiO$_2$/pc-Si contacts if processed on a similar device. The green triangle on Fig. 5 indicates our best Si/SiO$_2$/ITO contact and predicts an efficiency of 23.6%. Because the contact resistivity of the Si/SiO$_2$/ITO contact resistivity is about the same as the pc-Si/SiO$_2$ contact, but has a higher $J_{0,contact}$ value, the optimum contact area fraction coverage is about 10-15%. Practically speaking an optimized full area contact would likely be the simplest and most cost effective back contact for mass production.

4. Discussion

We developed a passivated contact to n-type silicon using a layer stack of Si/SiO$_2$/ITO/metal. The contact is an improvement over metal/Si contacts in terms of passivation, but lacks the single-digit fA/cm^2 quality of other passivated contacts to date. Though the contact parameters are not as good as the Si/SiO$_2$/pc-Si contacts, the Si/SiO$_2$/ITO contacts are still quite respectable, are better than metal/Si contacts and may be of benefit to some low-temperature device designs. Optically, there may be advantages to having a contacting layer with an index of refraction of about n~2 (ITO) compared with n~4 (pc-Si). However, if the contacts are in the back of the device, and the contacting layers are about 30 nm thick, there is little advantage to having ITO replace pc-Si due to the low absorption coefficient beyond 1000 nm in pc-Si. Optical models for the Si/SiO$_2$/ITO and Si/SiO$_2$/pc-Si contacts using Wafer Optics Calculator (PVlighthouse.com) reveal similar parasitic absorption for both contacts amounting to less than 0.1 mA/cm^2 in the rear contacting films. However, the high bandgap and higher transparency of ITO

make it a much better choice for a front contact where the n~2 also allows it to be an effective anti-reflective coating.

Much more experimentation is needed on the $Si/SiO_2/ITO$ contacts to better understand the nature of the passivation and the transport of carriers between the Si and ITO through the SiO_2 layer. Other TCOs like SnO:F or ZnO may offer benefits not afforded by ITO including more favorable band alignments and work functions, higher temperature processing, lower cost and gentler deposition techniques.

Finally, it is still an open question as to why the passivation quality decreases for SiO_2 layers less than 30 Å on a Si surface (Fig. 2). One reason may be that defect levels at the SiO_2/air interface begin to influence the recombination rate by allowing wavefunction overlap between states in the Si and defective states at the SiO_2/air interface. SiO_2 mainly provides chemical passivation to a Si surface, as opposed to field passivation via fixed charge. If thinning of the SiO_2 layer removes the fixed charge, there should still be decent chemical passivation to the Si/SiO_2 interface. The chemical passivation of the Si/SiO_2 interface should not be disturbed due to the thinning of the SiO_2. A complete understanding of the data in Fig. 3 must account for the fact that the surface passivation of thin SiO_2 can be nearly fully restored (to that of thick SiO_2) by placing a doped pc-Si (or a-Si) layer on top of the SiO_2 layer. This layer certainly provides some field passivation, but may also tie up dangling bonds at the SiO_2/pc-Si interface. Further study of this interface and the SiO_2/ITO interface is needed to guide further passivated contact developments.

Acknowledgements

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