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Analysis of Trap-Assisted Conduction Mechanisms through Silicon Dioxide Films Using Quantum Yield

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***Abstract*—In this paper we investigate the energy characteristics of the different trap-assisted conduction mechanisms through silicon dioxide films by means of QY measurements and simulations. Comparing experiments with simulations we show, for the first time, that tunneling assisted by native traps is elastic, while tunneling assisted by stress induced traps (SILC) is inelastic. A key new experiment was carried out on p^+ gate P-MOSFETs demonstrating that electrons tunneling through traps created by electrical stress lose energy irrespective of their initial band. It is then concluded that native and stress induced traps have different physical characteristics and that SILC electrons undergo an inelastic trap-assisted mechanism.**

I. Introduction

Thin silicon dioxide films exhibit many tunneling mechanisms [1], [2], which feature different energy characteristics. Recently it has been shown that the trap creation process depends on the secondary holes created by tunneling electrons [3]. It is then important to know the energy of tunneling electrons because the hole creation rate strongly depends on the electron energy in the anode. In addition, lately it was also shown that SILC electrons feature less energy than the ones tunneling directly. The reason of this reduced energy is still under debate. In this work, we investigate these two issues with the help of Quantum Yield (QY) experiments that allow us to infer the energy of tunneling electrons [4]–[7].

A schematic illustration of the QY experiment is briefly sketched in Fig.1. Applying a negative bias to the gate of a P-MOSFET, electrons are injected by tunneling into the silicon bulk (anode) with a large kinetic energy (E). These energetic electrons create new electron-hole pairs by impact ionization. The bulk electric field pushes the electrons toward the substrate contact while holes are collected by source and drain. The ratio of source-drain current (I_{SD}) to the gate current (I_G) is the quantum yield that strictly depends on E.

In the following, QY measurements will be compared to simulations. QY simulation involves two steps: first, simulation of the tunneling processes, and second, Monte Carlo (MC) simulation of the energy relaxation process

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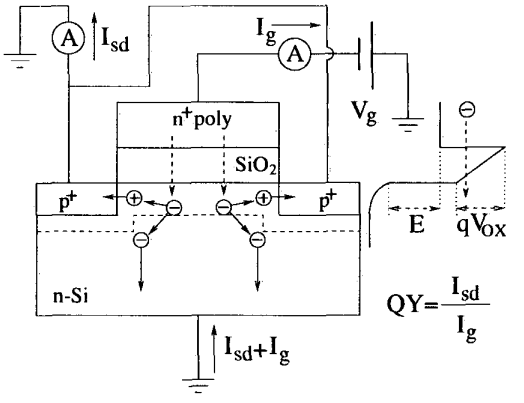

Fig. 1. Schematic illustration of quantum yield experiment. $E = qV_{OX}$ is approximately the mean injected electron energy.

and hole generation by impact ionization in the substrate. As for computation of the different components of the tunneling current, we used the quantum mechanical simulator QUASI [2], that has been validated in a large variety of cases and does not rely on device dependent parameters. As for MC simulations we have used the full band Monte Carlo program called FURBO [8]. It features the most relevant scattering mechanisms and the self-consistent solution of the Poisson equation. The total phonon and impact ionization scattering rates well agree with the most recent data used in the framework of MC simulation [9].

II. Virgin Devices

Fig.2 reports CV and IV data of two identical N-MOS capacitors used as reference devices. The two devices feature the same CV (Fig.2.a) and the same IV characteristics for high enough voltages, but different low voltage IV characteristics (Fig.2.b). The difference between their IV characteristics and the theoretical limit of direct tunneling (DT) in the low voltage part has been attributed to tunneling assisted by native traps (TAT), present in a different amount or distribution in the two devices [10].

Fig. 3 shows I_G before and after stress in one of the P-MOSFETs used for QY experiments together with simulations. Similar to Fig.2.b, before-stress I_G greatly differs from DT simulations in the low voltage regime (gate voltage $-4.5V < V_G < 0$). In addition, the after-stress I_G is larger than before-stress I_G (due to SILC), but fea-

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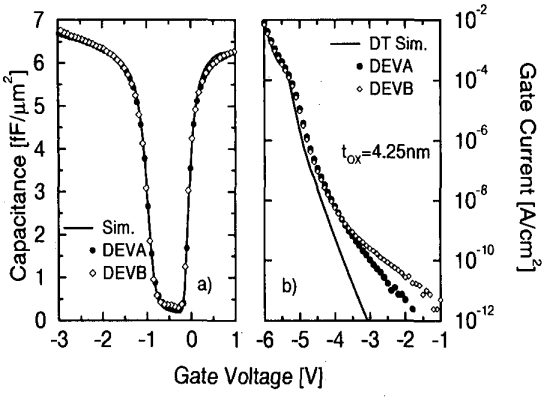

Fig. 2. CV (left) and IV (right) characteristics of two virgin N-MOS capacitors (labelled DEVA and DEVB) with the same $t_{ox} = 4.25nm$ but different low voltage IV characteristics. Solid line: DT simulations; symbols: measurements. The extra current with respect to the DT component is due to native traps.

tures the same slope as before stress in the low voltage regime. This suggests that, since SILC is attributed to trap assisted tunneling, the before-stress current is also due to trap assisted tunneling (native traps): in fact a direct component would feature a slope twice the one of the trap assisted component because of the double tunneling distance [10]. The experimental evidence in Figs. 2,3 indicates the presence of an additional TAT component even in this virgin device. As a matter of fact, by including a TAT component in the simulation, a very good agreement with experiments is obtained (Fig. 3). Lacking reliable data on the oxide trap distribution a simple distribution, constant in energy and space, was adopted. The trap density was used as fitting parameter.

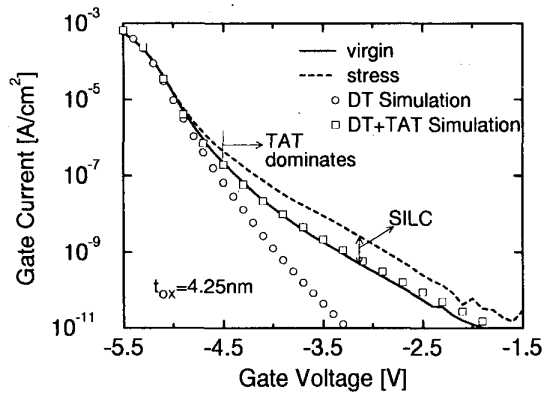

Fig. 3. I_G before and after stress in a P-MOSFET. Lines are the measurements. Symbols mark the simulations: only DT component (o), total simulation (DT+TAT) for the virgin device (□).

Fig.4 shows the typical behavior of I_G and I_{SD} during a QY experiment for the same device of Fig. 3. I_{SD} is detectable only at high enough voltages ($V_G < -3.5V$), when injected electrons have enough energy to create additional electron-hole pairs. The ratio of I_{SD} and I_G is the QY and is reported in Fig.5 together with the results of

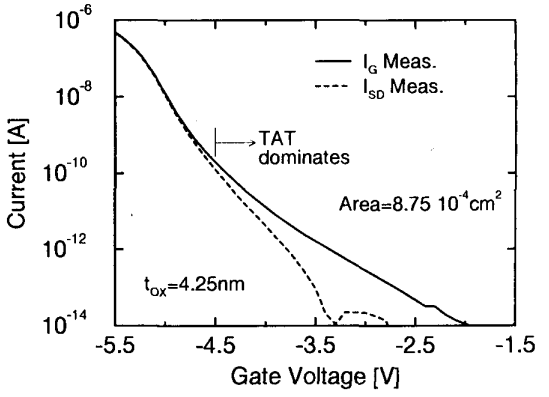

Fig. 4. Typical behavior of I_G and I_{SD} in a virgin device with $t_{ox} = 4.25nm$ during QY experiment.

QY simulations. Since the relationship QY(E) depends in a complex way on the device structure, the energy of injected electrons can be inferred only with numerical simulations [7]. Elastic QY simulations agree very well with the experiments showing that QY measurements in virgin devices featuring a native trap assisted component, are consistent with an elastic mechanism. On the other hand, simulations performed assuming an inelastic tunneling mechanism with an energy loss of $0.2eV$ clearly show a discrepancy between data and inelastic simulation, especially in the low voltage regime, where TAT dominates.

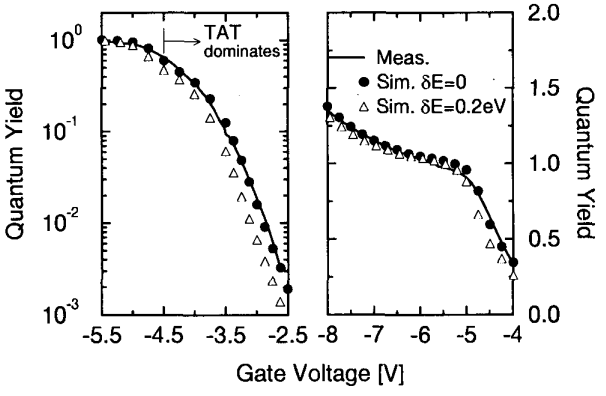

Fig. 5. QY data of a virgin devices in semilogarithmic (left) and linear (right) scales. Measurements (line); elastic ($\delta E = 0$) simulation (•); inelastic ($\delta E = 0.2eV$) simulation (△). The QY experimental data were collected on devices of the same type but different oxide thickness ($t_{ox} = 3, 4.25, 6.5nm$).

III. Stressed Devices

I_G and I_{SD} measured after stress during a QY experiment are reported in Fig.6. After-stress I_G is increased with respect to the virgin device and the difference is indeed SILC. On the contrary, after-stress I_{SD} changes shape and the dip featured at $V_G \approx -4.5V$ is due to a change of sign. Although I_G increases one order of magni-

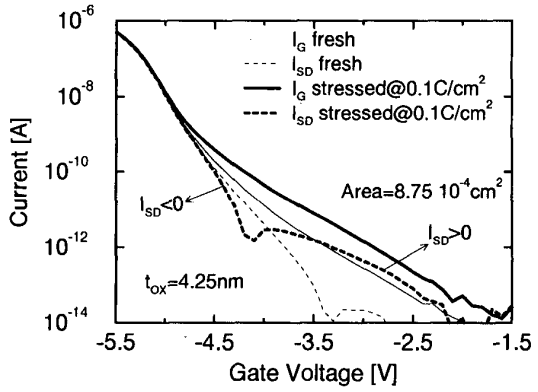

Fig. 6. I_G and I_{SD} measured before (thin lines, same data of Fig. 4) and after stress (thick lines) during QY experiment for the same device in Fig. 4.

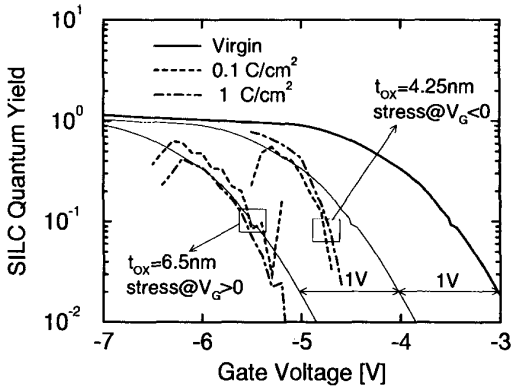

Fig. 8. QY measurements of the only SILC component for the same devices and stress conditions of Fig. 7. Thin solid lines are the virgin device QYs shifted by $2V$ and $1V$ respectively.

tude, I_{SD} stays almost the same for $V_G < -4.5V$, indicating that the additional electrons forming I_G have less efficiency in creating new electron-hole pairs. This is clearly shown in Fig.7. At high enough voltages (Fig.7.a) after-stress QY approaches before-stress QY because SILC is negligible respect to DT. On the contrary, when SILC is the dominant component (Fig.7.b), the QY clearly decreases after stress. Thus, it is concluded that the average energy of SILC electrons is smaller than the one of DT and TAT electrons.

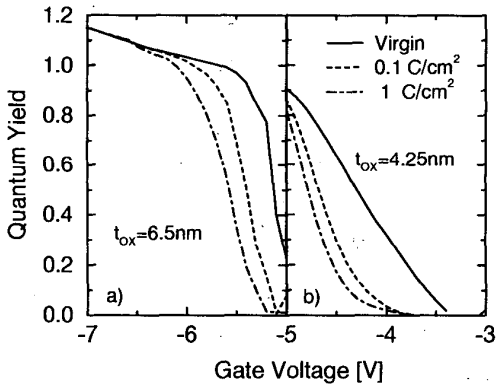

Fig. 7. QY measurements for stressed devices. Left: $t_{ox} = 6.5nm$, stress at $V_G > 0$; right: $t_{ox} = 4.25nm$, stress at $V_G < 0$.

with $t_{ox} = 6.5nm$ features an energy loss (represented by a shift of $QY(V_G)$ characteristics) of $\approx 2eV$, while SILC for the device with $t_{ox} = 4.25nm$ shows an energy loss of $\approx 1eV$. However, we must point out that the charge trapped into the oxide during stress changes the potential profile so that SILC QY extraction is difficult. In particular, SILC QY is overestimated in the case of a $V_G < 0$ stress, and underestimated when the stress is at $V_G > 0$. We can only conclude that the energy loss is between $1eV$ and $2eV$.

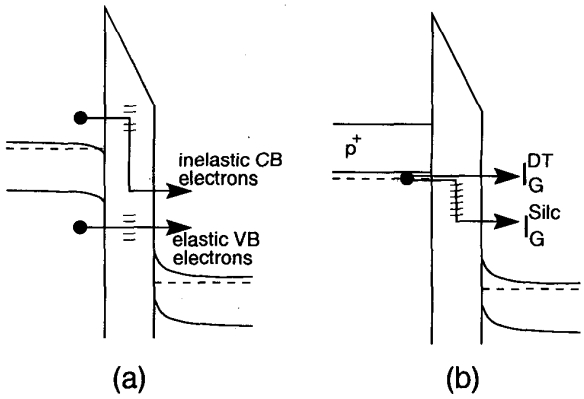

Fig. 9. Schematic band diagram during QY experiment in P-MOSFETs: a) possible SILC mechanisms; b) current components when the gate is p^+.

IV. SILC

Assuming that the current components not assisted by stress created traps stay the same in the virgin device as well in the stressed one, it is possible to compute the QY of the only SILC component as in [6]:

$$SILC\ QY = \frac{I_{SD}^{Stress} - I_{SD}^{Virgin}}{I_G^{Stress} - I_G^{Virgin}}.$$

SILC QYs extracted in this way from the data of Fig.7 are shown in Fig.8. It appears that SILC for the device

Performing QY in a p^+ gate P-MOSFET is possible to clarify the controversy about the SILC conduction mechanism: whether SILC is made of electrons coming from the cathode conduction band through inelastic tunneling [6], or SILC is made of electrons coming from the cathode valence band through elastic tunneling [11] (see Fig.9.a). In fact, when the cathode is p^+ and it is not inverted, tunneling electrons always come from the valence band (Fig.9.b), then the uncertainty about the source of SILC electrons is avoided.

Fig.10 shows the QY results on such kind of device. They are qualitatively similar to those in Figs. 7,8. After-

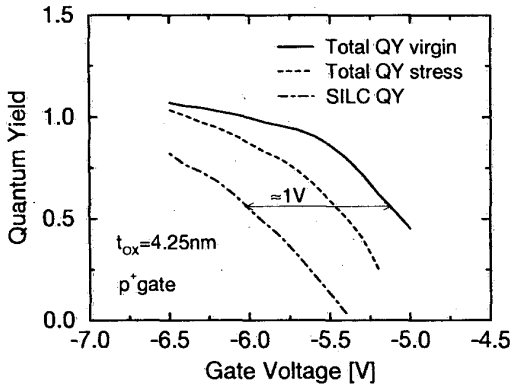

Fig. 10. QY measurements for a p^+ gate P-MOSFET device with $t_{ox} = 4.25nm$. The device was stressed at $V_G = 5.8V$ with $13.6C/cm^2$. SILC QY is shifted almost rigidly by $1V$ with respect to before-stress QY.

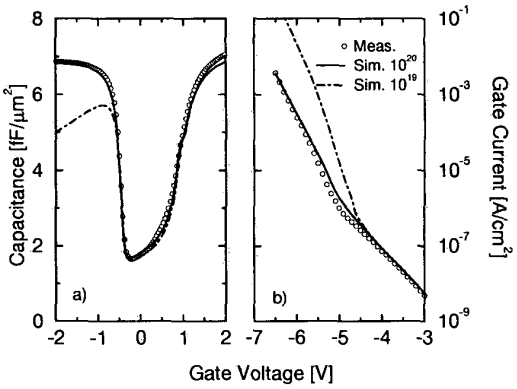

Fig. 11. CV (left) and IV (right) characteristics of the same p^+ device of Fig. 10. Experimental data: symbols; simulations: $N_{A_{poly}} = 10^{20}cm^{-3}$ solid line, $N_{A_{poly}} = 10^{19}cm^{-3}$ dashed line.

stress QY is clearly smaller than before-stress QY at low voltage, meaning that SILC electrons lose energy when tunneling through an electrically created trap even if they come from the valence band. It is then demonstrated that SILC traps are inelastic and therefore they are physically different from native traps.

Finally we verified that the p^+ gate of the devices under investigation is not inverted when QY is detected. Device simulation shows that, in order for the gate to be inverted at the bias voltages at which QY is detected, the poly doping should be less than $N_{A_{poly}} < 10^{19}cm^{-3}$. The signature of such low doping level should be very evident on both CV and IV characteristics. First, CV data would feature a very poor inversion capacitance because of large poly depletion effects. Instead, CV measurements do not show this feature, but rather are well fitted by $N_{A_{poly}} = 10^{20}cm^{-3}$ (Fig.11.a). Second, I_G would be much larger because conduction band electrons see a smaller energy barrier than valence band electrons (Fig. 12). Since even this second scenario is not present (Fig.11.b), we conclude that the device under test does not operate with an inverted gate.

V. Conclusions

In this paper we have analyzed the different trap-assisted tunneling mechanisms through silicon dioxide by means of QY measurements and simulations. We have shown that the tunneling current in excess of the DT component in vergin devices is due to native traps. With the help of simulations we showed that tunneling assisted by native traps is elastic. By performing QY experiments on p^+ gate P-MOSFET we demonstrated that SILC electrons undergo an inelastic trap-assisted mechanism. This evidence points out the different nature between native and stress created traps, and confirm the explanation of SILC as made of electrons coming from the cathode conduction band, in the case of n^+ gate, and suffering an energy loss.

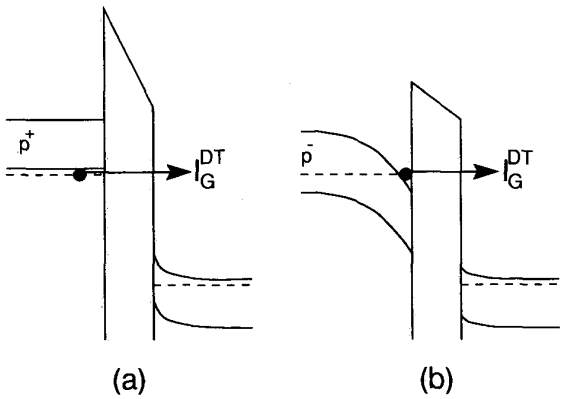

Fig. 12. Schematic band diagram during quantum yield experiment in a p gate P-MOSFET with: a) high gate doping; b) low gate doping (gate inverted).

Acknowledgements

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