Characteristic electronic defects at the Si-SiO_2 interface

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On unannealed, thermally oxidized silicon, electron spin resonance reveals an oriented interface defect which is termed the P_b center and identified as the trivalent silicon defect. Deep level transient spectroscopy (DLTS) reveals two broad characteristic peaks in the interface-state distribution: one ~ 0.3 eV above the silicon valence-band maximum and a second ~ 0.25 eV below the conduction band. Isochronal anneals of oxidized silicon, coated with aluminum, show that the spin density and the densities of the two DLTS peaks have the same annealing kinetics. On large-area, Al-gated capacitors the spin density can be modulated with an applied voltage; sweeping the silicon band gap at the interface through the Fermi level reveals that the spin density is approximately constant over the central region of the band gap but decreases near the band edges. The variation of the spin density with gate voltage identifies an amphoteric center with both electronic transitions in the band gap. Both the annealing behavior and the voltage dependence of the P_b center support the conclusion that these transitions correspond to the two characteristic peaks in the interface-state distribution. The ~ 0.6 eV separation of the peaks is the effective correlation energy of the dangling orbital on a trivalent silicon defect at the Si-SiO_2 interface. The similarity between the disordered interface and amorphous silicon is discussed.

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Thermal oxidation of single-crystal silicon produces characteristic electronic defects at the Si-SiO_2 interface. Electrical measurements on metal-oxide-silicon (MOS) devices reveal a continuous distribution of interface states that extends throughout the silicon band gap. For interfaces obtained by thermal oxidation without a subsequent anneal, a broad peak in the interface-state distribution centered ~ 0.3 eV above the silicon valence-band maximum (i.e., $E_v + 0.3$ eV) has been observed.[1-3] Electron spin resonance (ESR) reveals a paramagnetic defect, designated the P_b center, at the interface which has been identified as a trivalent silicon defect bonded to three silicon atoms with the nonbonding orbital aligned along the (111) directions.[4] A direct relationship between the above manifestations of interface defects has been proposed[1-3] based on theoretical studies of the density of states associated with the trivalent silicon defect.[5] Modulation of the P_b spin signal with an applied electric field was first demonstrated[6] by varying the gate voltage on an MOS capacitor during ESR measurements and subsequently confirmed[7] by using the corona charging method to vary the field. This letter presents a detailed comparison of new electrical and spin-resonance measurements of the P_b center and deep electronic levels at the interface. Results from ESR, capacitance-voltage (C-V) measurements, and deep level transient spectroscopy (DLTS) are shown to be consistent with an amphoteric model for the P_b center in which the characteristic interface states correspond to the electronic levels of the dangling orbital on a trivalent silicon defect.

Results from DLTS measurements of interface states across virtually the entire silicon band gap are shown in Fig. 1. Identically processed n-type and p-type MOS capacitors were used to determine the density of states in the upper and lower halves, respectively, of the band gap. The devices were fabricated on (111)-oriented epitaxial silicon. The oxide was grown in dry O_2 at 1000 °C to a thickness of 110 nm. Aluminum films were deposited from a flash-evaporation source to form gate electrodes and back (Ohmic) contacts, without introducing radiation damage into these unannealed test devices. The current-transient mode of measurement[8] was used to implement a high emission rate window ($e_0 = 1 \times 10^4$ s^{-1}) in order to detect emission from interface states near the band edges at temperatures down to 30 K. The analysis assumed constant capture cross sections for electrons (n type) and holes (p type) based on previous measurements on similarly prepared devices.[2,9] Near each band edge a peak is resolvable from the band tail of interface states; the dashed line segments indicate the region near midgap where the DLTS

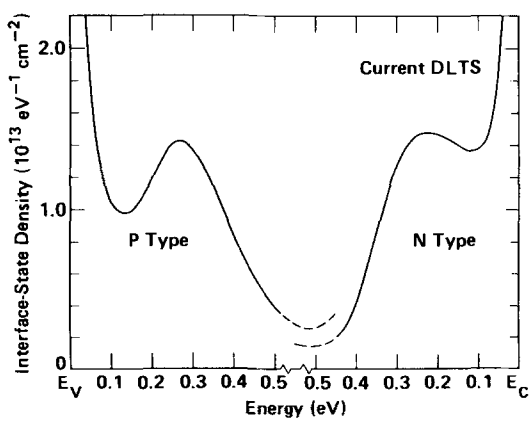

FIG. 1. Interface-state distribution measured by transient current spectroscopy on thermally oxidized, unannealed, (111)-oriented silicon. The distribution is a composite of measurements on identically processed n-type and p-type MOS capacitors. The energies E_v and E_c identify the silicon valence-band maximum and conduction-band minimum, respectively.

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majority-carrier analysis is generally inaccurate as discussed in Ref. 8. In the present study, no attempt was made to deconvolve the band tails from the peaks, hence, the band-tail distributions are only approximate since it is anticipated that their capture cross sections will differ from those of the peaks. These peaks, which are characteristic of thermally oxidized silicon, appear at approximately $E_v + 0.3$ eV and $E_c - 0.25$ eV and are of equal density within experimental uncertainty; their separation is ~ 0.6 eV. Both peaks were removed by annealing in forming gas at 450 °C (30 min).

Isochronal anneals were used to evaluate the relative annealing kinetics of the P_b spin center and the characteristic peak at $E_v + 0.3$ eV in the interface-state distribution. The samples consisted of epitaxial silicon on (111)-oriented silicon substrates, with semiconducting n-type epitaxial layers. For electrical measurements the substrates were degenerately doped for n^+ conductivity; for ESR undoped high-resistivity substrates were used to minimize loading of the microwave cavity. The different silicon wafers were simultaneously processed to fabricate MOS test structures. A thermal oxide was grown in dry O_2 at 1000 °C to a thickness of 110 nm, and an Al film, 300 nm thick, was vacuum evaporated onto the oxide layer. Isochronal anneals of 15-min duration were performed under vacuum. The specimens were annealed in pairs, with one sample for C-V measurements and the other for ESR. The density of the $E_v + 0.3$ eV peak was determined on the n-type capacitors by the quasi-static (i.e., high-low) C-V technique.[10] For spin-density measurements, the Al film was removed before ESR in order to minimize cavity loading.

In Fig. 2 the characteristic peak density and the P_b spin density, both normalized to their maximum (unannealed) values, are plotted together for the series of isochronal anneals. A maximum spin density of $\sim 1.5\times 10^{12}$ cm^{-2} was determined by numerically integrating the ESR signal from a stack of samples and comparing with a weak pitch standard.[3] The maximum density of interface states at the $E_v + 0.3$ eV peak was $\sim 1.6\times 10^{13}$ eV^{-1} cm^{-2}. These results reveal that the P_b center and the characteristic deep levels anneal identically. A check of the annealing behavior of the $E_v + 0.3$ eV peak on p-type MOS capacitors yielded similar results. In addition, the $E_c - 0.25$ eV peak anneals similarly to the lower peak and spin center, although this was more difficult to establish due to its close proximity to a large residual conduction-band tail. An essential factor in achieving a meaningful correlation between these two manifestations of interface defects is the identical chemical and thermal treatment which the different specimens received in preparation for the measurements. This is consistent with the generally held view that annealing with aluminum involves process-dependent residual water in the oxide and/or at the oxide-metal interface.[3] The simultaneous processing of the different wafers in the present study ensured that this factor had an identical influence on all of the specimens.

Large-area, Al-gated MOS capacitors were used to electric-field modulate the P_b spin density during ESR measurements. Czochralski-grown, p-type (30 Ω cm), (111)-oriented silicon wafers were oxidized in dry O_2 at 1000 °C. A high dose of boron was implanted into the back side of the wafers and activated during oxidation to provide a p^+ layer for Ohmic contact after metallization. Capacitors with an Al-gate area of 0.6 cm^2 displayed negligible leakage under strong accumulation and inversion biases, and the flatband voltage was approximately -12 V. For ESR measurements, the back metal and underlying p^+ layer were selectively etched to define a small bonding pad which minimally loaded the microwave cavity.

The dependence of the P_b spin signal on gate voltage is shown in Fig. 3. Each point is the relative peak-to-peak amplitude of the P_b (derivative) absorption spectrum which was recorded at a nonsaturating microwave power and averaged over ten or more scans. In addition, the relative amplitudes have been corrected for any small background signal by subtracting the signal from the same sample after a 300 °C anneal. The P_b spin signal decreases for either high negative or positive gate voltages which coincidentally correspond to strong accumulation and inversion, respectively, of the MOS capacitor. The signal is featureless within experimental error for gate voltages between the onset of strong accumulation and inversion, that is, for gate voltages roughly in the range from -20 to 0 V. This range corresponds to the Fermi level

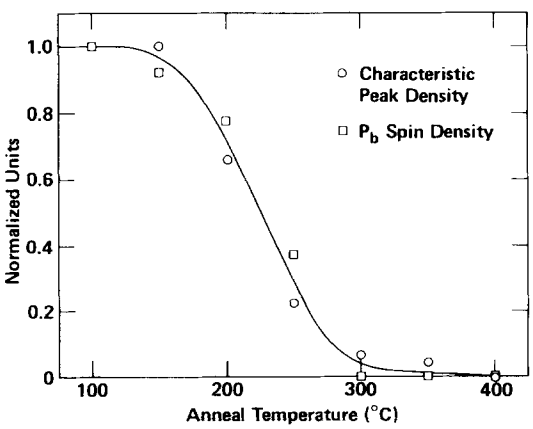

FIG. 2. Comparison of isochronal anneals of the P_b spin density and the density of the $E_v + 0.3$ eV peak in the interface-state distribution on (111)-oriented, n-type silicon. The specimens were coated with aluminum and annealed in vacuum for 15 min. The circles are the characteristic peak densities and the squares are the spin densities. Both densities are normalized to the maximum (unannealed) values.

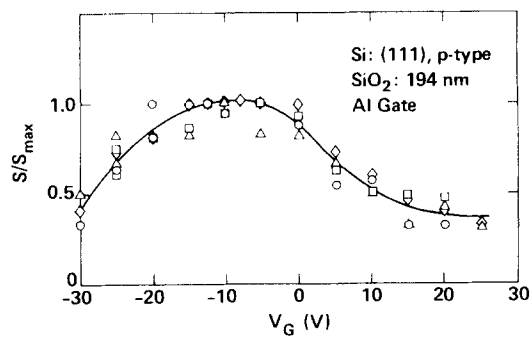

FIG. 3. Dependence on the P_b spin density, S, normalized to the maximum density S_{max}, on applied gate voltage V_G in a large-area MOS capacitor. The data are a compilation of measurements from four identically prepared capacitors, and each datum is the peak-to-peak amplitude of the P_b (derivative) absorption spectrum averaged over ten or more scans and corrected for any background signal.

intersecting the interface over the central region of the silicon band gap. For a given gate voltage this intersection occurs over a distribution of energies due to surface potential fluctuations,[10] the standard deviation of which is largest in depletion and estimated to be $\leqslant 0.14$ eV. The dependence of the ESR signal on V_G nearly mirrors the electric-field-induced free-carrier concentration at the interface, so rapid relaxation of interface states by free carriers can (and does) occur which could cause an apparent loss of signal through line broadening. However, voltage invariance of the line shape and saturation measurements of the spin-lattice relaxation time demonstrated that the relaxation rates were too low. The reduction in signal amplitude is thus due to a change in defect occupancy induced by the change in surface potential.

The declines of the spin density at each end of the voltage range identify an amphoteric defect center. At high negative voltages, the Fermi level intersects the interface near the silicon valence-band maximum, and the center is diamagnetic; in the intermediate voltage range, the center contains an unpaired electron and yields an ESR signal; for positive gate voltages, the Fermi level approaches the conduction band, and the center acquires a second electron which pairs with the first to again produce a diamagnetic site. Similar results have been obtained on n-type MOS capacitors, where it was also determined that the maximum spin density on a metallized capacitor is the same as that measured with the electrodes removed; that is, in the absence of an applied voltage, the Fermi level is pinned by the defect states.

The electronic properties of the P_b spin center, which has been identified as a trivalent silicon defect,[4,11] are also consistent with an amphoteric defect model. The results in Fig. 3 demonstrate that both electronic transitions of the center are in the silicon band gap. Correlating the P_b center with the characteristic DLTS peaks (Figs. 1 and 2) supports the assignments of the 0⟶1 electron (i.e., 2⟶1 hole) transition of the amphoteric center to the $E_v + 0.3$ eV peak and the 1⟶2 electron transition to the $E_c - 0.25$ eV peak.[12] The singly occupied center is charge neutral.

There are striking similarities between the Si-SiO_2 interface and hydrogenated amorphous silicon a-Si:H. The density of gap states in a-Si:H is composed of band tails of localized states (strained bonds) and a single dominant electrically active defect, the trivalent silicon atom, which has two levels in the mobility gap.[11,13,14] These levels correspond to single and double electron occupancy of the dangling orbital, with the occupancy varying with Fermi energy as described above. The levels are separated by an effective correlation energy of ~ 0.4 eV,[14,15] which is the difference between the energies required to add an electron to a singly occupied orbital and to an unoccupied site; it is the sum of two terms, a Coulombic repulsion and a compensating lattice relaxation energy. In comparison, the ~ 0.6 eV separation of the transition levels of the P_b center corresponds to the effective correlation energy of the trivalent silicon defect at the Si-SiO_2 interface.[16] It is suggested that the larger correlation energy for a Si dangling orbital at the Si-SiO_2 interface, as compared to that in a-Si:H, primarily reflects the reduced dielectric screening of the Coulombic repulsion between paired electrons which is due to the protrusion of the orbital into a half-space of SiO_2. A further contribution to this increase may come from the smaller lattice relaxation permitted by crystalline back bonds as compared to that determined by the matrix of lower average coordination in a-Si:H. In summary, the interfacial deep levels characteristic of thermally oxidized silicon correspond to the electronic transitions of the trivalent silicon defect at the Si-SiO_2 interface.

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[12] The existence of amphoteric defects can alter the analysis of DLTS (as well as C-V) measurements of interface states from that based on uncoupled levels. However, due to the large effective correlation energy of the P_b center and the close proximity of each transition level to a band edge, the DLTS signal is dominated by only a single transition (i.e., the $E_v + 0.3$ eV peak in p-type MOS capacitors and the $E_c - 0.25$ eV peak in n-type devices) so that the analysis of Ref. 8, which assumes uncoupled levels, is an accurate approximation and produces a self-consistent interface-state distribution (Fig. 1). For further discussion see N. M. Johnson, Final Report, U. S. Army contract No. DAAK20-81-C-0406, 1983.
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[16] The P_b spin density was found to be unchanged (within $\pm 5\%$) in the investigated temperature range of 30–300 K. This fact, coupled with the pinning of the Fermi energy between the two defect levels (in the absence of an applied voltage), imples a *lower bound* for the effective correlation energy of $\geqslant 50$ meV.