

The Si-SiO₂ interface: Correlation of atomic structure and electrical properties

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The roughness at the Si-SiO₂ interface has been determined quantitatively on an atomic scale by SPA-LEED (spot profile analysis of low energy electron diffraction) in ultrahigh vacuum after removal of the oxide. At the Si-SiO₂ interface the steps are randomly distributed. With the help of model calculations the measured spot broadening provides the step atom density and therefore the roughness on an atomic scale. The roughness will be decreased by low oxidation rates (thick oxides, dry atmosphere) and appropriate annealing in N₂ and will be increased by high oxidation rates (thin oxides and wet atmosphere). Furthermore metal oxide semiconductor (MOS) structures were built on chips which were also suited for LEED measurements. Hall mobilities for Si(111) *p*-channel inversion layers MOS-FETs with varying roughness at the Si-SiO₂ interface have been measured at temperatures between 4.2 K and room temperature. It was found that there exists a strong correlation between Hall mobility and atomic roughness at high inversion, nearly a proportionality. Even at room temperature the transistors with the lower interface roughness exhibit the higher mobility. Further quasistatic capacitance-voltage (*C-V*) measurements have been performed on Si(111) MOS structures with different but well-known atomic roughness. The results demonstrate a strong correlation between atomic roughness and interface state density too, even after an additional postmetallization-annealing (PMA) treatment. A simple model which is associated with each kind of step atom, i.e., edge or kink atoms, suggests the creation of a dangling bond and therefore, a surface state can explain the result. Assuming that ionized atoms which are responsible for Q_{fix} are located preferentially at those steps or kinks which are also correlated to the dangling bonds at the interface, we confirm the general opinion that Q_{fix} and surface states have at least one common physical origin: the atomic roughness.

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I. INTRODUCTION

The invention of the metal-oxide-semiconductor (MOS) devices in 1960 revolutionized semiconductor technology. Due to excellent properties like impedance, easy processibility (planar technology), and good aptitude for miniaturization, this device succeeded in the following years. But soon it was quite obvious that the most important properties, like mobility and threshold voltage and in general the quality of metal-oxide-semiconductor (MOS) devices, depended, among other parameters, strongly on the quality of the interface between silicon and silicon dioxide. Whereas the chemical composition (like migration of alkali ions) and electrical properties (interface states, interface charge, mobility, scattering of electrons, and holes at the interface) have been studied for a long time, the structural properties had been neglected due to a lack of appropriate measuring techniques. The state of the art is documented in the proceedings of several topical conferences¹⁻⁵ and review papers.^{6,7}

Only recently several new techniques have been applied. Depth profiling by ion bombardment and monitoring of the varying chemical composition of the surface during removal of the oxide provides some information on a "transition lay-

er," which has been interpreted as roughness at the interface.^{8,9} It is not clear if part of the measured transition layer is produced by ion bombardment.

Transmission electron microscopy of cross sections of Si-SiO₂ structures with very high resolutions shows directly the profile of the interface, revealing even monatomic steps.^{10,11} Due to averaging over the thickness of the cross section (about 10 nm) and the high effort to obtain the micrographs, a quantitative interpretation and a systematic investigation are still difficult.

Normal transmission electron microscopy of Si-SiO₂ structures after chemical dissolution of the silicon reveals undulations at the interface.¹² Especially a dependence of the interface roughness on the final oxidation rate is pointed out.

No systematic investigation is available showing the effect of both temperature and ambient, pretreatment, and post-treatment on interface roughness.

A novel technique studying the interface uses spot-profile analysis of low energy electron diffraction (SPA-LEED).^{13-18,54} If the surface of a single crystal shows different levels due to atomic steps, the diffracted electron beam is modified by interference of the electrons diffracted at adja-

cent terraces. By varying the energy and therefore also the wavelength of the electrons, this interference changes periodically between constructive and destructive interference. Therefore, the spot shape changes between sharp and broadened profiles. From the period of interference the step height is derived with high precision; from the spot shape the distribution of terraces with respect to orientation, width, and regularity is obtained.¹³⁻¹⁵ With the help of model calculations¹⁵ the spot profile gives us therefore, a direct and quantitative measure of the step density.

We obtain the step atom density representing the number of step atoms per unit surface area. This method has been applied here to study the interface of Si and SiO₂. After removal of the oxide the roughness is seen directly due to the broadening of the diffraction spots. Whereas a former paper showed the feasibility of the method,¹⁷ the present paper, in the first part, gives systematic results for variation of several oxidation parameters.

This knowledge enabled us to build MOS structures with different roughness. Furthermore, with SPA-LEED we were able to measure the amount of roughness at the Si-SiO₂ interface. Hall mobilities of Si(111) *p*-channel inversion layers have been measured at temperatures between 4.2 K and room temperature. The second part of the paper emphasizes the influence of the roughness on mobility, comparing both parameters experimentally. Up to now the roughness scattering was only theoretically calculated^{48,55,89,90} and used to explain results.^{48,91} Finally, for similar transistors quasistatic capacitance-voltage (*C-V*) measurements have been performed before and after a postmetallization annealing (PMA) in forming gas. Therefore, the third part of the paper exhibits the correlation of the roughness to interface state density N_{ST} and fixed oxide charge (Q_{fix}). The main result is that the atomic roughness plays a rather important role in controlling the properties of the Si-SiO₂ interface. The paper first reviews systematic experimental data on the influence of atomic roughness on mobility, interface state density, and interface state charge comparing with data from literature.

II. EXPERIMENTAL

A. Roughness determination

Silicon(111) and Si(100) samples have been oxidized at atmospheric pressure. After removal of the oxide, the measurements were done in an ultrahigh vacuum (UHV) system. An extensive description of the procedure is given in Ref. 21, some details are explained here.

1. Removal of oxide and sample transfer to UHV system

The experiments were performed in a conventional stainless steel UHV system equipped with a commercial four-grid LEED system. A base pressure of about 1×10^{-7} Pa was sufficient to avoid degradation of the LEED pattern during a measuring cycle.

To study the interface in UHV, it is necessary to remove the oxide without damage to the substrate and without contamination, since already a monolayer of disordered contamination degrades the pattern.

For that purpose the oxidized sample was etched in HF

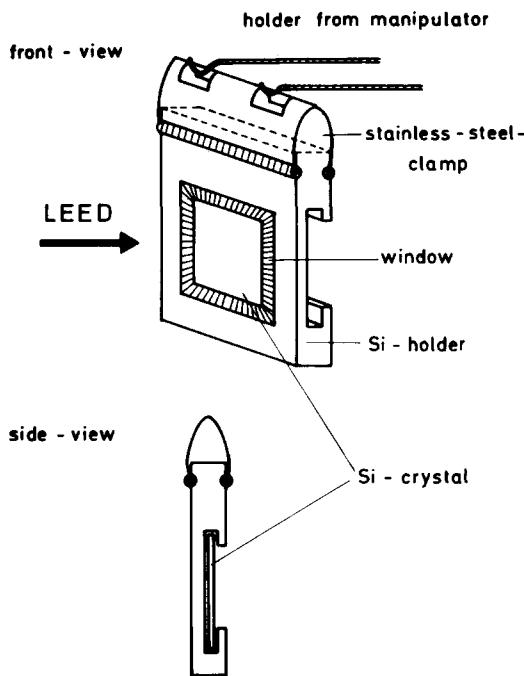


FIG. 1. Front and side view of the pure silicon frame including the sample.

after mounting into a silicon frame (Fig. 1). By thinning out in methanol, the silicon was protected by methanol during transfer to the UHV system via a magnetically operated lock. The drop of methanol evaporates only during pumpdown in the transfer system, so that the sample surface has never been exposed to atmospheric pressure. A bright LEED pattern at a pressure of less than 10^{-6} Pa is obtained in 30 min after etching in HF including sample transfer and pumpdown.

2. On-line-LEED spot profiling

The LEED spots at the phosphoric screen have been profiled with a closed TV video system. In this way the intensity profile on the screen could be recorded and evaluated directly on line on a computer. Finally, the computer directly calculated the step-atom density (for details see Refs. 17, 21, and 22).

B. Mobility and roughness measurements at suited transistors

Four kinds of MOS transistors were built with different atomic roughness at the Si-SiO₂ interface. The atomic roughness was measured on different portions of the same chips [Fig. 2(a)], since the gate area is too small for LEED studies the transistors with Hall probes were fabricated on *n*-type of silicon using three masks [Fig. 2(b)]. The samples were oxidized along four different procedures as shown in Table I (Ref. 21). All four gate oxides had a thickness of about 1200 Å. The final annealing (5 min in nitrogen at 540 °C) was the only heat treatment after gate oxidation. After mounting and bonding, the transistors showed the usual *I-V* characteristics.

Now the transistors were mounted in a cryostat permitting measurements in a temperature range from 1.5–300 K.

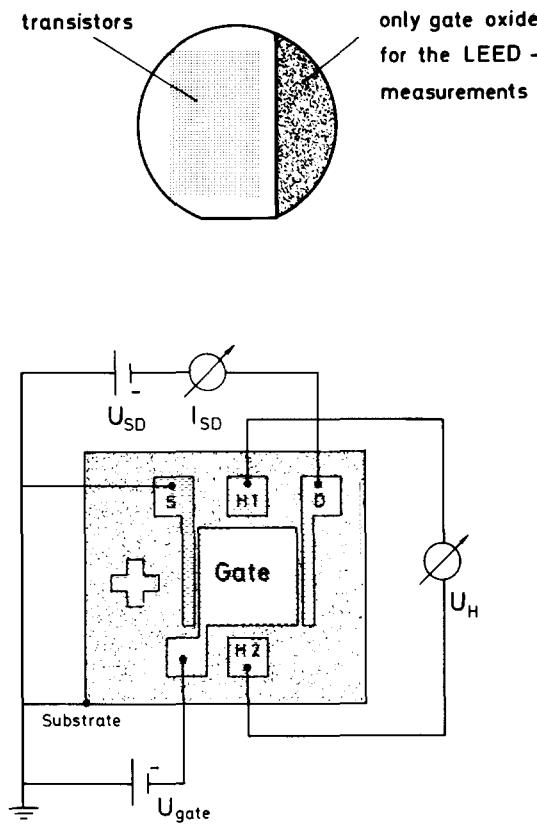


FIG. 2. (a) Silicon chip showing schematically the transistors for the electrical measurements (Q_{fix} , N_{ST} , μ_H) and the reference oxide for the roughness measurements (SPA-LEED). (b) MOS transistor and circuit for Hall effect and conductivity measurements (S: Source; D: Drain; H₁, H₂: Hall contacts).

A detailed description is given in Refs. 24 and 25. The magnetic field could reach a maximum magnetic field strength of 0.6 T in both directions. The mobility measurements were performed on a homogeneous channel realized by a low drain-source voltage V_{DS} of 0.5 eV above threshold.

From each chip several transistors have been used for measurements, yielding identical results.

C. Capacitance-voltage ($C-V$) measurements

Samples from the same chip as discussed and described in the previous subsection were used for the $C-V$ measurement. The source, drain, and Hall contacts were floating [Fig. 2(b)]. The values of the interface state density (N_{ST}) were determined by the quasistatic technique²⁷⁻²⁹ and measured by a computerized $C-V$ -analysis system. Simultaneously, the 1 MHz $C-V$ curves were measured. The ramp voltage was swept from -20 to 20 V automatically. First the samples were measured directly after gate oxidation and metallization without any further heat treatment. A second measurement was performed with the identical samples after a post-metallization annealing (PMA) in forming gas (10% H₂, 90% N₂ at 400 °C for 20 min).

Surface state density (N_{ST}) was obtained by comparing the measured quasistatic $C-V$ curve and the theoretical curve. The thickness of the oxide was obtained from capacitance measurements at 1 MHz for strong accumulation. The gate area was $7.3 \times 10^{-4} \text{ cm}^2$. Finally, we calculated the fixed oxide charge Q_{fix} from the data obtained (for details see Ref. 30).

III. INFLUENCE OF THE PROCEDURE ON THE ROUGHNESS DATA

Since the interface Si-SiO₂ can be studied by LEED only after removal of the oxide, it is necessary to check if the surface studied after removal of the oxide is relevant for the interface; that is the case if the procedure does not change the roughness as seen with the LEED pattern. For that purpose a series of test experiments has been performed (see Ref. 21).

A. Cleanliness of samples after removal of oxide

Auger electron spectroscopy has been applied to several samples, treated as for the LEED experiments. They did not indicate any traces of contamination besides oxygen and carbon. According to calibration^{31,32} the coverage of carbon and oxygen was less than 0.3 of a monolayer. This residual amount of contamination can just produce some background in the LEED pattern; it, however, cannot influence

TABLE I. Schematic summary of all results showing the correlation of electrical properties to the step atom density and oxidation parameters.

| Transistor | Oxidation at 1000 °C | Annealing in dry N ₂ at 1000 °C | Step atom density (%) | Mobility ($\frac{\text{cm}^2}{\text{vs}}$) at high inversion ($9 \times 10^{12} \text{ cm}^2$) and 4.2 K (Ref. 33) | As grown | | After PMA | |
|------------|-------------------------|--|--------------------------|--|---------------------------------------|--|---------------------------------------|----------------------|
| | | | | N_{ST} ($\frac{\text{cm}^{-2}}{\text{eV}}$) | Q_{fix} (cm^{-2}) | N_{ST} ($\frac{\text{cm}^{-2}}{\text{eV}}$) | Q_{fix} (cm^{-2}) | |
| R 1 | Dry oxygen 2 3/4 h | no | 17 ± 5 | 120 | 9×10^{11} | 11.4×10^{11} | 4.4×10^{11} | 5.6×10^{11} |
| R 2 | Same as R 1 | 4 h | 8 ± 1 | 280 | 2×10^{11} | 3×10^{11} | 0.4×10^{11} | 1×10^{11} |
| R 3 | Wet oxygen 9 min | no | 21.2 ± 2 | 230 | 3.8×10^{11} | 6.9×10^{11} | 2.4×10^{11} | 4.6×10^{11} |
| R 4 | Same as R 3 | 4 h | 10 ± 2 | 330 | 2.2×10^{11} | 4.3×10^{11} | 1.7×10^{11} | 3×10^{11} |

the oscillation of the half-width of the spots due to the random distribution of an amount of less than a monolayer.

B. Influence of multiple etching and of storage in air

A sample of high step density (16%) has been repeatedly measured by taking it out of the system, treating it in HF and bringing it back to UHV. Even multiple etching did not decrease step density. A step free sample (heating in UHV to at least 1000 °C) showed after bringing out and again in after etching, only a small step density (4%), which is most likely due to the oxidation during transfer in original from UHV to the HF solution.²¹ These experiments support the conclusion that the procedure does not alter the roughness at the interface appreciably and the surface under investigation is the wanted interface with respect to roughness.

IV. RESULTS

A. How the oxidation parameters determine the atomic roughness

1. Oxidation at 800 and 1000 °C

Two Si(111) samples had been oxidized repeatedly in a quartz tube at atmospheric pressure in dry oxygen at 800 °C. The roughness had been measured as described. Prior to the subsequent oxidation they had been annealed in UHV at 1000 °C to the 7×7 superstructure (step free surface). Figure 3 shows the step atom density for many different oxide thicknesses (upper curve). The crosses are the results from one sample, the circles for the other samples. The main result is that for low oxide thickness (< 20 nm) the edge atom density is appreciably higher (27%) than for higher thickness (only 15%). Obviously a change in the oxidation process occurs at about 20 nm. Wet oxidation results in an appreciably higher roughness (samples W1 and W2).

Oxidation in dry oxygen at 1000 °C shows a somewhat lower step atom density (triangles in Fig. 3). One sample W3, oxidized in wet oxygen, again shows a considerably higher roughness.

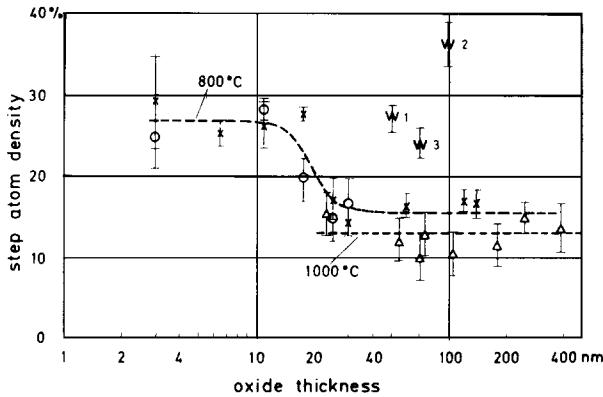


FIG. 3. Step atom density vs oxide thickness. Dotted curve: two samples (circles and crosses) repeatedly heated to the step-free surface (7×7 structure) were then oxidized at 800 °C, in dry atmosphere, samples W1 and W2 in wet atmosphere. Traced curve: oxidation temperatures now 1000 °C, sample W3 oxidized in wet oxygen again.

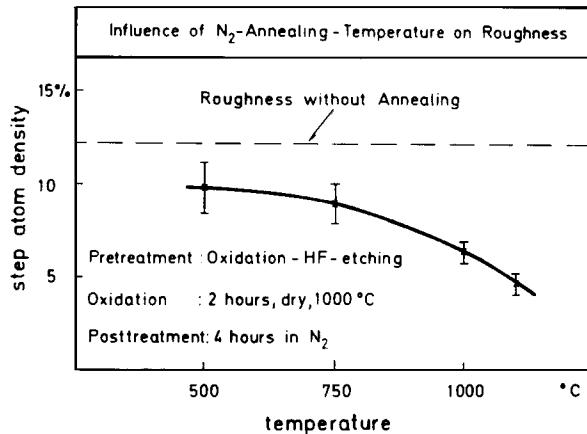


FIG. 4. Step atom density vs N₂ annealing temperature.

2. Pretreatment and posttreatment

The influence of pretreatment has been checked by simultaneous oxidation of several samples. Whereas long storage in air or chemical etching in CP6 yielded a high roughness, both annealing to a step free surface in UHV or oxidizing to a thick layer and removing it with HF immediately before oxidation provided low step atom density. A further reduction is possible with annealing in nonoxidizing atmosphere provided low step atom density (Fig. 4).²¹

B. Correlation of atomic roughness with mobility

The oxidation parameters and the measured step atom density (average and mean deviation from many measurements on the same chip) are shown in Table I for four different chips R 1 to R 4.

Figure 5 shows the Hall mobility of the transistors R 1-R 4 at 4.2 K. Whereas different transistors on the same chip showed identical results (different symbols in Fig. 5), a variation in oxidation parameters, as described in Table I, has a drastic effect on electronic properties at high inversion. The difference between R 1 and R 2 is especially noticeable, since

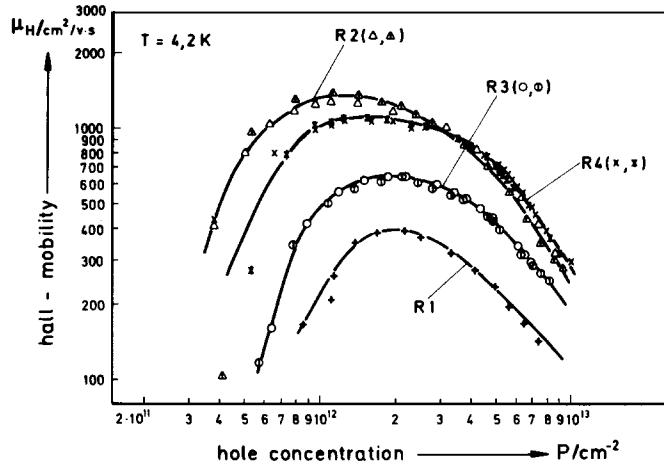


FIG. 5. Hall mobility vs hole concentration (derived from Hall coefficient, not from induced charge) at T = 4 K for the four different chips. The different symbols along a single curve correspond to different transistors from the same chip.

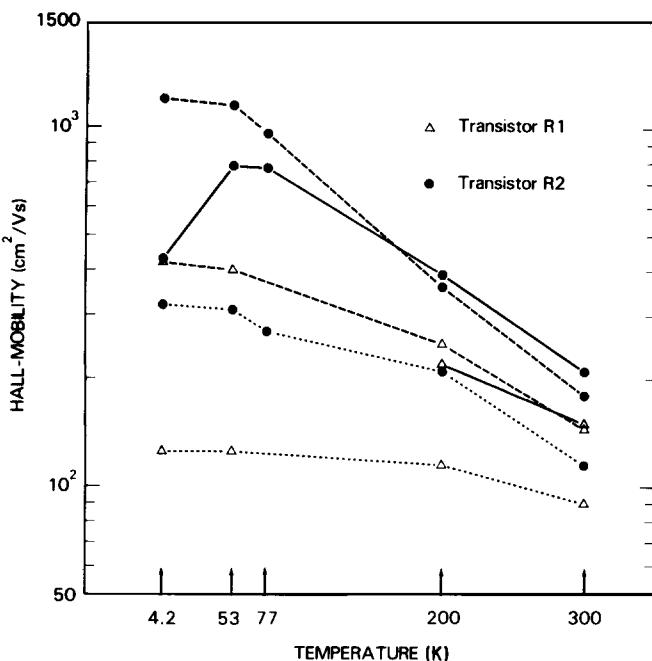


FIG. 6. Temperature dependence of Hall mobility for low inversion ($4 \times 10^{11} \text{ cm}^{-2}$, solid line), for maximum mobility ($2 \times 10^{12} \text{ cm}^{-2}$, dashed line), and for high inversion ($9 \times 10^{12} \text{ cm}^{-2}$, dotted line) for the transistors R 1 ($\Delta\Delta\Delta$) and R 2 ($\circ\circ\circ$).

only the post-treatment after oxidation makes all the difference.

Another surprise was the observation that the mobility of R 1 is in the whole range smaller than that of R 2, indicating a correlation of the different scattering processes. The temperature dependence of the mobility of R 1 and R 2 is shown in Fig. 6 for small inversion ($4 \times 10^{-11} \text{ cm}^{-2}$), maximum mobility ($2 \times 10^{-12} \text{ cm}^{-2}$), and high inversion ($9 \times 10^{-12} \text{ cm}^{-2}$). Whereas drastic differences are seen at low inversion and low temperature, the differences are smaller with increasing carrier concentration and temperature.

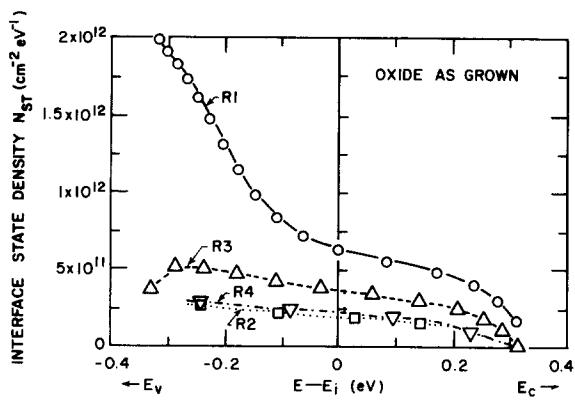


FIG. 7. Interface state density (N_{ST}) energy distribution for the transistors R 1(17%), R 2(8%), R 3(21.2%), and R 4(10%). Value in brackets is the step atom density (Si-edge atoms per unit surface area). R 1 and R 2 as well as R 3 and R 4 were processed in one experimental run.

C. Correlation of atomic roughness with interface state density, fixed oxide charge

The interface state density for all of the four MOS structures is shown in Fig. 7. Out of R 1 and R 2, which were oxidized simultaneously, R 1 shows in the whole gap a remarkably higher interface state density than R 2. The same relation holds for R 3 and R 4. The PMA treatment in all cases reduces the density of states. The average density of states was determined and added in Table I with and without PMA treatment. The fixed charge Q_{fix} , which has been calculated from flat band voltage as usual (see Ref. 30) is also shown in Table I.

V. DISCUSSION

A. Correlation of oxidation parameters with atomic roughness

1. A model explaining the final atomic roughness

The results demonstrate that the interface shows an appreciable number of edge atoms. The average terrace width is derived to about 6–40 atomic distances. The roughness strongly depends on the oxidation parameters.

A model including a roughening and a smoothing factor can explain the results, which are summarized in Table II. The random process of diffusion and reaction of oxygen at the interface is the roughening effect, which should pile up more and more roughness with growing oxide thickness (approximately square root of thickness). On the other hand, in thermal equilibrium a smooth, step-free surface is energetically favored similar to the free surface of silicon, where annealing in UHV produces a step-free surface. Therefore, diffusion of oxygen and/or silicon smoothes the interface depending on temperature, ambient, and duration of heat treatment. The balance between roughening and smoothing determines the final roughness. Therefore, high oxidation rate (at low thicknesses or with wet oxygen) increases roughness whereas high temperature and low oxidation rate (at high oxide thickness or in nonoxidizing ambient) lowers the roughness. The remarkable step in Fig. 4 may be related to growth kinetics. At low thickness ($d < 20 \text{ nm}$) the thickness increases linearly with time, at higher thickness with the square root in accordance with literature,^{34–36} where it is explained as reaction controlled and diffusion controlled, respectively. For the diffusion-controlled process (oxidation limited by diffusion of oxygen across oxide), obviously the smoothing effect by diffusion along the interface is more effective.

The dependence on pretreatment shows the influence of chemical differences. Contamination (e.g., metal or carbon) should alter the electronic properties, as studied in detail at the free clean surface,^{37,38} and therefore, the chemical reactivity leading to different step-atom densities. As shown by Auger electron spectroscopy, the contamination is high after storage, still high after chemical etching, and negligible after heat treatment in UHV. Obviously oxidation also yields substantial cleaning.

First experiments with the (100) surface show, on the one hand, the existence of mono- and double steps; on the other

TABLE II. Schematic summary of all results showing the dependence of roughness on the oxidation parameters.

Summary of the results

| Variation of the oxidation parameters → step atom density / % | | | |
|--|---|---|--------------------------------|
| Oxidation temperature | Atmosphere | Oxide thickness | |
| 800 °C | dry | $d < 20 \text{ nm}$ $d > 20 \text{ nm}$ $d > 20 \text{ nm}$ | high 27% low 15% low 13% |
| 1000 °C | Wet | $d > 20 \text{ nm}$ | Highest 35% |
| | Post-treatment: annealing in N ₂ at various temperatures | | |
| 1100 °C ↓ 500 °C | dry | 100 nm | lowest 3% ↓ low 7% |
| Pretreatment | | | |
| 1. Long storage in air 2. Chemically etched in CP 6 3. Oxidation-HF etching 4. Annealing in UHV to 7×7 structure | dry | 100 nm | high 27% low 12% |
| (B) (100) surface | | | |
| 1. Oxide thickness: 100 nm; without N ₂ annealing 2. Twice oxidized: 100 nm; annealed in N ₂ at 1000 °C | | | high > 16% low ~ 6% |

hand, this surface has in general the same dependence on the oxidation parameters.

2. Comparison with other techniques

A wide variety of methods and techniques has been developed to study both the structural and the chemical and the electronic properties of the interface.^{1–7} Those methods, like the Rutherford scattering,³⁹ AES depth profiling,^{8,9} SIMS depth profiling,⁴⁰ XPS,^{41–43} UPS,⁴⁵ low-energy ion scattering,⁴⁶ contact angle of a liquid,⁴⁷ TEM,^{10–12} and electronic mobility in the space-charge layer^{48–50} indicate the presence of a transition layer, the thickness of which is estimated to 0.3–5 nm, depending on the method.

Since the measured quantity is directly or indirectly the average chemical composition of the surface during growth or during removal of the oxide, the interpretation is given either by gradual change of composition or by roughness at the interface. Our results are strictly structural information. Therefore, a comparison is only sensible with experiments on structural properties.

Johannessen *et al.*⁸ found during ion milling a transition layer of 3–5 nm, which they interpreted as due to roughness at the interface. Helms *et al.*⁹ found, with an improved Auger depth profiling, that the transition region is independent of oxide thickness (25–100 nm) and increases only slightly with growth temperatures (800–1150 °C). The present results (Fig. 4) agree completely with respect to dependence on oxide thickness whereas a small decrease of roughness has been found for increased oxidation temperature (800–1000 °C). For very thin oxide layers, Wager and Wilmsen⁵¹ found an increase of the transition width. The author had to subtract from the measured width several contributions to the width by the ion beam, which are only rough estimates

although carefully studied. Theoretical⁵² and experimental⁵³ investigations show that the ion beam should produce a transition layer of the order of the reported transition layer depending on energy and mass of the ions and on the substrate. Random fluctuations may produce further roughness.

A LEED study of ion-bombarded germanium surface yields an appreciably higher roughness than the present results.¹⁸ It is therefore evident that the low roughness at the interface as seen by LEED is not observable after removal of the oxide by ion bombardment, since the roughness of the interface is totally obscured by the much higher roughness as produced by ion bombardment. Recently, direct observation was possible with transmission electron microscopy of cross sections through the interface.^{10,11} The interface was found to be flat down to 1 nm, monatomic steps were visible in distances of 2–4 nm, corresponding to 6–12 atomic distances at the surface or an edge atom density of 15%–30%. These results are compatible with our results. Finally, oxide layers were investigated with normal transmission electron microscopy after removal of the silicon with preferential etching. Besides silicon clusters in the oxide (which are not observable in our technique), a “gray network” has been found, which is interpreted as undulations of the interface with an asperity height of about one atomic step and a wavelength of about 4 nm, corresponding to an average terrace width of 2 nm or an edge-atom density of about 30%. Additionally, a critical final oxidation rate of 1 nm/min for the presence of silicon clusters and of interface roughness has been found. This is in qualitative agreement with the present result, where a decrease of roughness for high oxide thickness or after annealing in nonoxidizing atmosphere was found (see Figs. 5 and 6). The present results, however, indicate that not just the final oxidation rate, rather the equilibrium between

oxidations and lateral diffusion and other factors such as pretreatment and oxidation kinetics, also have to be considered.

B. Atomic roughness and electrical properties

1. Mobility

The results confirm the strong influence of the oxidation parameters on electronic properties of MOS-FETs even for identical oxide thicknesses.

For low carrier concentration all samples show, at $T = 4.2$ K, an increase in mobility with concentration. Fixed charges in the oxide and at the interface are screened by mobile carriers. This increase in mobility is approximately described by a power law $\mu \sim N_{\text{INV}}^{1.5}$ in agreement with measurements of Cheng^{48,55} and Yagi and Kawaji.⁵⁶⁻⁵⁸

The second important scattering process is roughness scattering at the interface due to atomic steps and other structural imperfections. Since the inversion layer becomes thinner and thinner with increasing density, a decrease of mobility is reasonable. The decrease can be approximately described by N_{INV}^n with $n = -1.3$ in agreement with calculations of $n = -0.5$ up to $n = -2.0$.^{48,55} Besides these common features of all curves there are distinct differences. Annealing in nitrogen reduces both Coulomb and roughness scattering (compare R 2 with R 1 and R 4 with R 3). Since annealing reduces the roughness, it has to be concluded that in this case the Coulomb centers are related to atomic steps. In Table I a comparison of atomic roughness and Hall mobility at high inversion density reveals a constant product of the two quantities within experimental error for R 1, R 2, R 4, showing that the scattering centers are the same for these samples, and their density is given by the step-atom density. All three samples had as a last temperature treatment heating in a dry gas producing obviously identical interfaces (except step density). Since for low as well as for high hole concentrations the rougher transistors show always the lower mobility, the physical origin of the roughness scattering, and the Coulomb scattering has to be correlated. The oxide charge near the interface is responsible for the Coulomb scattering. It is well known that dangling bonds of silicon atoms at the interface Si-SiO₂ and ionized impurities (like Na, K, Li) are the centers for the oxide charges. It is therefore concluded that in the present case the step edges provide the sites for the dangling bonds and therefore the interface charge and, in this way, determine both the mobility at high and at low inversion density. It should be pointed out that the density of step atoms ($\approx 10^{14}/\text{cm}^2$) is much higher than the interface charge ($10^{11}-10^{12}/\text{cm}^2$), so that only special edge sites like kink sites should be responsible for interface charge.

Only sample R 3 oxidized in wet oxygen shows a different behavior. The possible reasons are discussed in Ref. 33.

2. Interface state density and fixed oxide charge

The data shown in Table I confirm the general trends of the published dependencies of the processing variables on electronic parameters.⁶⁰⁻⁶⁷ Comparing the data with the also shown atomic roughness, we see quite clearly that there ex-

ists strong correlation between the atomic roughness and both the interface state density and the fixed charge Q_{fix} .

Earlier measurements^{21,22} have shown a low-temperature anneal in nitrogen does not change the roughness. Therefore, we can assume that an anneal during PMA does not change the roughness either, because the interface will not be provided with oxygen. Also, SiH₄, which may be created at the interface, cannot evaporate as it can at the free silicon surface during reaction with atomic hydrogen.⁹² Therefore, we can conclude that a low-temperature anneal in forming gas will not change the roughness. Comparing the roughness with the data of the PMA-treated samples, we observe the same strong correlation. The results further confirm a strong correlation to the total fixed charge Q_{fix} with and without PMA. Considering the whole set of data, it seems that the atomic roughness plays the dominant role in controlling the interface properties. But we have to keep in mind that the MOS structures discussed here were processed to produce a high atomic roughness, to make the influence of the roughness visible and measurable. New measurements with an improved SPA-LEED system⁹³ show that the roughness can be decreased further, by choosing the right oxidation condition to a value lower than 1% step-atom density.⁹⁴

Besides the atomic roughness there exist a couple of other explanations for the behavior discussed, such as neutral and charge impurities,⁷¹ mobile ion,^{72,73} radiation damage,⁷⁴ point defects, vacancies,^{75,76} and others. Deal⁶¹ proposed a model and classified all known process-dependent effects in four different categories [(1) Q_{fix} , fixed positive charge, (2) N_{ST} , fast interface states, (3) N_{of} , traps, (4) Q_0 , mobile ions]. We can explain our results with an extension of this model. He explained the interface states N_{ST} with uncompensated dangling bonds at the interface, which can be saturated with hydrogen. Further, an interface state can be created by a missing oxygen atom, which is also responsible for the Q_{fix} (explaining $Q_{\text{fix}} \sim N_{\text{ST}}$).

The present results suggest that the uncompensated dangling bonds are essentially found at step edges. If we assume a probability of 1% of an edge atom to provide a dangling bond the experimental data of R 1 are approximately met. If those sites are preferably due to kink sites at crossings of step edges in different directions, the density of dangling bonds is approximated by square of the step-atom density, if steps in different directions are considered independent. In this way the decrease from R 1 to R 2 may be explained. PMA treatment provides the surface states with atomic hydrogen which saturates some dangling bonds leading to a further decrease of the state density.

The discussion is in the same way applicable to R 3 and R 4. In the case of the wet oxidation of R 3, the interface is already provided with a lot of hydrogen, and therefore many dangling bonds are saturated. This explains the relatively high value of R 3 at the beginning, which also shows an exceptional mobility.³³

3. Comparison with literature

Since atomic roughness has not yet been measured quantitatively elsewhere, a comparison is not possible in this respect. The extensive literature data on electronic properties

TABLE III. Comparison of roughness data (SPA-LEED) with fixed oxide charge Q_{fix} , interface state density (N_{ST}), mobility (μ), and processing parameters in literature.

| Process parameter | Q_{fix} | N_{ST} | Roughness ^a | Mobility ^b |
|--|------------------------|------------------------|------------------------|------------------------|
| Increasing oxidation temp. (dry) | ↓ ^c | ↓ ^c | ↓ | ↑ ⁱ |
| Increasing oxidation temp. (wet) | ↓ ^d | ↓ ^d | ↓ | |
| Increasing oxidation thickness | no change ^e | no change ^e | no change | no change ^m |
| Dry anneal (N ₂ , Argon) short time (high temp.) | f | ↓ ^g | ↓ | ↑ ⁿ |
| PMA | no change ^h | h | no change | ↑ ^o |
| Water | ↓↑ ^d | ↓ ^j | ↑ | ↑↓ ^p |
| Cleaning (clean→contaminated) | ↑ ⁱ | ↑ ^k | ↑ | ↓ ^q |
| Silicon orientation (111)→(100) | ↓ ^h | ↓ ^c | ↓ | ↑ ^r |

^a References 11, 12, and 21.

^b References 6, 7, and 44.

^c References 60 and 68.

^d References 60 and 65.

^e Reference 64.

^f References 59, 80, and 81.

^g References 60, 68, and 80.

^h Reference 60.

ⁱ Reference 84.

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^m Reference 57.

ⁿ References 4, 33, and 56.

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^p Reference 33.

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of the Si-SiO₂ interface and our previous data^{21,22,30,33} may be used for an indirect comparison. The data taken are summarized in Table III.

Increasing the oxidation temperature for dry and for wet oxidation leads in both cases to a decrease in Q_{fix} and N_{ST} ^{60–68} and the atomic roughness too (see Table III), whereas the mobility increases at low temperatures.⁶⁹

For oxides thicker than 20 nm the roughness is independent of the oxide thickness.^{21,22} The same relationship shows Q_{fix} and N_{ST} .⁶⁴ Yagi and Kawaji⁵⁷ have shown that the mobility at high inversion does not depend on the oxide thickness (90–270 nm). Thinner oxides (thickness lower than 20 nm) are remarkably rougher.^{21,22} But due to a lack of (CV) and mobility measurements, there is no comparison possible for these oxides.⁷⁰

Annealing in an inert atmosphere like N₂ at high temperatures significantly decreases the roughness^{21,22} and Q_{fix} .^{30,33,60,80} Johnson *et al.*⁸⁰ also showed a decrease for N_{ST} , but these curves keep their typical shape for N₂ annealing. N₂ and argon annealing results in the same behavior.^{60,68,80} These results are summarized and described by the so-called “dry oxygen triangle” introduced by Deal.⁶⁰ We can now easily add the new parameter atomic roughness, which depends on the oxidation temperature. Annealing in dry N₂ always reduces the roughness.²² The lower the temperature the longer the annealing time required to produce the same low roughness. This coincidence of the roughness data with all kinds of electronic data is very striking support of our model, which reveals the edge atoms as source for interface states N_{ST} as well as for fixed charges Q_{fix} . Annealing experiments by Yagi,⁵⁶ Kawaji,⁵⁸ Kawaguchi *et al.*,⁸² Sugano *et al.*,⁷⁹ and Deal³⁵ showed an increase in the mobility, which is consistent with a decrease of step atom density due to annealing in nonoxidizing atmosphere.

Further, we have concluded from our roughness data that a PMA treatment will not change the roughness.²¹ It also should not change Q_{fix} ,⁶⁰ but it decreases N_{ST} dramatically,^{60,80,81} which can be explained by saturating the dangling bonds with hydrogen. Johnson *et al.*⁸⁰ showed that a high-temperature anneal in N₂ decreases the surface state density but keeps the shape of the distribution. The number of step atoms will be reduced. An additional PMA reduces N_{ST} further, but also changes the distribution of the density of states. Therefore, the best interface is obtained by optimum smoothness of the interface (high-temperature N₂ anneal) and by saturation of dangling bonds PMA. Sugano *et al.*⁸⁸ has shown that a PMA treatment increases the mobility for all carrier concentrations.

Only the wet oxidation is very complex. Water increases the roughness^{21,22} due to the high oxidation rate, but it also provides the interface with a lot of hydrogen which saturates the dangling bonds, so that N_{ST} will decrease finally.⁸³ In the case of Q_{fix} ,^{60,65} increments and decrements have been observed according to the two competing effects (roughness increase, hydrogen providing). The influence of water on mobility has been nicely demonstrated by Sugano,⁸⁸ and can now be completely explained with our roughness data. In the case of the only wet or dry oxidation the dry ones always show the higher mobility and should have the lower roughness. After an additional short high-temperature Ar anneal (30 min), the wet samples show the higher mobility, because the anneal smoothed the interface, and the wet ones were already provided with hydrogen. Performing Ar anneal a long time (20 h) instead of a short time, the wet samples are still better, but according to the short anneal, the mobility decreases. The long-time anneal does not change the roughness, but decreases the amount of hydrogen. An additional low-temperature N₂ anneal decreases the mobility further,

because no hydrogen will be provided.

Furthermore, Vass *et al.*⁷⁸ showed a correlation between interface roughness (determined theoretically) and oxide charge, whereas Sah *et al.*⁸⁷ showed the correlation between the oxide charge and the mobility, and Miyazaki *et al.*⁹⁶ demonstrated the correlation between the interface state density and the mobility, which is compatible with our result.

In addition, a strong dependence of state density N_{ST} , charge Q_{fix} , and mobility on silicon orientation has been observed, with values nearly a factor of 2–3 higher for the (111) face compared with the (100) face. Assuming similar quality of the oxides, the physical reason for this difference must be the interface. The ratio of the minimum step height of (111) and (100) faces is 3.1350/1.3575, i.e., a factor of 2.3. The SPA-LEED data show us similar densities of edge atoms for both orientations after identical treatments.²² Razouk and Deal⁶⁰ showed that the midgap state density of (111) faces versus the midgap state density of (100) faces is linear and independent of all the oxidation parameters. Therefore, we can conclude a higher step constitutes a stronger distortion at the step edge, which explains the difference.

VI. CONCLUSION

SPA-LEED measurements provide, for the first time, quantitative data on the atomic roughness at the Si-SiO₂ interface. Furthermore, by systematic variation of oxidation parameters including oxide thickness, oxidation temperature, pre- and post-treatments, atmosphere, and sample orientation, the influence on roughness (see Table II) has been established quantitatively and directly. The balance between a roughening effect (high oxidation rate, reaction controlled) and a smoothing effect (low oxidation rate, diffusion controlled) determines the final roughness.

Second, the atomic roughness is strongly correlated to all kinds of electronic properties like mobility, density of interface states and fixed oxide charge, demonstrated by special performed MOS transistors. The lower the roughness, the higher the mobility, and lower the density of interface states and fixed oxide charge.

Mobility measurements at 4.2 K yielded nearly a constant product of the mobility and roughness. Even at room temperature the samples with the smoother interface show a mobility 30% higher than those of the rougher ones. Further, the results demonstrate that the roughness scattering is correlated with the Coulomb scattering.

The (CV) measurements demonstrate quite obviously that edge sites are preferred sites for both surface states and oxide charge. Hydrogen treatment (PMA) cancels those centers only partially. To obtain low values of Q_{fix} and N_{ST} , it is necessary both to smooth the interface (high-temperature anneal in inert atmosphere) and saturate the dangling bonds (PMA). Therefore, it is very important to measure and to control the interface roughness for all new procedures, especially with thin oxides in VLSI.

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