

# Improving the performance of high-efficiency silicon heterojunction solar cells through low-temperature deposition of an i-a-Si:H anti-epitaxial buffer layer

Chen-Wei Peng<sup>a,b</sup>, Chenran He<sup>b</sup>, Hongfan Wu<sup>b</sup>, Si Huang<sup>b</sup>, Cao Yu<sup>b,\*\*\*</sup>, Xiaodong Su<sup>a,\*\*</sup>, Shuai Zou<sup>a,c,\*</sup>

<sup>a</sup> School of Physical Science and Technology, and Jiangsu Key Laboratory of Thin Films, Soochow University, 1 Shizi Street, Suzhou, 215006, China

<sup>b</sup> Suzhou Maxwell Technologies Co., Ltd., 228 Lulang Road, Wujiang District, Suzhou, 215200, China

<sup>c</sup> Jiangsu Key Laboratory of Advanced Negative Carbon Technologies, Soochow University, 199 Ren-ai Road t, Suzhou, 215123, China



## ARTICLE INFO

### Keywords:

Silicon heterojunction solar cells  
Surface passivation  
Amorphous silicon  
Anti-epitaxial layer  
Low-temperature procedure

## ABSTRACT

In this work, an effective strategy for realizing high-performance silicon heterojunction (SHJ) solar cells involves replacing the existing rear single intrinsic hydrogenated amorphous silicon (i-a-Si:H) layer by depositing a bi-layer i-a-Si:H stack on the rear side using two different deposition chambers and manipulating the deposition temperature to inhibit epitaxial growth at the interface and maintain a good interfacial passivation effect. A low-temperature procedure is implemented to deposit the first anti-epitaxial i-a-Si:H buffer layer (I1 layer) of ~1.5 nm thickness with a high hydrogen concentration and a low refractive index prior to the second bulk i-a-Si:H layer (I2 layer) of ~5.5 nm thickness. The effects of the growth temperature and ignition power during deposition on the optical and structural properties of the i-a-Si:H buffer layers are investigated, and the impact of the buffer layers on carrier transport and collection is also evaluated. Utilizing this strategy, a trade-off between guaranteed passivation capability and low contact resistivity results in an improvement of 0.21%<sub>abs</sub> in power conversion efficiency (PCE), which is mainly driven by increases in V<sub>oc</sub> and FF, and a certified PCE of 25.92 %, with a high open circuit voltage (V<sub>oc</sub>) of 749.7 mV, is achieved on a full-area M6-size industry-grade silicon wafer.

## 1. Introduction

Surface passivation of crystalline silicon (c-Si) is essential for achieving state-of-the-art photovoltaic devices [1–3]. Silicon heterojunction (SHJ) solar cells require a high open circuit voltage to achieve high power conversion efficiency [4–6], which can be realized by effective passivation. In this approach, a passivation layer is typically formed on the crystalline silicon surface of SHJ solar cells [7–9], which consists of hydrogenated amorphous silicon (a-Si:H) materials [10,11]. Passivation decreases the number of carrier recombination centers between the wafer and the amorphous silicon layer, resulting in an improved open-circuit voltage (V<sub>oc</sub>) of SHJ solar cells that can surpass 760 mV [12–14]. The ability of a-Si:H to provide exceptional passivation

has been well established. The introduction of hydrogen atoms effectively neutralizes silicon dangling bonds on both a-Si:H thin films and c-Si surfaces [11]. This process reduces the gap states, which consequentially lowers the carrier recombination rate that is required for SHJ solar cells to achieve efficiencies above 26 % [5,6]. An optimal a-Si:H layer is typically formed by employing a deposition process that ensures both a high density and excellent quality of the a-Si:H layer [15]. It is also crucial to prevent epitaxial development at the interface between the c-Si bulk and a-Si:H layer, which is detrimental to solar cell performance [16]. Recently, several methods have been proposed to improve the surface passivation quality of a-Si:H, such as passivation using hydrogen plasma treatment (HPT), along with post-annealing of amorphous silicon [17–19]. However, another requirement for effective

\* Corresponding author. School of Physical Science and Technology, and Jiangsu Key Laboratory of Thin Films, Soochow University, 1 Shizi Street, Suzhou, 215006, China.

\*\* Corresponding author.

\*\*\* Corresponding author.

E-mail addresses: [yucao@maxwell-gp.com.cn](mailto:yucao@maxwell-gp.com.cn) (C. Yu), [xdsu@suda.edu.cn](mailto:xdsu@suda.edu.cn) (X. Su), [szou@suda.edu.cn](mailto:szou@suda.edu.cn) (S. Zou).

passivation in SHJ solar cells is that the a-Si:H/c-Si interface must be deposited without epilayer formation [20,21]. Since there is a tendency for high-quality amorphous silicon passivated surfaces to produce epitaxial layers (epilayers), there is a trade-off between interfacial passivation quality and epilayer suppression [22]. Relatively high deposition rates for amorphous silicon layers have been shown to prevent epilayer growth adjacent to the a-Si:H/c-Si interface [23]. The addition of this amorphous layer reduces the interface defect density (Dit) [24–26] by removing surface dangling bonds (DBs) [27] and keeping the dopant layer away from the c-Si surface due to the hydrogenation effect described earlier.

It is well known that the substrate temperature during intrinsic amorphous silicon deposition is an important variable affecting film growth [28,29]. Ru et al. reported that an ultra-thin intrinsic a-Si:H buffer layer with a hydrogen content of 25.8 % was deposited on c-Si wafer surfaces using RF-PECVD at a temperature of 220 °C, which improved the  $V_{oc}$  of SHJ solar cells due to the effective inhibition of epilayer formation [22]. Notably, the elevated deposition temperature limited the increase in the hydrogen content in the a-Si:H layer. Here, we propose a low-temperature procedure to deposit an anti-epitaxial i-a-Si:H buffer layer (I1 layer) prior to a dense i-a-Si:H bulk passivation layer (I2 layer) to form a bi-layer i-a-Si:H stack for optimizing the interfacial passivation quality of SHJ solar cells. The optical and structural properties of the buffer layer were investigated by FTIR, and the impact of the buffer layer on carrier transport and collection was evaluated utilizing contact resistivity analysis. Finally, a buffer layer with 35.6 % hydrogen content and a 64.8 % microstructure factor was obtained at a substrate temperature of 160 °C and a 0.45 nm/s deposition rate. As a result, the i-a-Si:H buffer layer with a lower substrate temperature and decelerated deposition rate improved the series resistance of the SHJ solar cells while maintaining a high  $V_{oc}$ , resulting in an improvement of 0.21%abs in the average power conversion efficiency (PCE) and a certified PCE of 25.92 %, with a high open circuit voltage ( $V_{oc}$ ) of 749.7 mV, on a full-area M6-size industry-grade silicon wafer.

## 2. Experimental details

To assess the deposition rate and refractive index, I1 layers were first deposited on top of the non-tin surface of the bare glass. Since trial and error approaches for temperature adjustments can introduce errors, two independent process chambers were used for the I1 and I2 layers to ensure the stability of the process for the I2 layer at each time. After deposition, the thickness and refractive index (n) of the I1 layer were also defined by using a spectrum ellipsometer (SENTECH SE800PV). Another set of experiments was performed using RCA clean silicon wafers, where the passivation quality and microstructure of the I1 layer were investigated. The effective minority carrier lifetime ( $\tau$ ) was measured by a Sinton WCT-120 quasi-steady-state photoconductance (QSSPC) system. The microstructure factor ( $R^*$ ) of the amorphous I1 layer was characterized by Fourier transform infrared (FTIR) spectroscopy. The physical significance of  $R^*$  lies in the fact that it approximates the a-Si:H film as a two-phase system, with a densely structured amorphous network in one phase and a network containing micropores in the other. The  $R^*$  can be calculated as  $R^* = (I_{2080}) / (I_{2000} + I_{2080})$  based on the Gaussian formula, and the hydrogen content ( $C_H$ ) was calculated as described by Ru [22]. The transfer length measurement (TLM) method with a contact array was applied to determine the contact resistivity ( $\rho_c$ ) [30]. The current-voltage (I-V) characteristics were obtained by illuminating the solar cell with I-V testers (IVT solar) under standard test conditions (AM 1.5G, 25 °C).

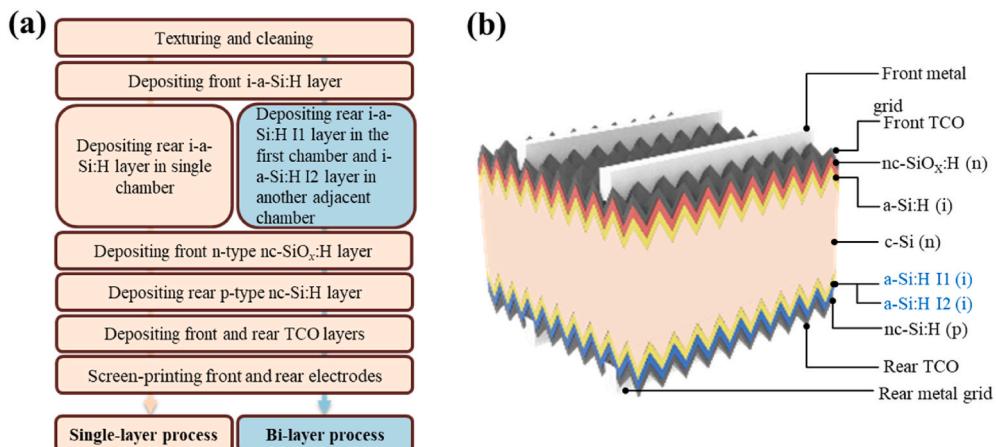
The SHJ solar cells were bifacial and fabricated on n-type M6-sized (274.5 cm<sup>2</sup>) Czochralski (CZ) c-Si wafers with a thickness of 130 μm and a resistivity of 0.3–2.1 Ω·cm. The wafer surfaces were first chemically textured to obtain pyramids that were randomly distributed with a size of approximately 1–2 μm. Then, the c-Si wafers were cleaned by modified RCA before amorphous layer deposition. Immediately

thereafter, 6–8 nm thick i-a-Si:H layers were deposited on both sides of the clean wafers as the passivation layer. Then, 15–20 nm thick n-type hydrogenated nanocrystalline silicon oxide (nc-SiO<sub>x</sub>:H) layer and 20–30 nm thick p-type hydrogenated nanocrystalline silicon (nc-Si:H) layer were deposited on the front and rear sides of the cells, respectively. All layers were deposited by plasma-enhanced chemical vapor deposition (PECVD) equipment, which was customized by Suzhou Maxwell Technologies Corporation. Following this step, approximately 80–90 nm TCO layers were sputtered on both wafer surfaces. Finally, Ag finger grids on both sides of the cells were introduced by screen printing. Subsequently, the SHJ solar cells were annealed at 190 °C for 20 min, and the average width of the fine line fingers was approximately 45 μm. Fig. 1(a) shows the process flow diagrams of the SHJ solar cells fabricated using the rear single-layer and bi-layer i-a-Si:H processes. The structure of the SHJ solar cells fabricated using the rear bi-layer i-a-Si:H process is illustrated in Fig. 1(b).

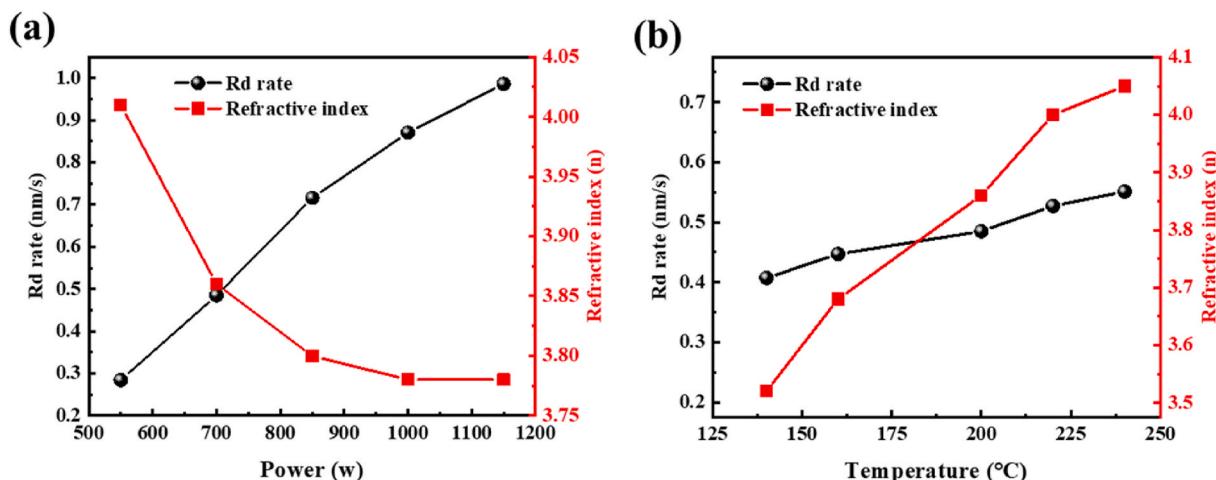
## 3. Results and discussion

The quality of the amorphous I layer was ascertained by modifying the PECVD process settings. To prevent the epitaxial reaction introduced by excess hydrogen gas in the experiment [31], a pure silane I1 procedure (I1 layer) was utilized, wherein no more hydrogen gas was injected into the plasma reaction during the deposition process. The link between the PECVD power density and the refractive index of the film is shown in Fig. 2(a). As the power density increased, so did the deposition rate of the amorphous film. This was indicative of the fact that the silane had not yet reached a depletion state and was effectively involved in the reaction to ensure that SiH<sub>4</sub> sufficiently reacted in the plasma. The presence of silane plasma in the high-depletion region enhances the development of superior amorphous silicon layers [32], leading to improved passivation. The refractive index of the I1 layer decreased as the deposition rate increased. This result indicates that higher deposition rates lower the density of the I1 layer, which makes the amorphous layer more suitable for contact with the I1 layer of the crystalline silicon surface. This in turn effectively reduces the formation of an epitaxial layer between the c-Si and I1 layers. Fig. 2(b) shows the trend of the refractive index of the film at different substrate deposition temperatures. As the process temperature increased, the deposition rate slightly increased, possibly due to the increase in the chamber temperature, which caused a minor increase in the collision capability of ions. It is worth mentioning that the refractive index of the film increases with increasing temperature, and the intrinsic amorphous silicon layer becomes increasingly dense during the higher temperature process. The refractive index is found to be in the range of 3.5–4.1, with an additional n ranging from 3.5 to 3.8 compared to the power series. PECVD with a high ignition power is commonly used for the I1 layer to avoid epilayer formation [22,33], and the process temperature can be optimized to decrease the refractive index of the film [34]. It is possible to obtain a porous layer with a low refractive index without increasing the deposition rate, which is usually accompanied by a large amount of powder accumulation and poor film uniformity [35].

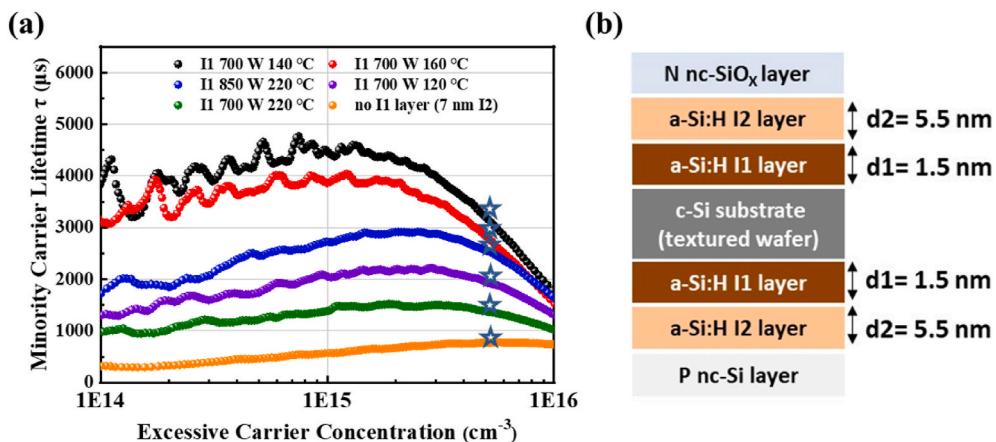
Next, the passivation ability of amorphous silicon was ascertained via the Sinton minority carrier test. Fig. 3(a) shows the minority carrier lifetime  $\tau_{eff}$  of the cell as a function of the density of excess carriers at different ignition powers and substrate temperatures for I1 layer deposition. A schematic diagram of the structure of the experimental samples is shown in Fig. 3(b). At the same 220 °C deposition temperature, the I1 layer with a higher ignition power (850 W) has a higher minority carrier lifetime. Furthermore, it can be concluded that the pure I2 layer deposited at 220 °C has insufficient passivation capability due to the epilayer growth itself and has the lowest minority carrier lifetime. When the I1 layer is utilized as an anti-epitaxial layer, the looser I1 layer can effectively facilitate the anti-epitaxial effect. As a result, the carriers of the 850 W group are better than those of the 700 W group due to the loose I1 layer. For groups with additional I1 layers, the use of a void-rich



**Fig. 1.** (a) Process flow diagrams of the two SHJ solar cell manufacturing processes. (b) Schematic illustration of the structure of the SHJ solar cell fabricated using the rear bi-layer i-a-Si:H process.



**Fig. 2.** (a) Deposition rate (Rd rate) and refractive index (n) as a function of ignition power for the I1 layer. (b) R<sub>d</sub> and n as a function of substrate temperature for the I1 layer.



**Fig. 3.** (a) Dependence of the growth temperature and ignition power on the minority carrier lifetime ( $\tau$ ) for variable buffer I1 layers. (b) Schematic diagram of the experimental samples.

layer allows sufficient saturation of the a-Si:H/c-Si interface with high-density silicon dangling bonds. The I1 layer at the interface serves two purposes: first, it acts as a buffer layer to hinder epilayer growth at the a-Si:H/c-Si interface; second, it prevents the diffusion of H radicals from

the H diluted plasma to the silicon interface by behaving as a protective layer. This diffusion is caused by the H dilution in the I2 layer of the high-quality layer, which is necessary for the growth of a dense i-a-Si:H layer for surface passivation [36]. The effects of different deposition

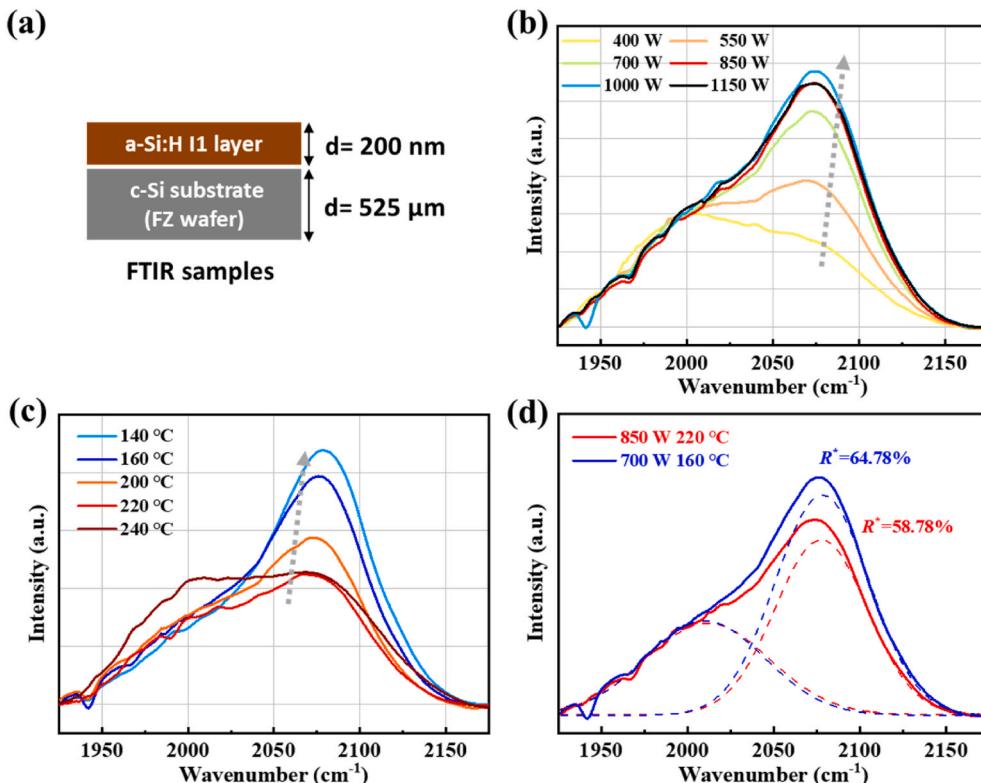
temperatures on the I1 layer were examined, and it was found that the minority carrier lifetime is higher when a low-temperature I1 layer is utilized. For instance, the minority carrier lifetime at 140 °C and 160 °C was superior to that of the layer formed at 220 °C. A higher minority carrier lifetime at lower process temperatures seems to be counterintuitive. This observation could be attributed to the use of a dual process chamber, which can effectively deposit the I1 and I2 layers at different temperatures in separate chambers. Hence, the relationship between the layers can be observed more accurately. Since lower deposition temperatures result in more porous and hydrogen-rich i-a-Si:H layers, this may lead to an increase in defects in the film, affecting the transport of charge carriers within the layer. An abundant hydrogen content can both promote epitaxial growth [31,37] and lead to lattice disorder, which affects the passivation capability of the i-a-Si:H layer. These two effects compete with each other to reach a balance [22,38]. Since the process temperature of the I layer generally falls in the range of 120–250 °C, it was expected that the I1 layers with a low refractive index deposited at low substrate temperature would have a good anti-epitaxial effect, but the passivation ability would be insufficient. However, since the low-temperature I1 layer is very loose, the anti-epitaxial growth ability of the c-Si surface is greatly improved. When we further lowered the temperature of the I1 layer to 120 °C, there was a significant decrease in the passivation capability of the I layer itself. Although we enhanced the anti-epitaxial properties, it remains crucial to preserve the layer's ability to provide effective passivation. Furthermore, with the high-temperature process of the I2 layer, the overall I layer passivation ability reaches a maximum, resulting in an excellent passivation effect.

The results indicate that a bi-layer i-a-Si:H stack composed of the I1 and I2 layers is necessary for achieving excellent passivation and that a looser I1 layer can enhance the passivation capability of the i-a-Si:H layer to increase the minority carrier lifetime. Therefore, the  $R^*$  of the I1 layer was further analyzed by decomposing the Si-H stretching mode into Gaussian deconvolution [28,34] of the low stretching mode (LSM)

and the high stretching mode (HSM), which are located at 2000 cm<sup>-1</sup> and 2080 cm<sup>-1</sup>, respectively, in the FTIR measurements [39]. At different deposition temperatures, a higher process temperature corresponds to a lower hydrogen content. This is ascribed to the escape of hydrogen due to high-temperature deposition conditions. In contrast, the low-temperature deposition of the film results in a sufficiently high hydrogen content [40,41].

A schematic diagram of the FTIR samples is shown in Fig. 4(a). Fig. 4(b) shows the absorption bands associated with the Si-H stretching modes obtained by FTIR spectroscopy through the I1 layers on FZ (Float Zone) Si wafers with a total thickness of 200 nm by using different PECVD ignition powers. There are significant differences in the microstructure between the film layers. As the ignition power increases from 400 W to 1150 W, HSM dominates in the less dense I1 layer, leading to a gradual increase in  $R^*$  to 0.64. A high deposition rate of the I1 layer decreases the refractive index of the film. A low refractive index is also accompanied by a high HSM, which is mostly a SiH<sub>2</sub>-bonded structure. The SiH<sub>2</sub> bonded layer is more likely to be looser in the amorphous silicon layer. The  $R^*$  and associated hydrogen content in the power experiments are listed in Table 1. The hydrogen content in the I1 layers is in the range of 26–37 %, making it a relatively hydrogen-rich silicon layer, with the highest hydrogen content in the 140 °C group.

The substrate temperature change in the void-rich I1 layer is harnessed, and differences in the microstructure between the film layers can be observed in both Fig. 4(c) and Table 1. As the substrate temperature decreases from 240 °C to 140 °C,  $R^*$  increases from 50.9 to 71.8, indicating that the amorphous silicon film becomes less dense. This also corresponds to the refractive index of the single film in Fig. 2(b), which is 3.5 even at a low deposition temperature of 140 °C. Hence, the  $R^*$  of i-a-Si:H can be effectively changed by modifying the deposition conditions. In Fig. 4(d), the I1 layer with a typical high temperature and high power (blue line) is selected and compared with that with a relatively low temperature and low power (red line). The  $R^*$  of the I1 layer of the blue line group is similar to that of the conventional high-speed



**Fig. 4.** (a) Schematic diagram of FTIR samples deposited on the FZ c-Si wafer. FTIR spectrum of the I1 layer under various conditions: (b) PECVD ignition power series, (c) substrate temperature series and (d) Si-H stretching modes (SM) and the deconvolution of the spectrum into low-SM (LSM) and high-SM (HSM).

**Table 1**

Statistical data of  $R^*$  and  $C_H$  with respect to the I1 layers as a function of power and substrate temperature.

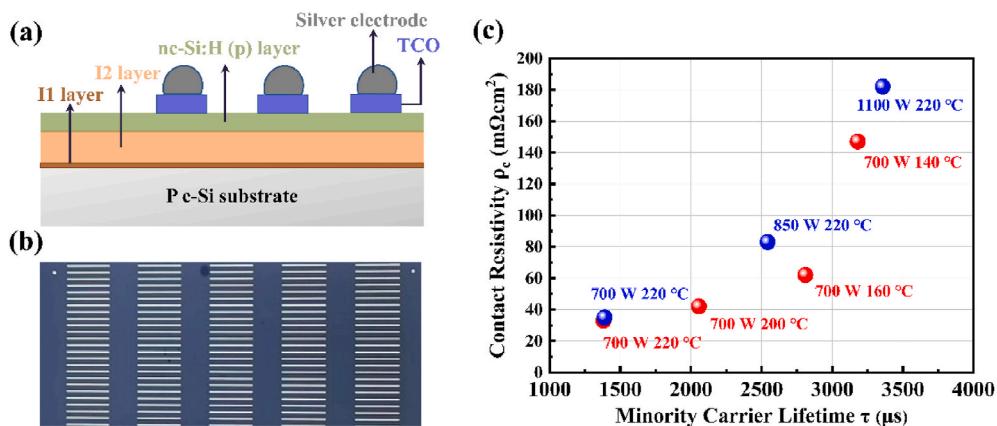
| SN | Power(W) | Temperature (°C) | $R^*(\%)$ | $C_H$ (at.%) |
|----|----------|------------------|-----------|--------------|
| 1  | 400      | 220              | 32.9      | 26.4         |
| 2  | 550      | 220              | 48.3      | 30.4         |
| 3  | 700      | 220              | 54.1      | 31.9         |
| 4  | 850      | 220              | 58.8      | 33.2         |
| 5  | 1000     | 220              | 60.1      | 33.5         |
| 6  | 1150     | 220              | 64.0      | 34.5         |
| 7  | 700      | 140              | 71.8      | 36.5         |
| 8  | 700      | 160              | 64.8      | 35.6         |
| 9  | 700      | 200              | 63.5      | 34.4         |
| 10 | 700      | 220              | 54.1      | 31.9         |
| 11 | 700      | 240              | 50.9      | 31.1         |

deposition of the I1 layer (blue group), and the  $R^*$  is higher. The  $R^*$  can indicate whether the I1 layer is dense. However, when applied to solar cells, the effect of the layer on carrier transport needs to be considered.

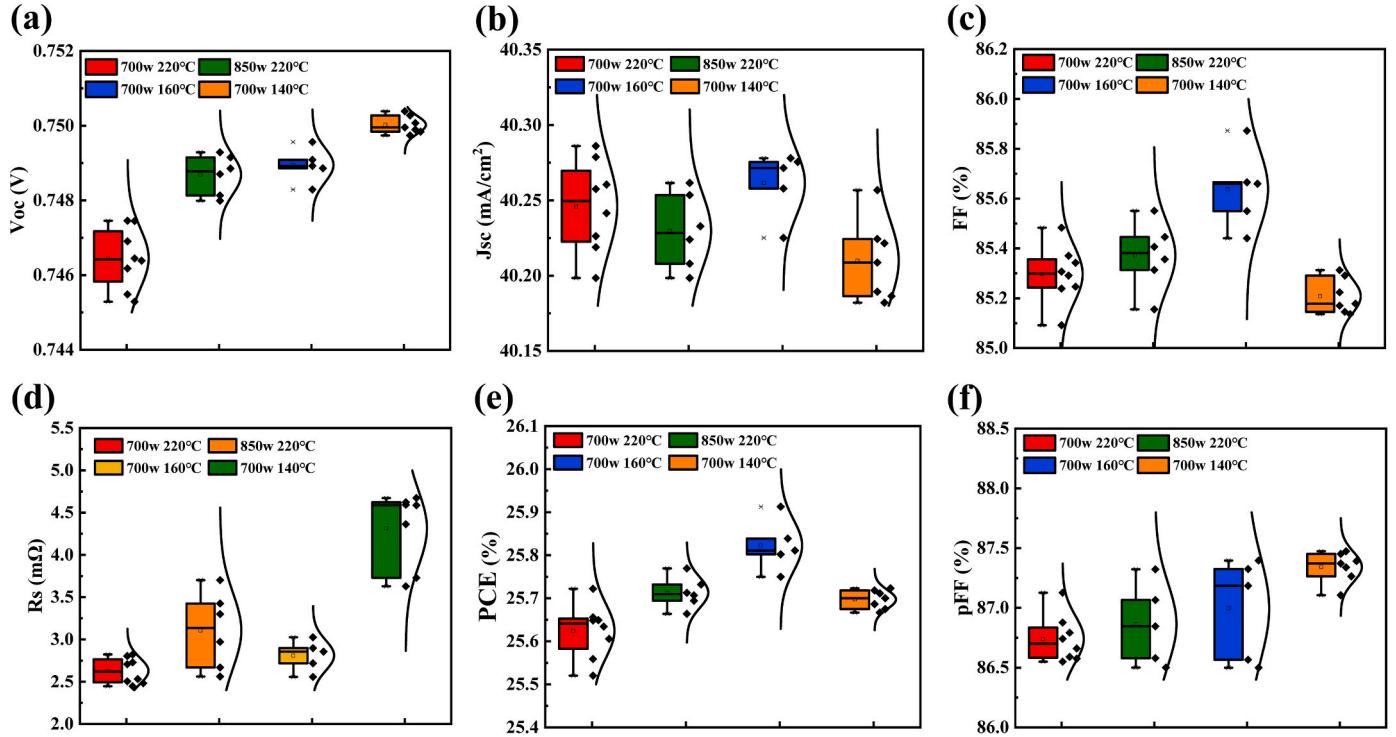
Carrier selectivity can be utilized to quantitatively describe the ability of a contact to collect one type of carrier. Since overall carrier transport is crucial in SHJ solar cells [42],  $\rho_c$  experiments were conducted to observe the effect of the buffer I1 layer. The conceptual diagram is shown in Fig. 5(a), while Fig. 5(b) shows a top view of the actual sample. The minority carrier lifetime ( $\tau$ ) and  $\rho_c$  of the I1 layer were measured, and the relationship between the transport of various hole carriers and the corresponding  $\tau$  for two series of i-a-Si:H layers (one is the power series with blue solid dots, and the other is the low-temperature series with red solid dots) was determined. The total thickness (I1+I2) of the i-a-Si:H layers was fixed at 7 nm, and the thicknesses of the I1 and I2 layers were 1.5 nm and 5.5 nm, respectively. From Table 1, it can be observed that increasing the power from 400 W to 1150 W at 220 °C lowered the refractive index of the I1 layer and worsened the film quality, which corresponds to better anti-epitaxial effectiveness. In the power series in Fig. 5(c) (blue points),  $\tau$  increases from 1 ms at 700 W to 3.5 ms at 1100 W. However,  $\rho_c$  also increases to 100 mΩ cm<sup>2</sup>, and  $\tau$  is approximately 3.5 ms when the whole I1 layer is relatively thin (7 nm). However, the problem that follows is the rapid increase in  $\rho_c$ . The 850 W group reaches a relatively optimal balance between passivation and carrier transport, with  $\tau = 2.7$  ms corresponding to a contact resistivity of 45 mΩ cm<sup>2</sup>. By replacing the deposition temperature of the i-a-Si:H layers in the low-power group (red solid dots), the refractive index decreases significantly with decreasing deposition temperature, and increasing the hydrogen content of the film layer greatly improves the anti-epitaxial capability. The  $\tau$  of the sample at 700 W increases from 1 ms at 220 °C to 3.1 ms at 160 °C. This indicates that decreasing the deposition temperature improved the

passivation effect. However, more defects at low temperatures lead to a significant increase in  $\rho_c$ . Defects lead to a significant increase in  $\rho_c$ , which seriously affects the collection and transport of holes. The carrier selectivity of passivated contacts in SHJ solar cells describes the ability of a contact to collect only one type of carrier, and good carrier selectivity is usually manifested by a lower  $\rho_c$  and higher  $\tau$ . The less desirable energetic position of defect states is the cause of impeded transport using a void-rich I1 layer, in conjunction with a potentially lower effective contact area of such void-rich films and the alteration of the induced band bending, which affects the hole density in the contact region [43]. The experimental results reveal that a trade-off exists between  $\rho_c$  and  $\tau$ , and better passivation results are usually achieved at the cost of a higher  $\rho_c$  in this mode of I1 + I2 structure passivation. The comparatively low-power low-temperature group achieves a reduced  $\rho_c$  while providing a longer hole carrier lifetime than the high-temperature group (solid blue dots in Fig. 5(c)). A thin, low-temperature, high-porosity I1 layer is joined to a thicker, low-porosity I2 layer. The low-temperature and low-speed change in the I1 microstructure results in an epitaxial layer, improving hole transport and achieving a better balance between transport and passivation.

The scattered point values of the  $V_{oc}$ , short-circuit current density ( $J_{sc}$ ), filling factor (FF), series resistance ( $R_s$ ), PCE, and pseudo fill factor (pFF) of the four groups of as-prepared SHJ solar cells are shown in Fig. 6 (a–e), and the corresponding average values of these electrical parameters are summarized in Table 2. The SHJ solar cells with buffer I1 layers deposited at 140 °C exhibited a maximum average  $V_{oc}$  of 750 mV, but the lowest average  $J_{sc}$  and FF. The low FF mostly arises from the contribution of low  $R_s$ , specifically low  $\rho_c$ . When the growth temperature of the I1 layer is increased to 220 °C, there is a noticeable reduction in the  $V_{oc}$ . This reduction is attributed to the creation of an epilayer at the interface between a-Si and c-Si. The ignition power of the 220 °C group increases from 700 W to 850 W, resulting in a 2.4 mV increase in the  $V_{oc}$  from 746.4 mV to 748.8 mV. A higher deposition rate of the I1 anti-epilayer ensures excellent surface passivation while minimally impacting carrier transport, leading to a significant enhancement in the  $V_{oc}$ . It is important to mention that the use of a high-quality film with high-temperature processing (refractive index = 4.35) for the I2 layer increases the likelihood of epilayer development. Utilizing a low-speed and low-temperature I1 layer can effectively prevent the increase in interface defect density induced by the dense I2 layer during epitaxial growth, thereby enhancing the efficiency of solar cells. The optimal group of SHJ solar cells with an average PCE of 25.81 % was achieved by depositing an a-Si:H I1 layer at a rate of 0.45 nm/s at a temperature of 160 °C. A slight trade-off between high  $V_{oc}$  and FF is demonstrated at this temperature when a 1.5 nm I1 layer with a porous structure is utilized. To optimize high-performance solar cells, it is necessary to achieve



**Fig. 5.** (a) Schematic diagram of the TLM measurement for the I1+I2+nc-Si:H (p) layer. (b) Top-view of a representative TLM sample. (c) Contact resistivity ( $\rho_c$ ) and minority carrier lifetime ( $\tau$ ) of SHJ hole contacts comprising different stacked a-Si:H (i) layers (I1 is a variable). The power series correspond to the blue points at a fixed substrate temperature of 220 °C, and the substrate temperature series correspond to the red points at a power of 700 W.



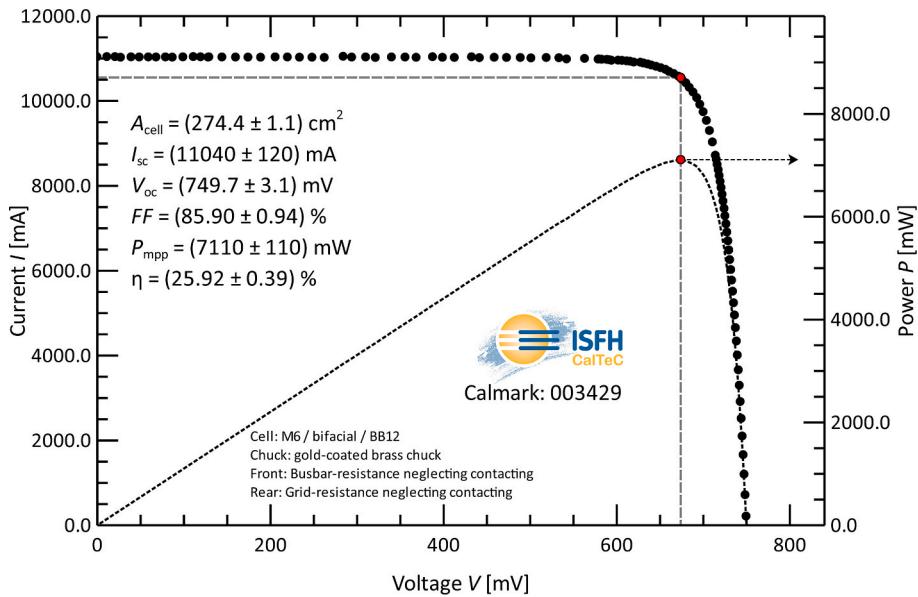
**Fig. 6.** Scatter plots of (a)  $V_{oc}$ , (b)  $J_{sc}$ , (c) FF, (d)  $R_s$ , (e) PCE and (f) pFF for the four groups of SHJ solar cells. Comparison of the electrical parameters of the SHJ solar cells corresponding to the buffer II layers deposited at different growth temperatures and ignition powers.

**Table 2**

Average electrical parameters of the four groups of SHJ solar cells with buffer II layers deposited under various deposition conditions.

| $T_{BII}$<br>layer<br>(°C) | $P_{BII}$<br>layer<br>(W) | $J_{sc}$<br>( $\text{mA}/\text{cm}^2$ ) | $V_{oc}$<br>(mV) | FF<br>(%) | PCE<br>(%) | Certified/in-house<br>measurements |
|----------------------------|---------------------------|---|------------------|-----------|------------|------------------------------------|
| 220                        | 700                       | 40.25                                   | 746.4            | 85.3      | 25.64      | In-house test                      |
| 220                        | 850                       | 40.23                                   | 748.8            | 85.4      | 25.71      | In-house test                      |
| 160                        | 700                       | 40.27                                   | 748.9            | 85.7      | 25.81      | In-house test                      |
| 140                        | 700                       | 40.21                                   | 750.0            | 85.2      | 25.70      | In-house test                      |
| 160                        | 700                       | 40.27                                   | 749.7            | 85.9      | 25.92      | ISFH CalTeC                        |

superior surface passivation quality to minimize losses resulting from interface recombination. Additionally, it is crucial to employ a-Si:H thin films with minimal imperfections to avoid any interference with charge carrier collection. Ultimately, a bi-layer process, which was meticulously optimized to fulfill these two criteria, was implemented. It can be deduced that as the series resistance increases, the pseudo fill factor (pFF) increases, leading to a reduced leakage current. The variability in the FF is contingent upon the interplay between the  $R_s$  and pFF. Finally, the best solar cell has been officially certified to reach a PCE of 25.92 % (Fig. 7), making it a valuable asset for enhancing the overall efficiency of SHJ solar cells.



**Fig. 7.** Current-voltage (I-V) and power-voltage (P-V) curves of the best SHJ solar cell featuring a bi-layer i-a-Si:H stack on the rear side, certified by ISFH CalTeC.

#### 4. Conclusion

In summary, we proposed depositing a bi-layer i-a-Si:H stack on the rear side of SHJ solar cells instead of the existing single i-a-Si:H layer to improve the interface passivation effect. We investigated the impacts of the different buffer I1 layers on epitaxial growth and carrier transport, as well as the effects of substrate temperature and ignition power on the optical and structural properties of the buffer I1 layers. The findings suggest that placing a buffer I1 layer with a high hydrogen concentration and a low refractive index between c-Si and a dense a-Si:H layer can effectively inhibit epitaxial growth. Lowering the substrate temperature to 160 °C resulted in a buffer I1 layer with 35.6 % hydrogen content and a 64.8 % microstructure factor at a deposition rate of 0.45 nm/s, in contrast to the high hydrogen content buffer layer achieved by increasing the power to increase the deposition rate. A greater hydrogen concentration prevented epitaxial growth and improved the interface passivation of the SHJ solar cells. Additionally, a lower deposition rate reduces the number of defects in the buffer I1 layer and greatly improves carrier transport and collection. By introducing an improved low-temperature buffer I1 layer, an improvement of 0.21%abs in the average PCE and a certified PCE of 25.92 %, with a high open circuit voltage ( $V_{oc}$ ) of 749.7 mV, is achieved on a full-area M6-size industry-grade silicon wafer. This work provides a reference for exploring further improvements in the interface passivation of SHJ solar cells.

#### CRediT authorship contribution statement

**Chen-Wei Peng:** Writing – original draft, Visualization, Validation, Methodology, Investigation, Data curation. **Chenran He:** Methodology, Formal analysis. **Hongfan Wu:** Methodology, Formal analysis. **Si Huang:** Methodology, Formal analysis. **Cao Yu:** Supervision, Resources, Project administration, Formal analysis. **Xiaodong Su:** Supervision, Resources, Project administration, Funding acquisition. **Shuai Zou:** Writing – review & editing, Supervision, Project administration, Funding acquisition, Conceptualization.

#### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

#### Data availability

Data will be made available on request.

#### Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant No. 52202276), the Natural Science Foundation of the Jiangsu Higher Education Institutions of China (Grant No. 22KJB480010), the Priority Academic Program Development of Jiangsu Higher Education Institutions (PAPD), and the Suzhou Science and Technology Plan Project (SYC2022041).

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