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Passivation properties of tunnel oxide layer in passivated contact silicon solar cells

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ABSTRACT

Passivated contact in advanced high-efficiency silicon solar cells based on the full back surface field (BSF) is reported here in based on the application of a tunnel oxide layer that is less than 2 nm thick. The open-circuit voltage (V_{oc}) was significantly improved via interface passivation due to insertion of the tunnel oxide layer. During oxide layer growth, a transition region, such as a sub-oxide, was observed at a depth of about 0.75 nm in the growth interface between the silicon oxide layer and silicon substrate. The properties of the less than 2 nm thick tunnel oxide layer were primarily affected by the characteristics of the transition region. The passivation characteristics of tunnel oxide layer should depend on the physical properties of the oxide. The interface trap density D_{it} is an important parameter in passivation and is influenced by the stoichiometry of the oxide which in turn strongly affected by the fabrication and the post annealing conditions. During heat treatment of a-Si:H thin films (for the purpose of crystallization to form doped layers), thin film blistering occurs due to hydrogen effusion on flat substrate surfaces. To minimize this behavior, we seek to control the surface morphology and annealing profile. Also, the passivation quality of passivataed contact structure declined for the sample annealed above 900 °C. This decline was attributed not only to local disruption of the tunnel oxide layer, but also to phosphorus diffusion. The resistivity of the tunnel oxide layer declined precipitously for the sample annealed above 900 °C. On the basis of these, implied V_{oc} over 740 mV was achieved in n-type Si wafer through the control of the oxide stoichiometry via optimizing the annealing conditions.

1. Introduction

A high-efficiency silicon solar cell that acts as a 25% passivated emitter has been developed by using a rear locally diffuse (PERL) cell by applying a photolithography process [1]. Recently, a 25.1% tunnel oxide passivated contact (TOPCon) cell based on an n-type Si wafer was reported. The highlight of this cell is the excellent interface passivation quality achieved by applying a < 2 nm tunnel oxide layer. A passivation contact structure was inserted into the <2 nm tunnel oxide layer between the doped poly-Si and the silicon substrate. Transport through the oxide was reported by the tunneling mechanism. The TOPCon cell achieved an open-circuit voltage of 718 mV and saturation current density ($J_{0,rear}$) of <7 fA/cm^2, attributed to the tunnel oxide layer [2–4]. Also, 23.1% of silicon solar cell based on tunnel oxide junction was achieved to apply to replace the intrinsic a-Si:H thin films with tunnel oxide (<2 nm) based on heterojunction with intrinsic thin layer (HIT) solar cells [5]. The tunnel oxide layers that were less than 2 nm thick were formed by various methods such as thermal and wet-chemical and UV/O_3 photo-oxidation [6–8].

The initial steps of oxide growth on silicon substrates at the molecular level are well established [9–11]. Notably, the growth interface between the silicon oxide layer and silicon substrate exists as a chemically graded transition region. The features of the transition region differ from the characteristic features of silicon dioxide and the silicon substrate. This region contains silicon atoms in an intermediate state of oxidation, i.e., a sub-oxide (SiO_x, $x < 2$), and is about 0.75 nm thick. A disordered Si layer of about 0.3–0.6 nm is

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formed under this region [12–15]. Thus, the tunnel oxide layer that is less than 2 nm-thick includes a sub-oxide region.

In this study, the passivation quality of the tunnel oxide layer is explained by analysis of the sub-oxide region based on the post-annealing conditions. Also, at flat surface substrate, the blistering in tunnel oxide junction occurs during the annealing process. This resulted in a passivation performance of tunnel oxide layer is degrade. This study is about improving the passivation of tunnel oxide junction, i.e., a minimization method of blistering for tunnel oxide layer. Further, the thermal stability of the tunnel oxide layer is evaluated via electrical analysis for samples subjected to high-temperature (over 900 °C) annealing.

2. Experimental

Surface textured n-type (100) Cz silicon wafers with a resistivity of 1.0–2.3 Ω cm and thickness of 200 μm were used for the experiments. The wafers were cleaned by using RCA cleaning methods [16,17]. The native oxide layer was removed by using a buffered oxide etchant (BOE). Subsequently, an ultra-thin oxide layer was grown via wet-chemical oxidation. The ultra-thin oxide layer grows at 80 °C for 10 min based on 30% hydrogen peroxide solution. Selected specimens were subjected to post-annealing using a tube furnace below 600 °C. To evaluate the passivation performance of the tunnel oxide passivated contact structure, phosphorus-doped a-Si:H thin films were deposited on both surfaces by radio frequency plasma enhanced chemical vapor deposition (RF-PECVD, RF = 13.56 MHz). The thin films were annealed by using a rapid thermal process (RTP) at 600–1000 °C. RTP annealing was conducted 5 min in the nitrogen atmosphere. Ramp-up rate was about 10–16 °C/s and perform about 5 min with natural cooling. Additionally these films were subjected to a hydrogen passivation process, such as forming-gas annealing (FGA). The passivation quality (iV_{oc}, implied open-circuit voltage) of these films was measured by the quasi-steady-state photo-conductance (QSSPC) method using bifacial structure samples [18]. The shape and thickness of the tunnel oxide layer were observed by transmission electron microscopy (TEM) for high resolution energy dispersive X-ray spectroscopy (EDS) mapping. To confirm the post-annealing effect, the stoichiometry of the tunnel oxide layer was analyzed by angle-resolved X-ray photoelectron spectroscopy (ARXPS) using detection angles of 21–77° before depositing the P-doped a-Si:H thin films. The effect of process steps such as post-annealing and H passivation on the interface state defect density, D_{it}, was also evaluated via capacitor-voltage (C-V) analysis by applying mercury probe systems after removing the poly-Si layer of sample with heat treated.

Also, we changed the surface morphology and the annealing profile for blistering minimization. The surface morphology of silicon wafer (Cz p-type, 2.3 Ω cm, 200 μm) samples was controlled etching temperature such as 70(S70), 80(S80), 90(S90) °C under etching time 10 min (see SEM image of top in Fig. 3). And surface cleaning was conducted according to the RCA cleaning procedure [16,17]. The phase transition of a-Si:H thin films take place in 800–900 °C heat treatment. On the basis of this, annealing profiles were adjusted to minimize blistering of thin films. The passivation quality of tunnel oxide junction was determined on symmetrical structure samples by QSSPC technique [18]. A passivation property was compared with blistering of degree through iV_{oc}. Also, the blistering in tunnel oxide junction structured was observed by and an optical microscope.

After annealing at 850–975 °C, the changes in the resistivity of the tunnel oxide layer were checked via current–voltage (*I–V*) analysis by applying mercury probe systems. Based on this evaluation, the activation energy for diffusion in a two-layer (SiO_x/Si structure) diffusion model was calculated.

3. Results and discussion

3.1. Si—O bonding via post annealing

The tunnel oxide passivated contact structure largely reduces leakage or recombination current due to the less than 2 nm tunnel oxide layer inserted between the substrate and back surface field (or doped poly-Si layer). The tunnel oxide layer has been fabricated by various methods [6–8]. In this study, we utilized wet-chemical oxidation in acid solution. The thickness of the tunnel oxide layer was confirmed to be between <0.7 nm and 1.8 nm by using TEM and EDS mapping images (Fig. 1). Further, the thickness of the thin layer formed on a polished silicon wafer (Cz n-type, 5–6 Ω cm, 650 μm) was confirmed to be 1.4 nm using spectroscopy ellipsometry (SE, J.A. Woollam, M-2000U). The passivation quality of the tunnel oxide layer was analyzed by QSSPC after 900 °C RTP annealing of symmetrical structure samples deposited on P-doped a-Si:H thin films of about 60 nm thickness on the tunnel oxide layer or silicon substrate. Fig. 2(a) shows the passivation effect of the tunnel oxide layer. The passivation quality of the tunnel oxide layer increased by 30 mV compared to that without the thin layer. The passivation quality was also improved by post-annealing after tunnel oxide layer for-

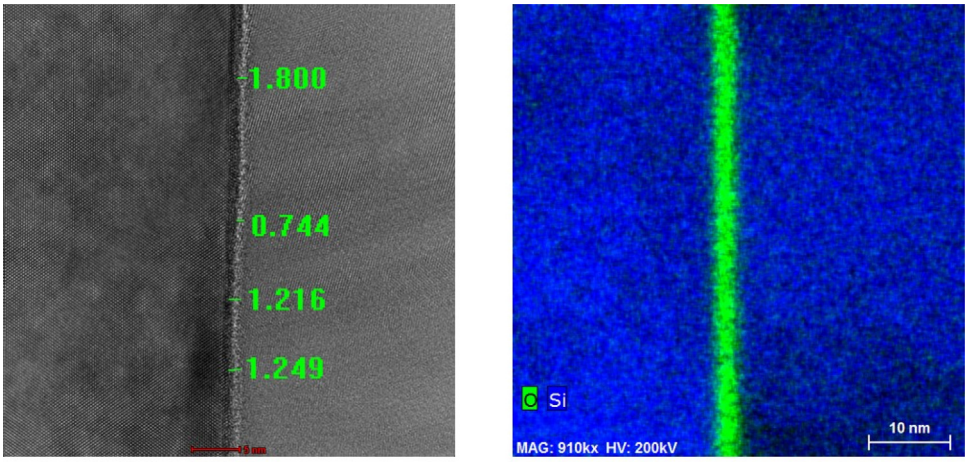

Fig. 1. (a) TEM images and (b) EDS mapping of tunnel oxide layer formed in Si/tunnel oxide/poly-Si structure using wet-chemical oxidation.

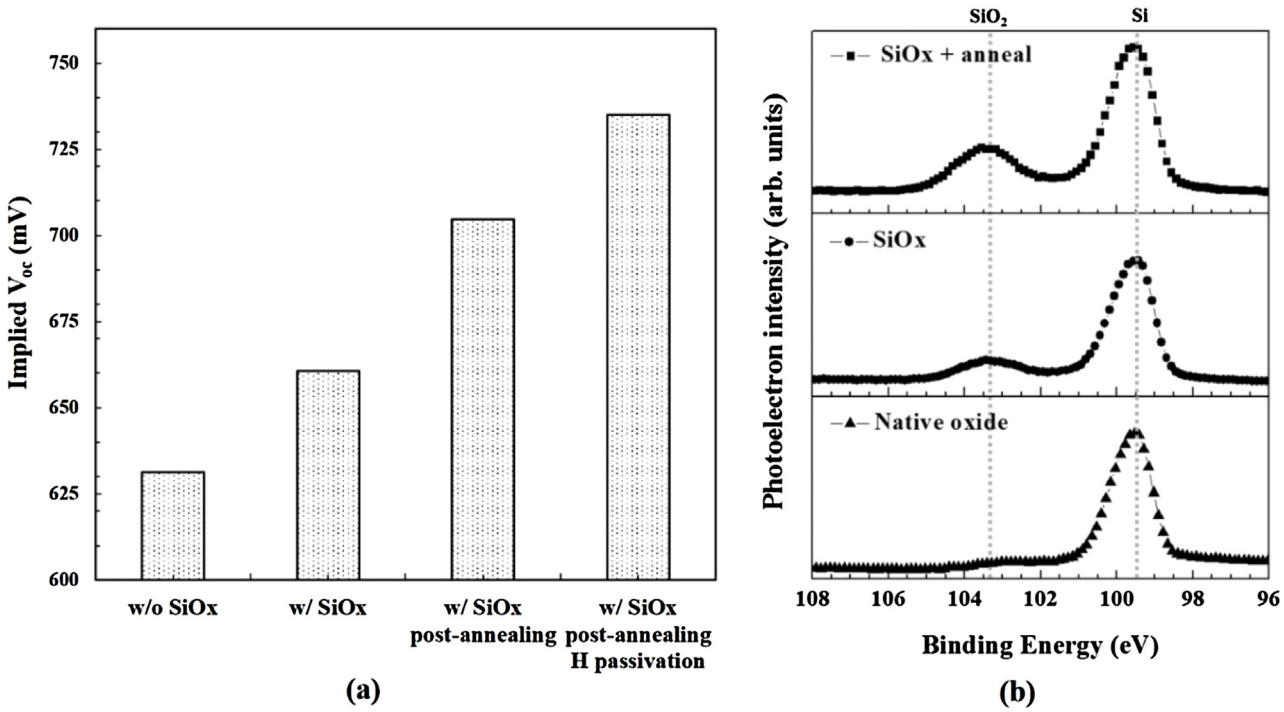

Fig. 2. (a) Implied V_{oc} data as indicator of passivation quality of tunnel oxide layer with post-annealing and H passivation. (b) XPS spectrum of tunnel oxide layer with post-annealing; peaks around 99.5 eV and 103.4 eV correspond to Si and SiO_2, respectively.

mation and H passivation. The passivation quality was confirmed to be over 730 mV due to application of the tunnel oxide layer.

During growth of silicon oxide on the silicon substrate, a sub-oxide region (SiO_x transition, ~0.75 nm) was formed at the interface [12–15]. The silicon oxide layer consisted mainly of SiO_2 (Si^{4+}), while the sub-oxide region at the interface was comprised of intermediate oxidation states, i.e., Si_2O (Si^{1+}), SiO (Si^{2+}), and Si_2O_3 (Si^{3+}) [19]. Silicon dioxide (SiO_2) has excellent passivation ability compared to the sub-oxides (with SiO, Si_2O_3, and Si_2O bonding) [20–22]. The tunnel oxide layer was observed based on detection of Si—O bonding using XPS, as shown in Fig. 2(b). The lower binding energy peak near 99.5 eV is associated with bulk Si and the higher binding energy peak near 103.4 eV is associated with SiO_2. A peak corresponding to a sub-oxide region was observed in-between these two peaks. As seen in Fig. 2(b), the intensity of the SiO_2 peak increased with formation of the tunnel oxide layer. The intensity of this peak was further enhanced by the post-annealing process. Thus, the passivation quality was augmented by the post-annealing process. The stoichiometry of the tunnel oxide layer was evaluated in depth by using ARXPS to monitor the effects of post-annealing (Fig. 3) [23]. ARXPS analysis enables monitoring of compositional changes of the tunnel oxide layer on the silicon substrate with depth. Si-O bonding in the interface region was principally observed at low detection angles, whereas Si—O bonding in the tunnel oxide layer bulk region was observed at higher detection angles. The Si—O bonding data indicate separation of the Si-rich (Si_2O) and O-rich (SiO, Si_2O_3) regions. The ratio in the tunnel oxide layer was determined based on the detection angle [24]. Before post annealing, the tunnel oxide layer was formed via Si-rich bonding at the interface on the substrate (Fig. 3(a)). On the other hand, annealing increased the O-rich and SiO_2 bonds in the layer (Fig. 3(b)). As shown in Fig. 3(c), post-annealing promoted the formation of O-rich bonds in the sub-oxide region in the interface. Therefore, the passivation quality was improved by post-annealing. The passivation quality of the tunnel oxide layer is associated with the Si—O bonding transition. The interface defect density (D_{it}) of the tunnel oxide layer was quantitatively assessed by C-V measurement. The D_{it} was calculated from the parallel conductance (G_m) measured at various frequencies (ω) with a bias voltage, and the peak value (G_p/ω_{peak}) was derived [25,26]. A mercury probe was used for the C-V measurement in order to minimize damage of the tunnel oxide layer. Fig. 4 confirms a decrease of the D_{it} due to the Si-O bonding transition induced by post-annealing. Further, the D_{it} of about 4.36×10^{10} ($cm^{-2}\,eV^{-1}$) was achieved due to the H passivation process. It is thought that dangling silicon bonds in the interface and tunnel oxide layer were passivated by hydrogen. In order to improve the passivation quality of the tunnel oxide layer, it is important to control the properties and stoichiometry of the tunnel oxide layer.

3.2. Hydrogen blistering on flat surface

Passivation quality has excellent in flat surface compared with textured surface (formed random pyramids) [27,28]. To improve it tunnel oxide junction structure was developed on flat surface substrate (polished wafer). But, a blistering of thin films takes place in flat surface structure at annealing. See Fig. 5, which can cause a critical loss in the tunnel oxide junction passivation property. It is similar to blistering of Al_2O_3 films during firing process at high temperature, the mechanism of which is clearly unknown. However, it was usually purpoted to concern the exess of hydrogen present in the Al_2O_3 films. [29]. Blistering phenomenon in this study occurs in structure inserted tunnel oxide layer at heat treatment, but it does not arise in structrue without tunnel oxid layer. It is considered that is realted to hydrogen diffusivity in tunnel oxide layer. The a-Si:H thin films contain numerous hydrogen, which is exellent for surface passivation. At heat treatment in tunnel oxide junction structure, hydrogen get out of the a-Si:H thin films toward surface and interface with substrate. Blistering of thin films is considered to cause by the hydrogen could not escape this time. In case of structure without tunnel oxide layer, hydrogen would have an escape toward Si substrate. On the other hand, in structure applied tunnel oxide

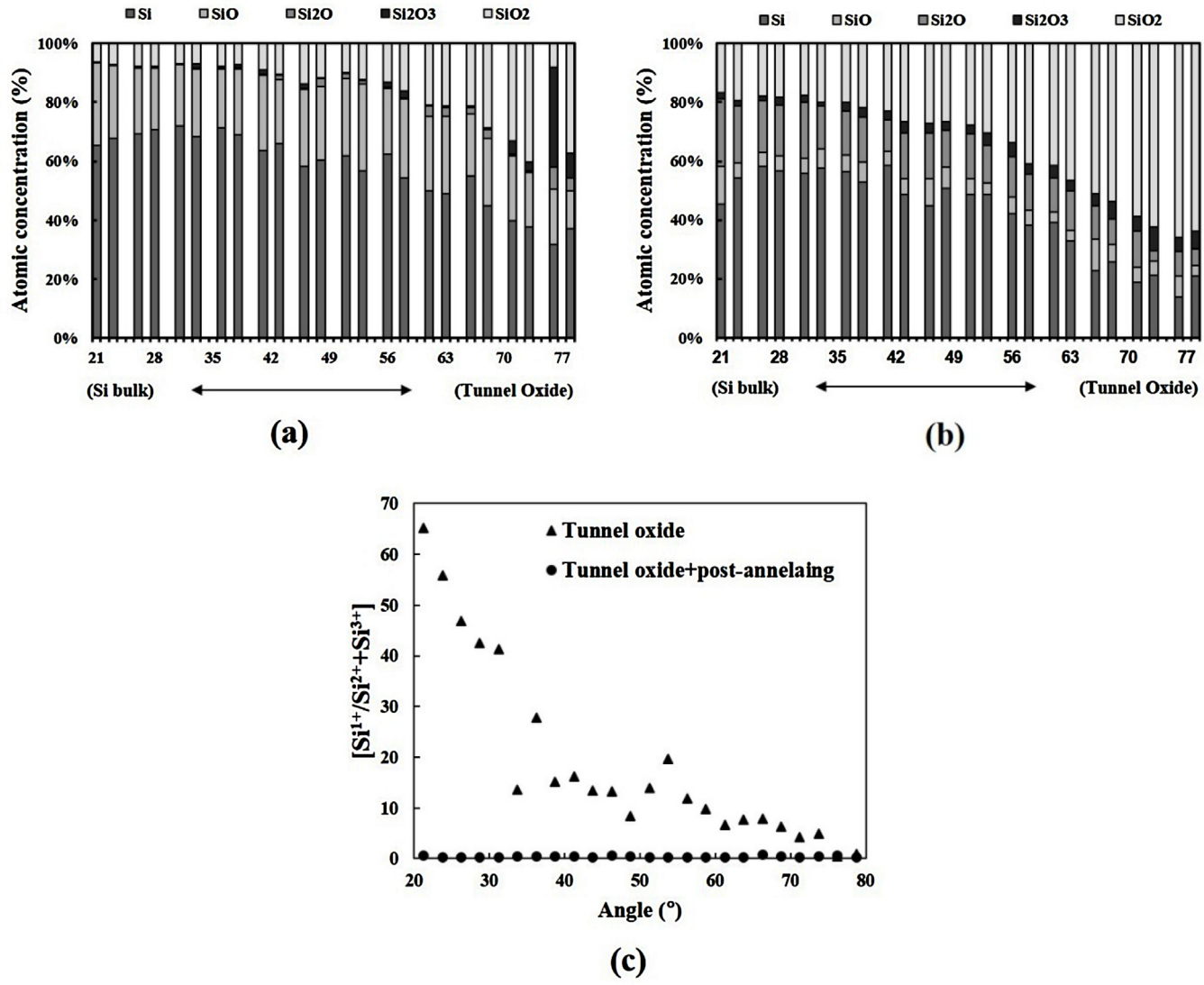

Fig. 3. ARXPS data and detection angle for Si—O bonding transition in tunnel oxide layer (a) without post-annealing and (b) with post-annealing. (c) O-rich bonding ratio in sub-oxide region with post-annealing process.

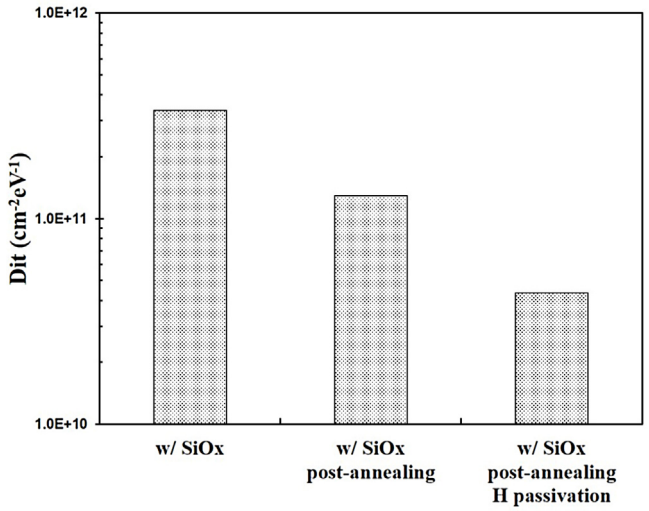

Fig. 4. Effect of post-annealing and H passivation on interface defect density (D_{it}) of tunnel oxide layer, assessed by *C-V* measurement using mercury probe systems.

layer, hydrogen get together in interface. Because of the diffusivity of hydrogen is different in silicon and silicon oxide. It is known that the diffusivity of hydrogen in silicon (Si) is described by [30]

$$\mathbf{D}(\mathbf{T}) = \left(9.4 \times 10^{-3}\right) exp\left(-0.48\mathrm{eV/kT}\right) \left[\mathrm{cm^2/s}\right],$$

and the diffusivity of hydrogen in silicon oxide (SiO_2) is described by [31,32]

$$\mathbf{D}(\mathbf{T}) = \left(8.1 \times 10^{-3}\right) exp\left(-0.2\mathrm{eV/kT}\right) \left[\mathrm{cm^2/s}\right]$$

At 900 °C temperature for crystallization of a-Si:H thin films, The diffusivity of hydrogen show a difference about 14 times between silicon dioxide ($D = 1.12 \times 10^{-3}$ cm^2/s) and silicon ($D = 8.14 \times 10^{-5}$ cm^2/s). We considered that blistering of thin films caused by the hydrogen could not escape due to the hydrogen diffusivity difference.

The hydrogen within a-Si:H thin films is excellent passivated by saturating surface dangling bonds. Passivation quality degradation is due to hydrogen effusion depending on heat treatment (>200 °C). Hydrogen effusion rate is different for the doped and intrinsic (not doped) a-Si:H thin films. [33,34] In case of phosphorus doped a-Si:H thin films, hydrogen effusion-rate is highest near 400 °C annealing process. To minimize a blistering of the thin

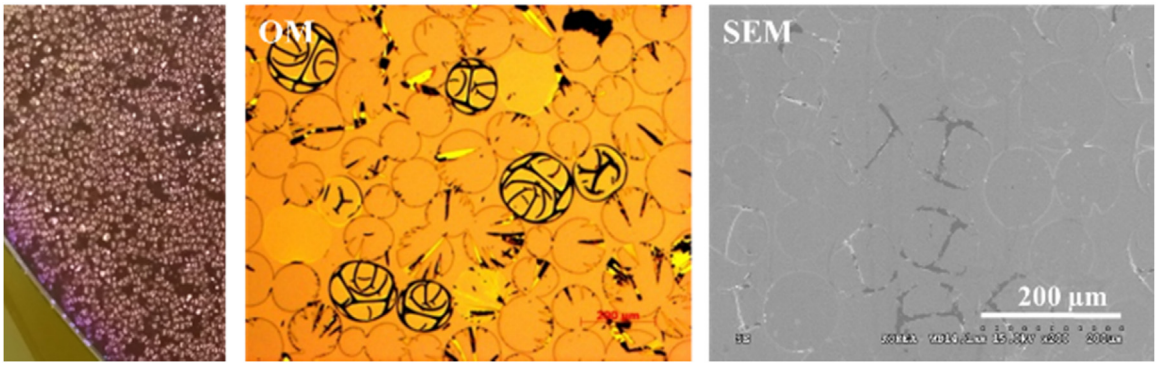

Fig. 5. A blistering image of tunnel oxdie junction structure through heat treatment on flat surface (polished silicon wafer). Surface photography after the heat treatment of the sample which is formed by tunnel oxide and doped a-Si:H layer on flat surface. Also, it is an image which is observed by optical microscope (OM) and scanning electron microscope (SEM).

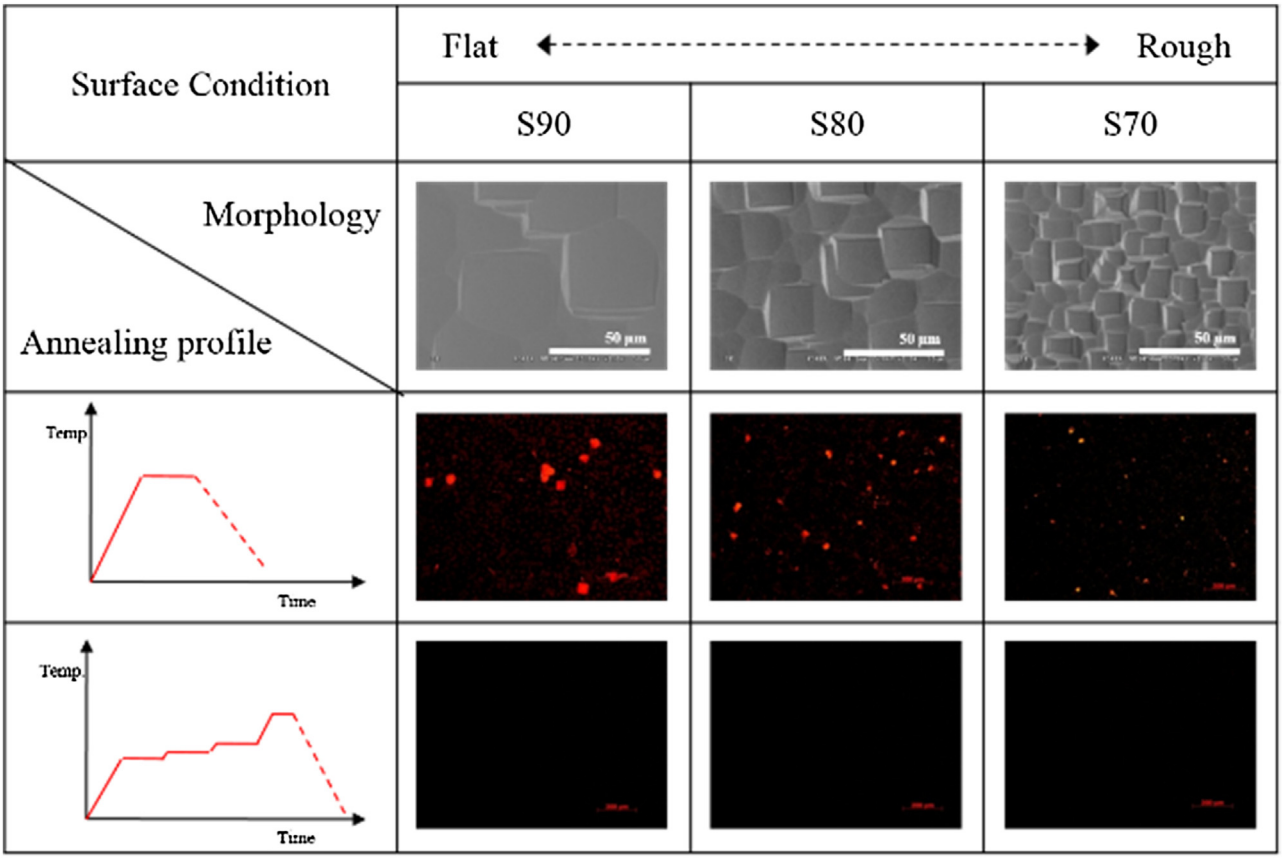

Fig. 6. SEM images of surface depending on the KOH etching temperature 70 (S70), 80 (S80), 90 (S90) °C and OM images(dark) of surface according to RTP annealing profile in order to observe blistering via hydrogen effusion.

films via hydrogen effusion, we controlled annealing profile and surface morphology. 3 step annealing was carried out for was carried out for each 10 min at 400,450,500 °C before 900 °C annealing for 5 min in order that can escaped enough hydrogen. Also, the surface roughness is controlled so that the hydrogen does not get together. As shown in the OM images (dark) of Fig. 6, a blistering of thin films reduced as the roughness surface. Furthermore, blistering phenomenon rarely occur at step annealing process, regardless of surface morphology. We confirmed that hydrogen blistering reduce or not proceed through step annealing and surface morphology control. Also, passivation quality of tunnel oxide junction was compared with blistering, see Fig. 7(a). The implied V_{oc} was improved above 30 mV as the surface rough, without step annealing. Furthermore, passivation quality was achieved above 690 mV through step annealing profile process. Also, it was observed with change of ramp-up rates. It was enhanced through decreasing ramp-up rates of heat treatment (Fig. 7(b)). And it was accomplished above 700 mV (iV_{oc}) regardless of H passivation process. Thus, in order to minimize hydrogen blistering of thin films, it is required sufficient time and path of escape of hydrogen.

3.3. Thermal stability of tunnel oxide junction structure

Fig. 8 shows the passivation performance of the tunnel oxide junction structure based on the annealing temperature. As mentioned earlier, the passivation quality was enhanced by insertion

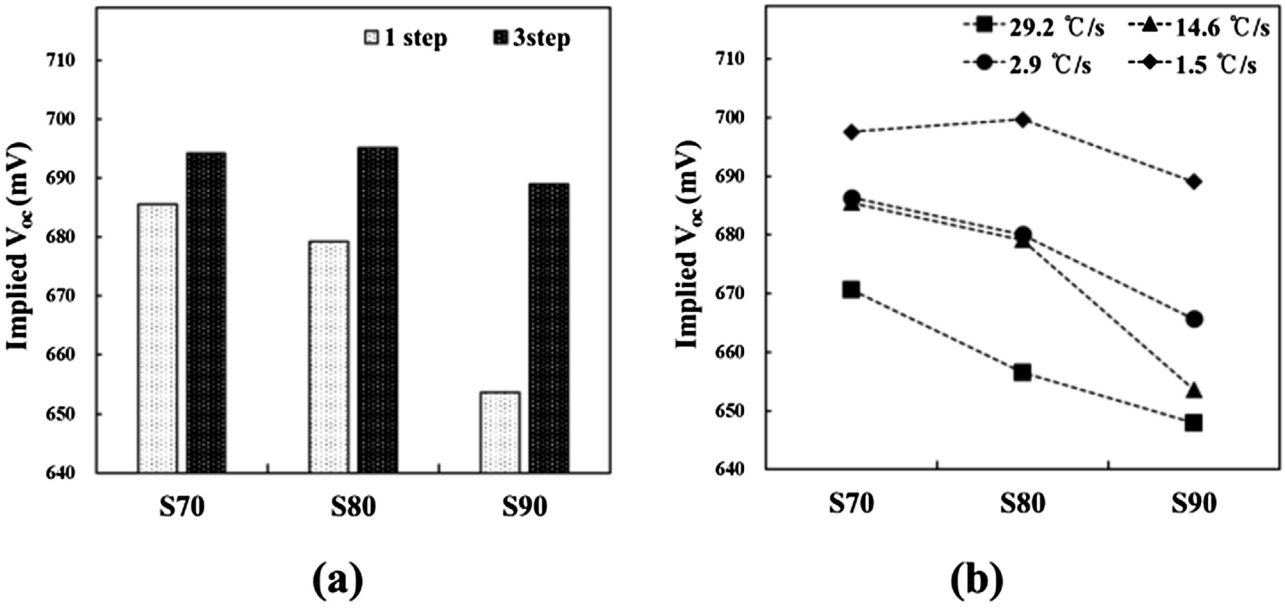

Fig. 7. Implied Voc plotted against the surface morphology (S70, S80, S90), comparison with (a) annealing profile and (b) ramp-up rate control.

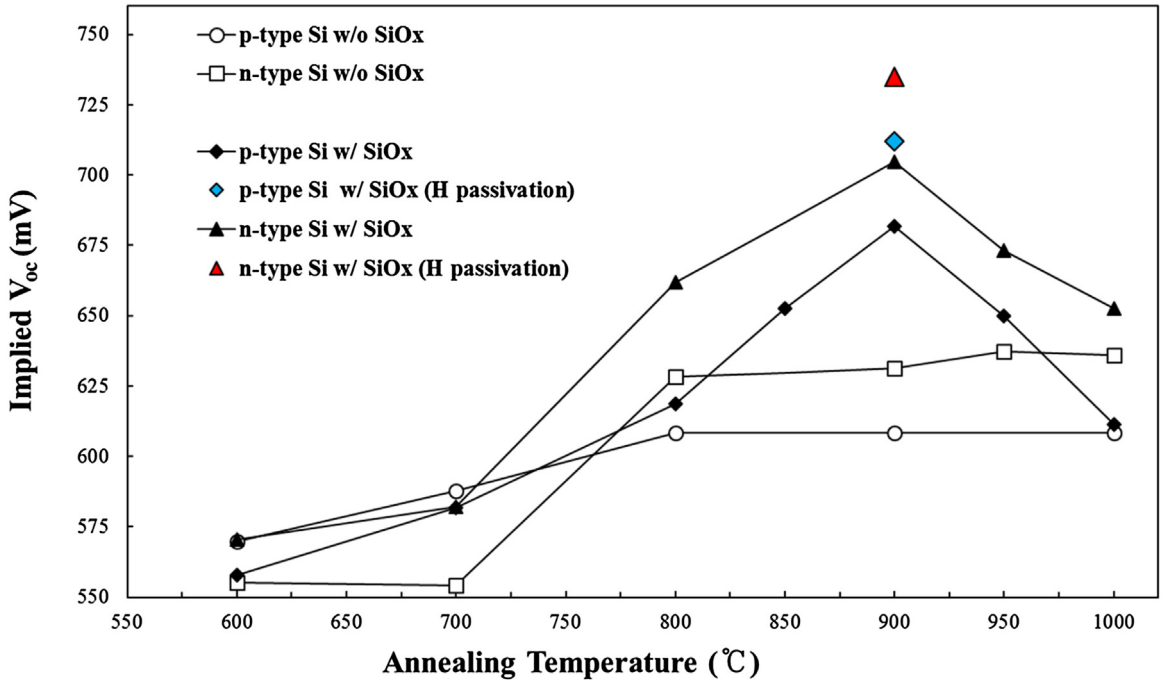

Fig. 8. Implied V_{oc} data as indicator of effect of annealing temperature on passivation quality of tunnel oxide layer for films on n-type silicon wafers; data is also provided for samples without tunnel oxide and samples subjected to H passivation process and 900 °C annealing.

of the tunnel oxide layer. In this study, passivation of the tunnel oxide junction structure was observed to be excellent for the sample subjected to 900 °C RTP annealing. However, the passivation quality decreased with heat treatment above 900 °C. This is reportedly attributed to local disruption of the tunnel oxide layer [35,36]. This disruption is not easy to observe through TEM and XPS measurements due to the fine area analysis on the atomic scale. Thus, electrical conductivity analysis was conducted for the samples subjected to different annealing temperatures to evaluate the *I–V* characteristics. A bifacial structure such as used for the QSSPC measurement was employed. A mercury probe was also utilized in order to avoid the influence of additional processes such as metallization. The results presented in Fig. 9(a) demonstrate that the total resistance declined gradually with increasing annealing temperature, whereas the drop was precipitous for the sample annealed above 900 °C. Thus, this is considered indirect evidence of local disruption of the tunnel oxide layer. Based on the total resistance, the resistivity of the tunnel oxide layer was deducted to separate the layers of the sample structure by considering the thickness and sheet resistance measurements of the poly-Si layer and the substrate properties (see Fig. 9 (b)). Similar to the trend described above, the resistivity of the tunnel oxide layer decreased rapidly for the samples annealed above 900 °C due to local disruption of the thin layer. In some ways, this is considered to be related to the

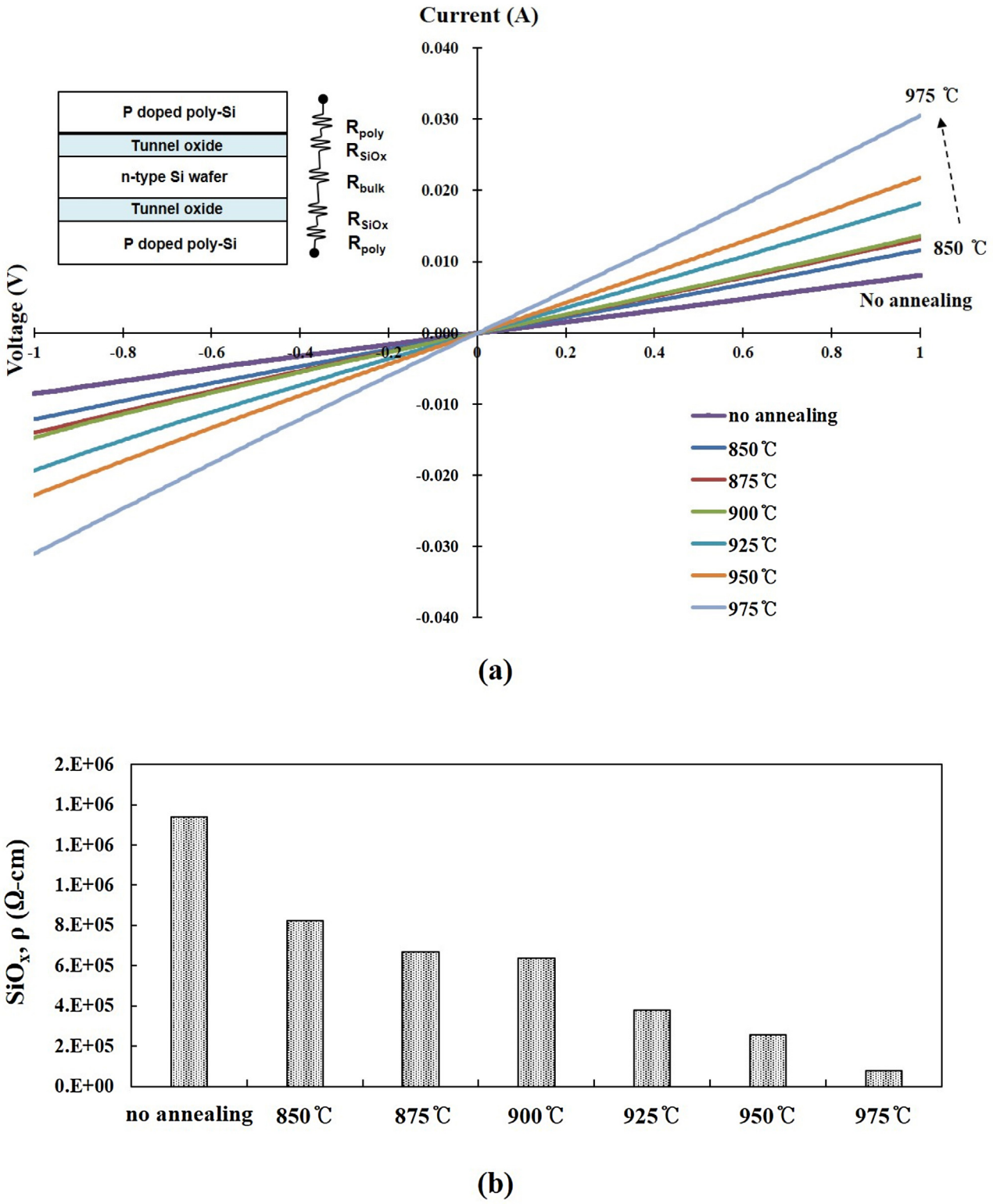

Fig. 9. (a) Current–voltage (*I–V*) curves as a function of annealing temperature for symmetric structures such as poly-Si/SiO_x/Si/SiO_x/poly-Si. (b) Resistivity of tunnel oxide layer calculated from *I–V* curves.

dopant diffusion behavior. The diffusivity, *D*, of phosphorus in the SiO_2 layer is expressed by $D = (4.0 \times 10^{-10}) \exp(-1.62/kT)$ [37]. For the samples annealed above 900 °C for 5 min, it is possible for phosphorus to diffuse into the silicon substrate through the <2 nm thick tunnel oxide layer. Therefore, the decline of the passivation property of the sample annealed above 900 °C is possibly related to auger recombination due to phosphorus diffusion on the silicon substrate [38]. The activation energy determined from a two-layer diffusion model, such as the SiO_2/Si structure, was reported to be 1.4 eV [39]. The conductivity of the tunnel oxide layer as a function of the annealing temperature was converted based on the resistivity calculated from the electrical analysis (Fig. 10(a)). From Fig. 10(b), the

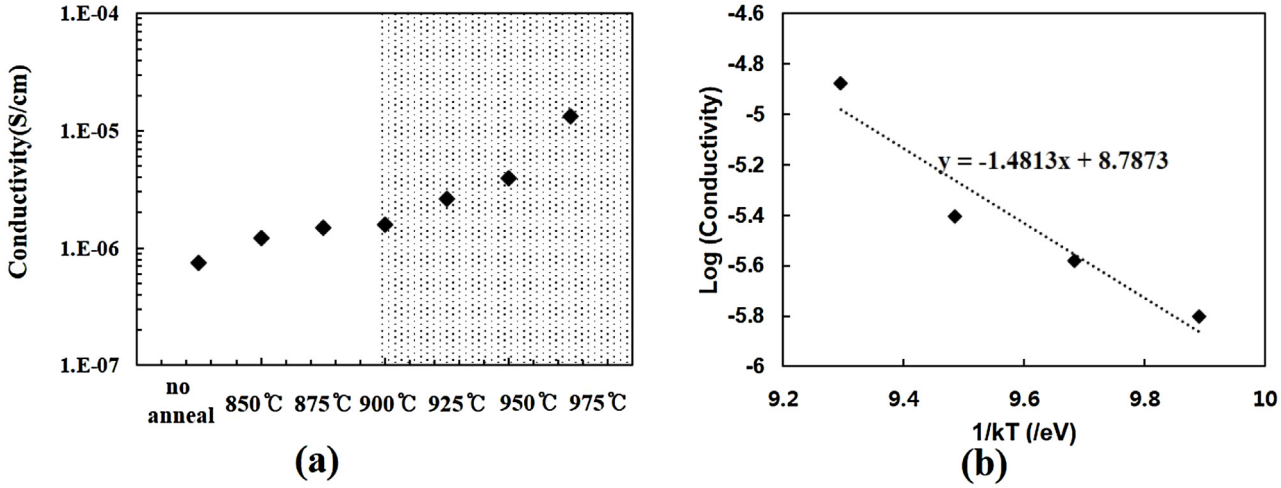

Fig. 10. (a) Deducted conductivity of tunnel oxide layer with annealing temperature. (b) Temperature dependence of the conductivity of tunnel oxide layer for sample subjected to annealing above 900 °C.

activation energy was calculated based on the conductivity change for the sample annealed above 900 °C using the Arrhenius equation, yielding a value of 1.48 eV, similar to the results of a previous study. Thus, the decrease of the passivation quality of the tunnel oxide for the sample annealed above 900 °C is thought to originate not only from local disruption of the tunnel oxide layer, but also in connection to phosphorus diffusion.

4. Conclusions

The tunnel oxide passivated contact structure has attracted attention for achieving high efficiency solar cells. The insertion of a tunnel oxide layer between poly-Si and the substrate is excellent for achieving interface passivation. The passivation quality of the tunnel oxide layer appears to depend on the Si—O bonding in the tunnel oxide layer, which is in turn influenced by post-annealing. The tunnel oxide layer was formed in the sub-oxide region (SiO, Si_2O, Si_2O_3) of the interface with the substrate. The sub-oxide region develops O-rich bonding due to post-annealing. Thus, annealing also improves the passivation quality. Post-annealing and H passivation also reduced the interface defect density due to the Si—O bonding transition and hydrogen passivation of the silicon dangling bonds at the interface. The passivation quality of the tunnel oxide is associated with the stoichiometry and properties of the thin layer.

At heat treatment for crystallization of a-Si:H thin films, in case of flat surface, the blistering of thin films occur due to hydrogen effusion. In order to minimize this, it is considered that required sufficient time and path for escape of hydrogen. For this purpose, we suggest to control surface morphology, annealing profile, and ramp-up rates. Accordingly, we have achieved tunnel oxide junction structure with a 700 mV or more passivation performance (iV_{oc}) in p-type wafer.

The passivation quality declined rapidly for samples subjected to RTP annealing at temperatures over 900 °C. This is reported to be related to local disruption of the tunnel oxide layer. Electrical analysis further confirmed the decline in the resistivity of the tunnel oxide layer with annealing above 900 °C. From another perspective, the decline in the passivation quality was affected by the phosphorus diffusion behavior based on a two-layer diffusion model. The activation energy for phosphorus diffusion in SiO_2/Si was deduced to be 1.48 eV based on the conductivity of the tunnel oxide layer of the sample annealed over 900 °C, which is similar to that reported in a previous study (1.4 eV). To improve the passivation quality of the tunnel oxide layer, the physical properties and thermal stability of the thin layer must be considered.

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