# Assignment 4 (EC39004: VLSI Laboratory)

**Deadline: Upto 4th Feb, 2 pm**

**Instruction: You are required to submit a neatly labeled circuit diagram of the combined unsigned and two's complement array multiplier in hard copy (one per group), and demonstrate the working of the verilog codes and simulation outputs in your respective laptops or computer. Kindly zip your Verilog codes and test bench codes in a folder named by GROUP< NO :> and email it to < sudiptabose1991@gmail.com > before coming to class on 4th Feb, 2019.**

## 1 Problem Statement

Refer to the Modified Baugh Wooley Multiplier discussed in the lab today. Modify the architecture which has an additional control input p. When p = 0, the multiplier treats the real time inputs as unsigned numbers and functions as Braun's array multiplier. When p = 1, the multiplier treats the real time inputs as two's complement numbers and functions as the modified Baugh Wooley Multiplier. The most optimized array multiplier in terms of hardware shall fetch full credit.

Write the Verilog Code for the above m×n combined unsigned and two's complement array multiplier accepting 5-bit multiplicand input a (m = 5), 4-bit multiplier input b (n = 4) and the control signal t, with exhaustive post route simulation outputs. Instantiate the requisite number of half adders and full adders in the code along with other logic gates as deemed necessary.