

Assignment 5 (EC39004: VLSI Laboratory)

Deadline: Upto 11th Feb, 2 pm

Instruction: You are required to submit in hard copy a neatly labelled circuit diagram of the pipelined controlled barrel shifter, and demonstrate the working of the Verilog codes and simulation outputs for the 32-bit pipelined controlled barrel shifter accepting unsigned inputs in your respective laptops or computer. Kindly zip your Verilog codes and test bench codes in a folder named by GROUP< NO :-> and email it to < sudiptabose1991@gmail.com > before coming to class on 11th Feb, 2019.

1 Problem Statement

Consider a controlled barrel shifter that accepts two inputs: a 32-bit unsigned data input A, a second input B denoting the shift amount and a control signal R using ONLY 2:1 multiplexers as the sole circuit building block. When R = 0, the circuit performs the left shift operation; otherwise when R = 1, it performs a right shift operation on the same input data A. Pipeline the circuit such that only a single 2:1 multiplexer comes in the critical path.

Write the Verilog Code for the above circuit description. For sub-mission in hard copy, it is sufficient to draw a neatly labelled circuit diagram for the same considering A to be a 4-bit input only.