

# Junction Field Effect Transistor

The Junction Field Effect Transistor, or JFET, is a voltage controlled three terminal unipolar semiconductor device available in N-channel and P-channel configurations.

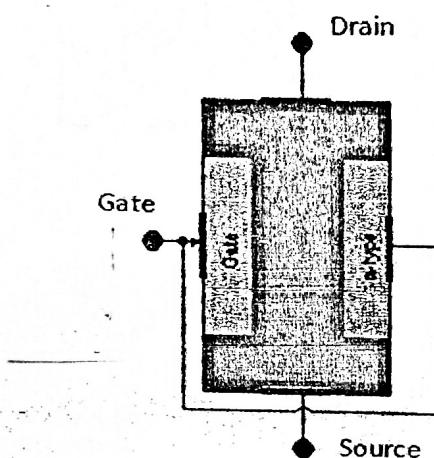


Fig.1(i)

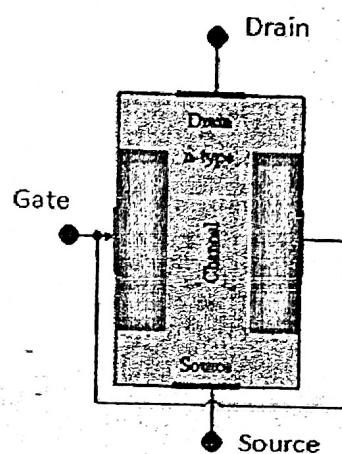


Fig.1 (ii)

A JFET is a three terminal semiconductor device in which current conduction is by one type of carrier i.e. electrons or holes.

The current conduction is controlled by means of an electric field between the gate and the conducting channel of the device.

The JFET has high input impedance and low noise level.

## Construction Details:

A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides as shown in fig.1.

The bar forms the conducting channel for the charge carriers.

The two pn junctions forming diodes are connected internally and a common terminal called gate is taken out.

Other terminals are source and drain taken out from the bar as shown in fig.1.

Thus a JFET has three terminals such as , gate (G), source (S) and drain (D).

If the bar is of p-type, it is called p-channel JFET as shown in fig.1(i) and if the bar is of n-type, it is called n-channel JFET as shown in fig.1(ii).

### JFET working

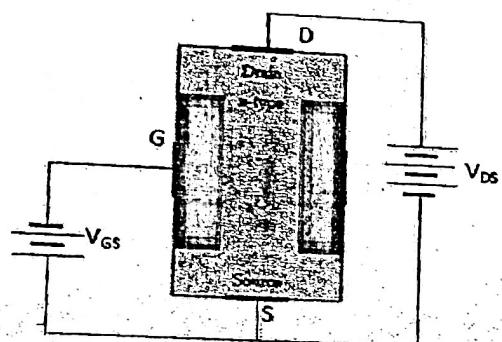


Fig.2 (i)

In each case, the voltage between the gate and source is such that the gate is reverse biased.

The source and the drain terminals are interchangeable.

The following points may be noted:

1. The input circuit ( i.e. gate to source) of a JFET is reverse biased. This means that the device has high input impedance.
2. The drain is so biased w.r.t. source that drain current  $I_D$  flows from the source to drain.
3. In all JFETs, source current  $I_S$  is equal to the drain current i.e  $I_S = I_D$ .

## Principle and Working of JFET

### Principle of JEFT

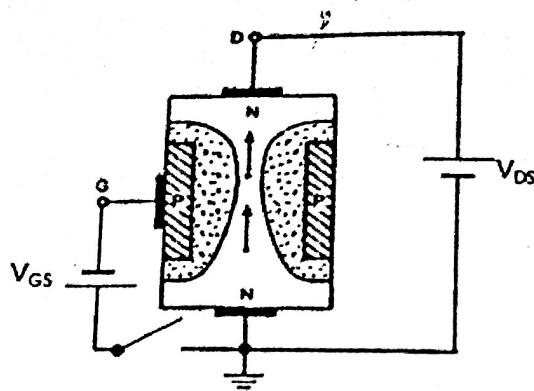


Fig.3 (i)

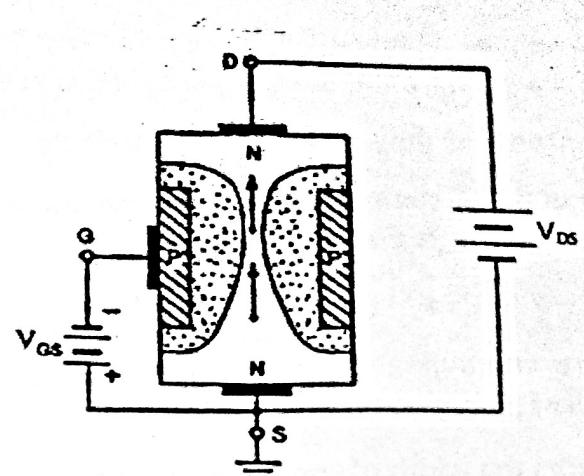


Fig.3 (ii)

Fig.3 shows the circuit of n-channel JFET with normal polarities.

- The two pn junctions at the sides form two depletion layers.
- The current conduction by charge carriers (i.e. electrons) is through the channel between the two depletion layers and out of the drain.
- The width and hence resistance of this channel can be controlled by changing the input voltage  $V_{GS}$ .
- The greater the reverse voltage  $V_{GS}$ , the wider will be the depletion layer and narrower will be the conducting channel.
- The narrower channel means greater resistance and hence source to drain current decreases.
- Reverse will happen when  $V_{GS}$  decreases.

Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage  $V_{GS}$ .

In other word, the magnitude of drain current  $I_D$  can be changed by altering  $V_{GS}$ .

### Working of JFET

The working of JFET can be explained as follows:

**Case-i:**

When a voltage  $V_{DS}$  is applied between drain and source terminals and voltage on the gate is zero as shown in fig.3(i), the two pn junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of the depletion layers determines the width of the channel and hence current conduction through the bar.

#### Case-ii:

When a reverse voltage  $V_{GS}$  is applied between gate and source terminals, as shown in fig.3(ii), the width of depletion layer is increased.

This reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from source to drain is decreased.

On the other hand, when the reverse bias on the gate is decreased, the width of the depletion layer also decreases.

This increases the width of the conducting channel and hence source to drain current.

A p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and polarities of  $V_{GS}$  and  $V_{DS}$  are reversed.

#### Schematic Symbol of JFET

Fig.4 shows the schematic symbol of JFET.

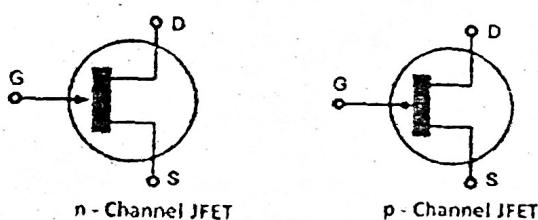
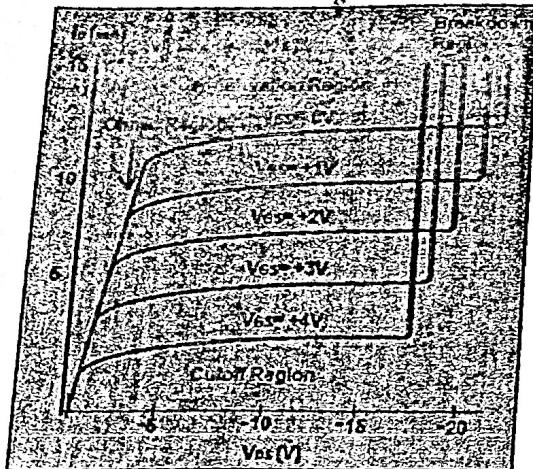


Fig.4

#### JFET Characteristics

The JFET characteristics can be studied for both N-channel and P-channel as discussed below:

#### N-Channel JFET Characteristics



P-Channel JFET Characteristics

### Parameters of JFET:

Main parameters of a JFET are (i) a.c. drain resistance (ii) transconductance (iii) amplification factor.

**a.c. drain resistance (rd).** Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a JFET. It may be defined as follows :

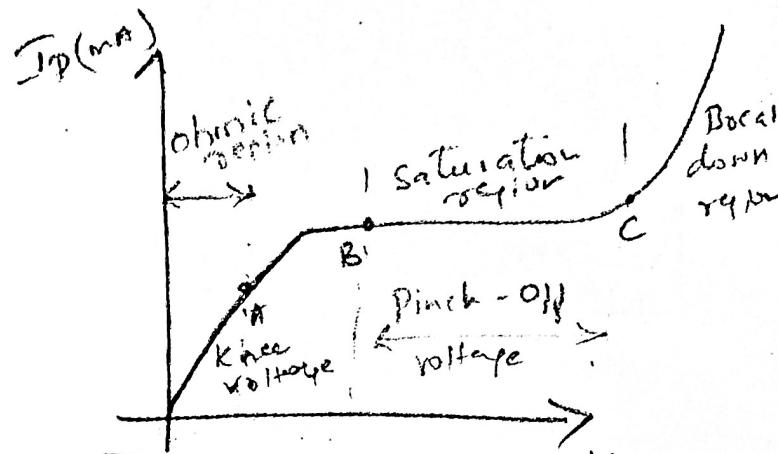
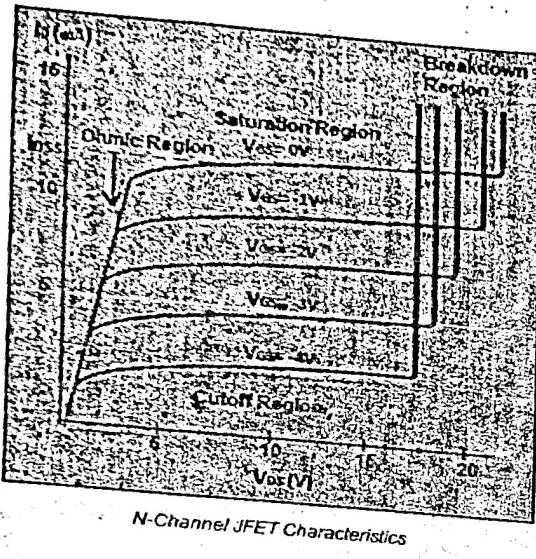
*It is the ratio of change in drain-source voltage ( $\Delta V_{DS}$ ) to the change in drain current ( $\Delta I_D$ ) at constant gate-source voltage i.e.*

$$\text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA; then,

$$\text{a.c. drain resistance, } r_d = \frac{2 \text{ V}}{0.02 \text{ mA}} = 100 \text{ k}\Omega$$

The N-channel JFET characteristics or transconductance curve is shown in the figure below which is graphed between drain current and gate-source voltage. There are multiple regions in the transconductance curve and they are ohmic, saturation, cutoff, and breakdown regions.



pt A  $\rightarrow$  knee voltage (Ohmic region)  $V_{DS} (V)$   
 $I_D$  & it is linear

pt BC  $\rightarrow$  Pinch off voltage (saturation)  
 ON (FET acts as amplifier)

### Ohmic Region

The only region in which transconductance curve shows linear response and drain current is opposed by the JFET transistor resistance is termed as Ohmic region.

### Saturation Region

In the saturation region, the N-channel junction field effect transistor is in ON condition and active, as maximum current flows because of the gate-source voltage applied.

### Cutoff Region

In this cutoff region, there will be no drain current flowing and thus, the N-channel JFET is in OFF condition.

### Breakdown Region

If the VDD voltage applied to the drain terminal exceeds the maximum necessary voltage, then the transistor fails to resist the current and thus, the current flows from drain terminal to source terminal. Hence, the transistor enters into the breakdown region.

### P-Channel JFET Characteristics

The P-channel JFET characteristics or transconductance curve is shown in the figure below which is graphed between drain current and gate-source voltage. There are multiple regions in the transconductance curve and they are ohmic, saturation, cutoff, and breakdown regions.

(ii) Transconductance ( $g_{fs}$ ). The control that the gate voltage has over the drain current is measured by transconductance  $g_{fs}$  and is similar to the transconductance  $g_m$  of the tube. It may be defined as follows :

*It is the ratio of change in drain current ( $\Delta I_D$ ) to the change in gate-source voltage ( $\Delta V_{GS}$ ) at constant drain-source voltage i.e.*

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a JFET is usually expressed either in mA/volt or micromho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then,

$$\begin{aligned}\text{Transconductance, } g_{fs} &= \frac{0.3 \text{ mA}}{0.1 \text{ V}} = 3 \text{ mA/V} = 3 \times 10^{-3} \text{ A/V or mho or S (siemens)} \\ &= 3 \times 10^{-3} \times 10^6 \mu \text{ mho} = 3000 \mu \text{ mho (or } \mu\text{S})\end{aligned}$$

(iii) Amplification factor ( $\mu$ ). *It is the ratio of change in drain-source voltage ( $\Delta V_{DS}$ ) to the change in gate-source voltage ( $\Delta V_{GS}$ ) at constant drain current i.e.*

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor of a JFET indicates how much more control the gate voltage has over drain current than has the drain voltage. For instance, if the amplification factor of a JFET is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

## Relation Among JFET Parameters

The relationship among JFET parameters can be established as under :

$$\text{We know } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying the numerator and denominator on R.H.S. by  $\Delta I_D$ , we get,

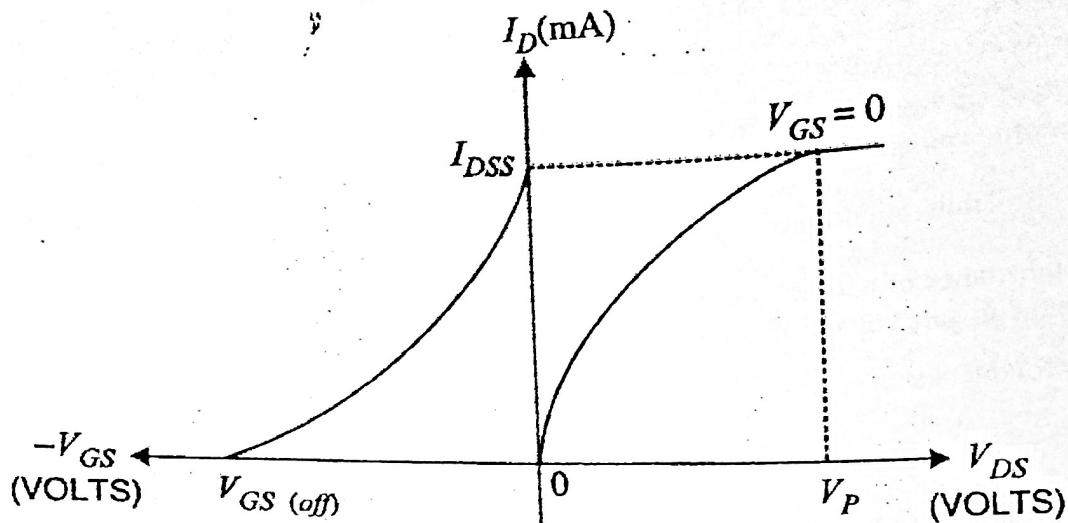
$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = r_d \times g_{fs}$$

i.e. amplification factor = a.c. drain resistance  $\times$  transconductance

## Expression for Drain Current ( $I_D$ )

The relation between  $I_{DSS}$  and  $V_p$  is shown in Fig. . We note that gate-source cut off voltage [i.e.  $V_{GS(off)}$ ] on the transfer characteristic is equal to pinch off voltage  $V_p$  on the drain characteristic i.e.



For example, if a JFET has  $V_{GS(\text{off})} = -4\text{V}$ , then  $V_P = 4\text{V}$

The transfer characteristic of JFET shown in Fig. is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

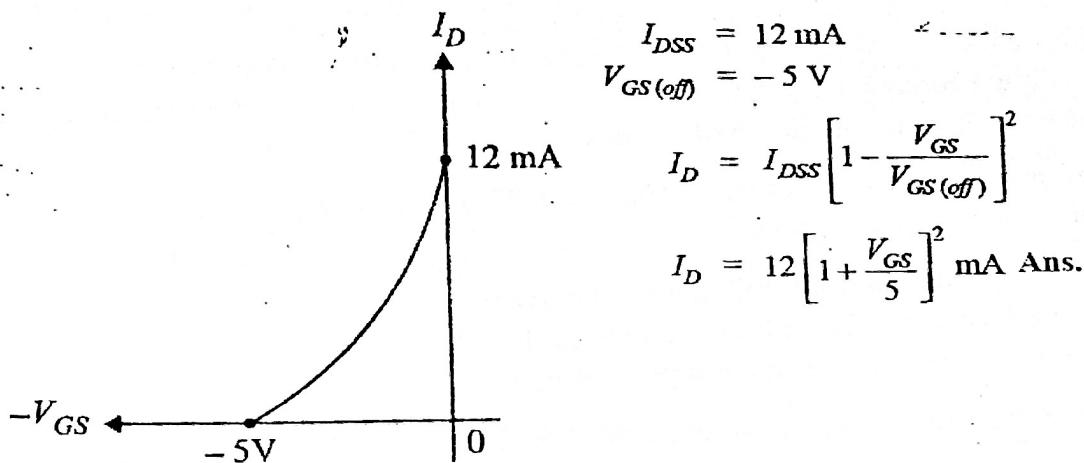
$I_D$  = drain current at given  $V_{GS}$

$I_{DSS}$  = shorted-gate drain current

$V_{GS}$  = gate-source voltage

$V_{GS(\text{off})}$  = gate-source cut off voltage

Problem 1: Fig. shows the transfer characteristic curve of a JFET. Write the equation for drain current.



Problem2: A JFET has the following parameters:  $I_{DSS} = 32 \text{ mA}$ ;  $V_{GS(\text{off})} = -8 \text{ V}$ ;  $V_{GS} = -4.5 \text{ V}$ . Find the value of drain current.

Solution.

$$\begin{aligned}
 I_D &= I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2 \\
 &= 32 \left[ 1 - \frac{(-4.5)}{-8} \right]^2 \text{ mA} \\
 &= 6.12 \text{ mA}
 \end{aligned}$$

Problem3: A JFET has a drain current of 5 mA. If  $I_{DSS} = 10 \text{ mA}$  and  $V_{GS(\text{off})} = -6 \text{ V}$ , find the value of (i)  $V_{GS}$  and (ii)  $V_P$

Solution.

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

$$5 = 10 \left[ 1 + \frac{V_{GS}}{6} \right]^2$$

or

$$1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

or

$$V_{GS} = -1.76 \text{ V}$$

(i)  $\therefore$

$$V_P = -V_{GS(\text{off})} = 6 \text{ V}$$

(ii) and

## Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

- (i) It has a very high input impedance (of the order of  $100 \text{ M}\Omega$ ). This permits high degree of isolation between the input and output circuits.
- (ii) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.
- (iii) A *JFET* has a negative temperature coefficient of resistance. This avoids the risk of thermal runaway.
- (iv) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.
- (v) A *JFET* has a smaller size, longer life and high efficiency.

In enhancement mode it does not exist initially.  
It is induced by applying a gate voltage.  
at saturation mode  
depletion mode (by depletion mode).  
greater than  $V_g$  at threshold voltage of enhancement mode.

### **Metal Oxide Semiconductor FET (MOSFET)**

A *MOSFET* is an important semiconductor device and can be used in any of the circuits covered for *JFET*. However, a *MOSFET* has several advantages over *JFET* including high input impedance and low cost of production.

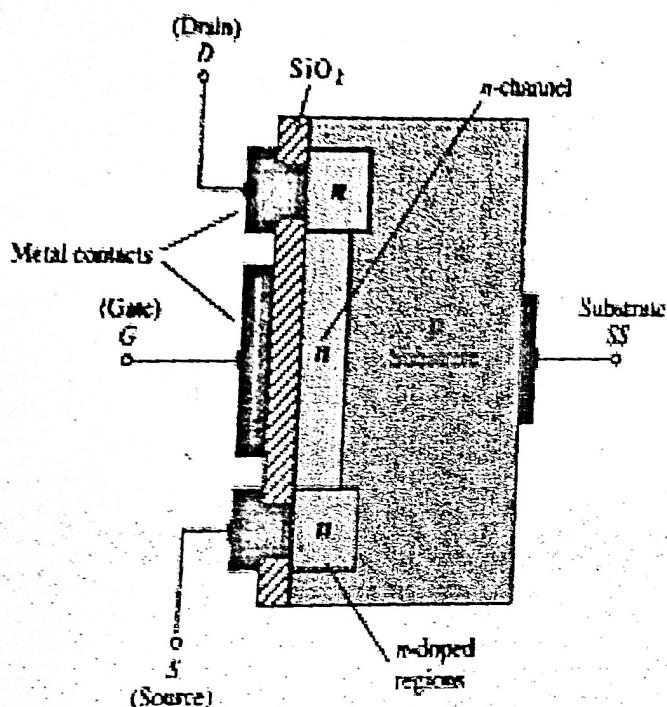
#### **Types of MOSFETs**

There are two basic types of *MOSFETs* viz.

1. Depletion-type *MOSFET* or **D-MOSFET**. The **D-MOSFET** can be operated in both the depletion-mode and the enhancement-mode. For this reason, a **D-MOSFET** is sometimes called depletion/enhancement *MOSFET*.

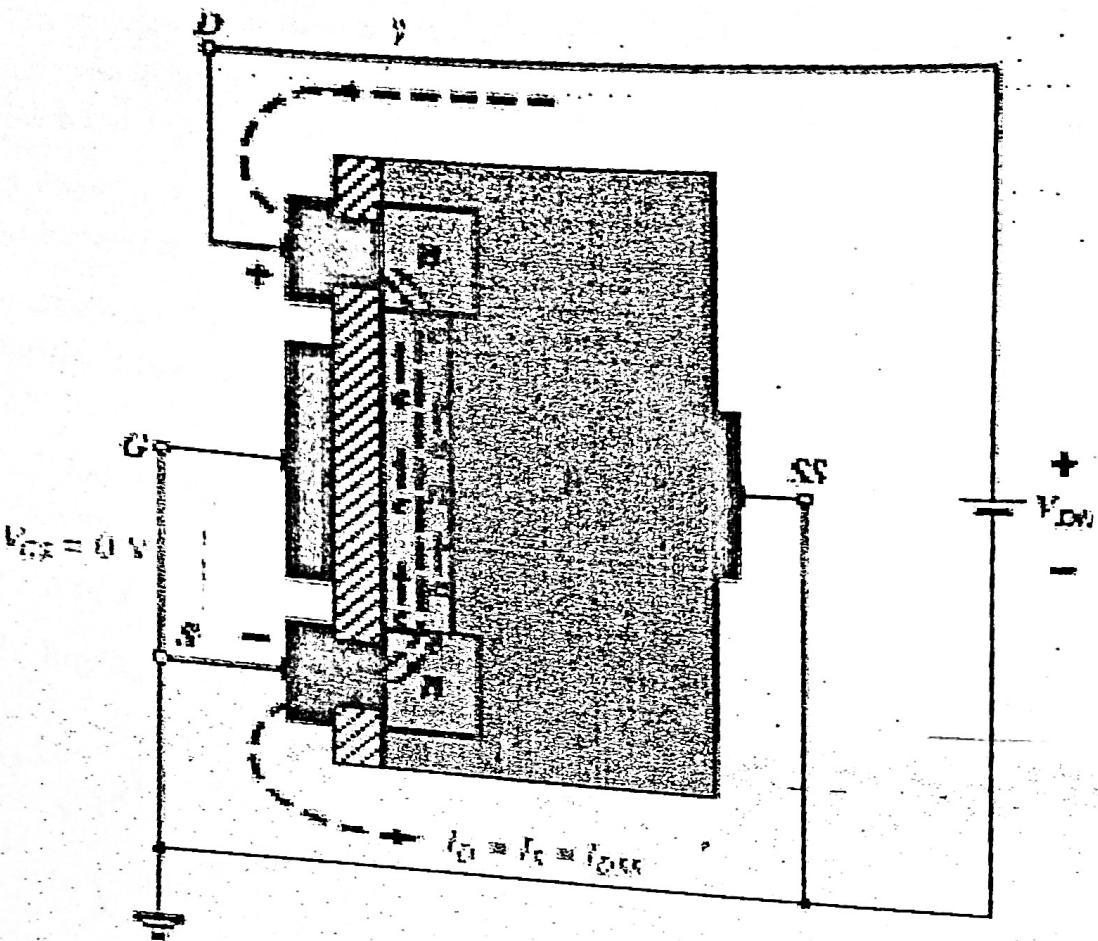
2. Enhancement-type *MOSFET* or *E-MOSFET*. The *E-MOSFET* can be operated *only* in enhancement-mode.

### DEPLETION-TYPE MOSFET



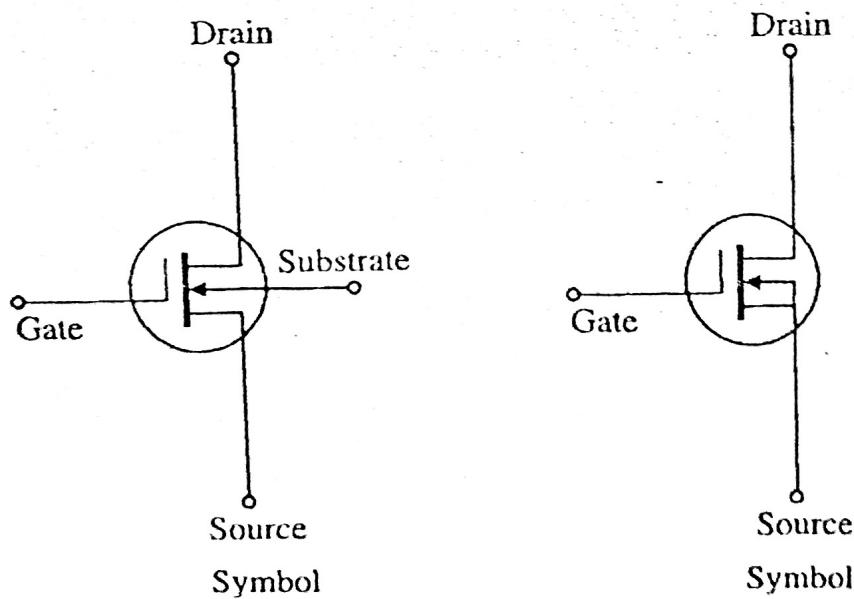
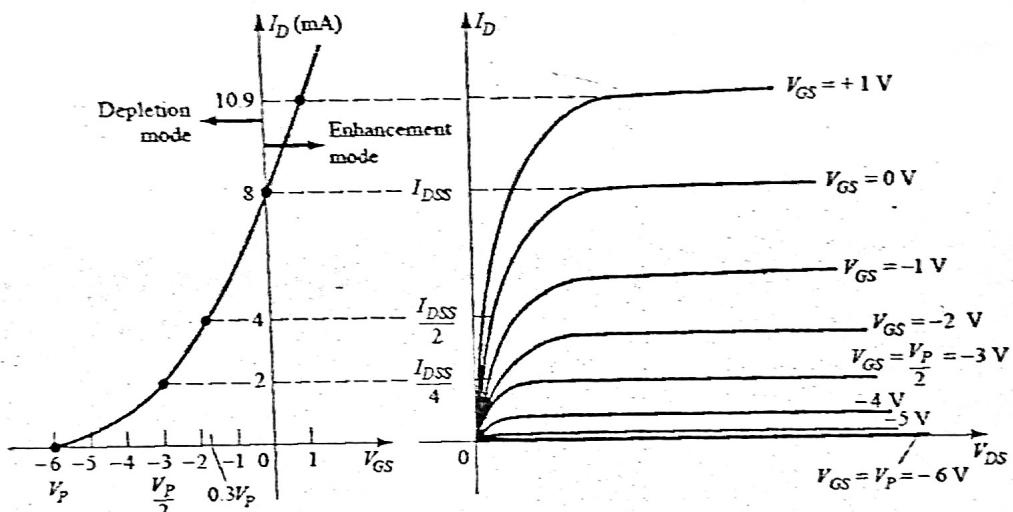
- A slab of *p*-type material is formed from a silicon base and is referred to as the substrate.
- The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the figure.
- The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO<sub>2</sub>) layer.
- SiO<sub>2</sub> is a particular type of insulator referred to as a *dielectric* that sets up opposing (as revealed by the prefix *di-*) electric fields within the dielectric when exposed to an externally applied field.
- There is no direct electrical connection between the gate terminal and the channel of a MOSFET.
- It is the insulating layer of SiO<sub>2</sub> in the MOSFET construction that accounts for the very desirable high input impedance of the device.

Basic Operation and Characteristics:



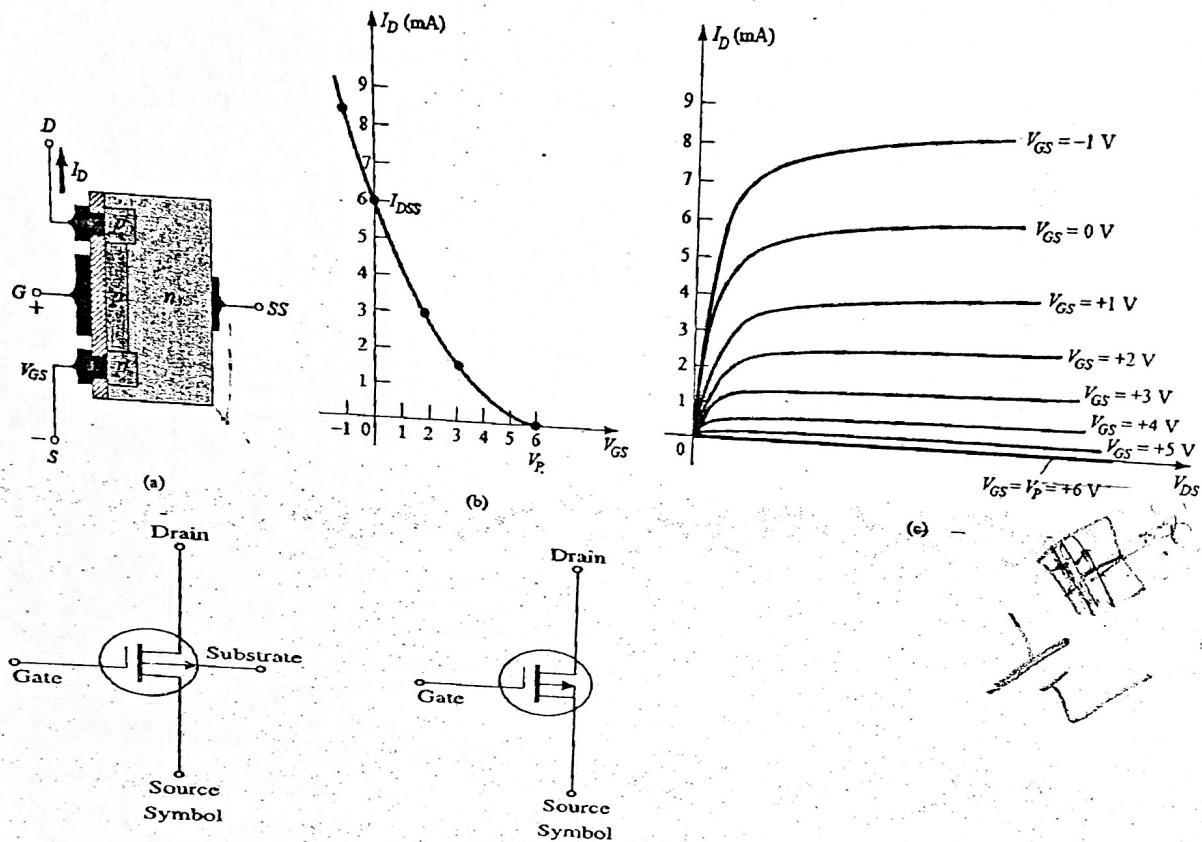
- In Fig. the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other.
- $V_{DS}$  is applied across the drain-to-sourceterminals.
- The result is an attraction for the positive potential at the drain by the freeelectrons of the n-channel and a current similar to that established through the channelof the JFET.
- Resulting maximum current is given by  $I_{DSS}$ .
- $V_{GS}$  has been set at a negative voltage such as -1 V. The negativepotential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) asshown in Fig.
- Depending on the magnitude of the negative bias established by  $V_{GS}$ , a level of recombination between electrons and holes will occur that will reducethe number of free electrons in the n-channel available for conduction.
- The resulting level of drain currentis therefore reduced with increasing negative bias for  $V_{GS}$  as shown in Fig

- for  $V_{GS} = -1$  V,  $-2$  V, and so on, to the pinch-off level of  $6$  V. The resulting levels of drain current and the plotting of the transfer curve proceeds exactly as described for the JFET.
- For positive values of  $V_{GS}$ , the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles.
- positive gate voltages on the drain or transfer characteristics is often referred to as the enhancement region, with the region between cutoff and the saturation level of  $I_{DSS}$  referred to as the depletion region.

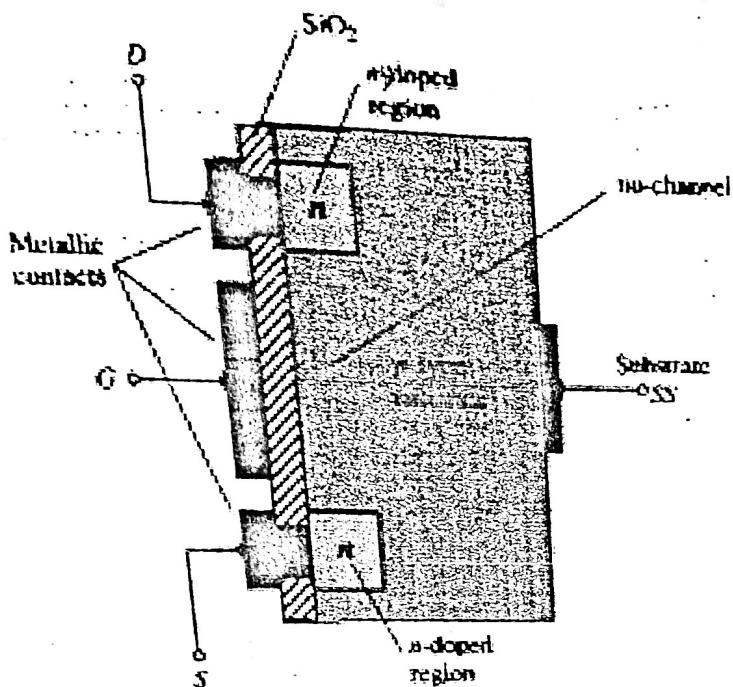


## P-Channel Depletion-Type MOSFET

$I_{DSS}/V_P$



## ENHANCEMENT-TYPE MOSFET



$V_{GS} = 0$   
 $I_D = 0$  (no channel)  
 $V_G > V_{GS}$   
 $V_{DS}$

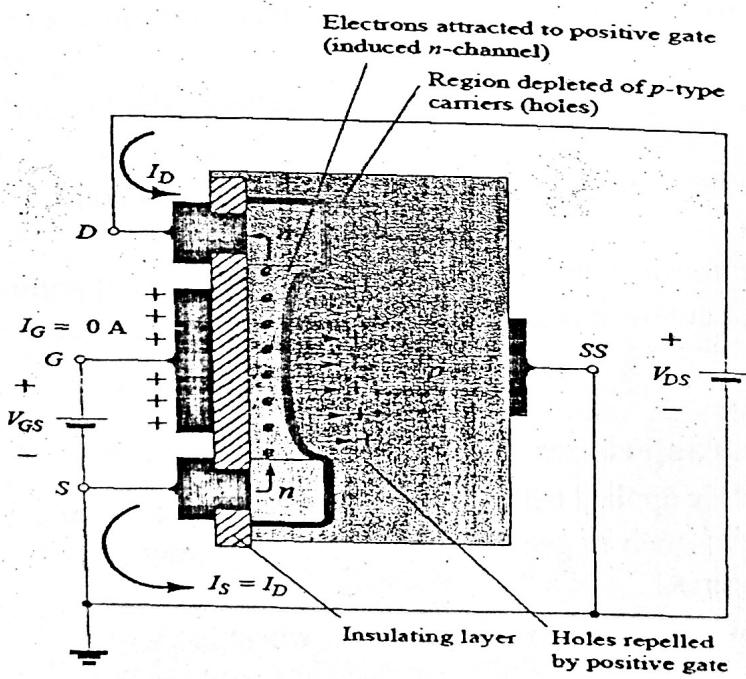
## Basic Construction

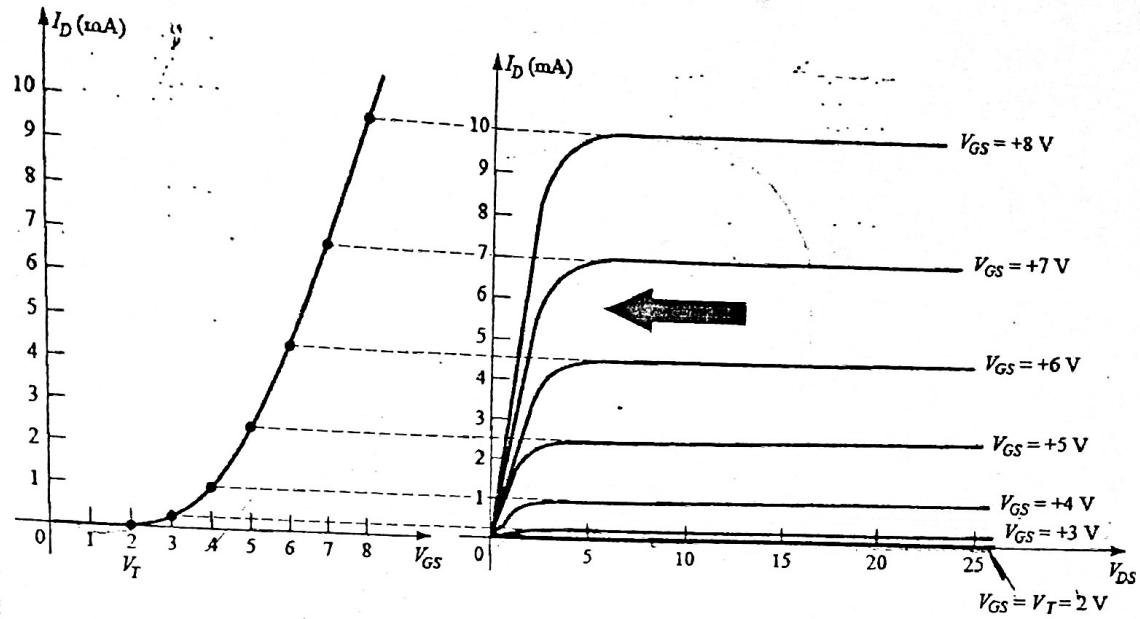
- A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate.
- The source and drain terminals are again connected through metallic contacts to *n*-doped regions.
- Two *n* channels are not connected. The absence of a channel between the two *n*-doped regions.
- This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs.
- The  $\text{SiO}_2$  layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material.

## Basic Operation and Characteristics

- If  $V_{GS}$  is set at 0 V and a voltage applied between the drain and source of the device of Fig, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively zero amperes.  
(quite different from the depletion-type MOSFET and JFET where  $I_D = I_{DSS}$ )
- Both  $V_{DS}$  and  $V_G$  have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source.

- The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO<sub>2</sub> layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure.
- Depletion region near the SiO<sub>2</sub> insulating layer void(less) of holes. However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO<sub>2</sub> layer.
- The SiO<sub>2</sub> layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal.
- As V<sub>GS</sub> increases in magnitude, the concentration of electrons near the SiO<sub>2</sub> surface increases until eventually the induced n-type region can support a measurable flow between drain and source.
- The level of V<sub>GS</sub> that results in the significant increase in drain current is called the threshold voltage and is given the symbol V<sub>T</sub>.
- As V<sub>GS</sub> is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current.





## CMOS (Complementary Metal Oxide Semiconductor)

Complementary MOSFET (CMOS) technology is widely used today to form circuits in numerous and varied applications. Today's computers CPUs and cell phones make use of CMOS due to several key advantages. CMOS offers low power dissipation, relatively high speed, high noise margins in both states, and will operate over a wide range of source and input voltages.

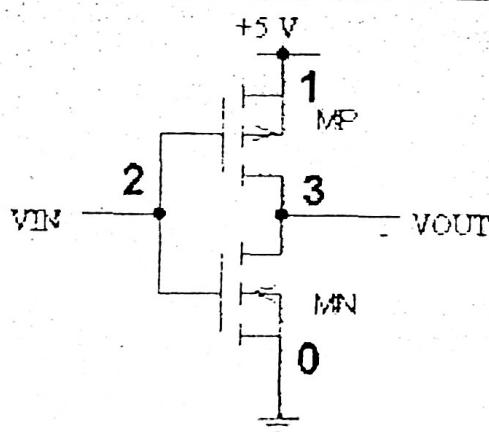


Figure 1: CMOS Inverter

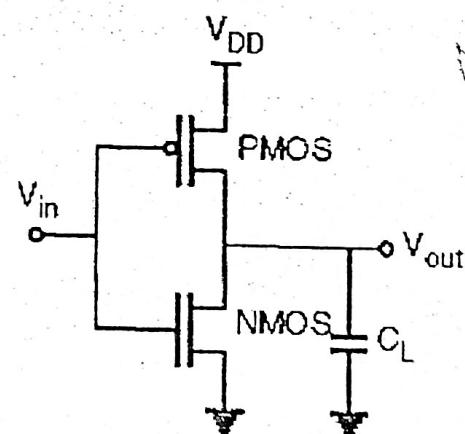
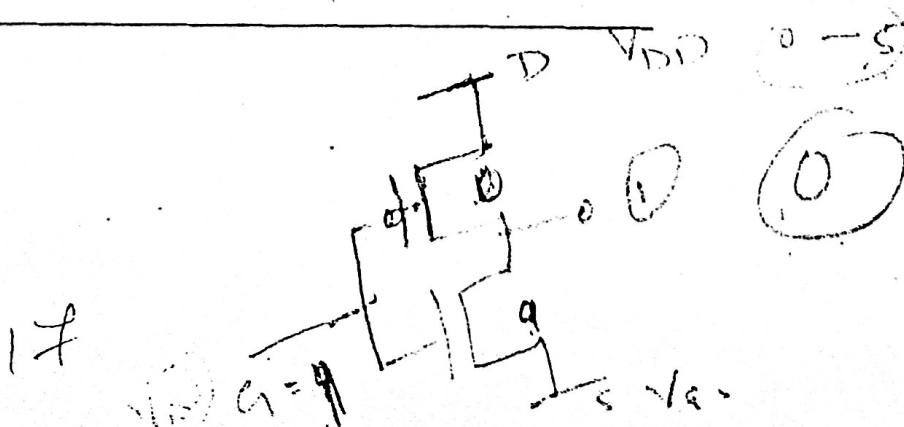


Fig CMOS-Inverter



From Figure 1, a CMOS circuit is composed of two MOSFETs. The top FET (MP) is a PMOS type device while the bottom FET (MN) is an NMOS type. The body effect is not present in either device since the body of each device is directly connected to the device's source. Both gates are connected to the input line. The output line connects to the drains of both FETs.

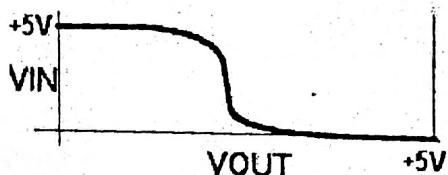
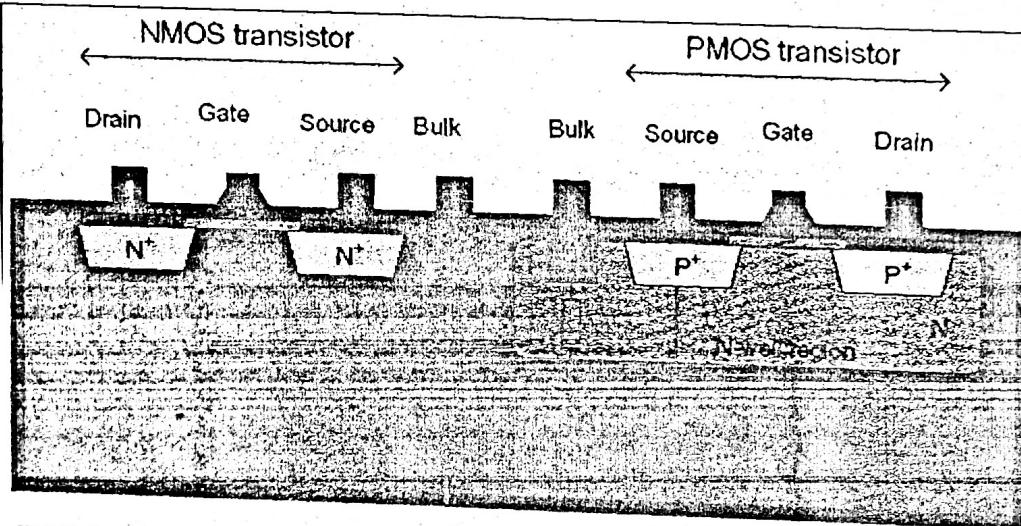


Figure 2: Basic Voltage Transfer Characteristic

Take a look at the VTC in Figure 2. The curve represents the output voltage taken from node 3. You can easily see that the CMOS circuit functions as an inverter by noting that when  $V_{IN}$  is five volts,  $V_{OUT}$  is zero, and vice versa. Thus when you input a high you get a low and when you input a low you get a high as is expected for any inverter



### NMOS

NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.