RAMAIAH
Institute of Technology

M. S. Ramaiah Institute of Technology
(Autonomous Institute, Affiliated to VTU)

Department of Computer Science and Engineering

Distributed Systems
CSE20

Sini Anna Alex

Parallel Systems

- Multiprocessor systems (direct access to shared memory, UMA model)
  - Interconnection network - bus, multi-stage sweitch
  - E.g., Omega, Butterfly, Clos, Shuffle-exchange networks
  - Interconnection generation function, routing function
- Multicomputer parallel systems (no direct access to shared memory, NUMA model)
  - bus, ring, mesh (w w/o wraparound), hypercube topologies
  - E.g., NYU Ultracomputer, CM* Conneciton Machine, IBM Blue gene
- Array processors (colocated, tightly coupled, common system clock)
  - Niche market, e.g., DSP applications

UMA vs. NUMA Models

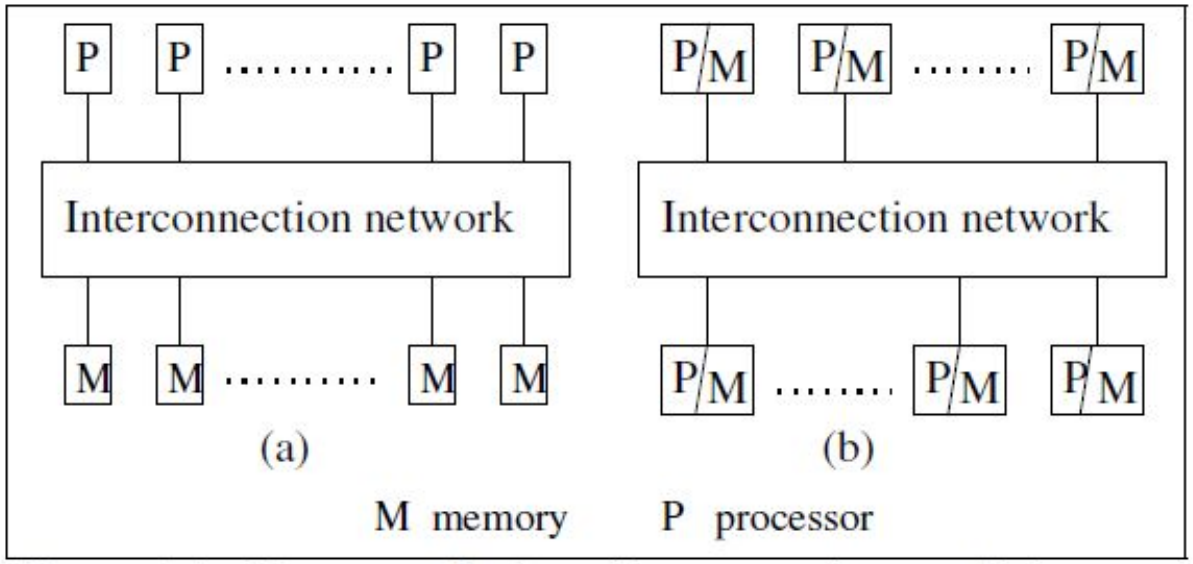

Figure 1.3: Two standard architectures for parallel systems. (a) Uniform memory access (UMA) multiprocessor system. (b) Non-uniform memory access (NUMA) multiprocessor. In both architectures, the processors may locally cache data from memory.

Omega and Butterfly Networks

Omega, Butterfly Interconnects

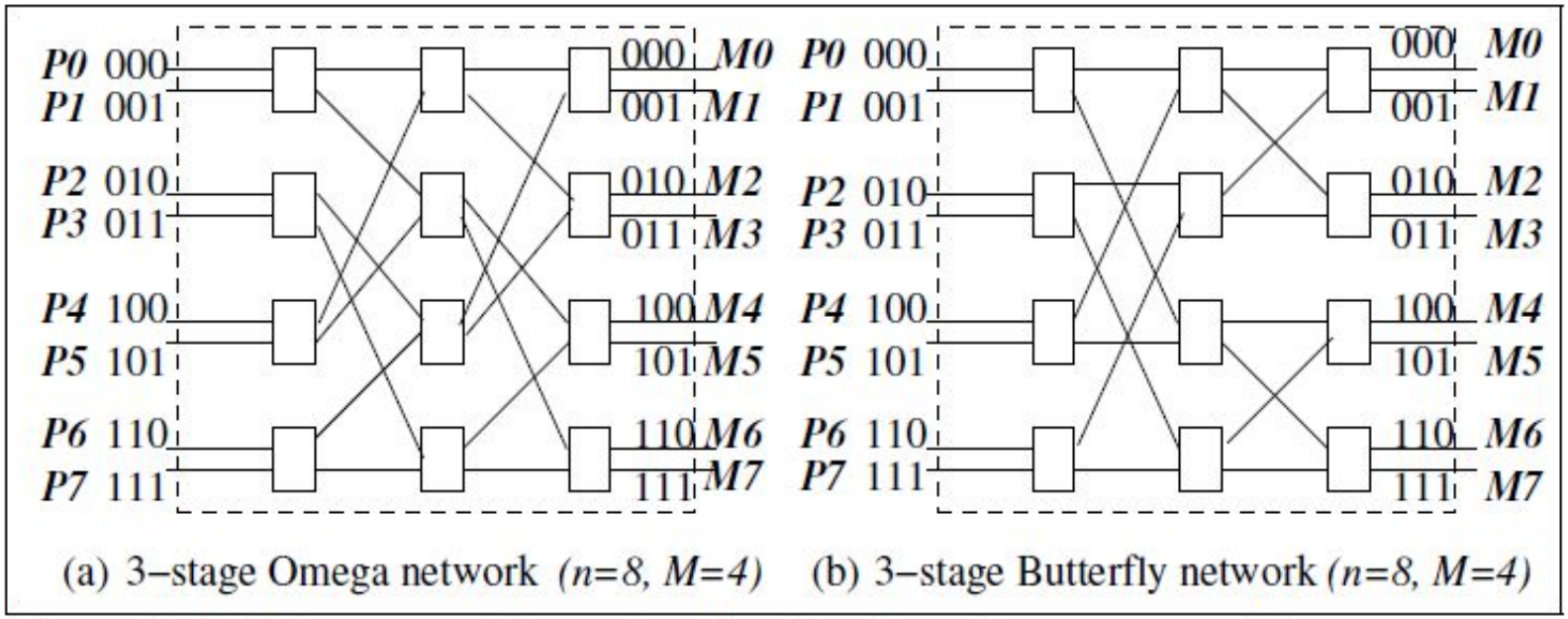

Figure 1.4: Interconnection networks for shared memory multiprocessor systems. (a) Omega network (b) Butterfly network.

Interconnection Networks

- Common Highway or interconnection network for processors in parallel to communicate.
- Based on a topology interconnection network is built
- Topology can be
  - Fixed
  - Reconfigurable(multistage interconnection network)

Omega Network

- Multistage switching network has self routing property.
- Multistage omega network used as connectors between CPUs and their shared memory, in order to decrease the probability of CPU-to –memory connection bottleneck.
- Outputs of each stages are connected to inputs of next stage using a perfect shuffle connection system

8x8 Omega Network (logical left shift)

000->000->000->000

001->010->100->001

010->100->001->010

011->110->101->011

100->001->010->100

101->011->110->101

110->101->011->110

111->111->111->111

Input	Output
0	0
1	2
2	4
3	6
4	1
5	3
6	5
7	7

Omega Network

- n processors, n memory banks
- $log\ n$ stages: with $n/2$ switches of size 2x2 in each stage
- Interconnection function: Output i of a stage connected to input j of next stage:

$$j = \begin{cases} 2i & \text{for } 0 \leq i \leq n/2 - 1 \\ 2i + 1 - n & \text{for } n/2 \leq i \leq n - 1 \end{cases}$$

- Routing function: in any stage s at any switch:
  to route to dest. j,
  if $s + 1$th MSB of $j = 0$ then route on upper wire
  else [$s + 1$th MSB of $j = 1$] then route on lower wire

Omega Network using Routing function

Building 8X8 Omega Network using Routing Function