16/10/21

Unit 3

Combinational circuit	Sequential
1) Doesn't depend on past input and output	1) Depends on past inputs
2) No feedback circuit	2) Feedback ckt is present
3) No memory	3) Memory is present.
4) Speed is more	4) speed is less
5) Easy to design.	5) complicate d design.
eg: Adders, encoders	eg: Latches . . . .

Latch: Basic component of flipflop.

→ stores only one bit (0 or 1).

→ level sensitive

flipflop:

→ edge sensitive

→ o/p changes only when clock signal is present.

SR NOR latch:

S=0 R=1 Q=0 $\bar{Q}$=1 (Reset)

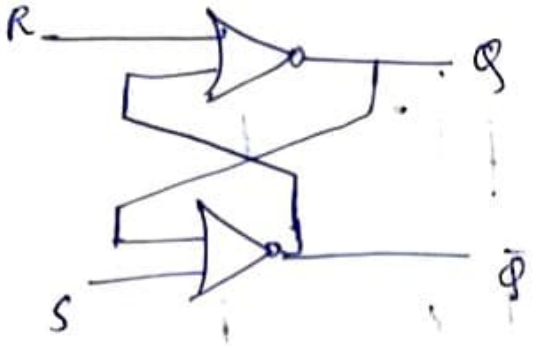
S=1 R=0 Q=1 $\bar{Q}$=0 (Set)

S=0 R=0 Q=1 $\bar{Q}$=0

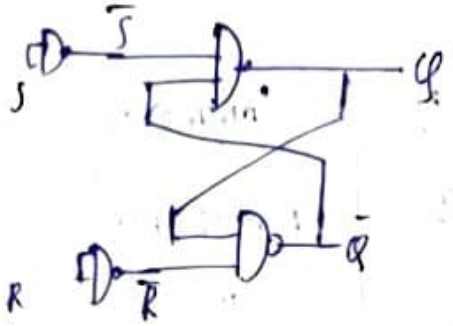
S=0 R=0 Q=0 $\bar{Q}$=1 (No change)

S=1 R=1 Q=$\bar{Q}$=0 (Invalid state)

SR NOR gate latch:



SR NAND latch:



$S = 0 \quad R = 0 \quad Q = \bar{Q}$

$S = 1 \quad R = 0 \quad Q = 1 \quad \bar{Q} = 0$

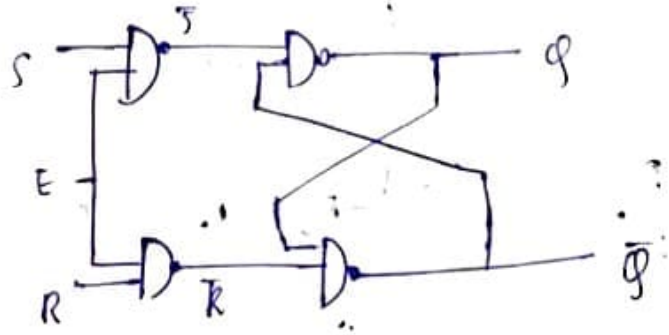
$S = 0 \quad R = 1 \quad Q = 0 \quad \bar{Q} = 1$

$S = 1 \quad R = 1 \quad Q = 1 \quad \bar{Q} = 1$

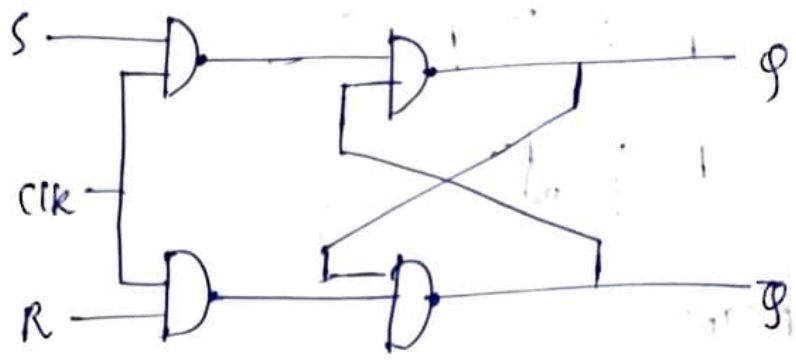
Gated latch (enable input for NAND latch)

Active high, E = 1

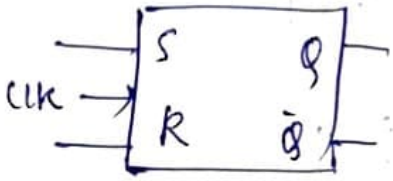
Active low, E = 0



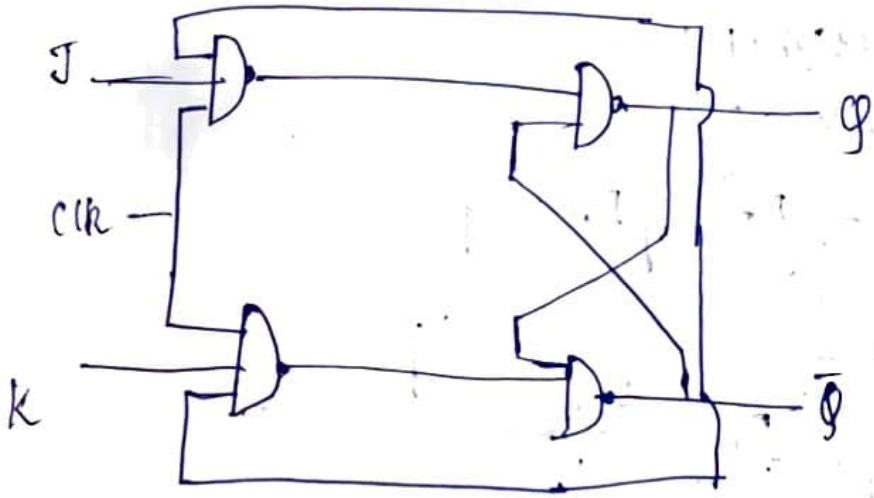
SR flip flop:

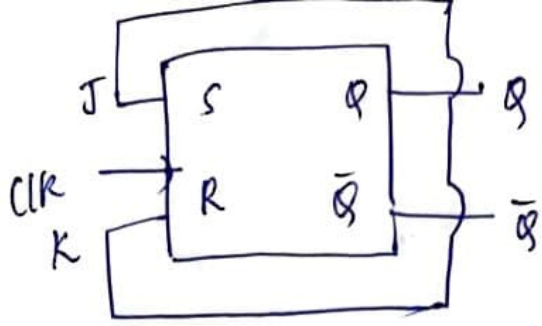


Clk	S	R	Q	$\bar{Q}$	Comments
0	x	x	Q	$\bar{Q}$	No change
1	0	0	Q	Q	"
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	0	0	Invalid.



JK flip flop:

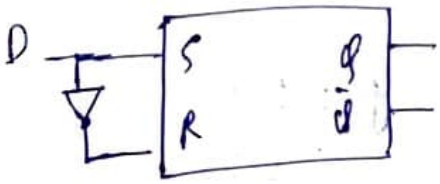




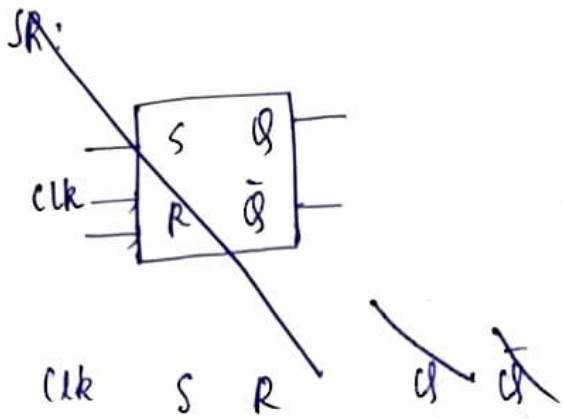
clk	J	K	Q	$\bar{Q}$	Comments
0	x	x	Q	$\bar{Q}$	NC
1	0	0	Q	$\bar{Q}$	"
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\bar{Q}$	Q	Toggling

D flipflop:

D → delay or data



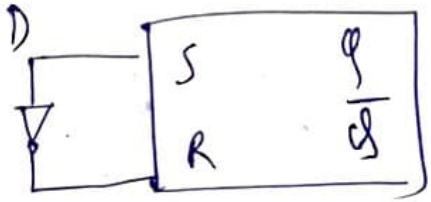
Flip flop:



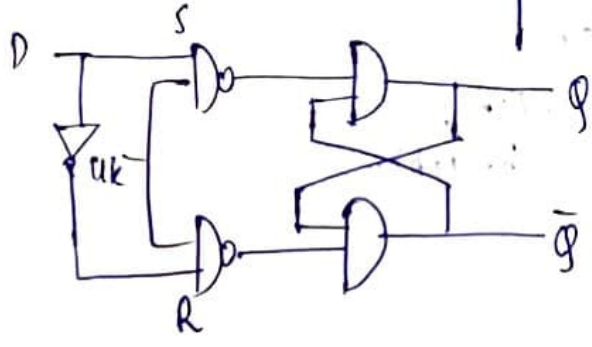
To avoid racing condition:

* $T/2$ < propagation delay of the flip flop
* Master slave flip flop
* Edge triggering flip flop.

D flip flop | data flip flop:

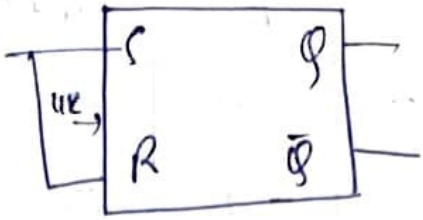


Clk	D	Q	$\bar{Q}$
0	X	Q	$\bar{Q}$
1	0	0	1
1	1	1	0



T flip flop:

T → toggling



Clk	T	Q	$\bar{Q}$
0	x	Q	$\bar{Q}$
1	0	Q	$\bar{Q}$
1	1	$\bar{Q}$	Q

characteristic table / excitation table:

→ Defines the behaviour of the flip flop. → Characteristic table

→ Excitation table - shows what i/p's necessary to generate a given o/p.

For SR flip flop:

→ Truth table:

Clk	S	R	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid.

Characteristic table: → write from truth table.

Q_n	S	R	Q_{n+1}	
0	0	0	0	} $Q_n = 0$ then $Q_{n+1} = 0$
0	0	1	0	
0	1	0	1	} see 10 and 11 in TT
0	1	1	X	
1	0	0	1	} $Q_n = Q_{n+1}$
1	0	1	0	
1	1	0	1	
1	1	1	X	

Excitation table: (write from characteristic table check for Q_n and Q_{n+1} value and write corresponding S and R value)

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Characteristic eqn

	00	01	11	10
0	0	0	X	1
1	1	0	X	1

$$Q_{n+1} = S + Q_n R$$

2) For JK flip flop:

Truth table:

Clk	J	K	Q	$\bar{Q}$	Q_{n+1}
0	X	X	Q	$\bar{Q}$	Q_n
1	0	0	Q	$\bar{Q}$	Q_n
1	0	1	0	1	0
1	1	0	1	0	1
1	1	1	$\bar{Q}$	Q	$\bar{Q}_n$

Characteristic table

Q_n	J	K	Q_{n+1}	
0	0	0	0	previous state
0	0	1	0	
0	1	0	1	
0	1	1	1	complement of prev state
1	0	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	

excitation table:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

3) for D flipflop:

T.T.:

Clk	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

Characteristic table:

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Q_n \ D	0	1
0	0	(1)
1	0	(1)

$Q_{n+1} = D$ //

4) T flip flop:

Clk	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$\bar{Q}_n$

Charac table:

Clk = 1

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table:

Q	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_n \ T	0	1
0	0	(1)
1	(1)	0

$Q_{n+1} = \bar{Q}_n T + Q_n \bar{T}$

$= Q_n \oplus T$ //

* Convert JK flip flop to D flip flop:

Solution: Step 1 - available → JK
required → D

Step 2 - Characteristic table → for required f/f

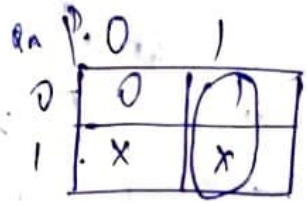
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Step 3 - excitation table for available f/f

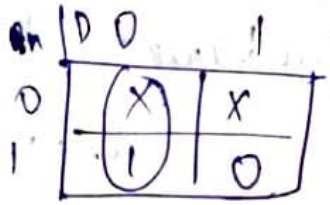
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Step 4 - Truth table (combine the characteristic table and excitation table)

Q_n	D	Q_{n+1}	J	K
0	0	0	0	x
0	1	1	1	x
1	0	0	x	1
1	1	1	x	0



$J = D$



$K = \bar{D}$

Convert SR flip flop to JK flip flop:

Step 1: available → SR flip flop
required → JK flip flop

Step 2: Characteristic table for JK flip flop.

Q_n	J	K	Q_{n+1}	
0	0	0	0	(previous)
0	0	1	0	
0	1	0	1	
0	1	1	1	
1	0	0	1	(previous)
1	0	1	0	
1	1	0	1	
1	1	1	0	

Step 3: excitation table for SR flip flop

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Step 4: Truth table (combine step 2 and 3)

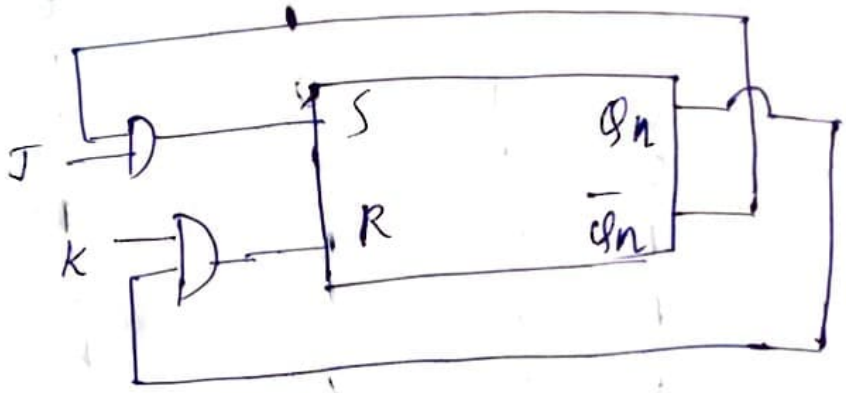
Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

Q_n \ JK	0	0	1	1
0	0	0	1	1
x	0	0	0	x

$S = \bar{Q}_n J$

x	x	0	0
0	1	1	0

$R = Q_n K$



Convert SR f/f to T flip flop:

Step 1: available - SR
required: T flip flop

Step 2: Characteristic for req (T f/f):

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Step 3: Excitation table for SR:

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Step 4:

Q_n	T	Q_{n+1}	S	R
0	0	0	0	x
0	0	0	0	x
0	1	1	1	0
0	1	1	x	0
1	0	0	0	1
1	0	0	x	0
1	1	1	0	x
1	1	1	0	x

write characteristic table from step 2 and add S and R values according to Q_n, Q_{n+1} → from (step 2)

Q_n	T	Q_{n+1}	S	R
0	0	0	0	x
0	1	1	1	0
1	0	1	x	0
1	1	0	0	1

Q_n \ T	0	1
0	0	(1)
1	x	0

$\bar{Q}_n T = S$

Q_n \ T	0	1
0	x	0
1	0	(1)

$Q_n T = R$

Convert T f/f to data f/f:

Step1: available : T f/f
required : D f/f

Step2: characteristic table for D f/f:

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Step3:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step4:

write step2 table as it is and add T column of step3

Q_n	D	Q_{n+1}	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

Q_n \ D	0	1
0	0	1
1	1	0

$T = \bar{Q_n} D + Q_n \bar{D}$

$T = Q_n \oplus D$ //

g) Convert JK to D

g) Convert D to SR b/b

g) TK to T (J=T, K=T → Ans)

g) JK to D

Step1: available → JK b/b
required → D b/b

Step2: characteristic table for D b/b:

q_n	D	q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Step3: excitation table for JK b/b:

q_n	q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step4:

q_n	D	q_{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

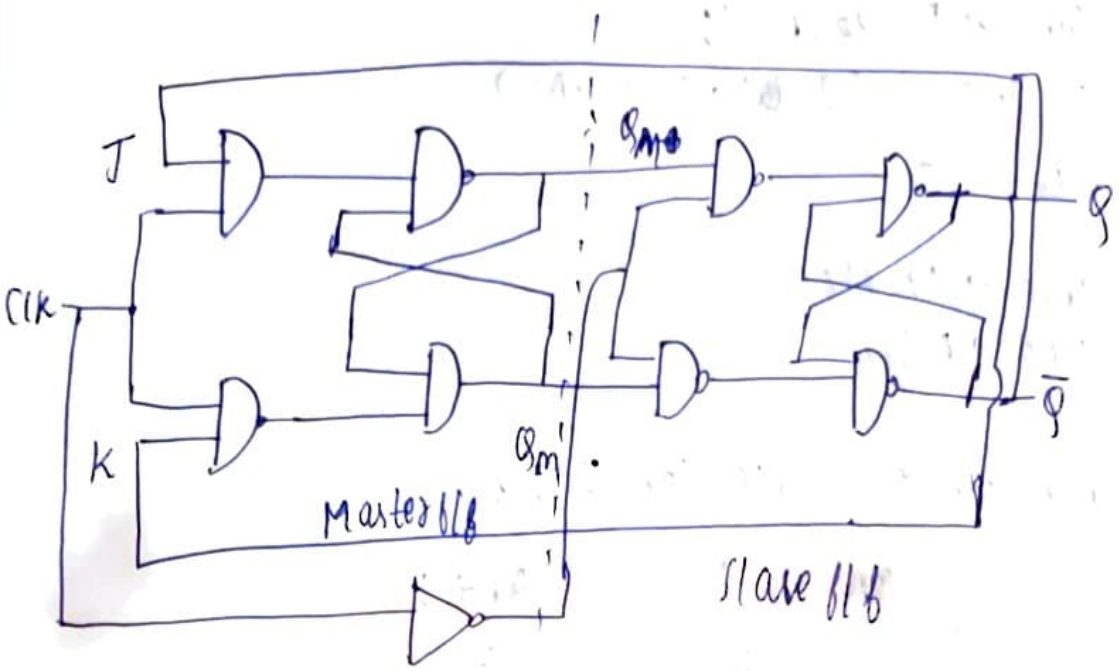
q_n \ D	0	1
0	0	1
1	X	X

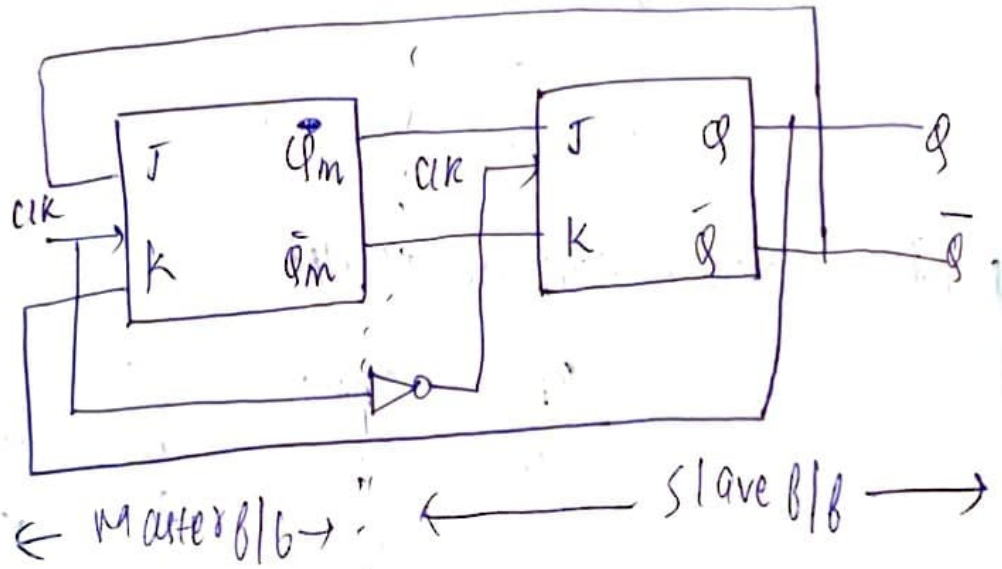
J = D

q_n \ D	0	1
0	X	X
1	1	0

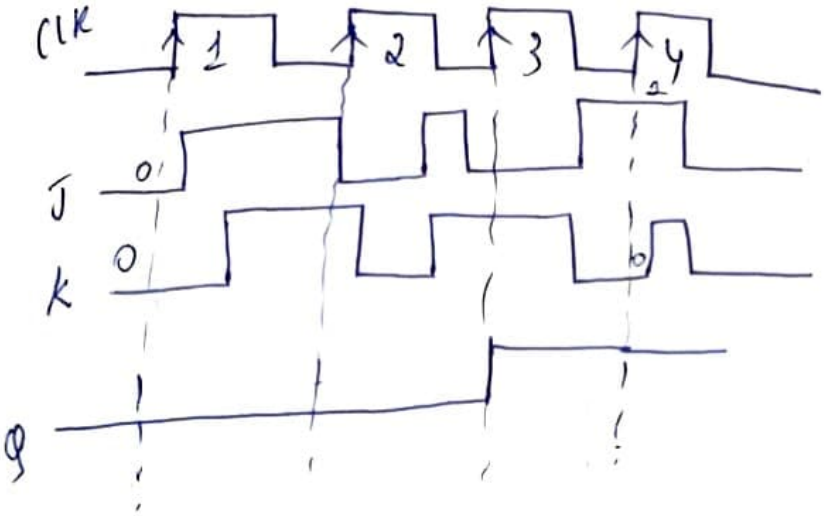
K = $\bar{D}$

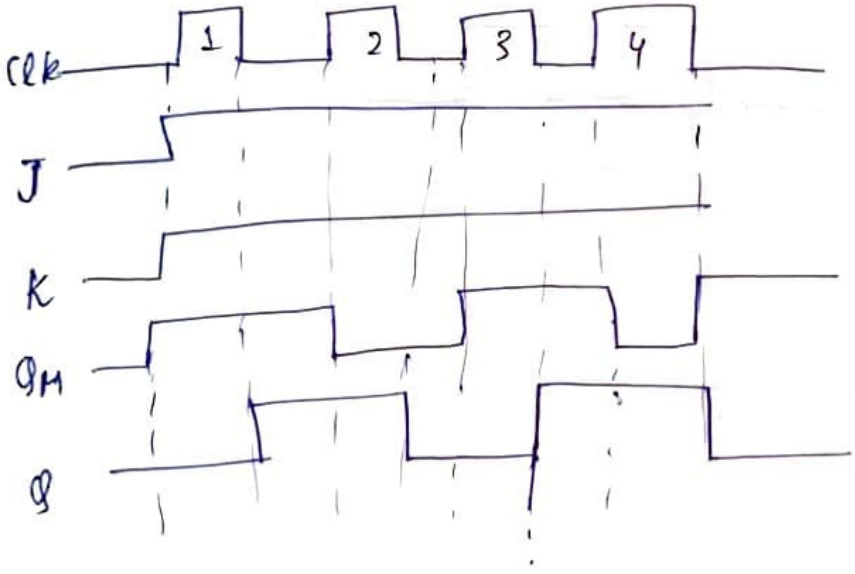
Master slave JK flipflop:



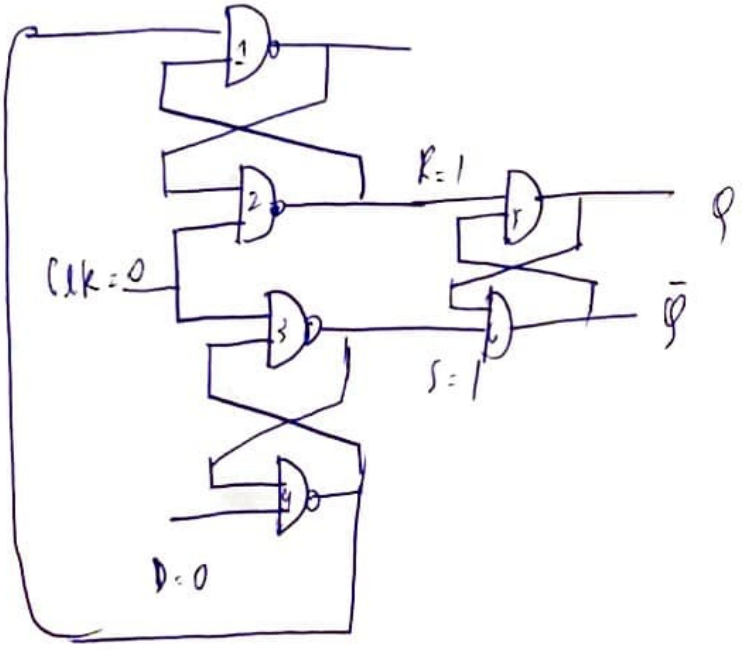


CLK	J	K	Q	$\bar{Q}$
0	x	x	Q	$\bar{Q}$
1	0	0	Q	$\bar{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\bar{Q}$	Q

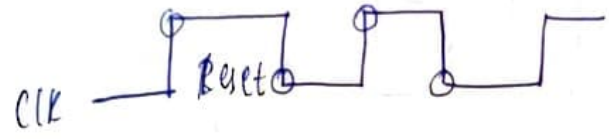




Edge triggered D flip flop :



Clk	D	R	S	Q_{n+1}	Comment
0	0	1	1	Q	NC
0	1	1	1	Q	NC
1	0	1	0	0	Reset
0	X	1	1	1	NC
1	1	0	1	1	Set
1	1	1	0	0	Reset



Registers:

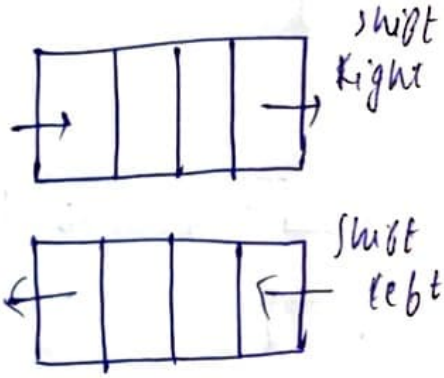
⇓

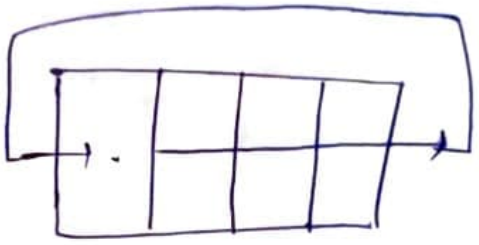
Group of flip flops, to increase the storage capacity.

N bit register consists N flip flops ⇒ capable of storing n bit words.

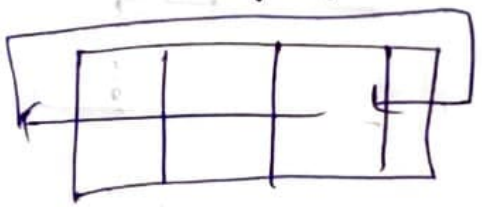
Registers

- Depending on i/p and o/p
  - SISO
  - SIPO
  - PIPO
  - PISO
- depending on application
  - shift registers
  - storage registors.
- Data format
  - serial
  - parallel



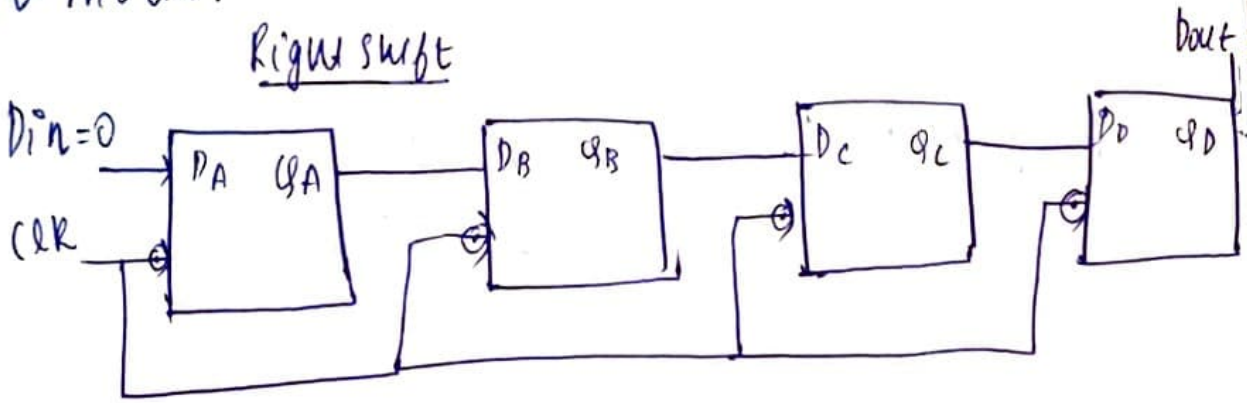


Shift right & rotate



Shift left & rotate.

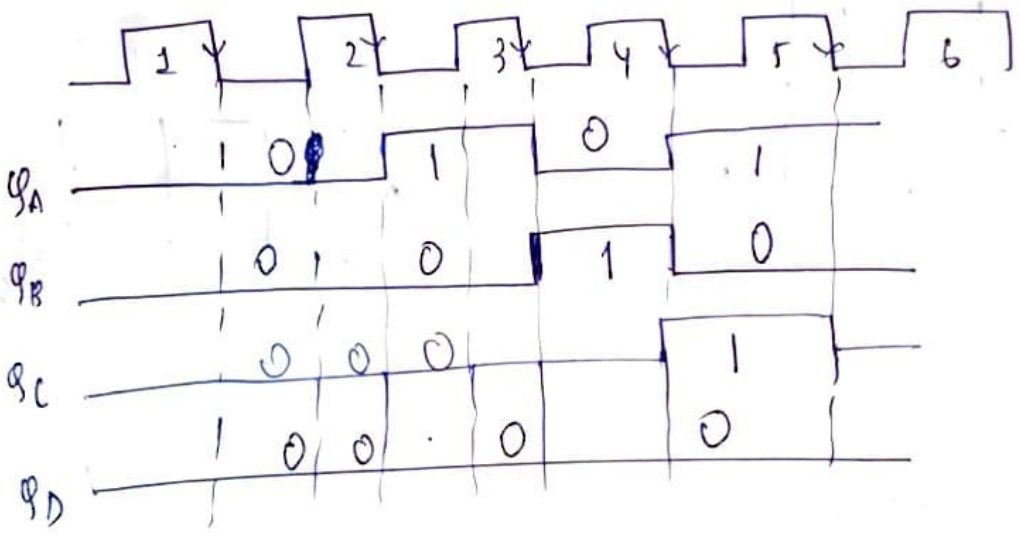
1) SISO mode:



	q_A	q_B	q_C	q_D
Initially	0	0	0	0
Clk 1	0	0	0	0
Clk 2	1	0	0	0
Clk 3	0	1	0	0
4	1	0	1	0
5				1
6				0
7				1

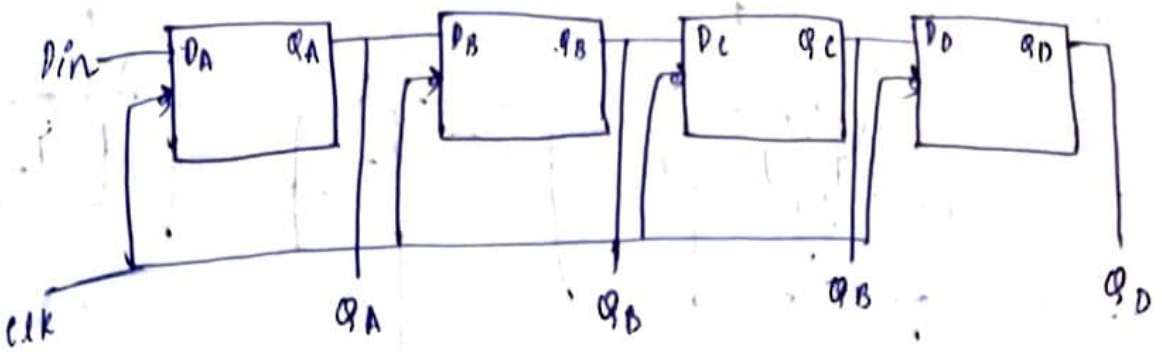
Dout: 1 0 1 0

SISO → requires 7 clock pulse for 4 bit.



Assignment: Design SISO left shift.

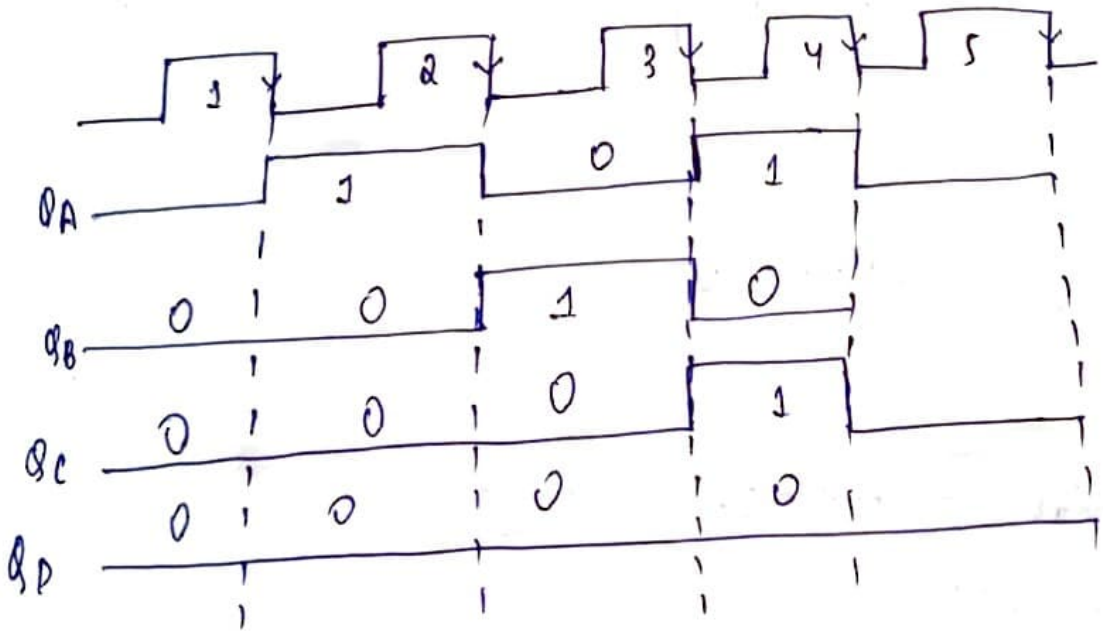
Serial in parallel out (SIPO)



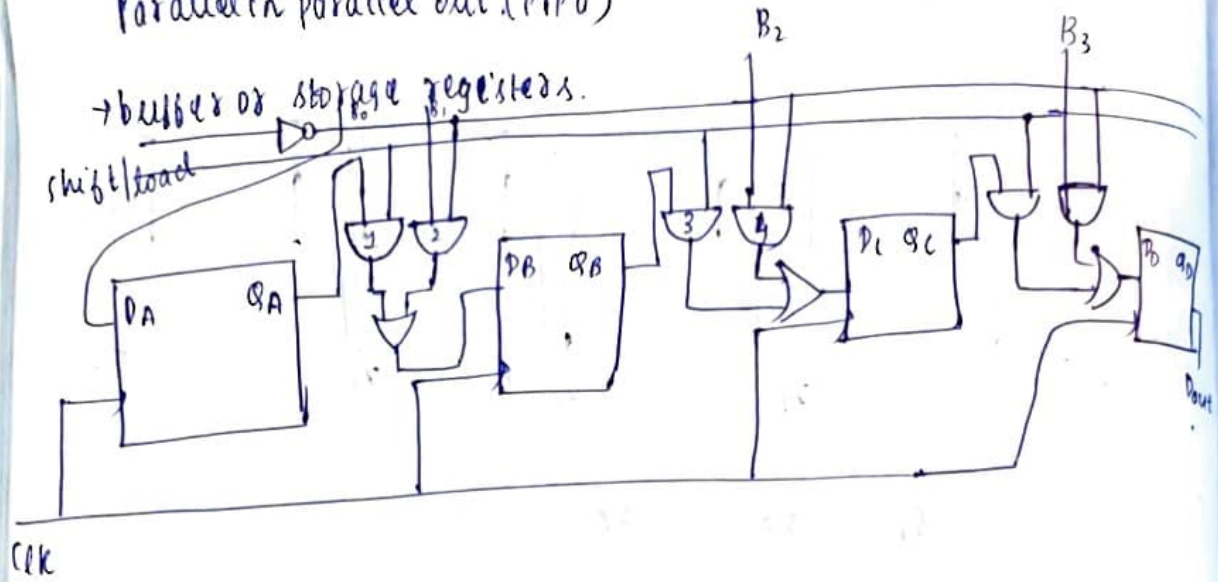
	Q_A	Q_B	Q_C	Q_D
	0 →	0 →	0 →	0
CLK-1	0 →	0 →	0 →	0
2	1 →	0 →	0 →	0
3	0 →	1 →	0 →	0
4	(1)	(0)	(1)	(0)

1010

4 clock pulses for SIPO.



Parallel in parallel out : (PIPO)



load mode : 1 0 1 0
B_0 B_1 B_2 B_3

shift = 0
$\longrightarrow B_0 = 1$

And ① → 0
② → B_1
} OR, $B_1 = 0$

To perform PIPO make shift = 0, load the data.

And ③ → 0
⑨ → B_2
} OR → $B_2 = 1$

And ⑤ → 0
⑥ → B_3
} OR → $B_3 = 0$

→ ~~Make shift = 0, load data as 1010~~

Shift 0 or all 1

When shift = 0, load operation

· shift = 0, serial operation

AND ① 0
② $B_1 = 1$
} $B_1 = 1$

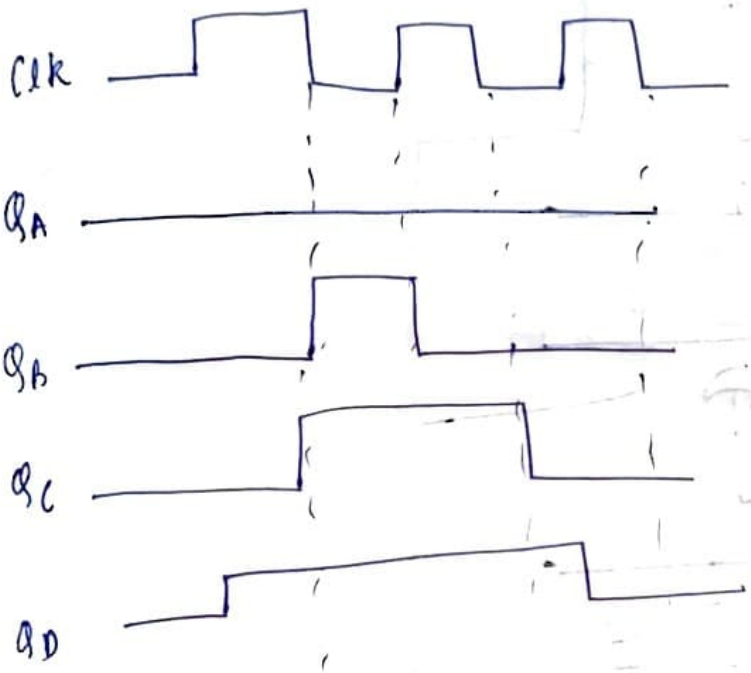
AND

③ 0 } $R_2 = 1$

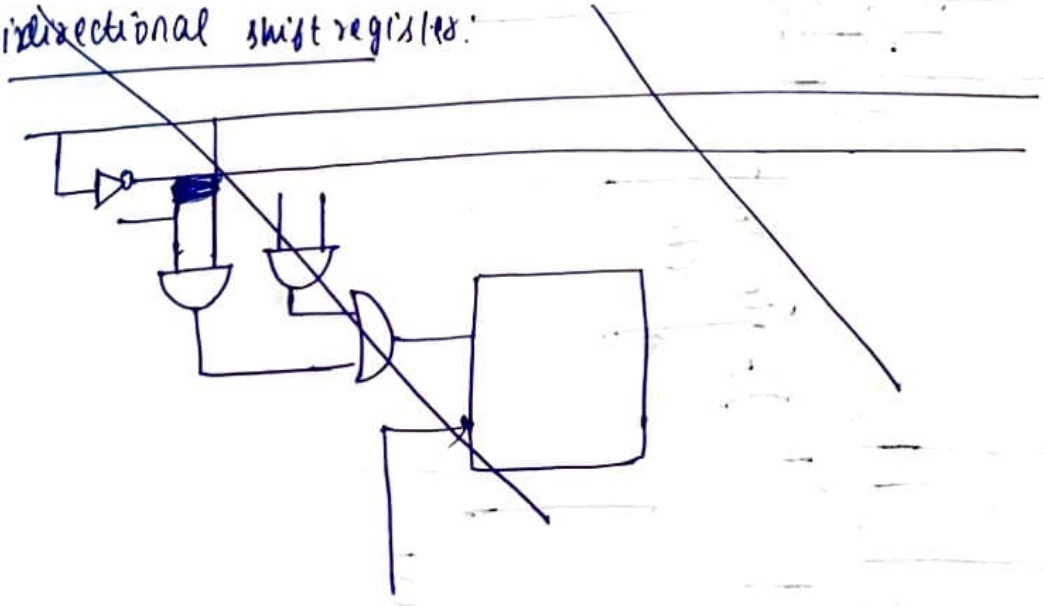
④ R_2

⑤ 0 } $R_3 = 1$

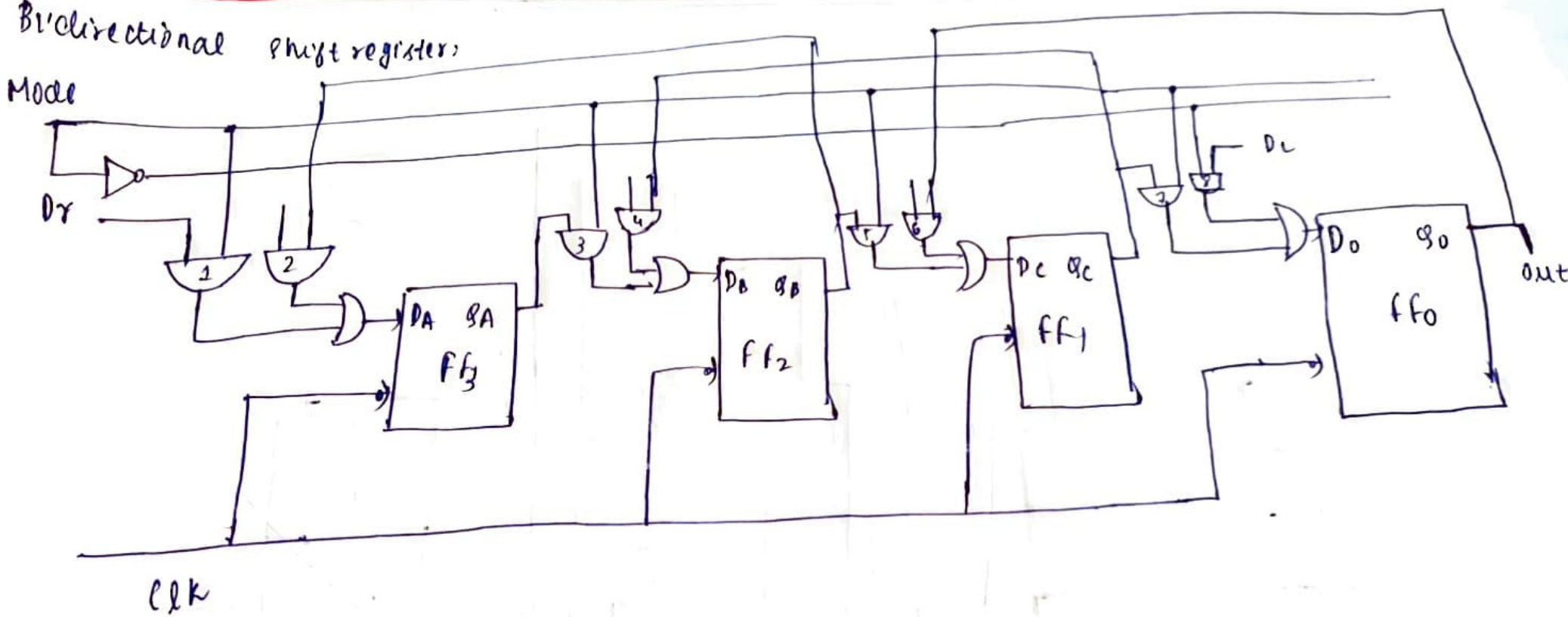
⑥ R_3



Bidirectional shift register:



Bi'directional shift register:



Universal shift register:

*

Mode control		Comment
S_1	S_0	
0	0	NC
0	1	shift right
1	0	shift left
1	1	Parallel loading

Bidirectional:

Right shift:

ip clk	Q_A	Q_B	Q_C	Q_D
	0	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1

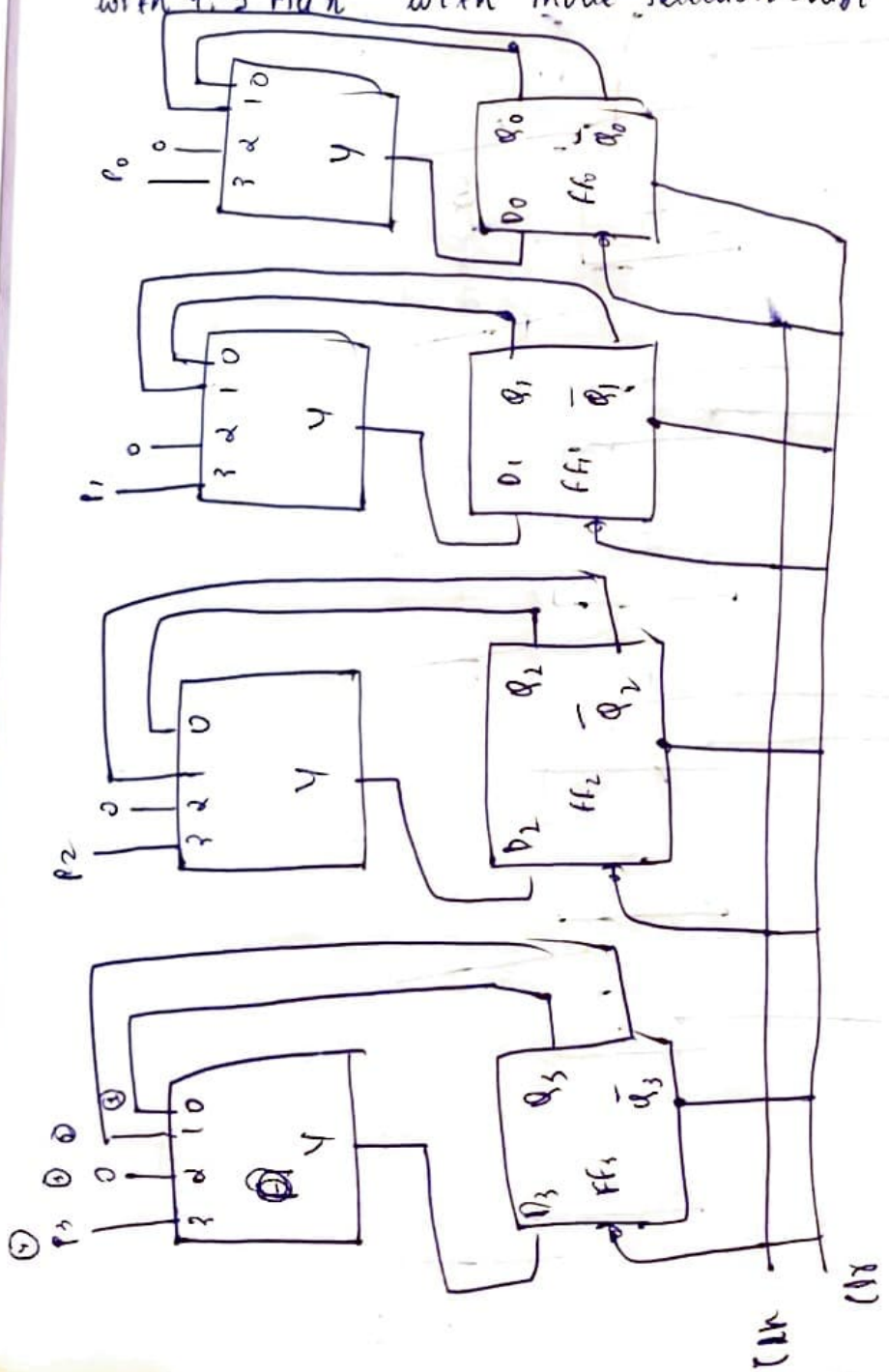
Left shift

	Q_A	Q_B	Q_C	Q_D
	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	1	0	0	0
5	0	0	0	0
6	0	0	0	0
7	0	0	0	0

Q)

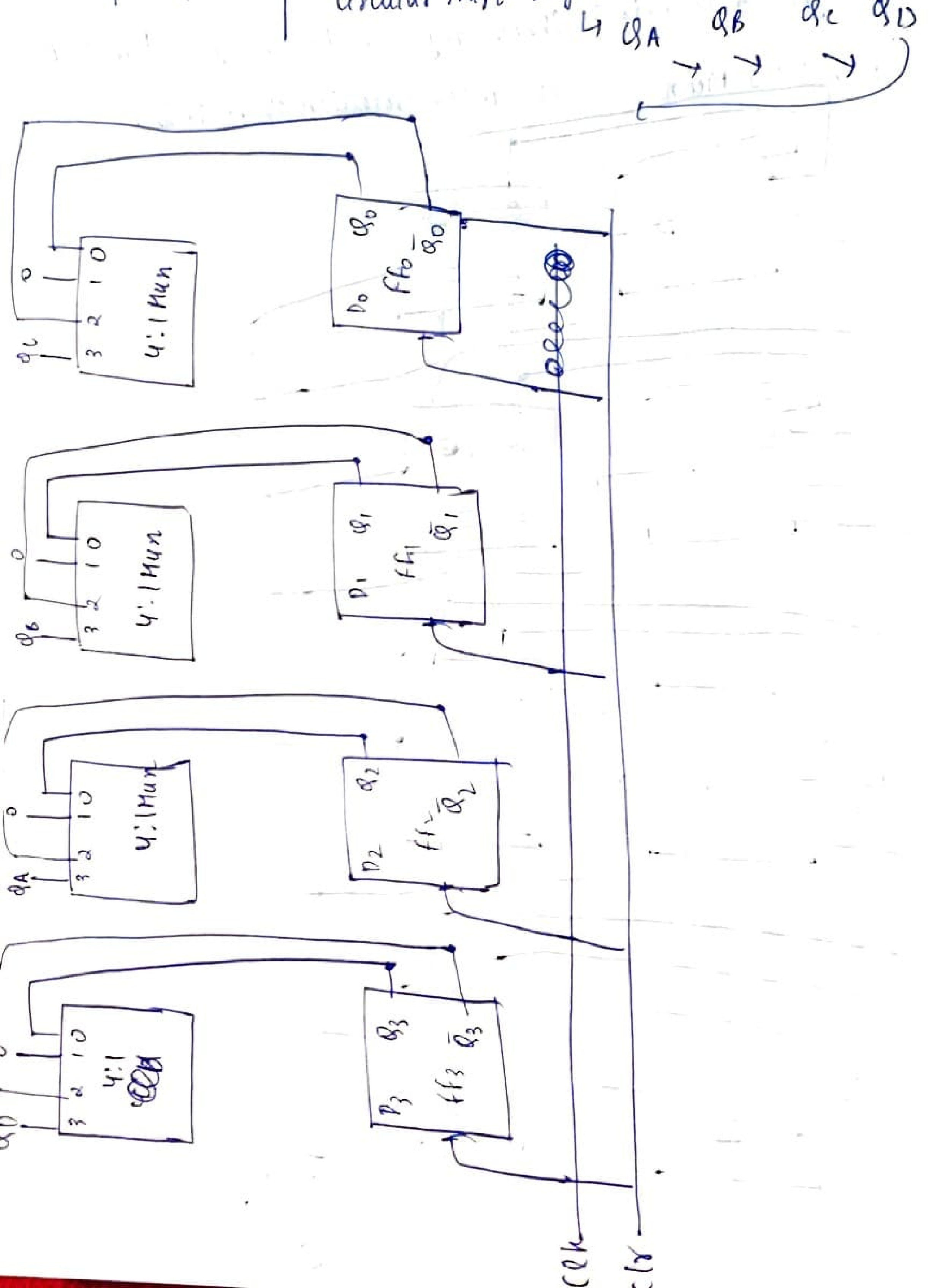
	Mode Control S_1	S_0	Comment
(1)	0	0	NC
(2)	0	1	Complement
(3)	1	0	Clear to 0
(4)	1	1	load II Data.

Design a universal shift register for the given table with 4:1 Mux with mode selection shift S_1 S_0.



Design a universal shift register for

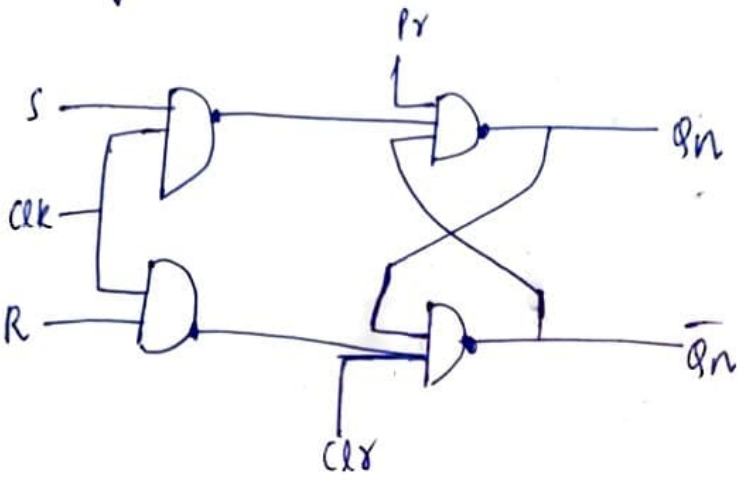
Mode S_1	Mode S_0	Operation
0	0	N C
0	1	synchronous clear
1	0	complement
1	1	circular shift right.



Asynchronous inputs or direct inputs or overriding i/ps:

Preset and clear inputs overrides the input from S, R and Clk.

Basically output is irrespective of S and R inputs.



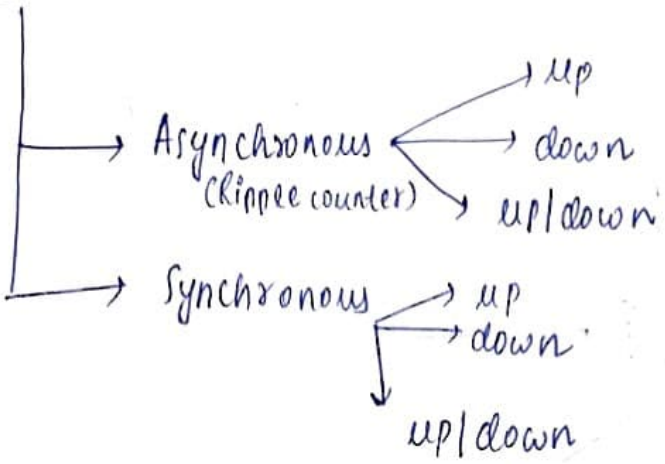
Active low:

Pr	Clr	Qn
0	0	Not used
0	1	1
1	0	0
1	1	b/b work normally

Active high:

Pr	Clr	Qn
0	0	b/b works normally
0	1	1
1	0	0
1	1	Not used

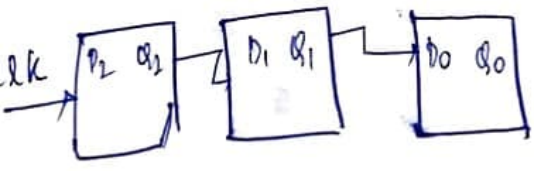
Counters:

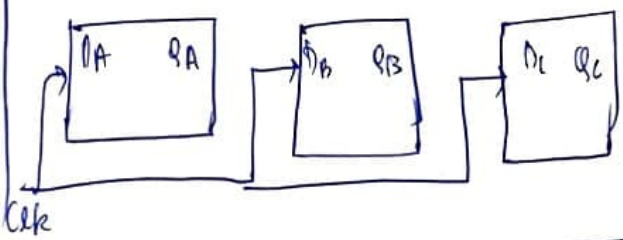


Asynchronous: easier, simpler
slower

Synchronous: complex
faster

Asychronous	Synchronous
a) flip flops are connected in such a way that the o/p of first f/f is clk for the next f/f.	a) there is no connection b/w o/p of first f/f and clock.
b) flip flops are not clocked simultaneously	b) Flip flops are clocked simultaneously.
c) circuit is simple for more no. of states.	c) circuit becomes complicated as no. of states increases.
d) speed is low	d) speed is high.

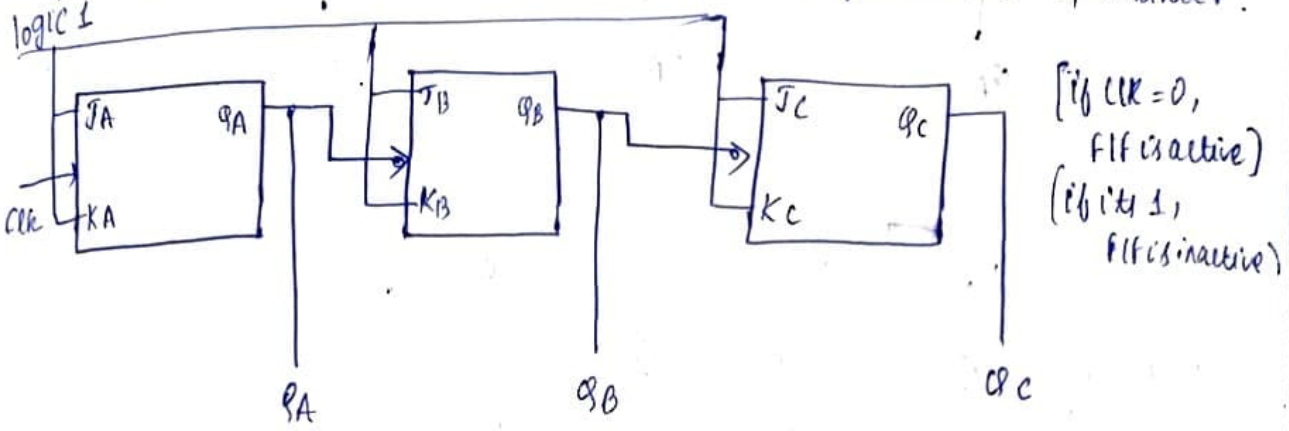




+ve edge → up counter → clk → $\bar{Q}$
→ down counter → clk → Q

-ve edge → up counter → clk → Q
→ down counter → clk → $\bar{Q}$

Q) Design a 3 bit negative edge triggered asynchronous up counter.

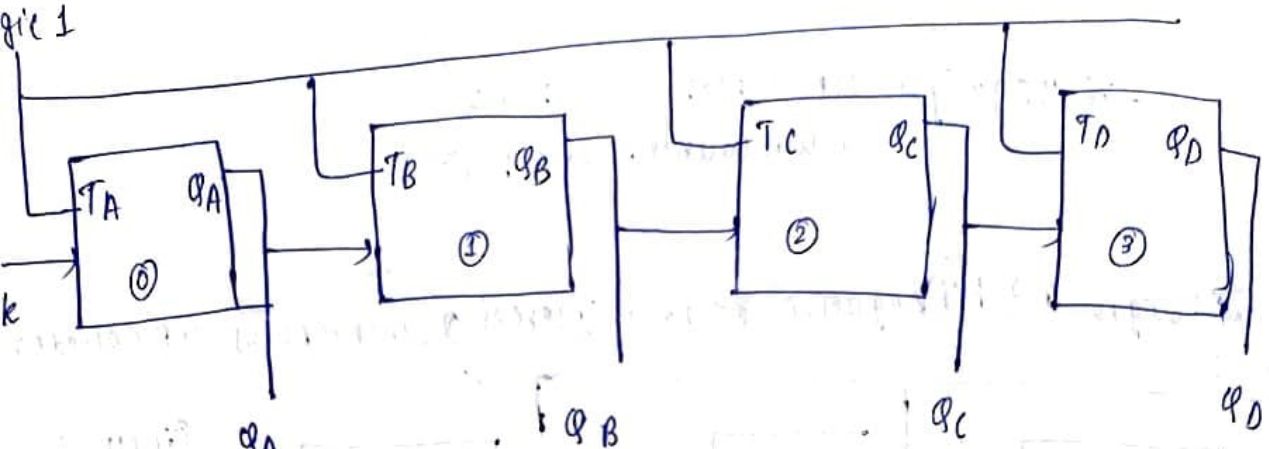


[if clk = 0, FF is active)
(if it's 1, FF is inactive)

clk	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

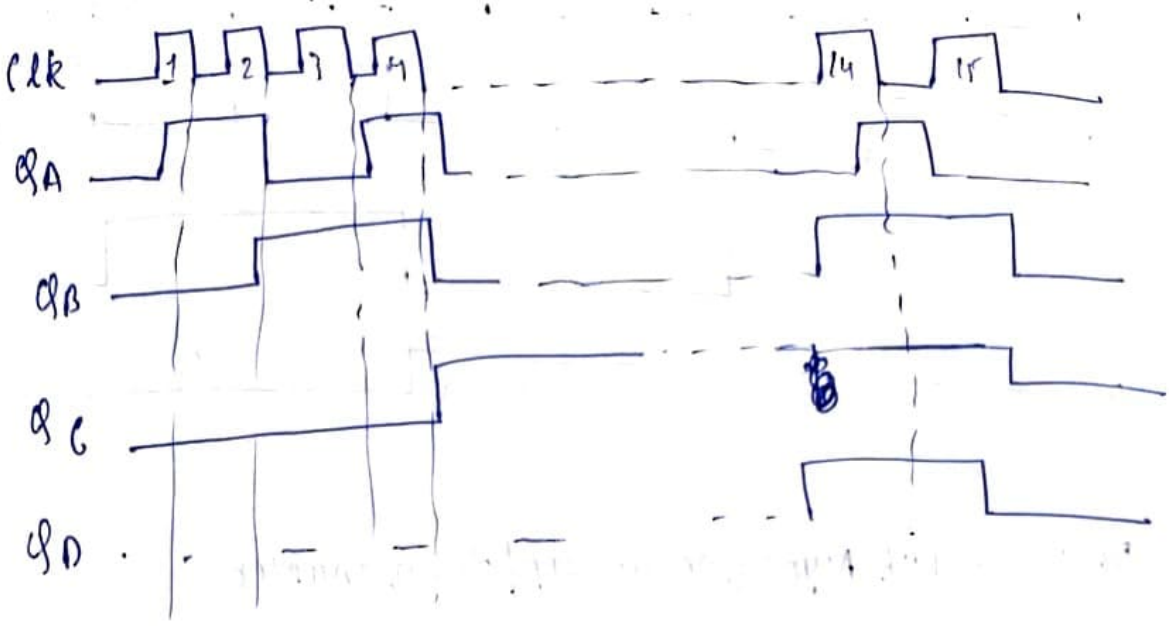
[For whichever bit clk is given it becomes LSB
∴ here → Q_A is LSB]

Q) Design a four bit asynchronous up counter using negative edge triggered T flip flop.

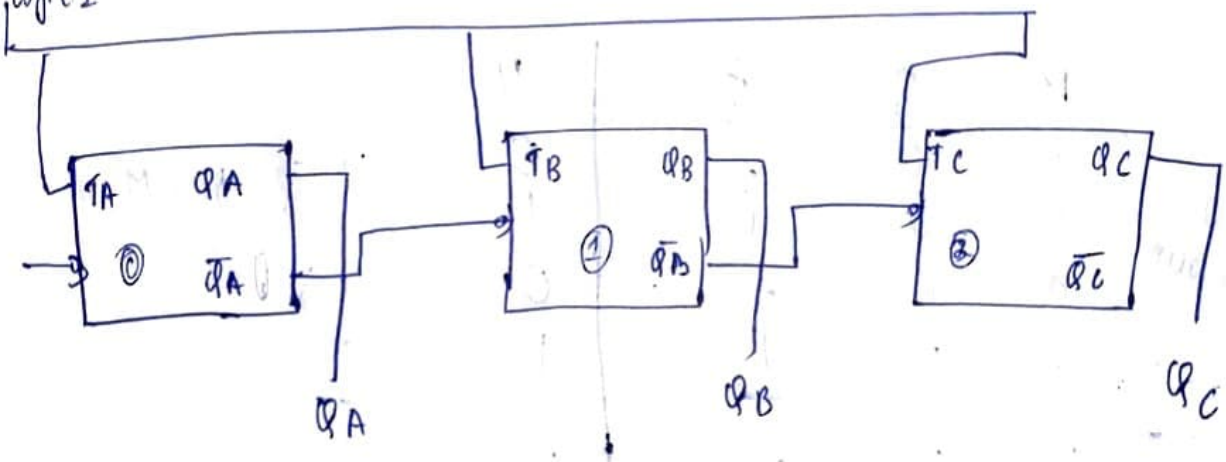


		Q_D	Q_C	Q_B	Q_A
Initially		0	0	0	0
Clk	1	0	0	0	1
	2	0	0	1	0
	3	0	0	1	1
	4	0	1	0	0
	5	0	1	0	1
	6	0	1	1	0
	7	0	1	1	1
	8	1	0	0	0
	9	1	0	0	1
	10	1	0	1	0
	11	1	0	1	1
	12	1	1	0	0
	13	1	1	0	1
	14	1	1	1	0
	15	1	1	1	1

Waveform:



Q) Design a 3 bit ripple counter (down) using T flip flop: (Negative trigger)



	Q_C	Q_B	Q_A
initial	X	X	X
clk 1			
initial	1	1	1
clk 1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1

$\bar{Q}_A, \bar{Q}_B$ or $\bar{Q}_C$ → 0 → change

1 → No change

Design of ripple counter / Asynchronous counter.

Step1: determine the no. of flipflops needed. (n)

Step2: choose the type of flipflop to be used. (T or JK)

Step3: Write truth table for counter.

Step4: derive reset logic by K map simplification.

Step5: draw the logic diagram

Q) Design decade ripple counter using JK flipflop or BCD ripple counter using JK flipflop.

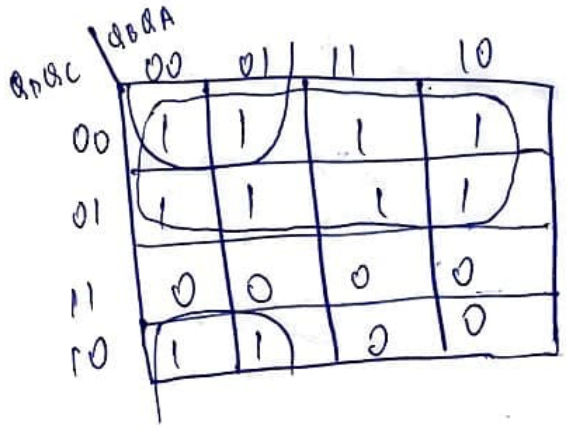
1) $2^n >= N$

$N = 10$ (0-9)

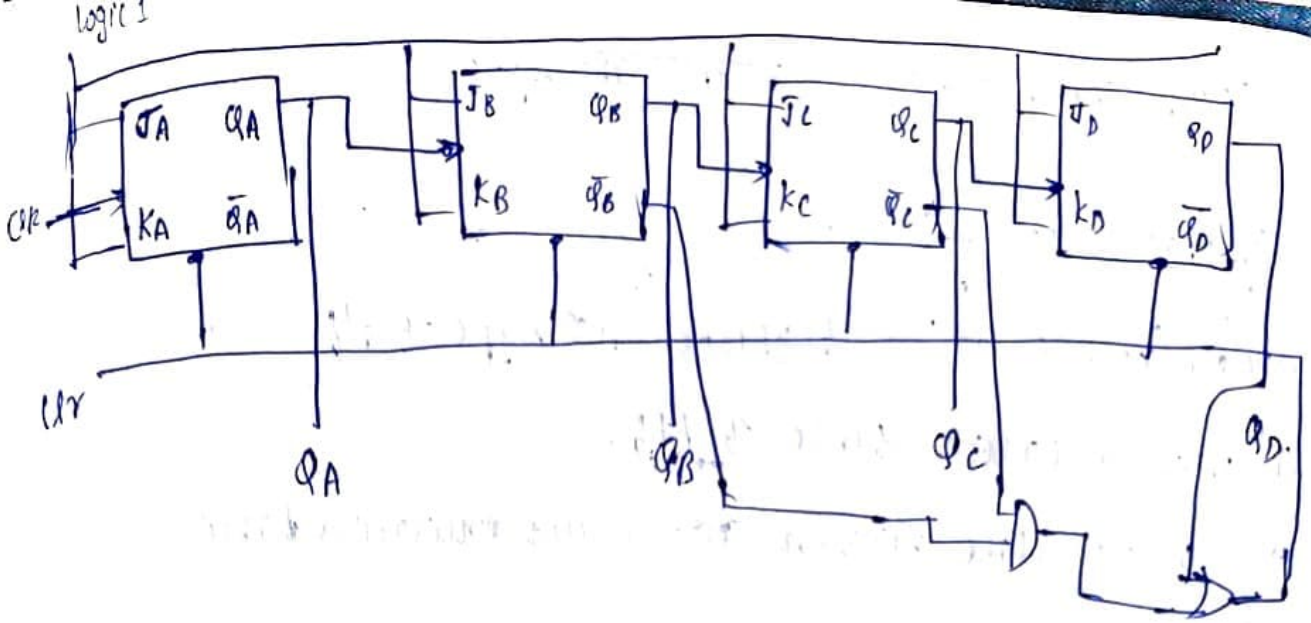
$n = 4$

2) JK flipflop

Q_D	Q_C	Q_B	Q_A	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1



$Y = \bar{Q}_D + Q_C \bar{Q}_B$



Q) Design mod 6 counter using T flip flop. (0 to 5)

a	b	c	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

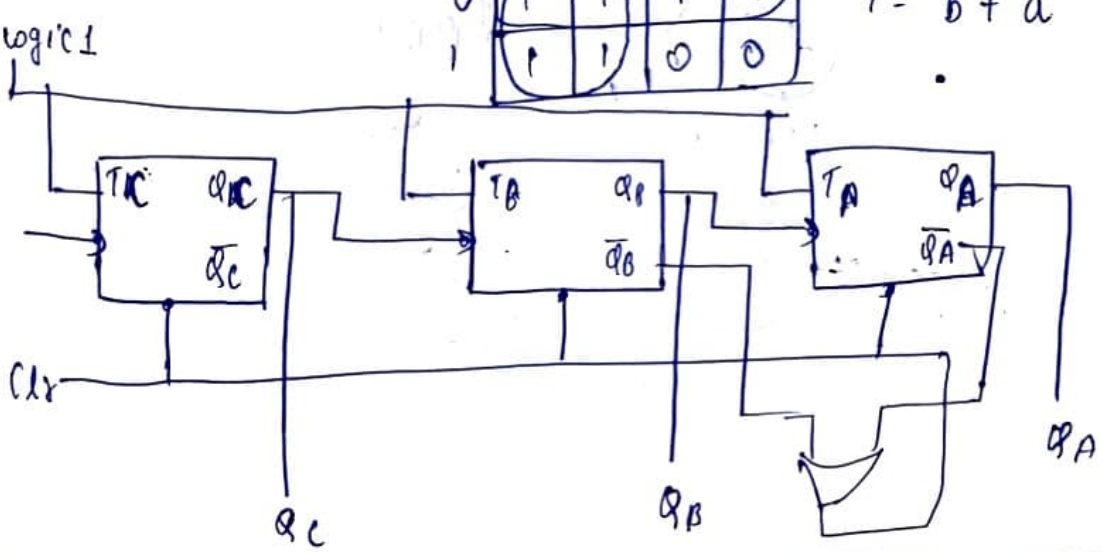
LSB → Clk

N = 6 (0-5)

n = 3

a \ bc	00	01	11	10
0	1	1	1	1
1	1	1	0	0

$Y = \bar{b} + \bar{a}$



Q) Determine the no. of flipflops and type.

Synchronous counter:

a) Determine the no. of flipflops and type of flip flop

b) Write excitation table of flip flop.

c) Write state diagram and circuit excitation table

d) obtain eqn using kmap

e) Draw logic diagram.

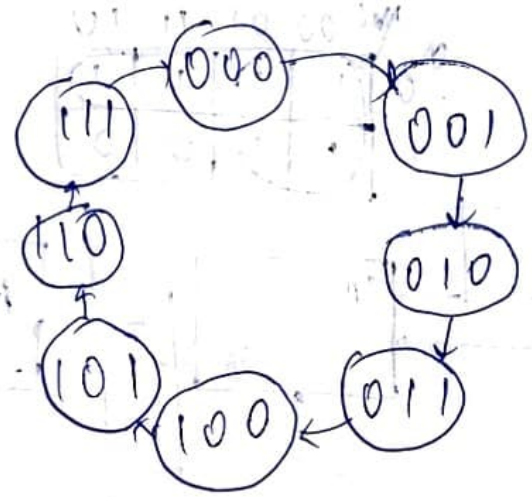
Q) Design 3 bit synchronous binary upcounter.

Step 1: n = 3 type: T flip flop

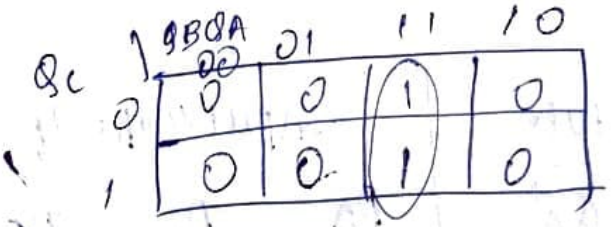
Step 2:

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

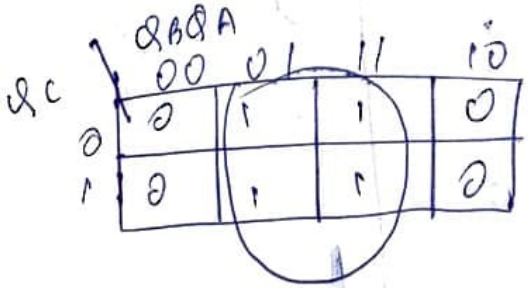
Steps:



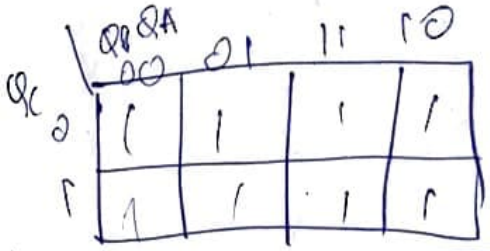
Present state (PS)			Next state			Output of the F/F		
Q_C	Q_B	Q_A	Q_C^+	Q_B^+	Q_A^+	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



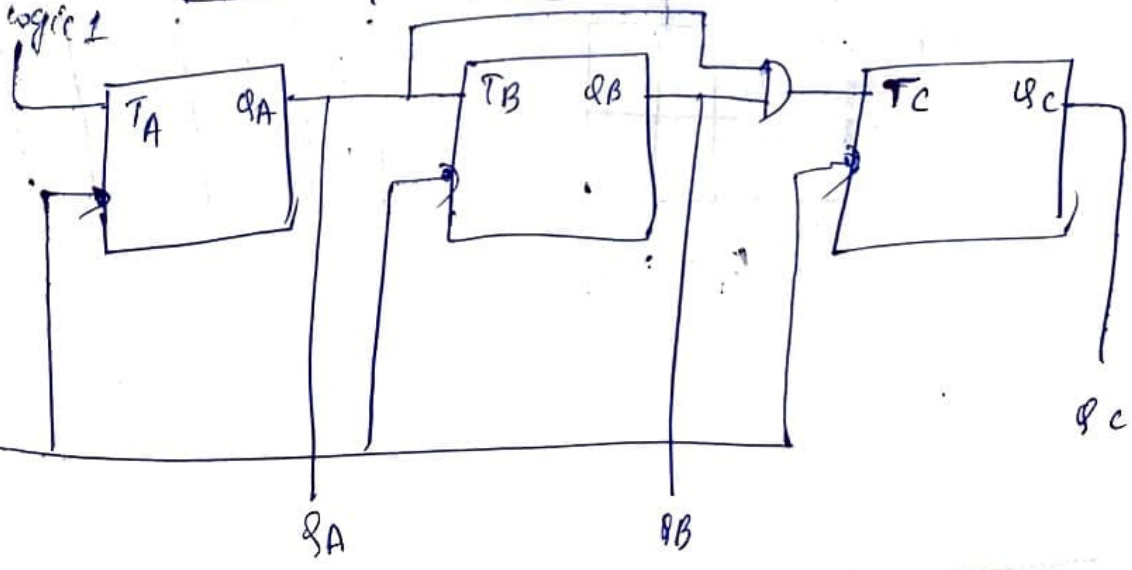
$T_C = Q_B Q_A$



$T_B = Q_A$



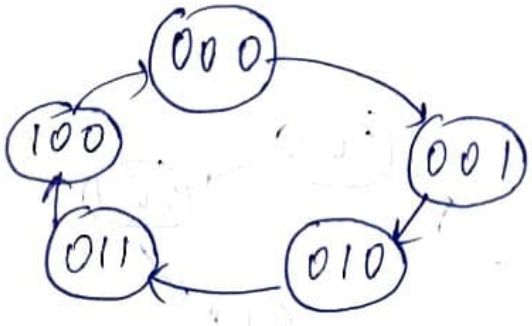
$T_A = 1$



8) Design mod 5 counter using JK f/f:

n=3, JK f/f

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0



Present state			Next state			i/p to f/f					
Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	0	x
1	0	0	0	0	0	x	1	0	x	0	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

$J_A = Q_B Q_C$

$K_A = 1$

$J_B = Q_A$

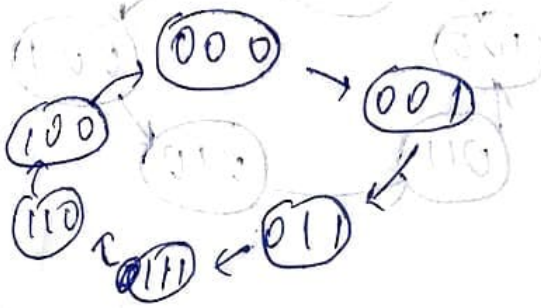
$K_B = Q_A$

$K_C = 1$

Q) Design the synchronous counter using JK f/f for the following sequence · 0, 1, 3, 7, 6, 4, 0

n = 3 , JK f/f

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
0	0	x	1
1	1	x	0
1			



Present state			Next state			i/p to JK f/f					
Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	1	0	x	1	x	x	0
0	1	0	x	x	x	x	x	x	x	x	x
0	1	1	1	1	1	1	x	x	0	x	0
1	0	0	0	0	0	x	1	0	x	0	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	1	0	0	x	0	x	1	0	x
1	1	1	1	1	0	x	0	x	0	x	1
1											

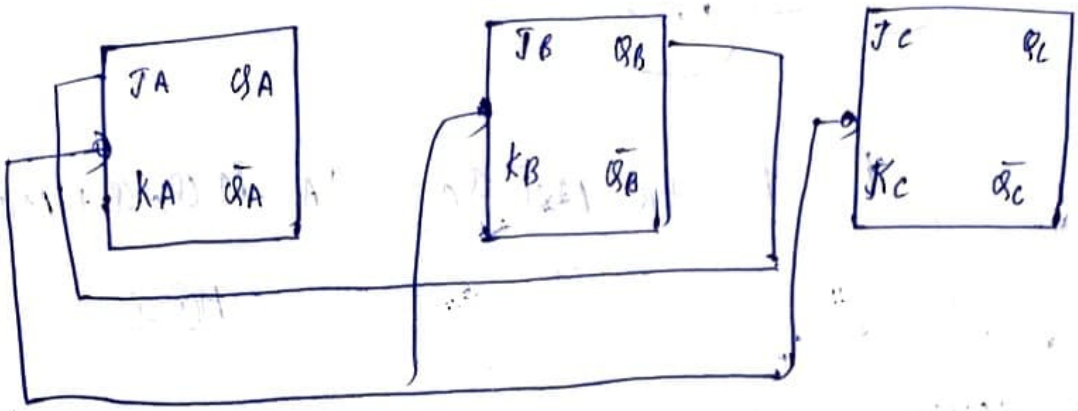
Q_A \ Q_BQ_C	00	01	11	10
0	0	0	1	X
1	X	X	X	X

$J_A = Q_B$

$K_A = \bar{Q}_B$

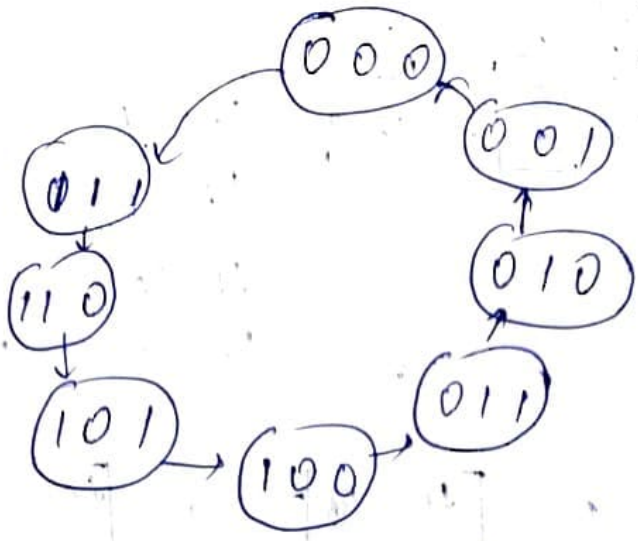
$J_B = Q_C$ $\quad J_C = \bar{Q}_A$

$K_B = \bar{Q}_C$ $\quad K_C = \bar{Q}_A$



up/down - T flip flop

M	Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
	0	0	1	0	1	0	0	1	1
	0	1	0	0	1	1	0	0	1
	0	1	1	1	0	0	1	1	1
	1	0	0	1	0	1	0	0	1
	1	0	1	1	1	0	0	1	1
	1	1	0	1	1	1	0	0	1
	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
	0	0	1	1	1	0	1	1	0
	0	1	0	1	0	1	1	0	1
	0	1	1	1	0	0	1	0	0
	1	0	0	0	1	1	0	1	1
	1	0	1	0	1	0	0	1	0
	1	1	0	0	0	1	0	0	1
	1	1	1	0	0	0	0	0	0



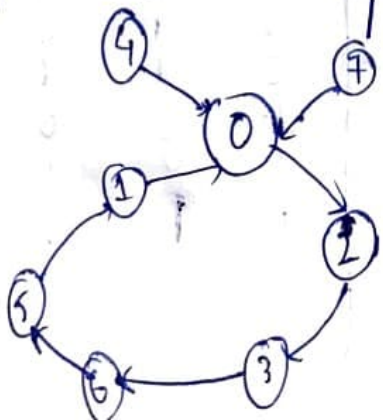
$T_C = 1 \quad T_B = M \oplus Q_C \quad T_A = \bar{M} Q_C Q_B + M \bar{Q}_B \bar{Q}_C$

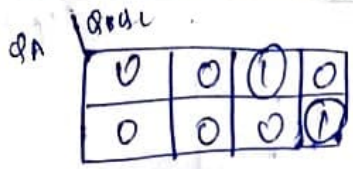
$= M \oplus Q_C$

Self starting counter:

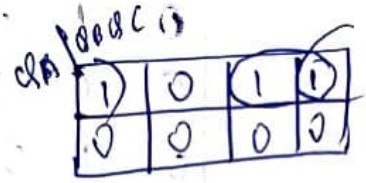
Q) 0, 2, 3, 6, 5, 1, 0 . . . .

PS			NS			i/p to D f/f		
Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	D_A	D_B	D_C
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	0
0	1	0	0	1	1	0	1	1
0	1	1	1	1	0	1	1	0
1	0	0	0	0	0	0	0	0
1	0	1	0	0	1	0	0	1
1	1	0	1	0	1	1	0	1
1	1	1	0	0	0	0	0	0

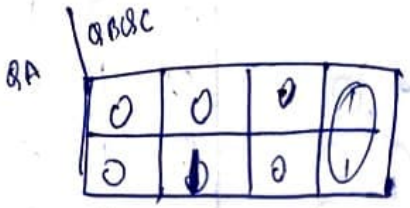




$$D_A = \bar{Q}_A Q_B Q_C + Q_A Q_B \bar{Q}_C$$



$$D_B = \bar{Q}_A \bar{Q}_C + \bar{Q}_A Q_B$$



$$D_C = Q_B \bar{Q}_C + Q_A \bar{Q}_B Q_C$$

Circuit:

Q) Design a self stasting synchronous decade counter using T flip flop for 0, 2, 6, 8, 9, 0

T flip flop

excitation table:

Q	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

(In self stasting counters if there's no next state it goes to zero, whereas in normal counters it goes to don't care)

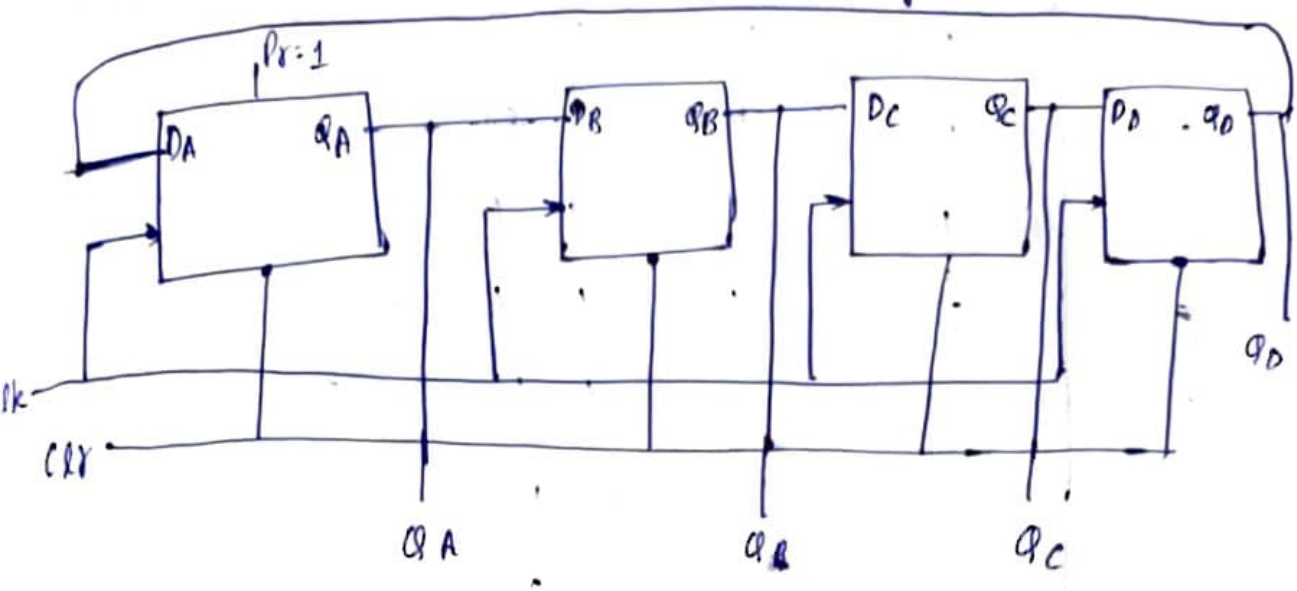
PS				NS				J/P to D/F			
Q_A	Q_B	Q_C	Q_D	Q_A^+	Q_B^+	Q_C^+	Q_D^+				
0	0	0	0	0	1	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	1	1	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	0	1	0	0
0	1	0	1	0	0	0	0	0	1	0	1
0	1	1	0	1	0	0	0	1	1	1	0
0	1	1	1	0	0	0	0	0	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	x	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x				
1	1	0	0	x	x	x	x				
1	1	0	1	x	x	x	x				
1	1	1	0	x	x	x	x				
1	1	1	1	x	x	x	x				

Kmaps, Circuit ..

Ring Counter:

→ 4 bit

→ Preset or Clear inputs are called Overriding inputs.

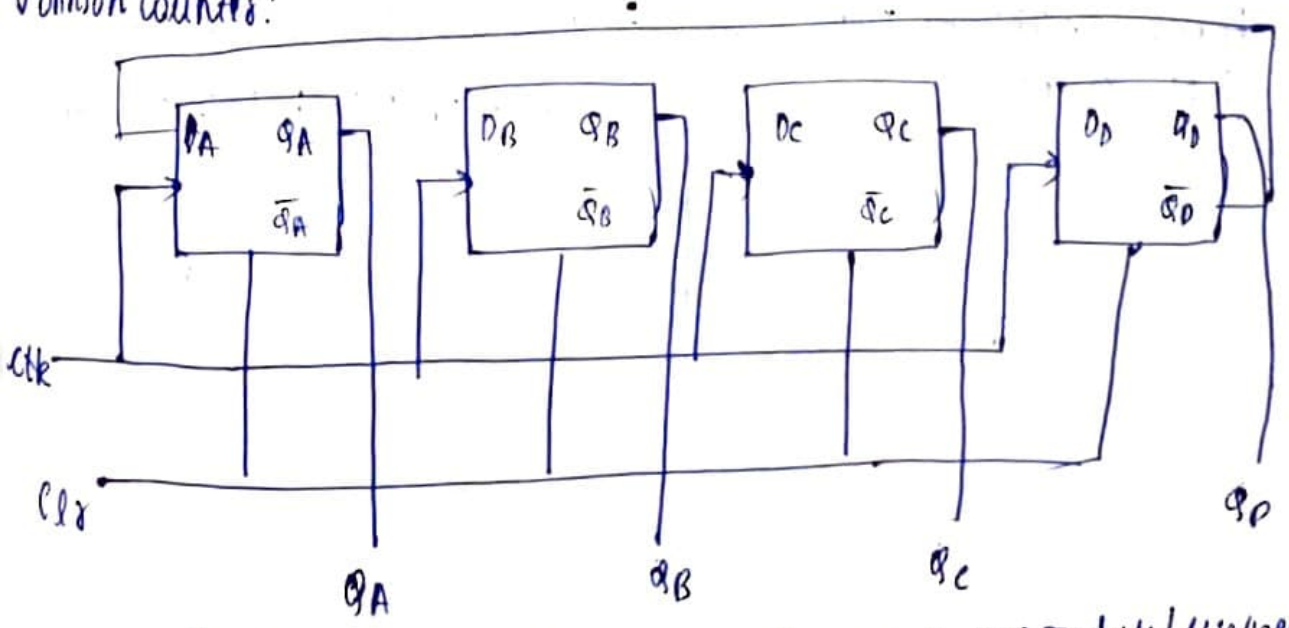


Q_A	Q_B	Q_C	Q_D	
0	0	0	0	0
1	0	0	0	8
0	1	0	0	4
0	0	1	0	2
0	0	0	1	1

Circular shift

In Ring counter, no. of bits = no. of states.

Johnson Counter:



In Johnson, no of states = 2xn (n => no. of bits / flip flops)

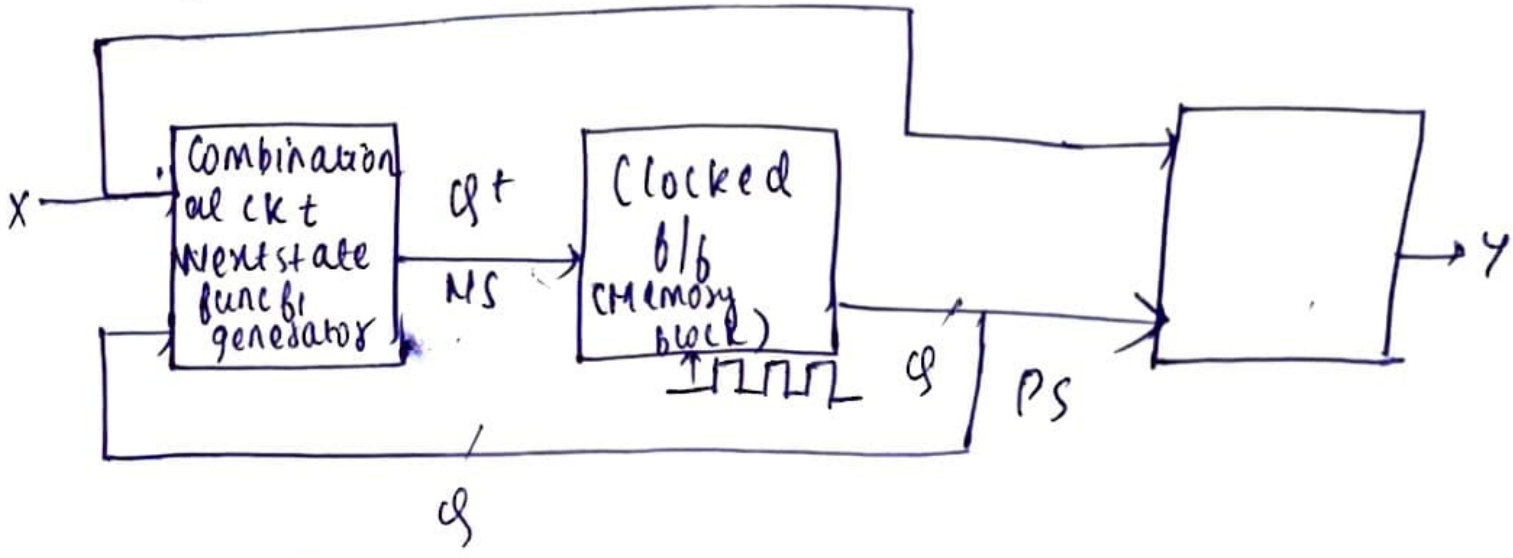
clk	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

Ring	Johnson
1) Initialization required.	1) Initialization not req since the o/p is taken from Q. as feed back to first ff.

Moore and Mealy model:

Moore model	Mealy model
* The output is for present state only.	* The output is for present state and as well as present input.
* The input changes does not affect the output.	* Input changes may affect the output.
* It requires more no. of states for implementing the same func	* It requires less no. of states for implementing the same func.

Mealy model:



Q) Design a synchronous circuit using +ve edge triggered JK f/f with minimal combinational gating to generate the following sequence: 0-1-2-0 if i/p x=0

0-2-1-0 if i/p x=1