

UNIT-II

DC Load Line & Bias Point

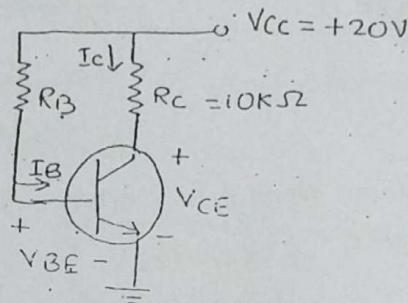
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DC Load Line

The dc load line for a transistor ckt is a straight line drawn on the transistor O/P characteristics.

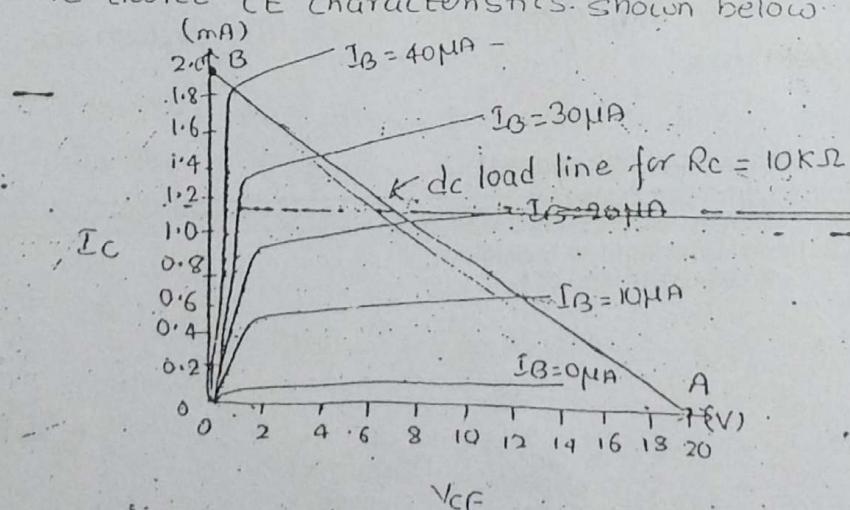
→ For a CE ckt, the load line is a graph of I_C vs. V_{CE} for a given value of R_C & given supply vdg V_{CC} .

→ The load line shows all corresponding levels of I_C & V_{CE} that can exist in particular circuit.



Common Emitter circuit with collector resistor

→ The dc load line for the ckt shown above is drawn on the device CE characteristics shown below.



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from ckt shown above:

$V_{CE} = \text{Supply voltage} - \text{voltage drop across } R_C$

$$V_{CE} = V_{CC} - I_C R_C$$

then, $I_C = 0$

$$V_{CE} = V_{CC} = 20V \rightarrow \text{point 'A' on x-axis}$$

when, $V_{CE} = 0$

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{20}{10k\Omega} = 2mA \rightarrow \text{point 'B' on y-axis}$$

for $V_{CE} = 0V$

& $I_C = 2mA$

→ The straight line drawn through points A & B is the load line for $R_C = 10k\Omega$ & $V_{CC} = 20V$.

if either of these two quantities (R_C or V_{CC}) is changed, new load line must be drawn.

Knowing any one of I_B , I_C or V_{CE} , it is easy to determine the other two from dc load line drawn on device characteristics.

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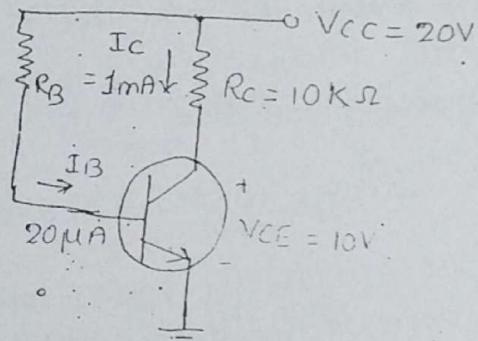
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DC Bias Point (Q-point)

SHERPA'S VIEWS
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- The dc bias point or quiescent point (Q-point) identifies the transistor collector current and collector-emitter voltage when there is no input signal at the base terminal.
- Thus, it defines the dc conditions in the ckt.
- When a signal is applied to the transistor base, I_B varies according to the instantaneous amplitude of signal.
- This causes I_C to vary and consequently produces a variation in V_{CE} .

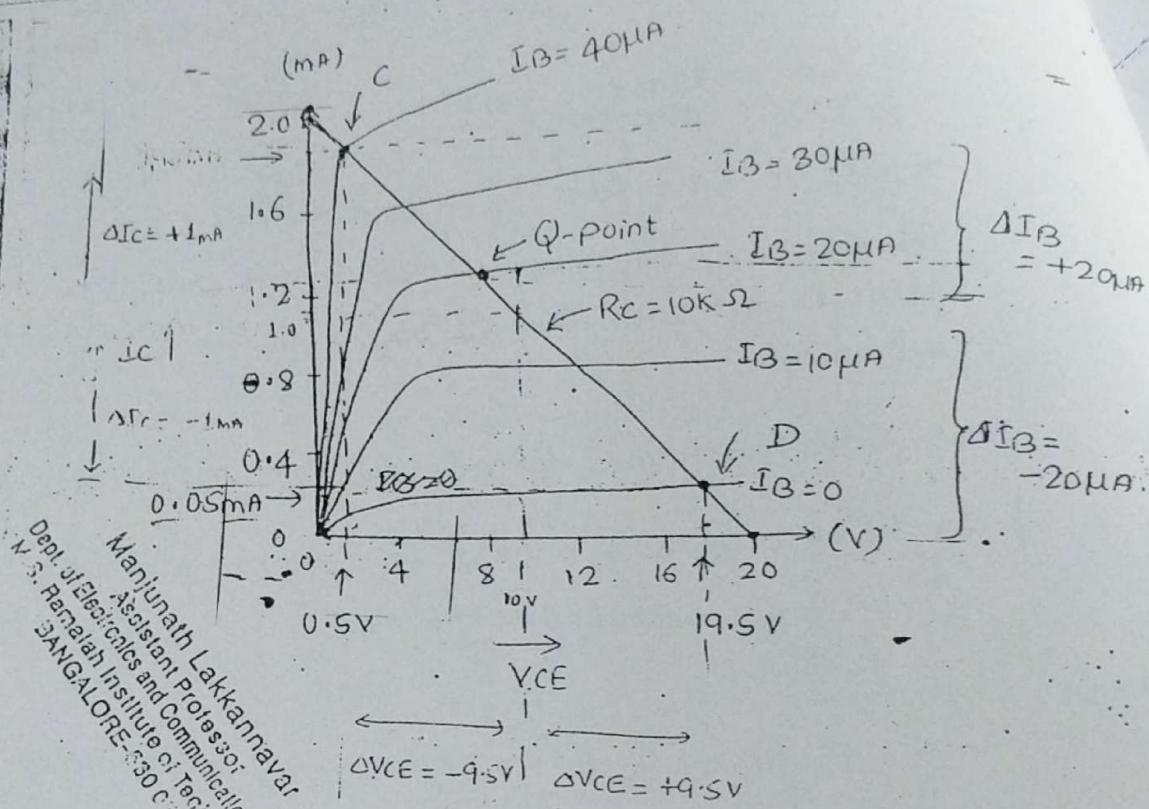


- Consider the above ckt and the $10\text{k}\Omega$ load line drawn for the ckt shown below. Assume that the bias conditions are as identified by the Q point on the load line.

$$I_B = 20\mu\text{A}, I_C = 1\text{mA}, \text{ & } V_{CE} = 10\text{V}.$$

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→ When I_B is increased from $20\mu A$ to $40\mu A$, I_c becomes approximately 1.95mA & V_{CE} becomes 0.5V , as illustrated.

$$\therefore \Delta V_{CE} = 10 - 0.5 = 9.5\text{V}$$

→ So, increasing I_B by $20\mu A$ ($20\mu A$ to $40\mu A$) caused V_{CE} to decrease by 9.5V (10V to 0.5V)

→ Now, look at the effect of decreasing the base current

→ When I_B is decreased from $20\mu A$ to 0 , I_c goes down to approximately $0.05\mu A$, & V_{CE} goes up to 19.5V as illustrated at pt. D on the load line.

$$\text{So, } \Delta V_{CE} = 19.5 - 10\text{V} = 9.5\text{V}$$

∴ Decreasing I_B by $20\mu A$ (from $20\mu A$ to zero), caused V_{CE} to increase by 9.5V (from 10V to 19.5V).

It is seen that with Q-point at $I_C = 1\text{mA}$ & $V_{CE} = 10\text{V}$, an I_B variation of $\pm 20\mu\text{A}$ produces a V_{CE} swing of $\pm 9.5\text{V}$.

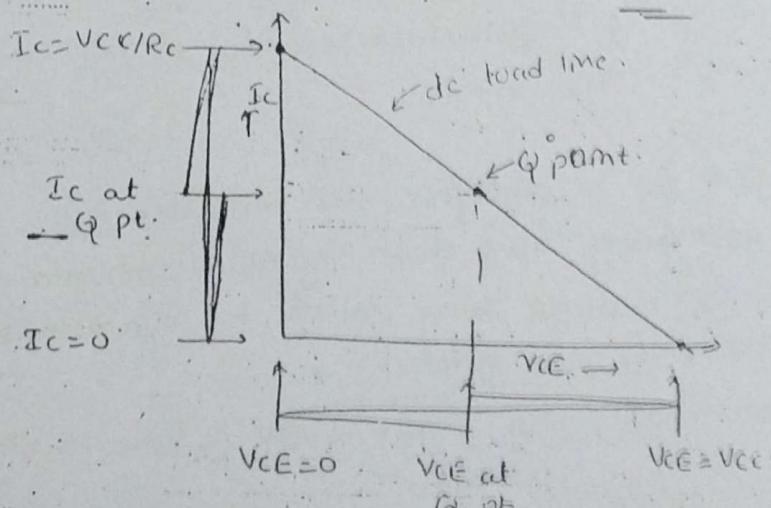
→ The base current does not have to be varied by the max. amounts as discussed above, it can be increased and decreased by smaller amounts.

For e.g.: $I_B = \pm 10\text{mA}$ would produce a change of $I_C = \pm 10\text{mA} \pm 0.5\text{mA}$ & change of $V_{CE} = \pm 5\text{V}$

→ The max. possible transistor collector-emitter voltage swing for a ckt can be determined without using the transistor characteristics.

→ For convenience, it may be assumed that I_C is driven to zero at one extreme and to $\frac{V_{CC}}{R_C}$ at other extreme.

→ This changes V_{CE} from V_{CC} to 0 respectively.



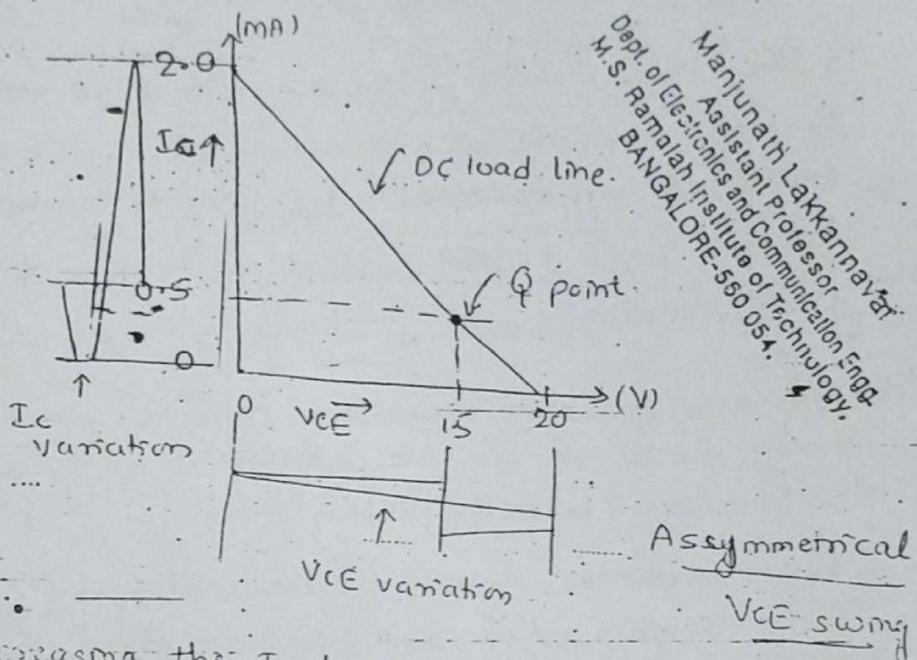
∴ The V_{CE} swing is $\pm \frac{V_{CC}}{2}$

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Selection of Q-point

- Suppose that, instead of being biased halfway along the load line, the transistor is biased at $I_C = 0.5\text{mA}$ & $V_{CE} = 15\text{V}$ as shown below.



Increasing the I_C to 2mA reduces V_{CE} to zero,
 $\Delta V_{CE} = -15\text{V}$.

- Reducing I_C to zero increases V_{CE} to V_{CC} producing $\Delta V_{CE} = +15\text{V}$.

- When used as a amplifier, the transistor o/p V_{CE} must swing up & down by equal amounts i.e., the o/p voltage swing must be symmetrical above & below the bias point.

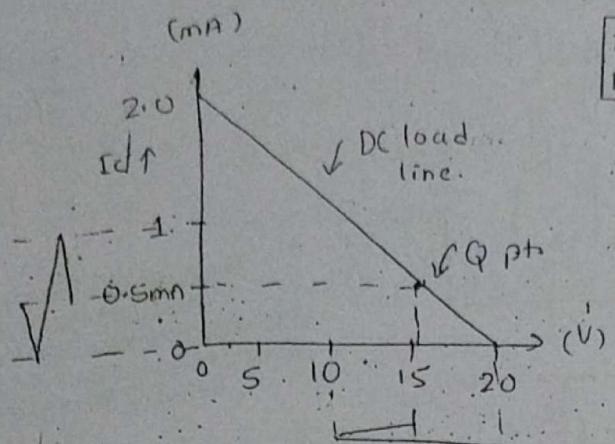
→ So asymmetrical swing -15V & $+15\text{V}$ is unsuitable.

- If I_C is driven up & down by $\pm 0.5\text{mA}$, a symmetrical o/p voltage swing that can be achieved with the bias pt. shown below.

of $\pm 15\text{V}$.

(max. symmetrical o/p).

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Symmetrical V_{CE} swing

- In many cases circuits are designed to have the Q pt. at the centre of the load line to give the largest possible symmetrical o/p vtg. swing.

The transistor ckt shown below has the collector characteristics shown below. Determine the ckt Q pt & estimate the max. Symmetrical o/p vtg. swing. $V_{CC} = 18V$, $R_C = 2.2k\Omega$, $I_B = 40\mu A$

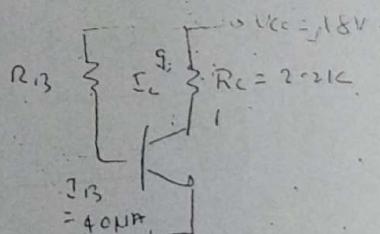
$$V_{CE} = V_{CC} - I_C R_C$$

at $I_C = 0$,

$$V_{CE} = V_{CC} = 18V.$$

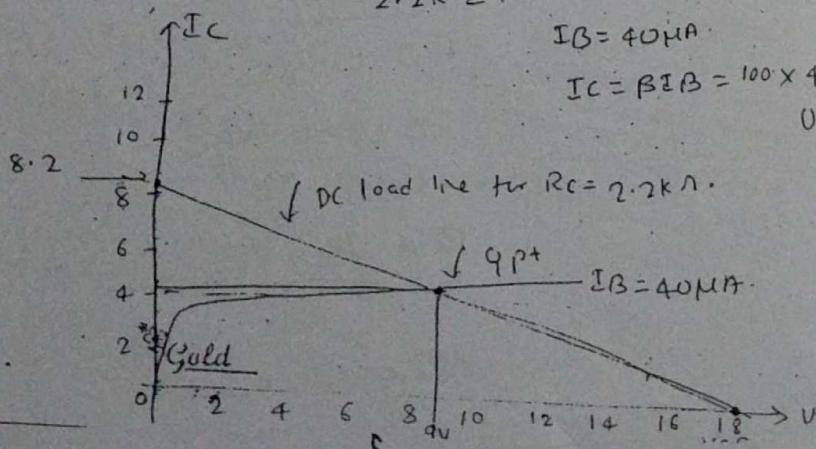
at $V_{CE} = 0$

$$\Delta I_C = \frac{V_{CC}}{R_C} = \frac{18}{2.2k\Omega} = 8.2 \text{ mA.}$$

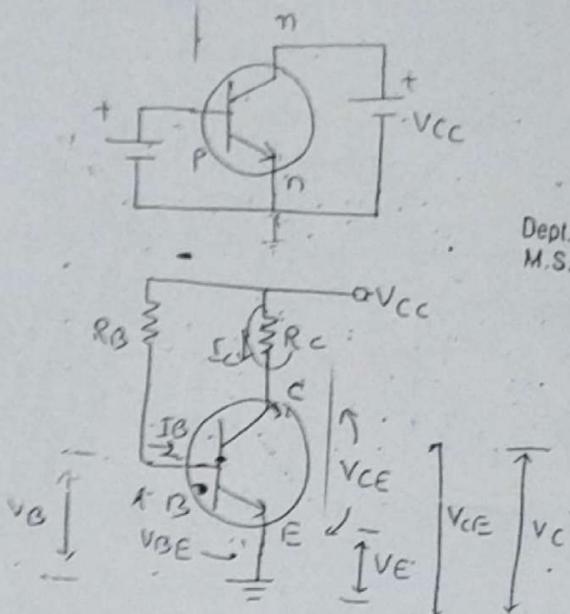


$$I_B = 40\mu A$$

$$I_C = \beta I_B = 100 \times 40 \times 10^{-6} = 0.4 \text{ mA}$$



Base Bias (Fixed Bias)



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$$V_{BE} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

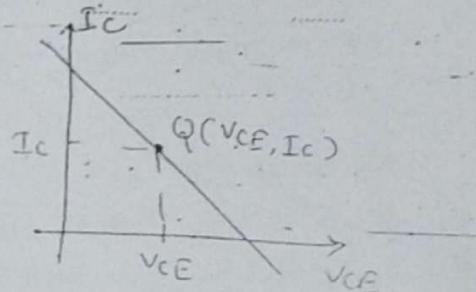
Analysis

V_{BE} , V_{CC} , R_B & R_C are given

$$I_B = ?$$

$$I_C = ?$$

$$V_{CE} = ?$$



Design

β , V_{CC} , V_{BE} , V_{CE} , I_B & I_C

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$V_{CE} \neq V_{CC}/\beta$

Advantages

- 1) The biasing ckt is very simple.
- 2) Single power supply is used.
- 3) By changing R_B , the Q. pt. can be shifted within active region.

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Disadvantages

- a) Fixed bias provides poor stabilization because if I_C increases due to increase in temperature, I_{CBO} also increases & transistor is pushed to sat.
- b) There are strong chances of thermal runaway.
So this method is rarely used

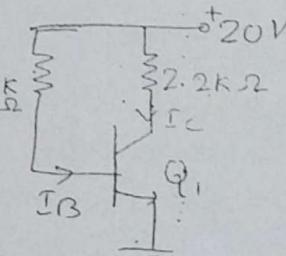
Prob.

The base bias ckt shown in fig determine I_C , I_B & V_{CE} . When transistor has β or $hFE = 150$.

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{20 - 0.7}{470 \times 10^3} = 41 \mu A$$



$$I_C = \beta I_B = 150 \times 41 \times 10^{-6} = 6.19 \text{ mA}$$

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore V_{CE} = V_{CC} - I_C R_C$$

$$= 20 - (6.19 \times 10^{-3} \times 2.2 \times 10^3)$$

$$V_{CE} = 6.3 \text{ V}$$

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Biassing Methods.

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→ In order to operate transistor in the desired region we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biassing of the transistor.

→ The I_E must be forward biased (0.6V to 0.7V) & I_C junction must be reverse biased (within max. limits). i.e., transistor should be operated in the middle of the active region or operating point (Q -point) should be fixed at the center of the active region.
→ Q -pt. should be made independent of ' β '.

Techniques used to Stabilize Q -point

→ The Q -point of transistor varies due to change in temperature.

→ To maintain the Q -point stable by keeping I_C & V_{CE} constant so that transistor will always work in active region, the following techniques are normally used:

- 1) Stabilization Techniques: use of resistive biassing ckt's which allow I_B to vary keeping I_C constant.
- 2) Compensation Techniques: use of tempere-sensitve diodes, transistors, thermistors etc. which compensating utgs & currents to maintain Q -pt. stable.

List of Transistor Biassing Circuits:

1) Base Bias

Biassing ckt's must ensure constant levels of Q -pt I_C & V_{CE} .

2) Collector to Base Bias. regardless of transistor replacement & tempere variation

3) Voltage Divider Bias.

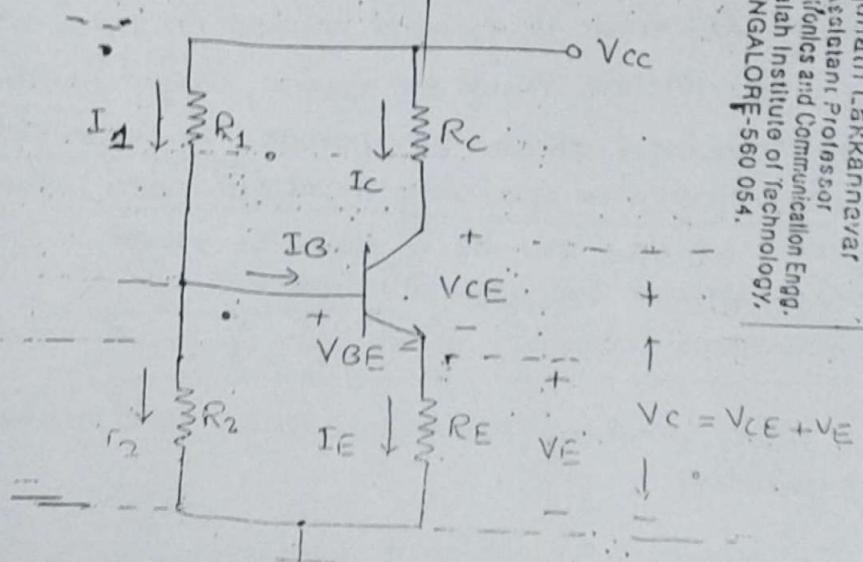
*Gold - Voltage Divider bias ckt provides excellent stability of I_C & V_{CE} levels & hence it is in number one.

Voltage Divider Bias (Approximate Analysis).

→ Voltage Divider Bias also known as Emitter current bias gives the most stable operating point.

- In ckt the levels of I_C & V_{CE} are almost dependent of ' β ' value.

→ Fig. below shows the ckt of V-D bias.



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→ In approximate analysis the base current is assumed to be much smaller than the voltage divider current I_2 .

→ Resistors R_1 & R_2 constitute a voltage divider that divides the supply voltage to produce the base bias voltage V_B .

$$I_1 = I_2 + I_B \quad \rightarrow (1)$$

as we have $I_2 \gg I_B$

$$I_2 \approx I_1$$

Clearly remain

Note thr

Note that the same current flows through R_1 & R_2 .

$$V_{CC} = I_1 R_1 + I_2 R_2 = I_2 [R_1 + R_2] \quad [\because I_2 = I_1]$$

$$\therefore I_2 = \frac{V_{CC}}{R_1 + R_2}$$

Voltage across R_2 is $V_B = I_2 R_2$

$$\therefore V_B = \frac{V_{CC} R_2}{R_1 + R_2}$$

→ (2)

Note that V_B is a constant quantity.

$$V_B = V_{BE} + V_E$$

$$\therefore V_E = V_B - V_{BE}$$

But $V_E = I_E R_E$. Using the relation in eqn (3)

$$I_E R_E = V_B - V_{BE}$$

$$\therefore I_E = \frac{V_B - V_{BE}}{R_E} = \frac{V_E}{R_E} \rightarrow (4)$$

$I_E = I_B + I_C \approx I_C$, since base current is small.

Since V_B is a constant quantity, I_C & I_E are held at constant level.

Applying KVL to the collector-emitter circuit we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Since $I_E \approx I_C$, we can write

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \rightarrow (5)$$

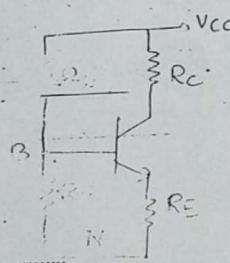
Clearly, with I_C & I_E constant, the transistor C-E voltage remains at a constant level.

Note that the transistor 'B' is not involved in any of the 3rd equations.

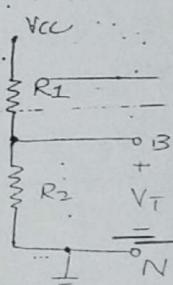
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Exact OR Voltage Divider Bias (Accurate Analysis)

- In accurate analysis, the base current I_B is considered in the analysis of the circuit.
- This is done by representing the voltage divider network consisting of V_{CC} , R_1 & R_2 by an equivalent circuit consisting of voltage source V_T in series with a resistance R_T between base & ground.
- This equivalent circuit is called the Thevenin's Equivalent circuit.



(a) V-D Bias ckt



(b) V-D network

Consider the V-D network shown in fig(b). V_T is the voltage across R_2 . Using voltage division rule we get

$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} \rightarrow (1)$$

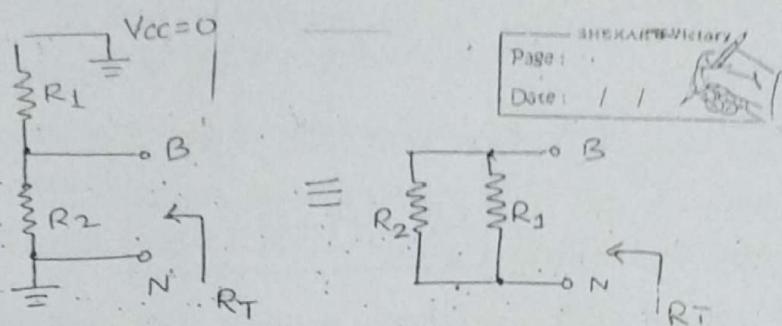
V_T is Thevenin's vtg.

To find R_T we have to connect V_{CC} point to ground as shown below fig(c).

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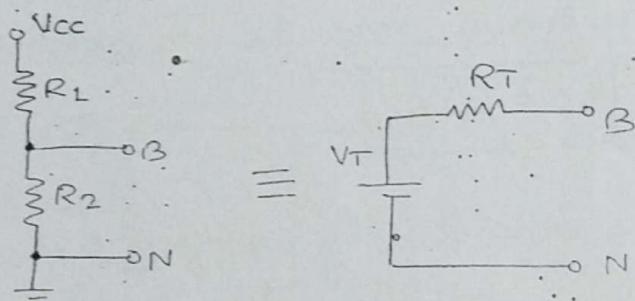
(c) Circuit to find R_T

R_T is the equivalent resistance betⁿ B & N

$$R_T = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \rightarrow (2)$$

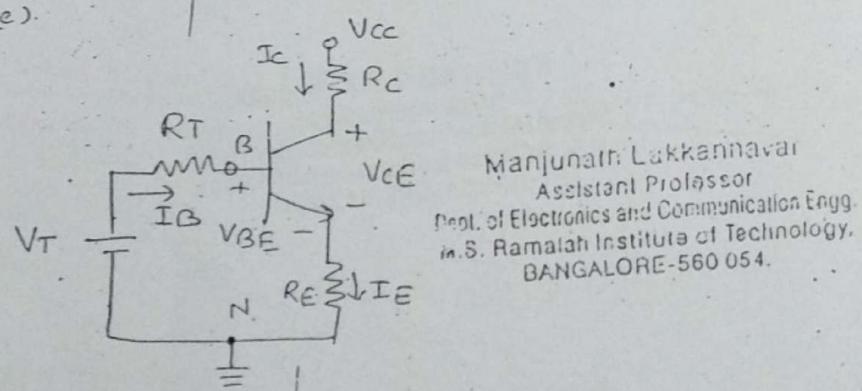
R_T is the Thevenin's resistance

The Thevenin's Equivalent ckt of voltage divider network of fig (b) betⁿ the points B & N is shown below fig(d)



(d) Thevenin's equivalent of V-D network

Now let us replace the voltage divider network in fig(a) with its Thevenin's Equivalent ckt betⁿ B & N as shown below fig(e).



(e) V-D bias with Thevenin's Equivalent ckt.

Gold

Applying KVL to the B-E ckt of fig (e) we have

$$V_T = R_T I_B + V_{BE} + I_E R_E \rightarrow (3)$$

$$\text{But } I_E = I_B + I_C = I_B + \beta I_B$$

$$\boxed{I_E = (1 + \beta) I_B}$$

Using this relation in eqn (3) we have

$$V_T - V_{BE} = I_B [R_T + (1 + \beta) R_E]$$

$$\boxed{I_B = \frac{V_T - V_{BE}}{R_T + (1 + \beta) R_E}} \rightarrow (4)$$

Once I_B is known, the I_C is obtained by

$$\boxed{I_C = \beta I_B} \rightarrow (5)$$

we can be obtained by applying KVL to C-E ckt

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - I_E R_E} \rightarrow (6)$$

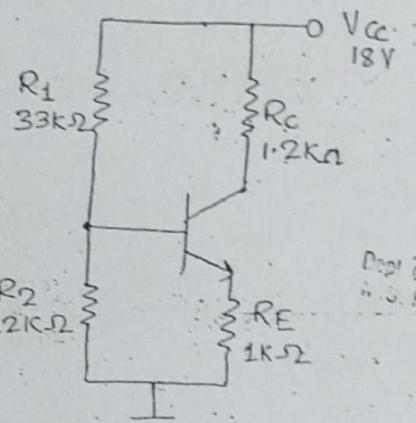
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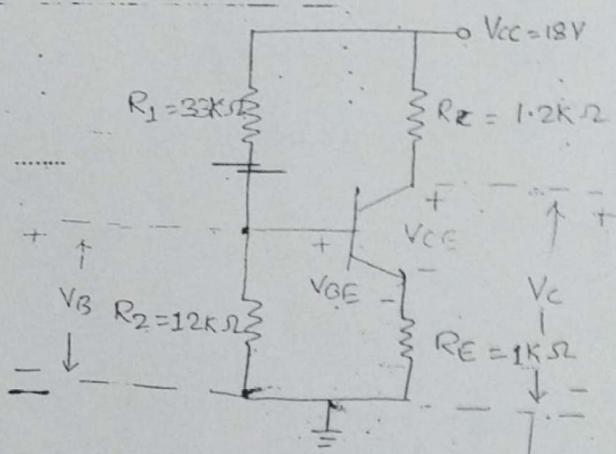
Problems on Voltage Divider Bias.

SHEKAR'S Pictures
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- 3) Analyse the voltage divider bias circuit shown below to determine emitter voltage V_E , V_C , V_B , I_C & V_{CE} . Assume $V_{BE} = 0.7V$. Draw the DC load line & mark the Q point.



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→ Since ' β ' is not given, we cannot find I_B . ∴ we have to use approximate analysis neglecting I_B .

$$\therefore V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{18 \times 12 \times 10^3}{33 \times 10^3 + 12 \times 10^3} = 4.8V$$

$$V_E = V_B - V_{BE} = 4.8 - 0.7 = 4.1V$$

Gold

$$I_E = \frac{V_E}{R_E} = \frac{4.1V}{1k\Omega} = [4.1mA]$$

$$[I_C \approx I_E = 4.1mA]$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 18V - (4.1mA)(1.2 + 1k\Omega)$$

$$= [8.98V]$$

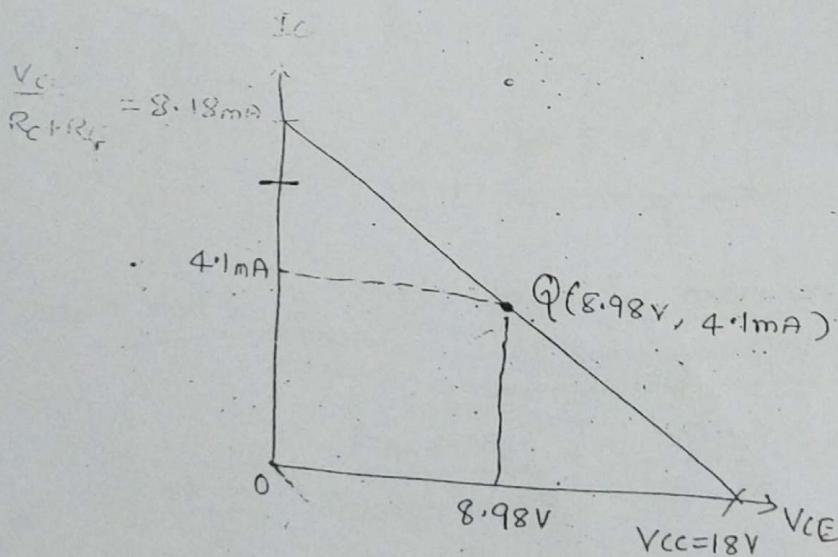
$$V_{CE} = V_{CE} + I_E R_E$$

$$= 8.98 + (4.1mA)(1k\Omega)$$

$$= [13.08V]$$

$$Q(V_{CE}, I_C) = Q(8.98V, 4.1mA)$$

Qpt is marked on the DC load line in the fig.



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Since B
- And

V_{CE}
 $\therefore Q($
 $\frac{V_{CC}}{R_C + R_E}$

2) A voltage divider bias circuit has

$$V_{CC} = 15V, R_C = 2.7K\Omega, R_E = 2.2K\Omega,$$

$$R_1 = 22K\Omega, R_2 = 12K\Omega. \text{ Calculate } V_E, V_C, I_C \text{ & } V_{CE}$$

DC load line & mark the Q pt. Take $V_{BE} = 0.7V$.

Soln: Given

$$V_{CC} = 15V, R_C = 2.7K\Omega, R_E = 2.2K\Omega, R_1 = 22K\Omega, \\ R_2 = 12K\Omega, V_{BE} = 0.7V.$$

Since B is not given, hence neglect I_B & choose Approximate Analysis method.

$$V_E = \frac{V_{CC}R_2}{R_1+R_2} = \frac{15 \times 12K\Omega}{2.2K\Omega + 12K\Omega} = [5.29V]$$

$$I_E = \frac{V_E}{R_E} = \frac{4.59V}{2.2K\Omega} = [2.09mA]$$

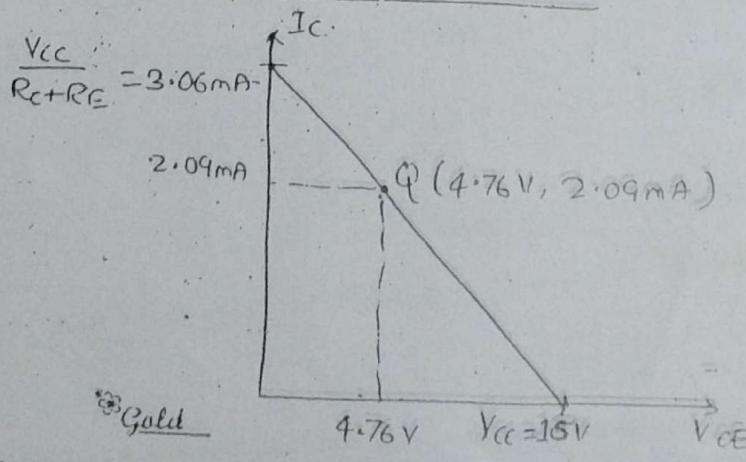
$$[I_C \approx I_E = 2.09mA]$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 15V - (2.09mA)(2.7 + 2.2)K\Omega = [4.76V]$$

$$\rightarrow V_C = V_{CE} + V_E = 4.76V + 4.59V = [9.35V]$$

$\therefore Q(V_{CE}, I_C) = Q(4.76V, 2.09mA)$.



Q) A voltage divider bias circuit has $V_{CC} = 18V$, $R_1 = 33k\Omega$, $R_2 = 12k\Omega$, $R_E = 1k\Omega$, $R_C = 1.2k\Omega$, $\beta = 50$. Taking $V_{BE} = 0.7V$, find V_E , I_C , V_{CE} & V_C . Draw the DC load line & locate the Q-point.

Given

$$V_{CC} = 18V, V_{BE} = 0.7V, \beta = 50$$

$$R_1 = 33k\Omega, R_2 = 12k\Omega, R_C = 1.2k\Omega, R_E = 1k\Omega$$

Since β is given, I_B can be calculated. Hence we can use exact or accurate analysis.

$$V_T = V_{CC} R_2$$

$$R_1 + R_2 = \frac{18V \times 12k\Omega}{33k\Omega + 12k\Omega} = 4.8V$$

$$\frac{R_1 R_2}{R_1 + R_2} = \frac{33k\Omega \times 12k\Omega}{33k\Omega + 12k\Omega} = 8.8k\Omega$$

$$I_B = \frac{V_T - V_{BE}}{R_T + (1+\beta) R_E}$$

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$$I_B = \frac{4.8V - 0.7V}{8.8k\Omega + (1+50)(1k\Omega)} = 0.0686 \text{ mA}$$

$$I_E = \beta I_B = (50)(0.0686 \text{ mA}) = 3.43 \text{ mA}$$

$$V_E = I_E R_E = (3.43 \text{ mA})(1k\Omega) = 3.43V$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 18V - (3.43 \text{ mA})(1.2k\Omega) - (3.43 \text{ mA})(1k\Omega)$$

$$= 10.38V$$

$$\frac{V_{CC}}{R_C + R_E}$$

4) B

Also

$$R_1 = 6$$

$$\beta = 8$$

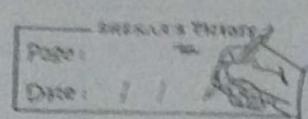
Soln

Since analysis

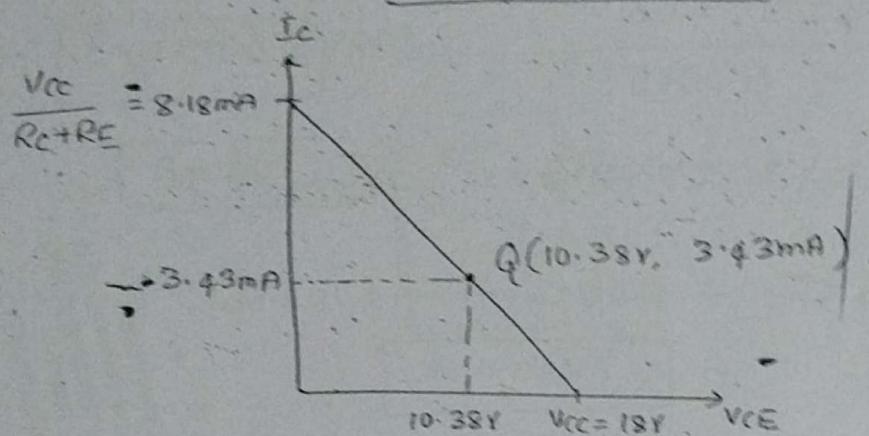
R_T

33k Ω

$$\begin{aligned} V_C &= V_{CE} + V_E \\ &= 10.38V + 3.5V \\ &= 13.88V \end{aligned}$$



$$Q(V_{CE}, I_C) = Q(10.38V, 3.43mA)$$



4) Determine I_C & V_{CE} for the voltage divider bias method.

Also draw the dc load line with Q-point Given in

$$R_1 = 62k\Omega, R_2 = 9.1k\Omega, R_C = 3.9k\Omega, R_E = 0.68k\Omega,$$

$$\beta = 80, V_{BE} = 0.7 \text{ & } V_{CC} = 16V$$

Soln: Given: $R_1 = 62k\Omega, R_2 = 9.1k\Omega, R_C = 3.9k\Omega$...
 $R_E = 0.68k\Omega, \beta = 80, V_{BE} = 0.7, V_{CC} = 16V$.

Since ' β ' is given, calculate I_B by selecting Accurate analysis method.

$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{16 \times 9.1k\Omega}{62k\Omega + 9.1k\Omega} = \frac{145600}{71100} = 2.047V$$

$$\begin{aligned} R_T &= \frac{R_1 R_2}{R_1 + R_2} = \frac{62k\Omega \times 9.1k\Omega}{62k\Omega + 9.1k\Omega} \\ &= \frac{564200000}{71100} = 7.935k\Omega \end{aligned}$$

Q_{point}

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$$\frac{1.347}{63015} = 0.0213 \text{ mA}$$

$$I_{CO} = \beta I_B = 20 \times 0.0213 \times 10^{-3} = 1.704 \text{ mA}$$

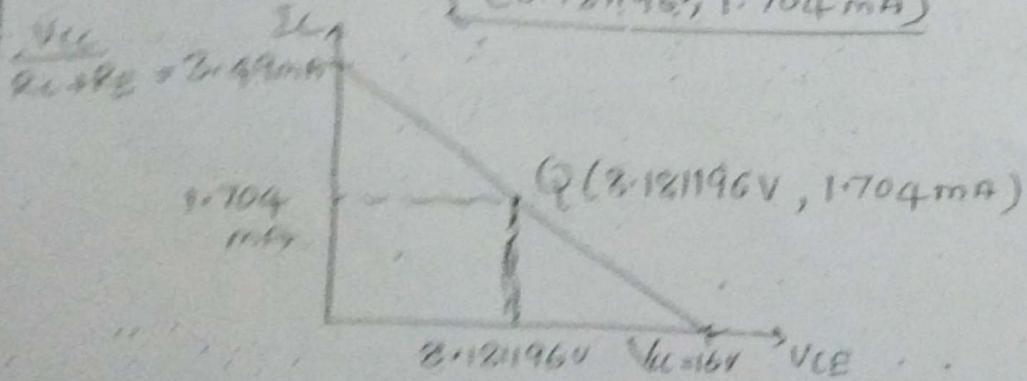
$$I_{\text{m}} = I_{G51C} = 0.0213 \text{ mA} + 1.704 \text{ mA} \\ = 1.7253 \text{ mA}$$

$$V_E = I_{CER} R_E = 1.7253 \text{ mA} \times 0.68 \text{ k}\Omega$$

$\approx 1.1732 \text{ V}$

$$V_C = T_{CE} + V_E = 8.181196 + 1.1732 \\ = 9.354 \text{ V}$$

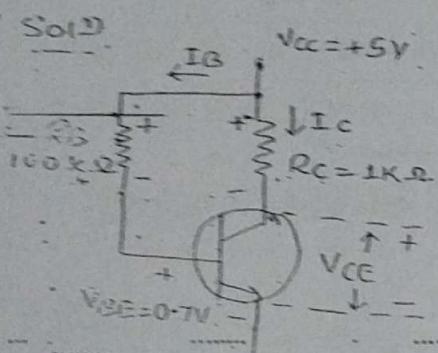
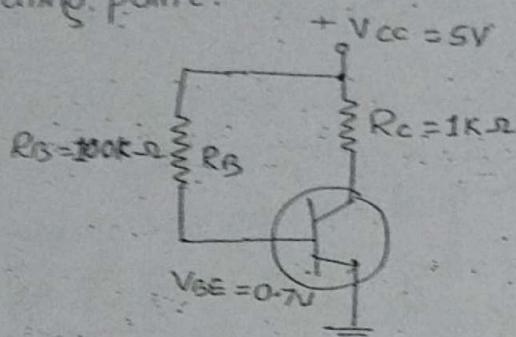
$$Q(100, I_0) = Q(2.121196V, 1.704mA)$$



Problem on DC load line & Bias Point

Date: 11/1/2023

- 1) For the ckt diagram shown below, a si transistor with $\beta = 50$ is used. Draw the dc load line & determine the operating point.



Applying KVL to base ckt, we have

$$+V_{CC} - I_B R_B + V_{BE} = 0$$

$$-I_B R_B - V_{BE} + V_{CC} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{5 - 0.7}{100 \times 10^3} = 43 \mu A$$

$$I_C = \beta I_B = 50 \times 43 \times 10^{-6} = 2.15 \text{ mA}$$

$$I_{CQ} = 2.15 \text{ mA}$$

Applying KVL to collector ckt, we have

$$-I_C R_C - V_{CE} + V_{CC} = 0 \quad \text{or} \quad V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C = 5 - 2.15 \times 10^{-3} \times 1 \times 10^3 = 2.85 \text{ V}$$

$$\therefore V_{CEQ} = 2.85 \text{ V}$$

$V_{CE} = (\text{Supply voltage}) - (\text{Voltage drop across } R_C)$

$$V_{CE, \text{gold}} = V_{CC} - I_C R_C$$

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To get two points on the load line,

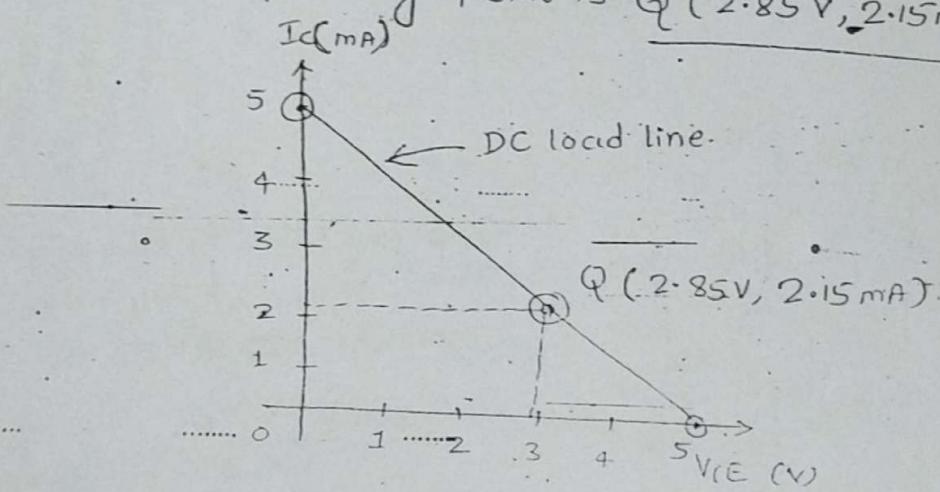
a) $V_{CE} = V_{CC}$, $I_C = 0$,

So A (5, 0)

b) $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} = 5 \text{ mA}$

∴ B (0, 5 mA)

Through A & B, load line can be drawn as shown below, The operating point is Q (2.85 V, 2.15 mA).



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UNIT 6 II

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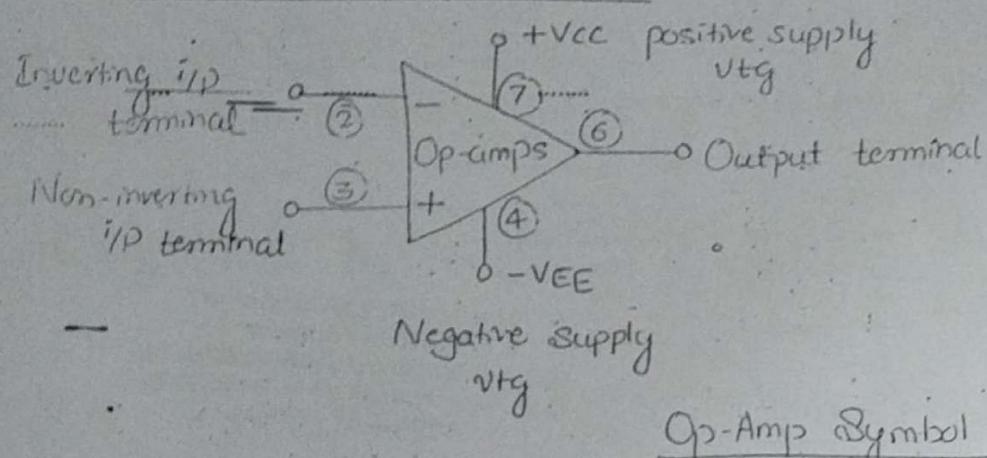
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OPERATIONAL AMPLIFIERS:

Introduction

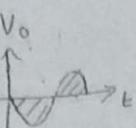
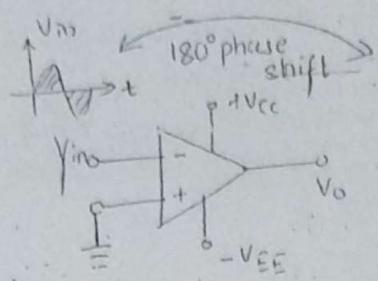
- The operational amplifier, most commonly referred as 'op-amp' was introduced in 1940s.
- In those days, it was used in the analog computers to perform a variety of mathematical operations such as addition, subtraction, multiplication etc.
- Due to its use in performing mathematical operations it has been given a name operational amplifier.

Op-amp Symbol & Terminals



Op-Amp Symbol

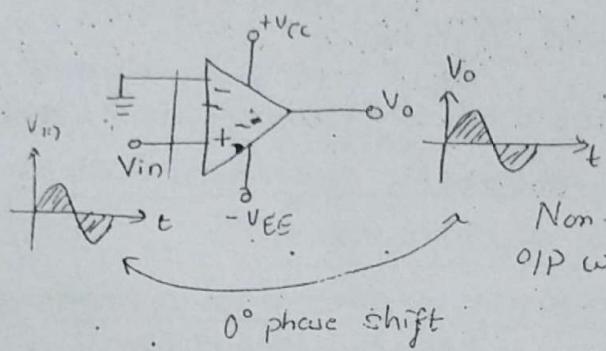
- The op-amp is indicated basically by a triangle which points in the direction of the signal flow.
- All the op-amps have minimum following five terminals:
 - 1) +ve supply vtg terminal $+V_{CC}$ or $+V$.
 - 2) -ve supply vtg terminal $-V_{EE}$ or $-V$.
 - 3) The o/p terminal.
 - 4) The inverting i/p terminal, - symbol
 - 5) The non-inverting i/p terminal, + symbol.



→ The i/p at inverting i/p terminal results in opposite polarity O/P.

Inverted O/P
with respect
to i/p..

→ The i/p & O/P are
in out phase having
180° phase difference
in between them.



Non-Inverted
O/P wrt i/p.

→ The i/p at
non-inverting i/p
terminal results

in the same
polarity O/P.

→ The i/p & O/P are in
Inphase having 0° phase
difference in betw them.

The op-amp works on a dual Supply (two dc supply).

→ The dual supply generally balances the vtgs of the +Vcc & -VEE are same in magnitude.

→ The typically commercially used power supply vtgs are $\pm 15V$.

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Ideal Opamp

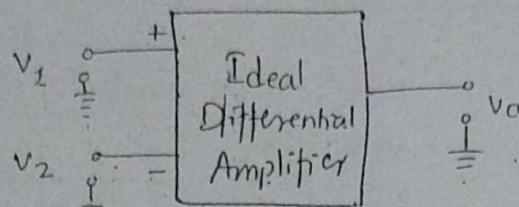
Function of Differential amplifier

→ The ideal opamp is basically an amplifier which amplifies the difference betw the two i/p signals.

→ Hence it is called the differential amplifier or difference amplifier.

i/p i/p
opposite

acc
having
difference.



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- V_1 & V_2 are two i/p signals while V_o is the single o/p.
- Each signal is measured with respect to the ground.
- In an ideal differential amplifier, the o/p v.tg V_o is proportional to the difference b/w two i/p signals.

$$V_o \propto (V_1 - V_2)$$

Differential Gain.

- From the above eqn, we can write, $V_o = A_d(V_1 - V_2)$
where A_d is constant of proportionality.
- A_d is the gain with which differential amp. amplifies the difference b/w two i/p signals. Hence it is called Differential Gain, A_d .

- The difference b/w the two signals $(V_1 - V_2)$ is generally called difference voltage & denoted as V_d .

$$V_o = A_d V_d$$

$\therefore A_d$ can be expressed as

$$A_d = \frac{V_o}{V_d}$$

- Generally A_d is expressed in dB value as,

$$A_d = 20 \log_{10}(A_d) \text{ in dB}$$

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Gold

Common Mode Gain, A_c

- If we apply two i/p vtgs which are equal in all the respects to the differential amplifier i.e., $V_1 = V_2$, ideally the o/p vtg must be equal to zero.
- But the o/p vtg of the practical differential amp. not only depends on the difference vtg, but also depends on the avg. common level of the two inputs.
- Such an avg. level of the two i/p signals is called Common mode Signal denoted as V_c .

$$V_c = \frac{V_1 + V_2}{2}$$

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- Practically, the differential amp. produces the o/p proportional to such common mode signal, also.
- The gain with which op-amp amplifies common mode signal to produce the o/p is called Common Mode Gain, A_c .

$$V_o = A_c V_c$$

So the total o/p of any differential amp. can be

$$V_o = A_d V_d + A_c V_c$$

Common Mode Rejection Ratio (CMRR)

- The ability of an op-amp to reject a common mode signal is expressed by a ratio called common mode rejection ratio, denoted as CMRR or P .

- For ideal op-amp, the diff. gain A_d must be infinite while the A_c must be zero.

Offset Null	<input type="checkbox"/>	1
Inv. i/p	<input type="checkbox"/>	2
Non Inv. i/p	<input type="checkbox"/>	3
$V_{(C-VEE)}$	<input type="checkbox"/>	4
	<input type="checkbox"/>	5
	<input type="checkbox"/>	6
	<input type="checkbox"/>	7
	<input type="checkbox"/>	8
	<input type="checkbox"/>	9
	<input type="checkbox"/>	10

→ It is defined as the ratio of the differential voltage gain A_d , to common mode voltage gain A_c .

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$$CMRR = P = \left| \frac{A_d}{A_c} \right|$$

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→ Ideally the A_c is zero, hence the ideal value of CMRR is infinite.

→ Many a times, CMRR is also expressed in dB as

$$CMRR \text{ in } dB = 20 \log \left| \frac{A_d}{A_c} \right| dB$$

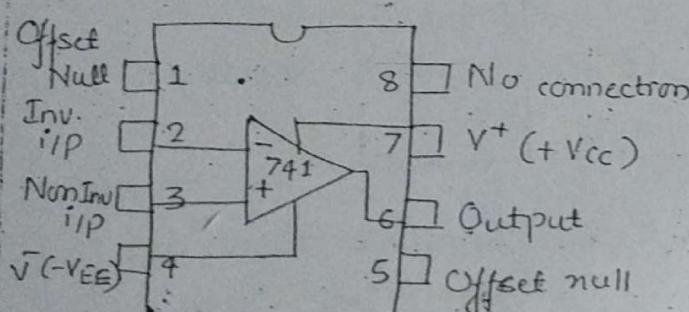
Op-amp IC 741

→ A very popular IC version of op-amp is IC 741.

→ Various Op-amps named MC1741, LM741 etc.

→ For convenience, widely used Op-amp IC is IC 741 opamp dropping the prefixes.

Pin Diagram



→ IC 741 is 8-pin IC available in dual in line package (DIP).

→ The pins 1 & 5 are offset null pins.

They used to nullify the offset voltages and provide offset voltage compensation.

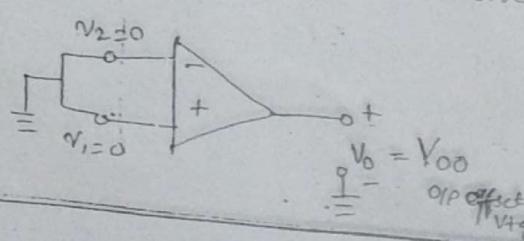
→ Pin 8 is the dummy pin & no connection has to be made to this pin externally.

Ideal Vs Practical Characteristics of IC 741 Op-amp.

Sr. No.	Parameter	Symbol	Ideal	Typical for 741 IC
1	Open loop v _{tg} gain	A _{OL}	∞	2×10^5
2	O/I P Impedance or O/P Resistance	Z _{out}	0	75 Ω
3	Input Impedance or I/P Resistance	Z _{in}	∞	2 MΩ
4	Input offset current	I _{ios}	0	20 nA
5	Offset v _{tg}	V _{ios}	0	2 mV
6	Bandwidth	B.W	∞	1 MHz
7	CMRR	P	∞	90 dB
8	Settling rate	S or SR	∞	0.5 V / usec
9	Input Bias Current	I _B	0	80 nA
10	Power Supply rejection ratio	P.S.R.R	0	30 μV/V

Output offset voltage: It is defined as the dc output voltage of op-amp when both its input terminals are grounded i.e., $v_1 = v_2 = 0$

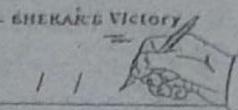
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CHARACTERISTICS

Open loop

1) Voltage gain: It is the v_{tg} gain of op-amp when no feedback is applied.



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O/P Impedance/Resistance

Ideal: $R_o = 0$, this ensures that the o/p v_{tg} of op-amp remains same, irrespective of the value of load resistance connected.

Practical: It is few hundred Ohms. With the help of -ve feedback it can be reduced to very small value like $1\text{ or }2\Omega$.

Input Impedance/Resistance

Ideal: $R_{in} = \infty$, this ensures no current flow into an ideal op-amp.

Practical: It is finite & typically $\geq 1\text{ M}\Omega$. But using FETs for the i/p stage, it can be increased upto several hundred $\text{M}\Omega$.

Input offset Voltage

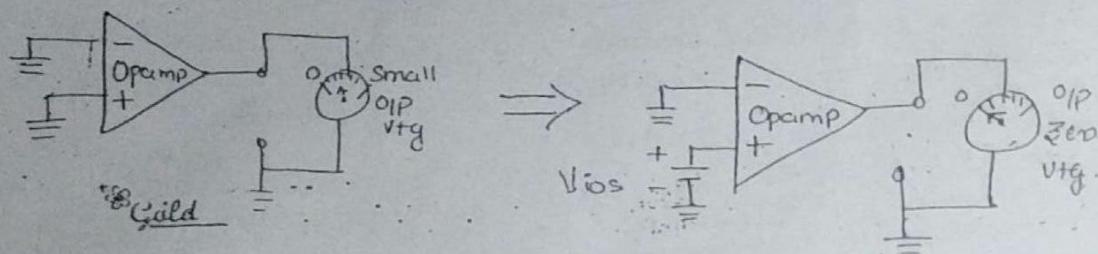
Ideal: $V_{ios} = 0$. The presence of small o/p v_{tg} though $v_1 = v_2 = 0$ is called offset v_{tg}. This ensures zero o/p v_{tg} for zero i/p v_{tg}.

Practical: Whenever both i/p terminals of the op-amp

are grounded ideally, V_o should be zero but practically shows a small non-zero o/p v_{tg}.

→ To make this o/p v_{tg} zero, a small v_{tg} in mV's is required to be applied to one of the i/p terminals which makes the o/p v_{tg} zero, when the other terminal is grounded.

→ The i/p offset v_{tg} depends on the temperature.



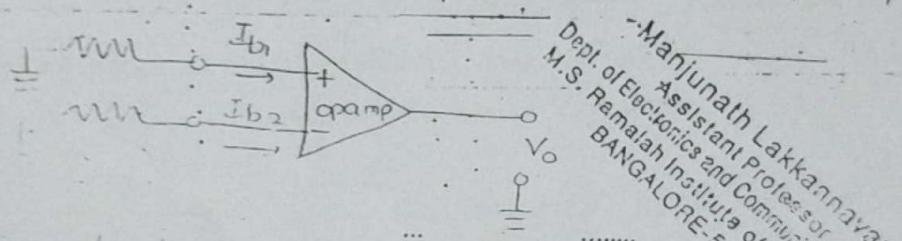
5) Input Bias Current

Ideal: No current flows into the i/p terminals.

Practical: have i/p currents of the order of $10^{-6} A$ to $10^{-9} A$.

Mostly the op-amps use differential amp. as the i/p stage using the transistors.

- Two transistors of the diff-amp must be perfectly matched & biased correctly. But practically it is not possible
- Thus, there exists small dc current, called bias currents as I_{b1} & I_{b2} .
- So, Input Bias current can be defined as the current flowing into each of the two i/p terminals when they are biased to the same vtg level. i.e., when op-amp is balanced.



Mathematically I_b is expressed as

$$I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$$

Input bias current.

6) Input offset current:

The difference in magnitudes of I_{b1} & I_{b2} is called as i/p offset current, I_{ios} . Thus

$$I_{ios} = |I_{b1} - I_{b2}|$$

Problem: For a particular op-amp, $I_{ios} = 20\text{nA}$, $I_b = 60\text{nA}$. Calculate the values of two i/p bias currents.

Sol: $I_{ios} = 20\text{nA}$, $I_b = 60\text{nA}$.

$$I_{ios} = I_{b1} - I_{b2} = 20 \quad \& \quad I_b = \frac{I_{b1} + I_{b2}}{2} = 60$$

$$I_{b1} + I_{b2} = 120 \quad \text{re: } 2I_{b1} = 140 \quad \text{i.e. } I_{b1} = 70\text{nA} \quad \& \quad I_{b2} = 50\text{nA}$$

9) Pow
→ $\frac{dV}{dt}$
of the
Voltage
→ $\frac{dI}{dt}$
→ $\frac{dV}{dt}$

7) Bandwidth: The range of frequency over which the amp. performance is satisfactory is called its BW.

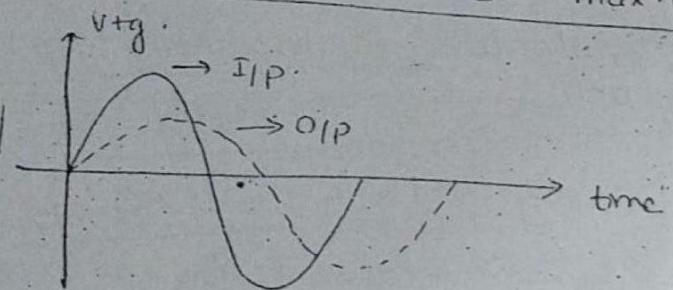
Ideal: $BW = \infty$ it means operating range is from 0 to ∞ . It ensures that the gain of op-amp will be constant over the freq. range

Practical: BW is very small, it can be increased by applying -ve feedback.

3) Slew Rate:

- When i/p voltage applied, o/p changes instantaneously then the o/p also must change rapidly as i/p changes
- If o/p does not change with the same rate as i/p then there occurs distortion in the o/p.
- So Slew rate or Max. Slew Rate (MSR) of the opamp is defined as the max. time rate of change of its o/p voltage,

$$\text{Slew Rate or MSR} = \frac{dV_o}{dt} \Big|_{\text{max.}}$$

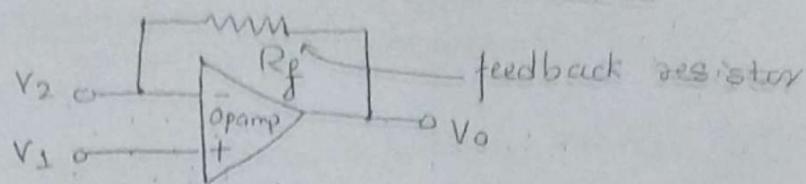


4) Power Supply Rejection Ratio (PSRR):

- The power supply rejection ratio is defined as the ratio of the change in i/p offset voltage due to the change in supply voltage producing it, keeping other power supply voltages constant
- It is called PSRR or Supply Voltage Rejection Ratio (SVRR)
- It is expressed in mV/V or $\mu\text{V/V}$.

$$PSRR = \frac{\Delta V_{io}}{\Delta V} \text{ mV/V}$$

Closed Loop Configuration of Op-amp



Some advantages of -ve feedback are

- 1) It reduces the gain & makes it controllable
- 2) It reduces the possibility of distortion.
- 3) It increases the bandwidth i.e., freq. range
- 4) It increases the i/p resistance of the op-amp
- 5) It decreases the o/p resistance of the op-amp
- 6) It reduces the effects of temp., power supply on the working of the ckt.

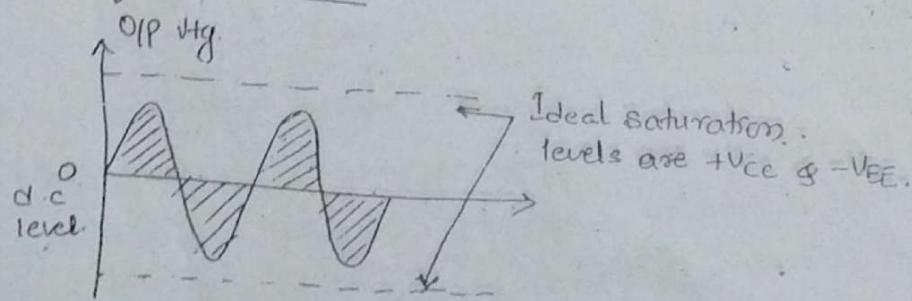
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Working Property of Op-amp

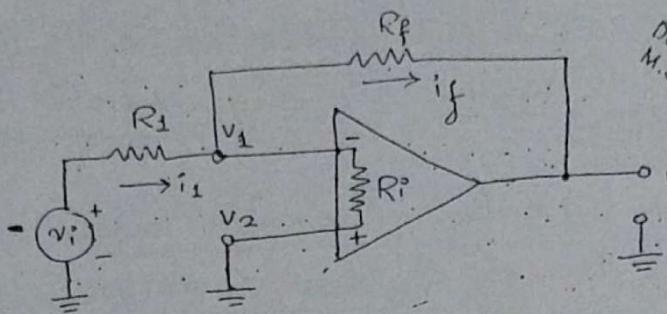
- Practically the op-amp saturates at the vtgs slightly less than the supply vtgs: $+V_{CC}$ & $-V_{EE}$.
- As the thumb rule, the maximum o/p vtgs may be taken as 1.5V less than the supply vtgs
- For typical supply vtgs $\pm 15V$, the o/p vtg is limited to a max of $\pm 13.5V$.



Concept of Virtual Short in an Opamp

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→ R_i represents the i/p resistance of Op-amp measured betw the inverting & non-inverting i/p terminals.

→ The V_o is given by -

$$\left. \begin{aligned} V_o &= A[V_2 - V_1] \\ \text{or } V_2 - V_1 &= \frac{V_o}{A} \end{aligned} \right\} \rightarrow (1)$$

where A is the open loop gain of op-amp

→ The o/p vtg V_o cannot exceed the DC supply vtg given to the op-amp.

→ For μA741 typical value of supply vtg is ±12V. A is 2×10^5 .

→ To get an o/p vtg of 10V by applying an i/p vtg vi'g say 1V, the required differential i/p vtg is

$$V_2 - V_1 = \frac{10V}{2 \times 10^5} + 0.5mV$$

→ This value is very small compared to the i/p & o/p vtgs & may be considered as 0V.

$$\left. \begin{aligned} \text{i.e., } V_2 - V_1 &\approx 0V \\ \therefore V_2 &= V_1 \end{aligned} \right\} \rightarrow (2)$$

→ From eqn (2), we find that inut i/p & non. inv i/p terminals are at the same potential i.e. appears to be tied together or shorted. ∴ Vtg across R_i is zero.

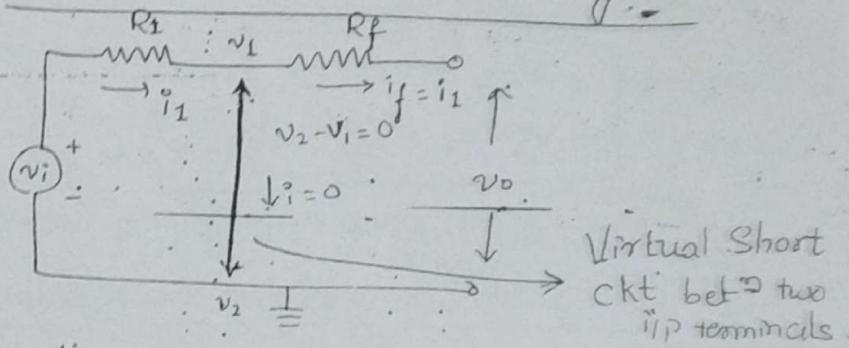
→ Further since R_i is very large ($2M\Omega$), current through R_i is zero.

Thus, the v_{tg} across R_i & the current through R_f are both zero.

If two terminals are physically shorted, the v_{tg} bet^D the two terminals will be zero & a large current flows through this short.

Since, the v_{tg} bet^D the i/p terminals is zero & no current flows through the short to the ground, we say that a virtual short exists bet^D the i/p terminals of Op-amp.

The virtual short is called the virtual ground.



Note that the same current flows through R_i & R_f. The concept of virtual concept is very much useful for the analysis of Op-amp ckt's.

Now, if the non-inv. terminal is grounded, by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection bet^D the inverting terminal and the ground. This is the principle of virtual ground.

The steps of analysis based on these assumptions are:

Step 1: Input current of the ideal opamp is always zero, Using this the current distribution in the circuit is obtained.

Step 2: The o/p terminals of the opamp are always at the same potential.

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Thus if one is grounded, the other can be treated to be virtually grounded. From this, the expressions for various branch currents can be obtained.

Step 3: Analyzing the various expressions obtained, eliminating unwanted variables, the o/p expression in terms of o/p & ckt parameters can be obtained.

Op-amp Applications:

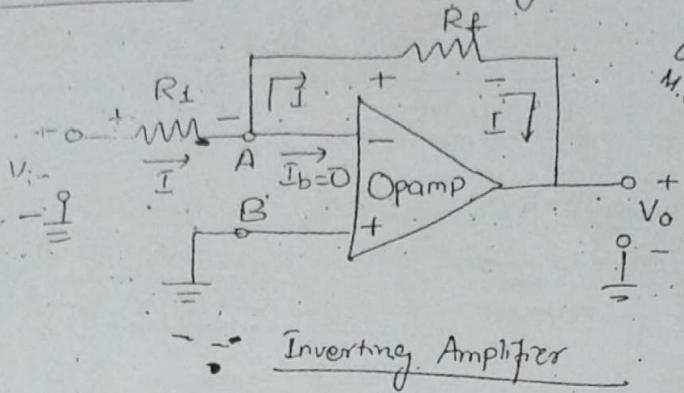
- The countless simple ckts using one or more op-amps, some external resistors & the capacitors can be constructed.
- Such op-amp appl'n's are classified as Linear & Non-linear type of applications.
- Linear applications: O/P vgt. varies linearly wrt o/p vgt. e.g. vgt follower, differential amp \pm , Inv. amp \pm , Non. Inv. Amp \pm etc.
- Non-linear Applications: Rectifiers, Comparators, Schmitt Trigger ckt etc

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Gold

Ideal Inverting Amplifier

An amplifier which provides a phase shift of 180° between input & output is called Inverting amplifier.



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→ By the concept of virtual ground, the two input terminals are always at the same potential.

→ At node B is grounded, node A is also at ground
 $\therefore V_A = 0$

$$\therefore \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \quad (\because V_A = 0) \rightarrow (1)$$

→ As opamp current is always zero hence entire current I passes through the resistance R_f .

→ Now from the O/P side, considering the direction of current 'I' we can write as;

$$I = \frac{V_A - V_o}{R_f} = -\frac{V_o}{R_f} \quad (\because V_A = 0) \rightarrow (2)$$

→ Equating (1) & (2) we get.

$$\frac{V_{in}}{R_1} = -\frac{V_o}{R_f}$$

$$\therefore \boxed{A_v = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}} \quad (\text{Gain with feedback}) \rightarrow (3)$$

Ideal

→ An
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amplifier

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Entered current passed through R_1 as i/p current
if opamp is zero.

→ Equating eqⁿ's. (1) & (2)

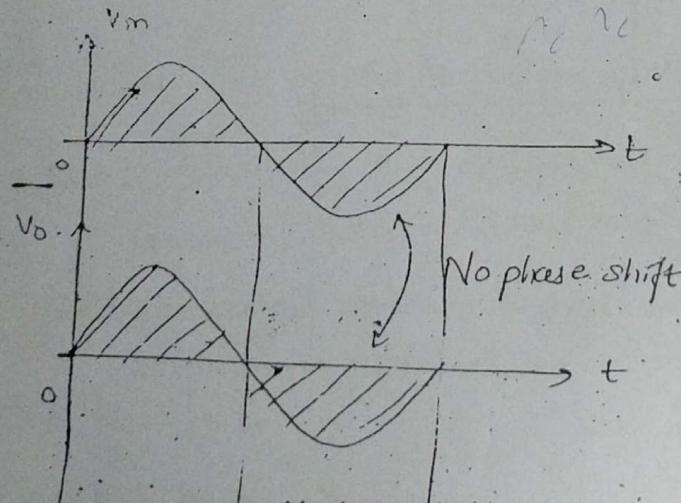
$$\frac{V_o - V_m}{R_f} = \frac{V_{in}}{R_1}$$

$$\frac{V_o}{R_f} = \frac{V_m}{R_f} + \frac{V_m}{R_1} = V_{in} \left[\frac{R_f + R_1}{R_f R_1} \right]$$

$$\frac{V_o}{V_{in}} = \frac{(R_1 + R_f) R_f}{R_1 R_f} = \frac{R_1 + R_f}{R_1}$$

$$A_v = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$$

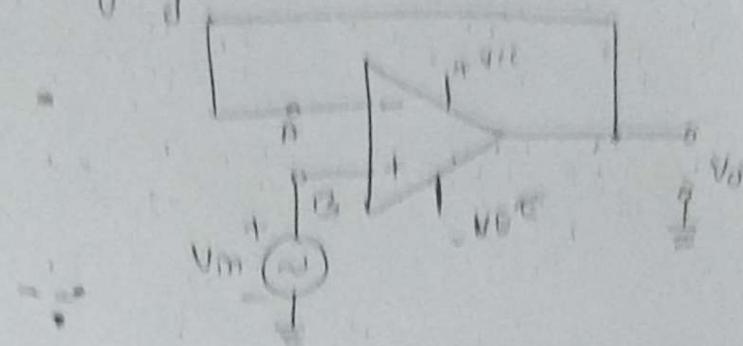
The sign indicates that there is no phase shift
i.e. i/p & o/p



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Voltage Follower

A circuit in which the output voltage follows the input voltage is called voltage follower circuit.



The node 'A' is virtual potential V_m .

$V_A = V_3 = V_m$ (as per virtual ground concept)

Node 'A' is directly connected to the op-amp.
Hence we can write, $\{V_o = V_A\}$ — (2)

Equating the eqns (1) & (2),

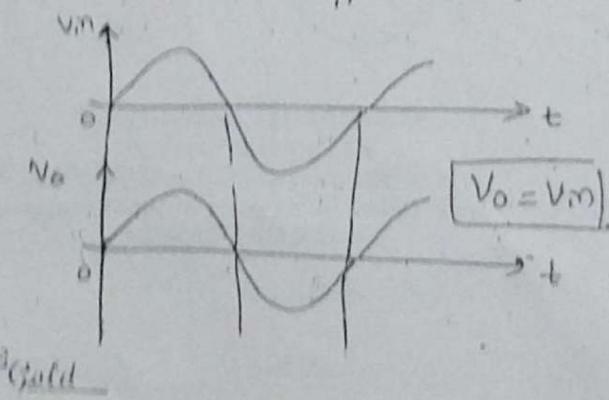
$$\{V_o = V_m\}$$

The voltage gain is Unity.

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The V_o is equal to V_m . If V_m increases, V_o also increases.
If V_m decreases, V_o also decreases.

It is also called Source follower, Unity gain amplifier, Buffer Amplifier, or Isolation amplifier.



Problems on Non Inverting & Inverting Amplifier.

1) A sine wave of 0.5V peak voltage is applied to an inverting amp using $R_1 = 10\text{ k}\Omega$, $R_f = 50\text{ k}\Omega$. If the supply voltage is $\pm 12\text{ V}$. Determine the O/P and sketch the waveform.

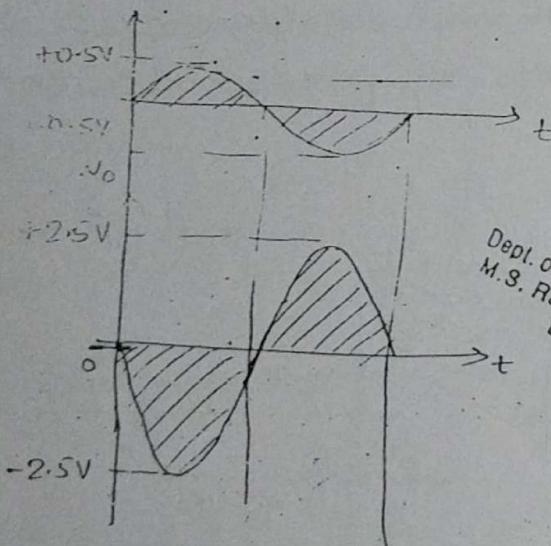
If now the magnitude amplitude of i/p sine wave is increased to 5V, what will be the O/P? Is it practically possible? Sketch the waveform.

Solⁿ: Case 1: For an inverting amp

$$G_{am} = \frac{V_o}{V_m} = -\frac{R_f}{R_1} = -\frac{50}{10} = [-5]$$

Now $V_m = 0.5\text{ V}$ for the i/p, hence

$$(V_o)_m = (V_m)_m \times G_{am} = 0.5 \times 5 = [2.5\text{ V peak}]$$



Case 2: Now $V_m = 5\text{ V}$ for the i/p hence,

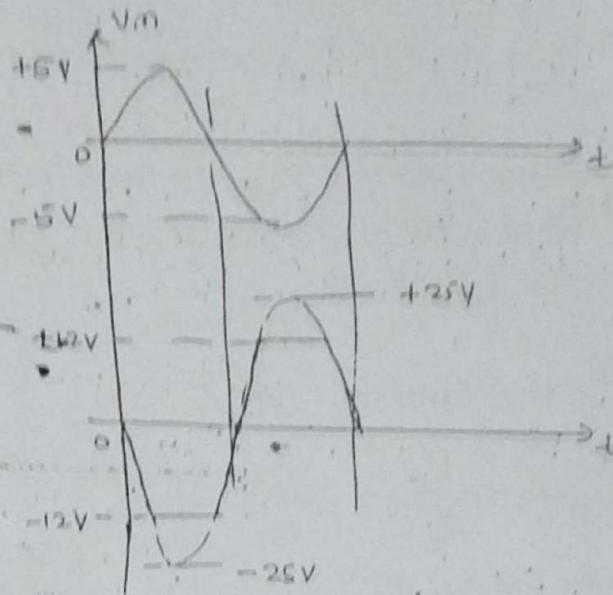
$$(V_o)_m = (V_m)_m \times G_{am} = 5 \times 5 = [25\text{ V peak}]$$

But opamp o/p saturates at $\pm 12\text{ V}$. i.e. at supply vgs used.

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→ So portion above +12V & below -12V will be clipped off from the O/P.

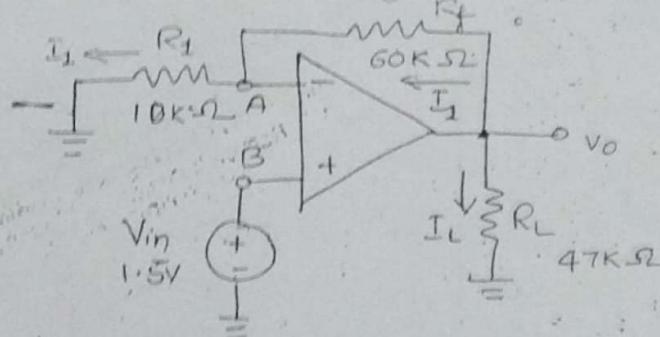
→ So 25V peak o/p is not possible practically.



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- 2) A non inverting amp has i/p resistance $10\text{ k}\Omega$ & feedback resistance $60\text{ k}\Omega$ with load resistance $47\text{ k}\Omega$. Draw the ckt & calculate O/P vtg, v_{tg} gain & load current when i/p vtg is 1.5V.

Sol: Given $R_i = 10\text{ k}\Omega$, $R_f = 60\text{ k}\Omega$, $R_L = 47\text{ k}\Omega$, $V_{in} = 1.5V$



The node 'B' is at V_{in} , hence due to virtual ground, the node 'A' is also at V_m $\Rightarrow V_B = V_A = V_m = 1.5V$

$$\therefore I_1 = \frac{V_A - 0}{R_1} = \frac{1.5}{10\text{ k}} = 0.15\text{ mA}$$

Ans: I_1 at R_f , $I_2 = \frac{V_o - V_A}{R_f} = \frac{V_o - 1.5}{60 \times 10^3} = 0.15 \times 10^{-3}$

$$\therefore V_o = 0.15 \times 10^3 \times 60 \times 10^3 + 1.5$$

$$= 10.5V$$

Output v_{tg}

$$\text{v.e.gain} = \frac{V_o}{V_{in}} = \frac{10.5}{1.5} = 7$$

Cross check that v_{tg} gain = $1 + \frac{R_f}{R_i}$

$$= 1 + \frac{60}{10} = 1 + 6 = 7$$

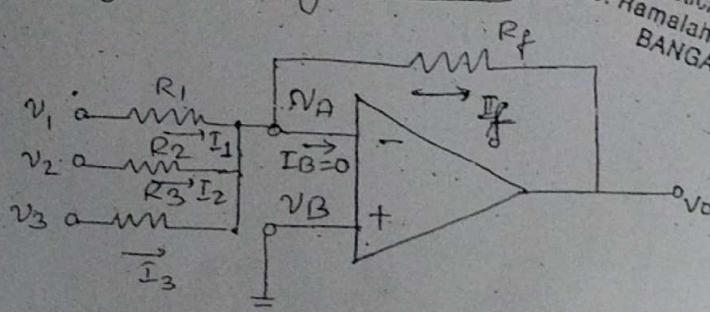
$$\therefore I_L = \frac{V_o}{R_L} = \frac{10.5}{47 \times 10^3} = 0.2234 \text{ mA}$$

Summing Amplifier or Adder Circuit:

→ The input impedance of an op-amp is extremely large so that one i/p signal can be applied to the inverting amp.

→ Such a circuit amplifies the addition of the applied signals at the o/p. Hence, it is summing amplifier or adder circuit.

Inverting Summing Amplifier



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Since $V_B = 0$, due to virtual short, $V_A = 0$

$$\therefore V_A = V_B = 0$$

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1}$$

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2}$$

$$I_3 = \frac{V_3 - V_A}{R_3} = \frac{V_3}{R_3}$$

$$I_f = \frac{V_A - V_O}{R_f} = -\frac{V_O}{R_f}$$

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Applying KCL at node A.

$$I_1 + I_2 + I_3 = I_f + I_A$$

$$I_1 + I_2 + I_3 = I_f \quad (\because I_A = 0)$$

Substituting the values, we get

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_O}{R_f}$$

$$V_O = \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

If we choose $R_f = R_1 = R_2 = R_3$, then

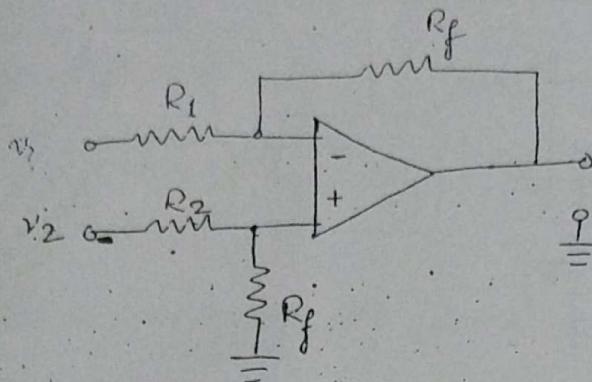
$$V_O = -[V_1 + V_2 + V_3]$$

The O/P v_O is equal to the -ve sum of i/p v_i's

R₂

Gold

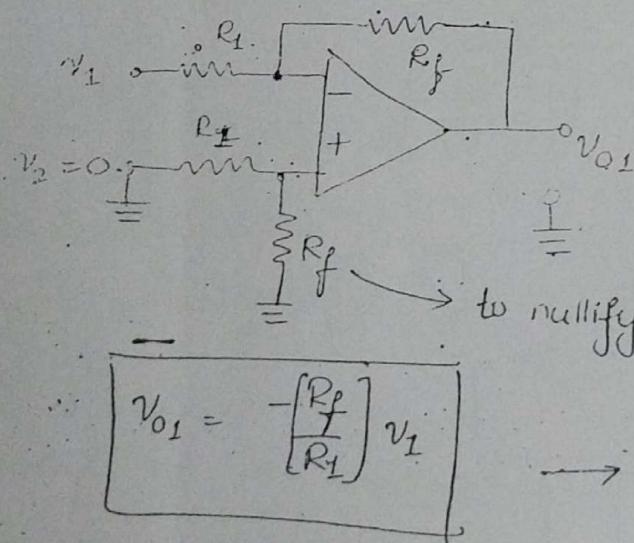
Difference Amplifier or Subtractor.



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Let us obtain the v_o using Superposition principle by applying the following steps.

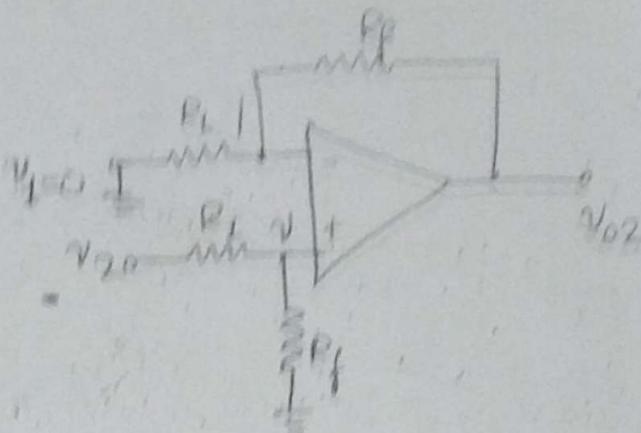
Step 1: Reduce v_2 to zero & find the o/p vtg due to v_1 .
 The resulting ckt is shown below which is nothing but an inverting amp.



→ (1)

Step 2: Reduce v_1 to zero & find the o/p vtg due to v_2 . The resulting ckt is shown below & which is nothing but a non-inverting amp.

Step 3



$$v_02 = v \times \text{Gain of non-inverting amp} \\ = v \cdot \left[1 + \frac{R_f}{R_1} \right] \quad \rightarrow (2)$$

v is the vtg drop across R_f , using vtg division rule

$$v = v_2 \cdot \frac{R_f}{R_1 + R_f} \\ v = v_2 \cdot \frac{R_f}{R_1 \left[1 + \frac{R_f}{R_1} \right]} \quad \rightarrow (3)$$

Substituting eqn (3) into (2) we have

$$v_{02} = v_2 \cdot \frac{R_f}{R_1 \left[1 + \frac{R_f}{R_1} \right]} \cdot \left[1 + \frac{R_f}{R_1} \right]$$

$$\boxed{v_{02} = v_2 \left[\frac{R_f}{R_1} \right]} \quad \rightarrow (4)$$

Step 3: Resulting o/p vtg is given by principle of Superposition.

$$v_o = v_{01} + v_{02}$$

$$v_{\text{Gold}} = -\frac{R_f}{R_1} v_1 + \frac{R_f}{R_1} v_2$$

Due to
short

$$v_o = \frac{R_f}{R_1} [v_2 - v_1] \rightarrow (5)$$

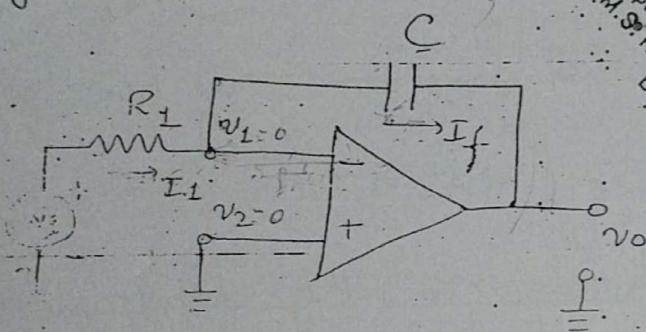
If we choose $R_f = R_1$ then

$$v_o = [v_2 - v_1] \rightarrow (6)$$

Subs

Hence the given ckt. works as subtractor.

Integrator



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where
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→ If
the

It has a capacitor in the feedback loop.

→ Since non-inverting i/p terminal is grounder, $v_2 = 0$.

→ Due to virtual ground we get $[v_1 = v_2 = 0]$.

→ Due to high i/p impedance of op-amp, the flows current into its inverting terminal is zero.

Same current flows through R & C .

$$\text{ie, } I_1 = I_f$$

But

$$I_1 = \frac{V_i - V_1}{R_f} = \frac{V_i}{R_f} \rightarrow (1)$$

$\rightarrow (2)$

→ The

i/p

→ If to

If thi

$$8 \quad I_f = C \frac{d}{dt} [v_i - v_o]$$

$$\boxed{I_f = -C \frac{dv_o}{dt}} \quad \rightarrow (3)$$

Substituting eqn. (2) & (3) into (1), we get

$$\frac{v_o}{R} = -C \frac{dv_o}{dt}$$

$$\therefore \frac{dv_o}{dt} = -\frac{1}{RC} v_o$$

Integrating both sides wrt 't' we have

$$v_o = -\frac{1}{RC} \int_0^t v_o dt + v_o(0) \quad \rightarrow (4)$$

where $v_o(0)$ is the initial voltage on the capacitor at $t=0$.

Note that $v_o(0)$ represents the constant of integration.

From eqn (4) we find that the o/p ~~is proportional to the integral of the i/p vgt v_i~~ is proportional to the integral of the i/p vgt v_i

If the initial vgt on the capacitor at $t=0$ is zero then $v_o(0) = 0$.

$$\boxed{v_o = -\frac{1}{RC} \int_0^t v_i dt}$$

The o/p of integrator is a Cosine waveform if an i/p is Sinusoidal

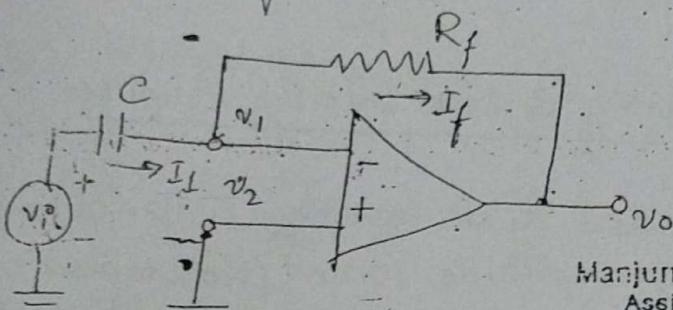
If the i/p is Step type, o/p is ramp type

If the i/p is Square wave, o/p is triangular wave

Gold

Differentiator

→ The ckt of op-amp differentiator can be obtained from op-amp integrator ckt by simply interchanging positions of R & C .



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Prob'l'm

1) Arm
an i/p

The o/p
Calculta

Sol(2)

Since $v_2 = 0$ & due to virtual ground concept.

$$\therefore [v_1 = v_2 = 0]$$

→ Due to high impedance of op-amp, current flow is $I_1 = I_f$.

$$\text{i.e., } I_1 = I_f \rightarrow (1)$$

But

$$I_1 = C \frac{d}{dt} [v_i - v_f] = C \frac{d v_i}{dt} \rightarrow (2)$$

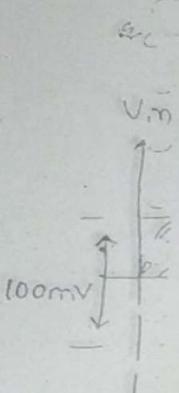
$$\& I_f = \frac{v_f - v_o}{R_f} = -\frac{v_o}{R_f} \rightarrow (3)$$

Using these eqns in (1), we get:

$$\frac{d v_i}{dt} = -\frac{v_o}{R}$$

$$\therefore v_o = -RC \frac{d v_i}{dt}$$

→ (4) The v_o is proportional to the time derivative of the v_i .



- The o/p of differentiator is a -ve cosine waveform if an i/p is sinusoidal.
- If i/p is step type, o/p is spike.
- If i/p is square wave, o/p is trailing impulses.

Problems on Inverting & Non Inverting Amplifiers

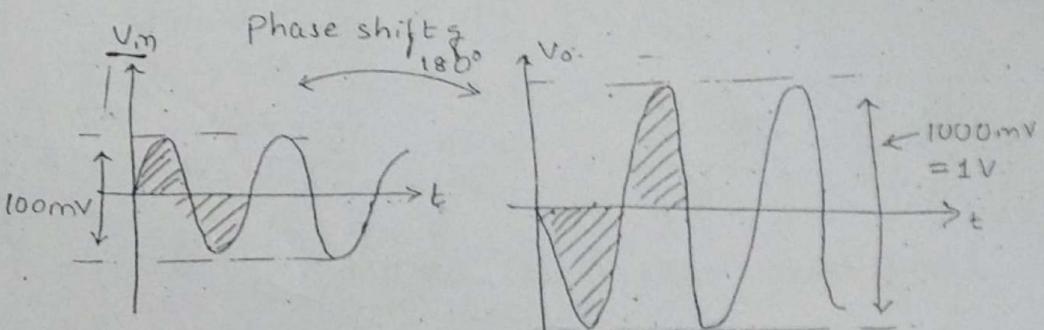
- 1) An op-amp is used as an inverting ampl. to amplify an i/p sine wave of amplitude 100mV (peak to peak). The i/p resistance $R_1 = 1\text{ k}\Omega$ & feedback resistance, $R_f = 10\text{ k}\Omega$. Calculate the v/o gain & sketch the o/p waveform to scale.

Sol⁽¹⁾: Given: $R_1 = 1\text{ k}\Omega$, $R_f = 10\text{ k}\Omega$, $V_m = 100 \times 10^{-3} \text{ V}$.

$$A_v = \frac{V_o}{V_m} = -\frac{R_f}{R_1} = -\frac{10 \times 10^3}{1 \times 10^3} = [-10]$$

$$V_o = -10 \times 100 \times 10^{-3} = [-1\text{ V}] = -1000\text{ mV}$$

The waveforms are shown below:



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Gull

The o/p of this ckt is given by.

$$V_o = - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

∴ required o/p is $V_o = - [3V_1 + 4V_2 + 5V_3]$

$$\therefore \frac{R_f}{R_1} = 3, \quad \frac{R_f}{R_2} = 4 \quad \text{&} \quad \frac{R_f}{R_3} = 5$$

Choose $R_f = 100\text{ k}\Omega$.

$$R_1 = 33.33\text{ k}\Omega, \quad R_2 = 25\text{ k}\Omega, \quad R_3 = 20\text{ k}\Omega$$

For

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Neat
Same as

Q) Design the opamp ckt which can give the o/p as
 $2V_1 - 3V_2 + 4V_3 - 5V_4$.

Hence
 V_{o2}
from

Sol: The +ve & -ve terms can be added separately
using two adders and then subtractor can be
used. $\therefore V_o = (2V_1 + 4V_3) - (3V_2 + 5V_4)$.

For $2V_1 + 4V_3$, let $R_{f1} = 100\text{ k}\Omega$.

$$\therefore V_{o1} = - \left[\frac{R_{f1}}{R_1} V_1 + \frac{R_{f1}}{R_3} V_3 \right]$$

$$\therefore \frac{R_{f1}}{R_1} = 2 \quad \text{&} \quad \frac{R_{f1}}{R_3} = 4$$

$$\therefore R_1 = \frac{200}{2} \quad \therefore R_3 = \frac{100}{4}$$

$$R_1 = 50\text{ k}\Omega$$

$$R_3 = 25\text{ k}\Omega$$

This is

$V_1 \rightarrow n$
 $V_3 \rightarrow n$

$V_2 \rightarrow m$
 $V_4 \rightarrow m$

For $3V_2 + 5V_4$, let $R_{f2} = 120\text{ k}\Omega$

$$V_{o2} = - \left[\frac{R_{f2}}{R_2} V_1 + \frac{R_{f2}}{R_4} V_3 \right]$$

$$V_{o2} = (-3V_2 - 5V_4)$$

$$\frac{R_{f2}}{R_2} = 3$$

$$\frac{R_{f2}}{R_4} = 5$$

$$R_2 = \frac{120}{3}$$

$$R_4 = \frac{120}{5}$$

$$R_2 = 40\text{ k}\Omega$$

$$R_4 = 24\text{ k}\Omega$$

Next, Use the Subtractor with all the resistances of same value of $R = 100\text{ k}\Omega$

Hence the O/P of the Subtractor is $V_o = V_{o2} - V_{o1}$ where V_{o2} & V_{o1} are the two i/p's of the Subtractor, derived from the previous adders.

The O/P V_{tg} is

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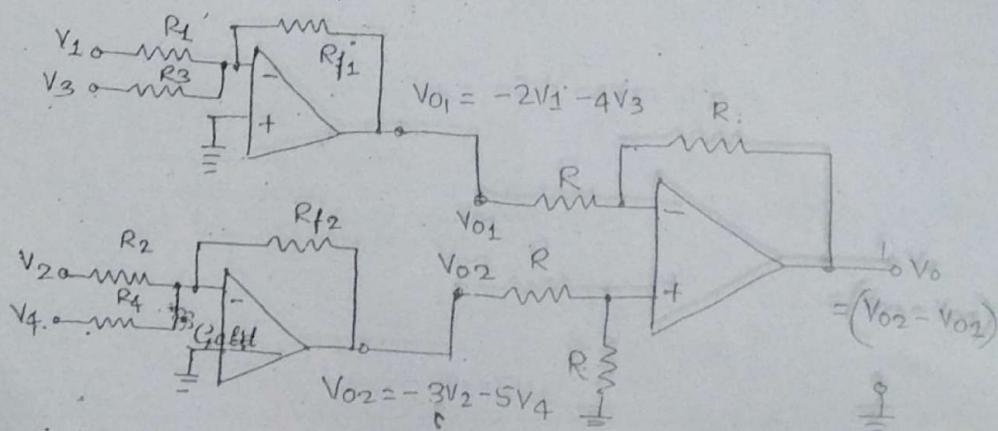
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$$V_o = V_{o2} - V_{o1} = (3V_2 - 5V_4) - (-2V_1 - 4V_3)$$

$$= -3V_2 - 5V_4 + 2V_1 + 4V_3$$

$$V_o = 2V_1 - 3V_2 + 4V_3 - 5V_4$$

This is required O/P.



4) Design an adder ckt using an Op-amp to obtain an o/p expression $V_o = 2(0.1V_1 + 0.5V_2 + 20V_3)$ where V_1, V_2 & V_3 are i/p's.

Prob

Soln:

$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right].$$

1) In ,

$\frac{R_f}{R_2}$

the

The above eqn consists of -ve sign but given O/P equation is not having any -ve sign. Hence O/P of inverting adder is given to a non-inverting amplifier.

Soln:

Given that $V_o = 2(0.1V_1 + 0.5V_2 + 20V_3)$

$$V_o = 0.2V_1 + V_2 + 40V_3.$$

Let us assume $R_f = 5K\Omega$, \therefore

$$\frac{R_f}{R_1} = 0.2 \Rightarrow R_1 = \frac{5K\Omega}{0.2} = 25K\Omega$$

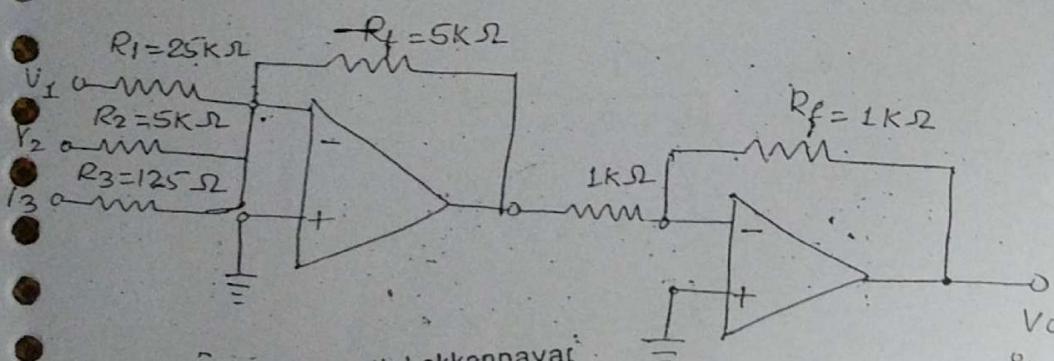
2) Q .

$$\frac{R_f}{R_2} = 1 \Rightarrow R_2 = \frac{5K\Omega}{1} = 5K\Omega$$

$$\frac{R_f}{R_3} = 40, \quad \therefore R_3 = \frac{5K\Omega}{40} = 125\Omega$$

Soln:

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Problems on Schmitt Trigger

Page:

Date:

- 1) In a symmetric inverting Schmitt Trigger ckt. If $R_2 = 47\text{ k}\Omega$. If the saturation vts are $\pm 14\text{ V}$, calculate the threshold vts V_{UT} & V_{LT} .

Solⁿ:

$$V_{UT} = \frac{R_1}{R_1+R_2} (+V_{sat}) = \frac{120(14)}{120+47 \times 10^3}$$

$$\boxed{V_{UT} = 35.7\text{ mV}}$$

$$\& V_{LT} = \frac{R_1}{R_1+R_2} (-V_{sat}) = \frac{120(-14)}{120+47 \times 10^3}$$

$$\boxed{V_{LT} = -35.7\text{ mV}}$$

- 2) Design an inverting op-amp Schmitt trigger with the following specification.

$$V_{UT} = 7\text{ V}, V_{LT} = 3\text{ V}, V_{sat} = \pm 15\text{ V}$$

Solⁿ:

The hysteresis vtg $V_H = V_{UT} - V_{LT} = 7 - 3 = 4\text{ V}$

Since $V_{sat} = \pm 15\text{ V}$

$$\therefore V_H = \frac{2R_1}{R_1+R_2} V_{sat}$$

$$4\text{ V} = 2 \left(\frac{R_1}{R_1+R_2} \right) 15$$

$$\therefore \frac{R_1}{R_1+R_2} = \frac{4\text{ V}}{30} = 0.133$$

$$\text{Or } R_1 = 0.133R_1 + 0.133R_2$$

$$R_1(1 - 0.133) = 0.133R_2$$

$$\therefore \frac{0.867R_1}{R_2} = 0.133R_2$$

$$\therefore R_2 = 6.518R_1$$

Select $R_1 = 1.8K$, then $R_2 = 11.74K \approx 12K$ (standard value).

$$\begin{aligned} R_{\text{comp}} &= R_1 || R_2 = 1.8K || 11.74K \\ &= \frac{1.8 \times 11.74}{1.8 + 11.74} \\ &= 1.5607K \end{aligned}$$

$R_{\text{comp}} \approx 1.5K$ standard value.

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3) Jr
Schm

n/w

$\pm 12V$

Soln

(standard
value).

3) In a symmetrical inverting Schmitt Trigger calculate the values of feedback w/o resistors R_1 & R_2 if the saturation voltages are $\pm 12V$ & the hysteresis width is $5V$.

Soln.: Since saturation vtgs are equal in magnitude
value.

$$V_H = \frac{2R_1}{R_1 + R_2} (V_{sat})$$

$$5 = \frac{2R_1}{R_1 + R_2} (12)$$

$$\text{i.e., } \frac{R_1}{R_1 + R_2} = \frac{5}{24} = 0.21$$

$$R_2 = 3.76 R_1$$

Selecting $[R_1 = 10K]$, we have

$$R_2 = 37.6 K$$

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B Gold

Signal Conversion Using OP-AMP

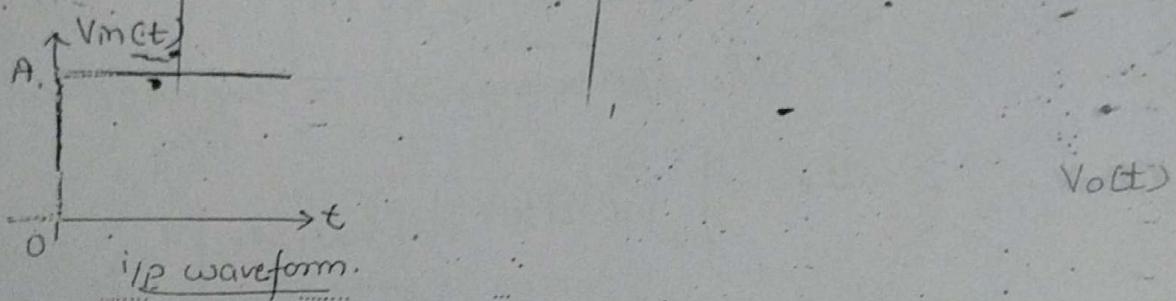
(b) 83.

(1) Integrator

For simplicity, consider the time constant

$$R'C = 1 \quad \text{& initial O/P vgt } V_o(0) = 0V.$$

(a) Step Input Signal



A step i/p signal with a magnitude of ' A ' volts applied at i/p & it can be expressed as

$$V_{in}(t) = -A \quad \text{for } t \geq 0$$

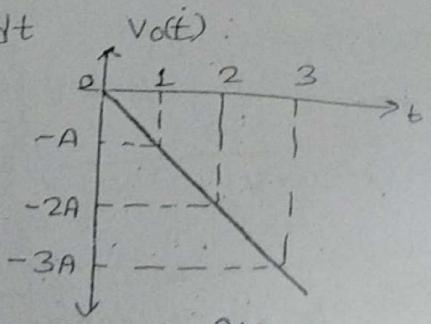
$$V_{in}(t) = 0 \quad \text{for } t < 0$$

$$V_o(t) = - \int_0^t V_{in}(t) dt$$

$$V_o(t) = - \int_0^t A dt$$

$$V_o(t) = - A \int_0^t dt$$

$$V_o(t) = - A [t]_0^t$$



The o/p voltage is decreasing to -ve maximum at ' t ' increases.

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(b) Square Wave Input Signal

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→ The square wave signal can be made up of step signals ie, a step of +ve 'V' volts between time 0 to $T/2$ & step of -ve 'V' volts between time $T/2$ to T & it repeats. It can be expressed as

$$V_{in}(t) = V, \quad 0 \leq t \leq T/2$$

$$V_{in}(t) = -V, \quad T/2 \leq t \leq T$$

∴ The o/p voltage can be expressed as

$$V_{o(t)} = - \left[\int_0^{T/2} V_{in}(t) dt + \int_{T/2}^T V_{in}(t) dt \right]$$

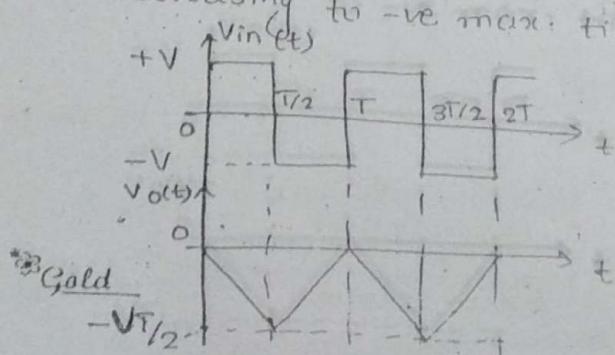
$$= \left[\int_0^{T/2} V dt + \int_{T/2}^T (-V) dt \right]$$

$$= \left[V \int_0^{T/2} dt - V \int_{T/2}^T dt \right]$$

$$V_{o(t)} = - V \int_0^{T/2} dt + V \int_{T/2}^T dt$$

$$V_{o(t)} = -V [t]_0^{T/2} + V [t]_{T/2}^T$$

The o/p is decreasing to -ve max till $T/2$ & it increases till 'T'



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c) Sine wave Input Signal

(2)

$$V_{in}(t) = V_m \sin \omega t$$

where V_m = peak amplitude

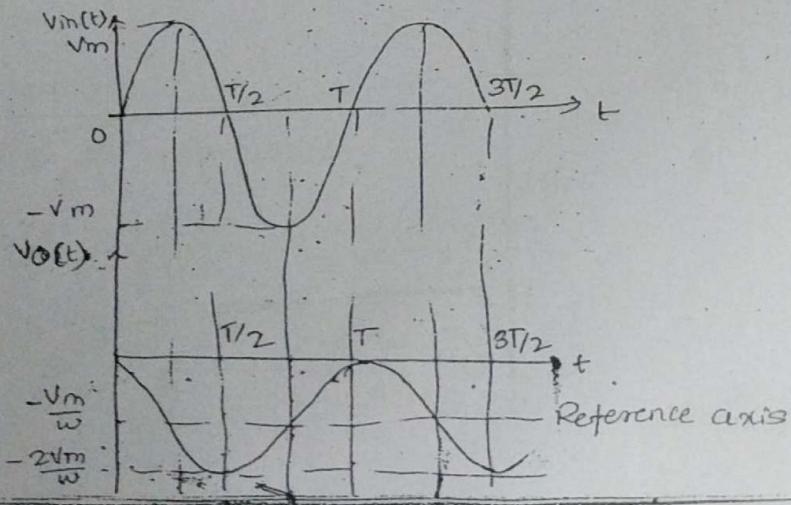
ω = angular freq. in rad/s.

The op. vgt is given by.

$$\begin{aligned} V_{o(t)} &= \int V_m(t) dt \\ &= - \int V_m \sin \omega t dt \\ &= -V_m \int \sin \omega t dt \\ &= -V_m \left[-\frac{\cos \omega t}{\omega} \right] \\ &= -\frac{V_m}{\omega} (-\cos \omega t) \end{aligned}$$

$$V_{o(t)} = +\frac{V_m}{\omega} \cos \omega t$$

The op. of an integrator is a cosine waveform for a sine wave i/p signal & both the waveforms shown below.



Simpl
and

Effect
 V_o
not at
 $t=$

(2) Differentiator

Page: / / = 

For simplicity of understanding, assume that the values of R & C are selected to have a time constant in unity i.e., $CR = 1$.

a) Step Input Signal

$$V_{in}(t) = V \text{ for } t > 0$$

$$V_{in}(t) = 0 \text{ for } t < 0$$

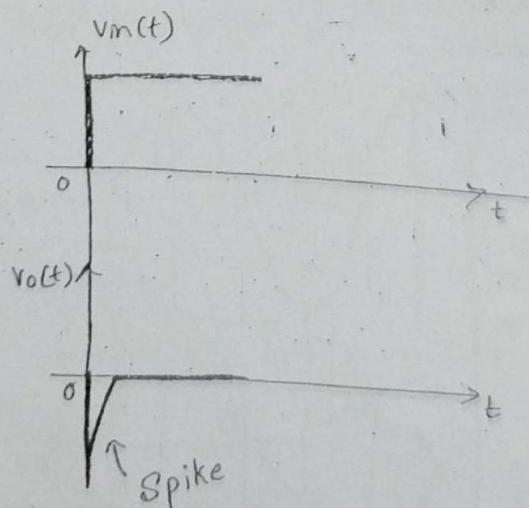
As from o/p equation.

$$V_o = -\frac{dV_m}{dt} = -\frac{dV}{dt}$$

Since the magnitude of step i/p 'V' is constant and constant of differentiation is zero i.e.,

$$V_o(t) = 0$$

Actually the step take a finite time to rise from '0' volts. Due to this time, the differentiator o/p is not zero, instead it appears in the form of spikes at $t=0$.



Guld

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(b) Square Wave Input Signal

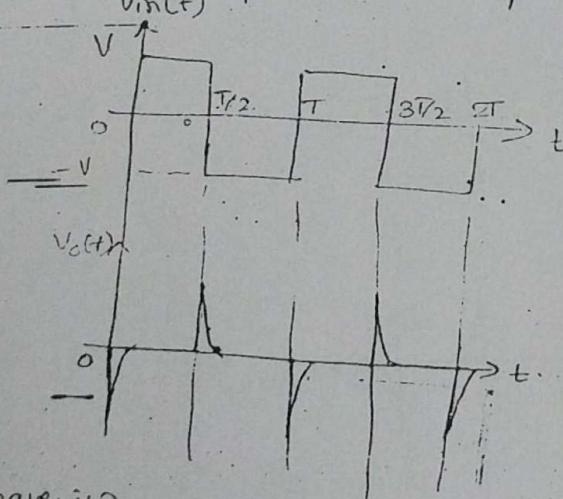
As we know, a square wave is made by a step signal of $+V$ volts from $t=0$ to $t=T/2$ & $-V$ volt from $t=T/2$ to $t=T$ and it repeats. It can be expressed as:

$$V_{in}(t) = +V \quad 0 \leq t < T/2$$

$$V_{in}(t) = -V \quad T/2 \leq t \leq T$$

The differentiator behaves similar to its behavior of step i/p. For the going pulse, the o/p shows -ve going spike and for -ve going pulse, the o/p shows +ve going spike. Hence the total o/p for the square wave

is a train of +ve & -ve spikes.



(c) Sine wave i/p

Let $V_m(t) = V_m \sin \omega t$.

$$V_o(t) = -\frac{d V_m}{dt} = -\frac{d(V_m \sin \omega t)}{dt}$$

$$\boxed{V_o(t) = -V_m \omega \cos \omega t}$$

at $t=0$

$$V_o(0) = -V_m \omega$$

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Integ.

Step Inv

V_{o_1}

V_{o_2}

V_{o_3}

Neat

$V_{o_1}(t) = +A$

$V_{o_2}(t) = +B$

$V_{o_3}(t) = V_i$

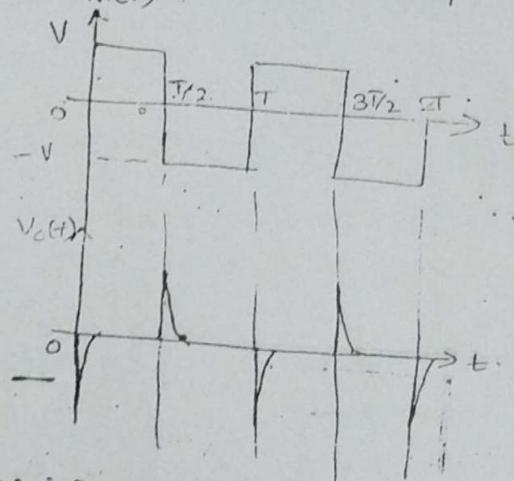
b) Square Wave Input Signal

As we know, a square wave is made by a step signal of +V volts from $t=0$ to $t=T/2$ & -V volts from $t=T/2$ to $t=T$, and it repeats. It can be expressed as:

$$V_{in}(t) = +V \quad 0 \leq t < T/2$$

$$V_{in}(t) = -V \quad T/2 \leq t < T$$

The differentiator behaves similar to its behavior at step i/p. For the going pulse, the o/p shows -ve going spike and for -ve going pulse, the o/p shows +ve going spike. Hence the total o/p for the square wave is a train of +ve & -ve spikes.



c) Sine wave i/p.

$$\text{Let } V_{in}(t) = V_m \sin \omega t$$

$$V_o(t) = -\frac{d}{dt} V_{in} = -\frac{d}{dt} (V_m \sin \omega t)$$

$$V_o(t) = -V_m \omega \cos \omega t$$

$$\text{at } t=0, V_o(t) = -V_m \omega$$

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Integ

Step Inv

V_{o1}

V_{o2}

V_{o3}

Next

V_{o1(t)} = +V

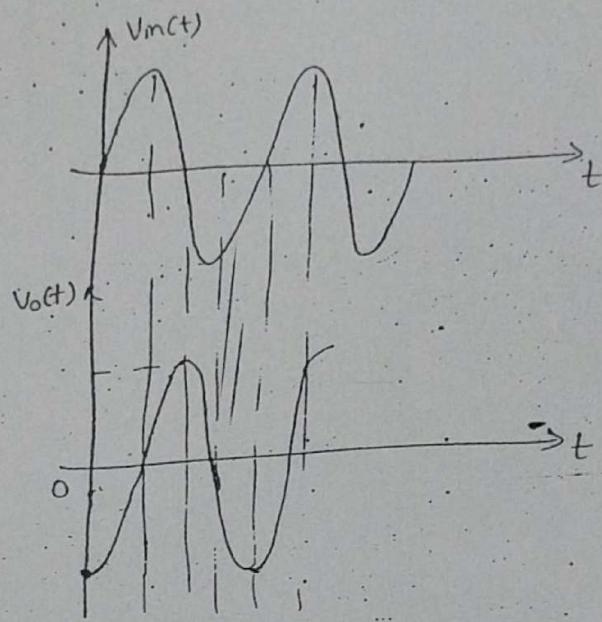
V_{o2(t)} = +V

V_{o3(t)} = V

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$$t = T/4, V_o(t) = 0$$

$$t = T/2, V_o(t) = +V_m \omega \text{ and so on.}$$



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Integrator

Step Input Signal

$$V_o(t) = - \int_{0}^{t} V_m(t) dt$$

$$= - \int_{0}^{t} A dt$$

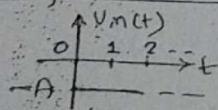
$$\boxed{V_o(t) = -A \int_{0}^{t} dt}$$

$$V_{o_1}(t) = -A[t]_0^1 = -A[1-0] = -A$$

$$V_{o_2}(t) = -A[t]_1^2 = -A[2-1] = -A$$

$$\therefore V_o(t) = V_{o_1}(t) + V_{o_2}(t), \therefore -A + (-A) = -2A \rightarrow \text{for the range } 0 \text{ to } 2.$$

Next for -ve Step i/p



$$V_o(t) = - \int_{0}^{t} V_m(t) dt$$

$$= - \int_{0}^{t} (-A) dt = +A \int_{0}^{t} dt$$

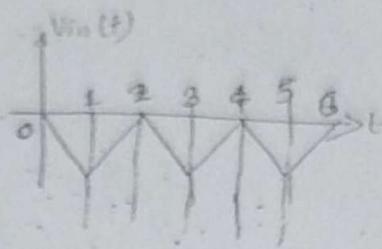
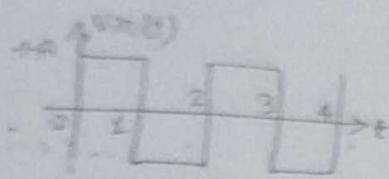
$$\boxed{V_o(t) = +A \int_{0}^{t} dt}$$

$$V_{o_1}(t) = +A[t]_0^1 = +A[1-0] = +A$$

$$V_{o_2}(t) = +A[t]_1^2 = +A[2-1] = +A$$

$$\therefore V_o(t) = V_{o_1}(t) + V_{o_2}(t) = +A + A = +2A \rightarrow \text{for the range } 0 \text{ to } 2.$$

Square-Top Signal



$$V_{o_1}(t) = - \int_0^t V_m(t) dt$$

$$V_{o_1}(t) = - \left[A dt \right]_0^t = -A \int_0^t dt = -A [t]_0^t = -A[1-0] = -A$$

$$V_{o_2}(t) = - \int_1^2 (-A) dt = +A \int_1^2 dt = +A [t]_1^2 = +A[2-1] = +A$$

$$V(t) = V_{o_1}(t) + V_{o_2}(t) = -A + A = 0 \rightarrow \text{for the range } 0 \text{ to } 2$$

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