

7

Fundamentals of Sequential Design

Chapter Outline

- 7.1 Sequential Machine Models
- 7.2 Analysis of Sequential Circuits Simplified
- 7.3 Analysis of Clocked Synchronous Sequential Circuits

The basic models of sequential systems are described in this chapter besides the transition and excitation tables of various flip flops. Systematic analysis of simple sequential machines are dealt along with illustrative examples.

7.1 Sequential Machine Models

Clocked synchronous sequential circuits have a master clock which is connected simultaneously to the control clock inputs of all the flip-flops in the memory block of the circuit. Fig. 7.1 shows the general configuration of a clocked synchronous sequential circuit.

Depending on the type of flip-flops used, they either respond to the pulse level or pulse edges. The states change together because all the flip-flops are simultaneously clocked.

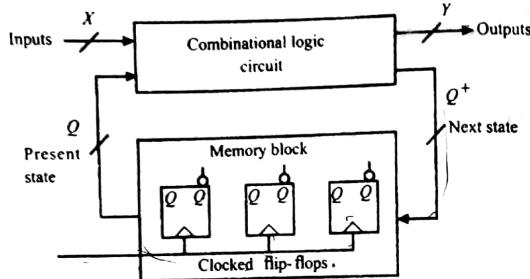


Fig. 7.1 Configuration of clocked synchronous sequential circuits

Using our conventional notations, with reference to Fig. 7.1, let

- $Q = \{Q_0, Q_1, \dots, Q_n\}$ be the present state of the circuit,
- $Q^* = \{Q_0^*, Q_1^*, \dots, Q_n^*\}$ be the next state of the circuit,
- $X = \{X_1, X_2, \dots, X_l\}$ be the present input and
- $Y = \{Y_1, Y_2, \dots, Y_m\}$ be the outputs.

The next state is a Boolean function of the present inputs and the present state.

$$Q^* = f_1(X, Q) \quad (7.1)$$

and the outputs are also a function of present inputs and the present state

$$Y = f_2(X, Q) \quad (7.2)$$

Figure 7.2 shows the general model of a clocked synchronous sequential circuit based on Equations 7.1 and 7.2 called the Mealy model.

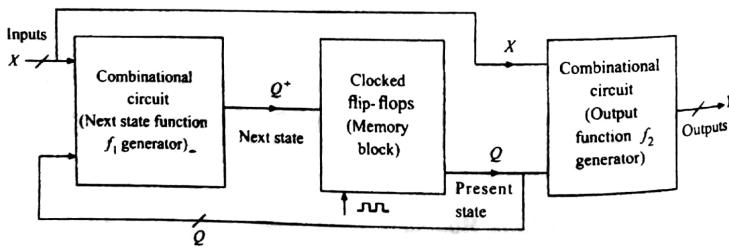


Fig. 7.2 Mealy model of a clocked synchronous sequential circuits

Let us illustrate this with an example.

Design a synchronous circuit using positive edge triggered JK flip-flops with minimal combinational gating to generate the following sequence.

0 - 1 - 2 - 0 if input $X = 0$ and 0 - 2 - 1 - 0 if input $X = 1$

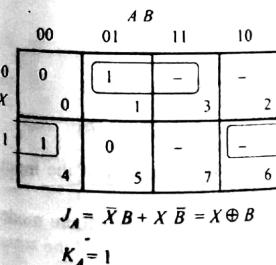
Provide an output which goes high to indicate the non-zero states in the 0 - 1 - 2 - 0 sequence
Is this a Mealy machine?

Solution: Let us write the excitation table as shown in Fig. 7.3

Cell no.	Input	Present state		Next state		Flip-flop inputs				Output		
		X		A	B	A*	B*	J _A	K _A			
0	0	0		0	0	0	1	0	-	1	-	0
1	0	0		1	1	1	0	1	-	-	1	
2	0	1		0	0	0	0	-	-	1	-	
3	0	1		1	1	-	-	-	-	-	1	
4	1	0		0	1	1	0	1	-	0	-	
5	1	0		1	0	0	0	0	-	-	0	
6	1	1		0	0	0	1	-	1	1	-	
7	1	1		1	1	-	-	-	-	-	0	

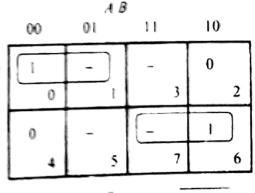
Fig. 7.3 Excitation table for Example 7.1

The Karnaugh maps for simplifying flip-flop inputs and the output are shown in Fig. 7.4.



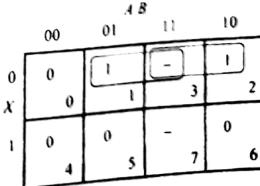
$$J_A = \bar{X}B + X\bar{B} = X \oplus B$$

$$K_A = 1$$



$$J_B = \bar{X}A + XA = \bar{X} \oplus A$$

$$K_B = 1$$



$$Y = \bar{X}B + \bar{X}A = \bar{X}(A + B)$$

Fig. 7.4 Karnaugh maps related to table in Fig. 7.3

The implementation is shown in Fig. 7.5.

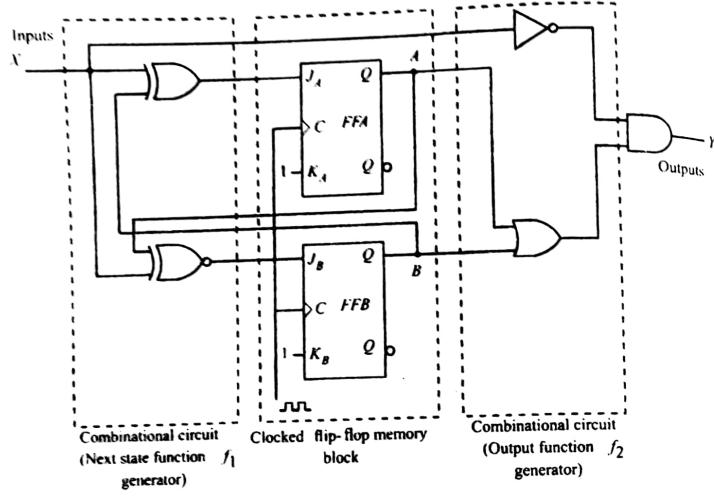


Fig. 7.5 Implementation of Example 7.1

$$\text{Here, } Q = \{A, B\}, Q^* = \{A^*, B^*\}$$

$$Q^* = f_1(X, Q) = f_1(X, A, B)$$

$$Y = f_2(X, Q) = f_2(X, A, B) = \bar{X}(A + B)$$

Observe that both the next state and the output are Boolean functions of the input and the present state. This is indeed a Mealy machine.

Besides the Mealy model, there is another important model called the Moore model. Let us slightly modify the output specification of Example 7.1 in order to understand the structure of Moore machine, as illustrated in Example 7.2.

Repeat Example 7.1 with the output now to go high whenever the circuit is in non-zero state irrespective of the sequence.

Solution: The synchronous circuit design remains same with exception to the output combination circuit. The truth table for the output and the Karnaugh map are shown in Fig. 7.6.

Cell no.	Input X	Present state		Output Y
		A	B	
0	0	0	0	0
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	—

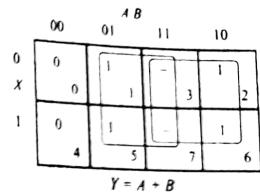


Fig. 7.6 Truth table and Karnaugh map for the output function of Example 7.2

The implementation is shown in Fig. 7.7.

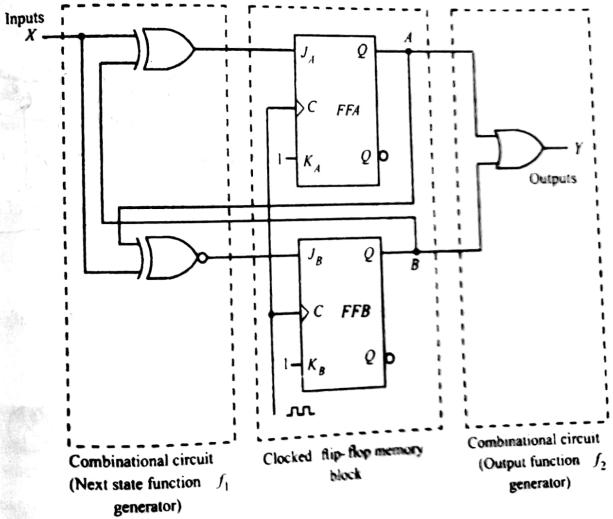


Fig. 7.7 Implementation for Example 7.2

Observe that the next state remains a function of the input and the present state whereas the output is a function of only the present state.

$$\text{i.e., } Q = f_1(X, A, B) \text{ and } Y = f_2(A, B)$$

In other words

$$Q^* = f_1(X, Q) \quad \text{and} \quad Y = f_2(Q)$$

Such a configuration is called a Moore machine. Fig. 7.8 shows the general Moore model of a clocked synchronous sequential circuit.

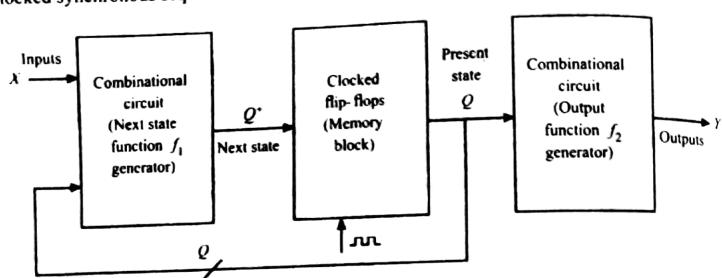


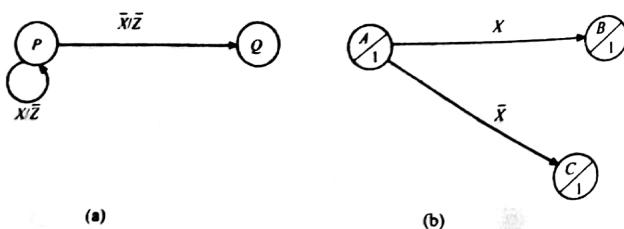
Fig. 7.8 Moore model of a clocked synchronous sequential circuit

The Moore machine is characterized by

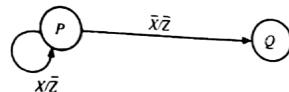
$$\begin{aligned} Q^* &= f_1(X, Q) \\ Y &= f_2(Q) \end{aligned} \quad (7.3)$$

The characteristic feature of the Moore machine is that the output is a function of only the present state.

Explain the prevalent conditions in the segments of the state diagram shown and identify the type of the machine.



Solution:
(a) Given



There are two states P and Q . When at state P ,

- when input is 1, it remains in state P and the output is 0
- when input is 0, it makes a transition to state Q and the output is 0

$$Q^* = f_1(X, Q)$$

$$\text{and} \quad Y = f_2(Q)$$

where

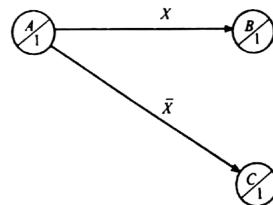
X is the input

Y is the output

Q is the present state and Q^* is the next state

Hence it is a Mealy machine.

(b) Given



There are three states A , B and C , when at state A ,

- when input is 1, it makes a transition to state B and output is 1
- when input is 0, it makes a transition to state C and output is 1

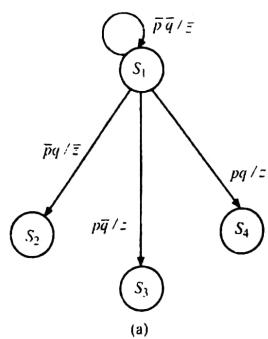
The output depends only on the present state as the output variable is represented within the state circle

$$Q^* = f_1(X, Q)$$

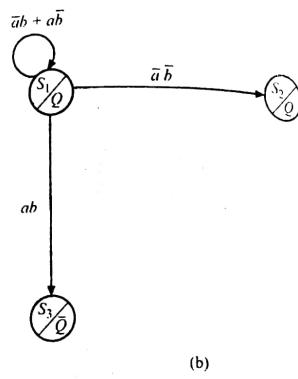
$$\text{and} \quad y = f_2(Q)$$

Hence it is a Moore machine.

Identify the transition pattern and the types of machine in the following cases:



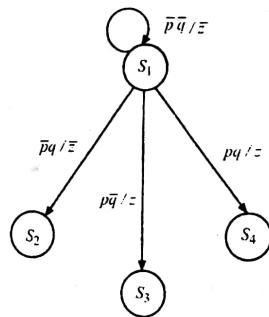
(a)



(b)

Solution:

(a) Given



There are four states S_1, S_2, S_3 and S_4 , two inputs P and Q and an output Z . When at state S_1 ,

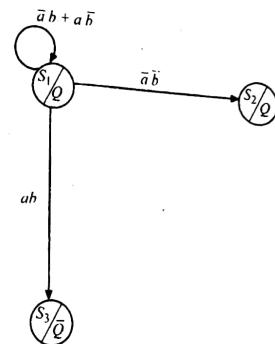
- when the input is at $p = 0, q = 0$, it remains in state S_1 and the output is 0.
- when the input is at $p = 0, q = 1$, it makes a transition to state S_2 and the output is 0.
- when the input is at $p = 1, q = 0$, it makes a transition to state S_3 and the output is 1 and
- when the input is at $p = 1, q = 1$, it makes a transition to state S_4 and the output is 1.

It is easy to see that here,

$$Q^* = f_1(X, Q) \quad \text{and} \quad Y = f_2(X, Q)$$

Hence it is a Mealy machine.

(b) Given



There are three states S_1, S_2 and S_3 , two inputs a and b and an output Q which is in the state circle.

When at state S_1 ,

- when the inputs are either $a = 0, b = 1$ or $a = 1, b = 0$ it remains in the same state and the output is 0
- when the inputs are $a = 0, b = 0$, it makes a transition to state S_2 and the output is 1
- when the inputs are $a = 1, b = 1$ it makes a transition to state S_3 and the output is 0.

It is easy to see that here,

$$Q^* = f_1(X, Q)$$

$$\text{and} \quad Y = f_2(Q)$$

Hence it is a Moore machine.

7.2 Analysis of Sequential Circuits Simplified

Combinational circuits are easy to analyse. We simply need to write the Boolean expression for the outputs and write the truth table. The operation of sequential circuits on the other hand is not quite apparent from the diagram. We need to write the state diagram in order to understand the sequence of states for every clock pulse applied.

The procedure to analyse synchronous counter is as follows:

- Identify the state variables (flip-flop outputs).
- Identify the flip-flop types.

3. Write the flip-flop input equations.
4. Construct the Karnaugh map using the flip-flop equations.
5. Fill the excitation table using the Karnaugh map data and the flip-flop function tables as discussed in Section 6.1 as shown below.

S	R	Q^*
0	0	Q
0	1	0
1	0	1
1	1	-

J	K	Q^*
0	0	Q
0	1	0
1	0	1

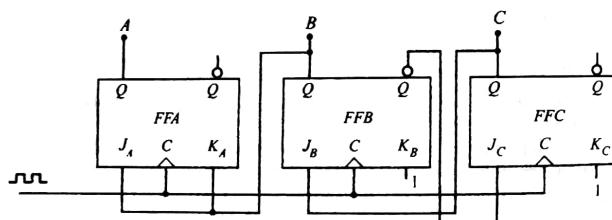
D	Q^*
0	Q
1	\bar{Q}

T	Q^*
0	Q
1	\bar{Q}

6. Write the state diagram from the excitation table.

This procedure is illustrated with the following examples:

Analyse the following synchronous sequential circuit:



Solution: Let us follow the step by step procedure.

1. Identify the state variables (flip-flop outputs): A, B and C .
2. Identify flip-flop types; All are JK flip-flops.
3. Write the flip-flop input equations:

$$J_A = K_A = B$$

$$J_B = C, K_B = 1$$

$$J_C = \bar{B}, K_C = 1$$

4. Construct the Karnaugh maps using the flip-flop equations.

A	BC			
	00	01	11	10
0	0	0	1	1
1	0	0	1	1

$J_A = K_A = B$

A	BC			
	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$J_B = C$

A	BC			
	00	01	11	10
0	1	1	0	0
1	1	1	0	0

$J_C = \bar{B}$

5. Fill the excitation table using the function table of the JK flip-flop.

J	K	Q^*
0	0	Q
0	1	0
1	0	1
1	1	\bar{Q}

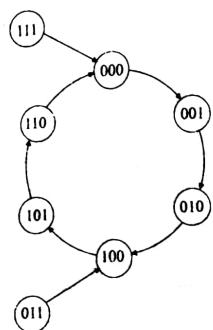
Cell no.	Present state			Next state			Flip-flop Inputs					
	A	B	C	A^*	B^*	C^*	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	1	0	0	0	1	1	1
1	0	0	1	0	1	0	0	0	1	1	1	1
2	0	1	0	1	0	0	1	1	0	1	0	1
3	0	1	1	1	0	0	1	1	1	1	0	1
4	1	0	0	1	0	1	0	0	0	0	1	1
5	1	0	1	1	1	0	0	1	1	0	1	0
6	1	1	0	0	0	0	1	1	0	1	1	0
7	1	1	1	0	0	0	1	1	1	1	0	1

First fill in the cell numbers and the present states in binary sequence.

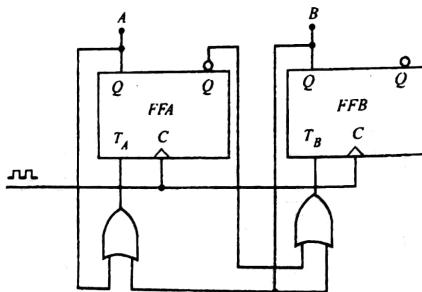
Next fill in the flip-flop inputs from the Karnaugh maps.

Finally, fill in the next states by referring to the flip-flop function table and the present state.

6. Write the state diagram from the excitation table.



Analyse the following synchronous circuit.



Solution:

1. The state variables are A and B
2. Both are T flip-flops
3. The flip-flop input equations are

$$T_A = A + B \quad \text{and} \quad T_B = \bar{A} + B$$

4. The Karnaugh maps for the flip-flop inputs are

		B	
		0	1
A	0	0	1
	1	0	1

$T_A = A + B$

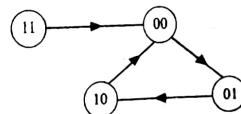
		B	
		0	1
A	0	1	1
	1	0	1

$T_B = \bar{A} + B$

5. The excitation table using the T flip-flop function table is now written.

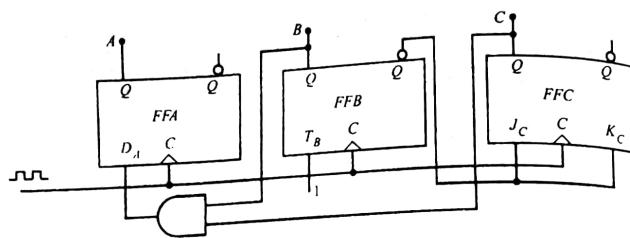
Cell no.	Present state		Next state		Flip-flop Inputs	
	A	B	A^*	B^*	T_A	T_B
0	0	0	0	1	0	1
1	0	1	1	0	1	1
2	1	0	0	0	1	0
3	1	1	0	0	1	1

6. Write the state diagram.



Thus the counter sequences $0 \rightarrow 1 \rightarrow 2 \rightarrow 0$. Observe that if it gets into an invalid state 11, it goes into the valid state 00 during the next clock pulse. Such counters are referred to as self-correcting counters.

Analyse the following synchronous sequential circuit.

**Solution:**

1. The state variables are A , B and C
2. Flip-flops are D , T and JK
3. The flip-flop input equations are

$$D_A = B_C$$

$$T_B = 1$$

$$J_C = K_C = \bar{B}$$

4. The Karnaugh map needs to be written for D_A , the rest can be filled directly in the excitation table.

		B C					
		00	01	11	10		
A		0	0	0	1	3	2
		1	0	0	1	0	6

$D_A = BC$

5. Write the excitation table using the function tables of the three flip-flop types.

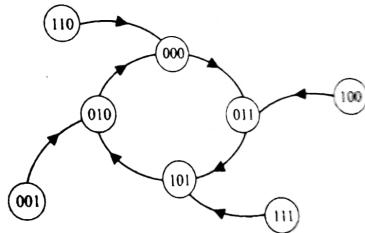
D	Q^*
0	0
1	1

T	Q^*
0	Q
1	\bar{Q}

J	K	Q^*
0	0	Q
0	1	0
1	0	1
1	1	\bar{Q}

Cell no.	Present state			Next state			Flip-flop Inputs			
	A	B	C	A^*	B^*	C^*	D_s	T_s	J_c	K_c
0	0	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	0	0	1	1	1
2	0	1	0	0	0	0	0	1	1	1
3	0	1	1	1	0	1	1	1	0	0
4	1	0	0	0	1	1	0	1	1	1
5	1	0	1	0	1	0	0	0	1	1
6	1	1	0	0	0	0	0	0	1	0
7	1	1	1	1	0	1	1	1	0	0

6. Write the state diagram

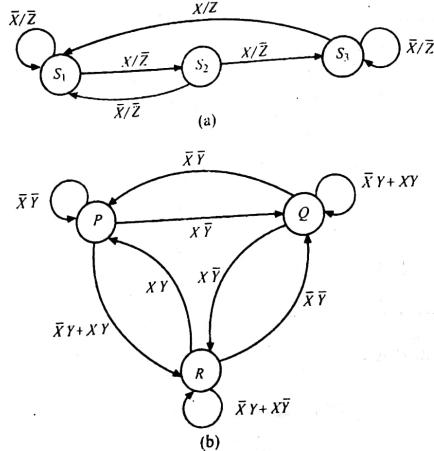


The counter's sequence is $0 \rightarrow 3 \rightarrow 5 \rightarrow 2 \rightarrow 0$.

In case it gets into one of the invalid states it gets back into one of the valid sequence states during the next clock pulse.

Realize the system represented by the following state diagrams using

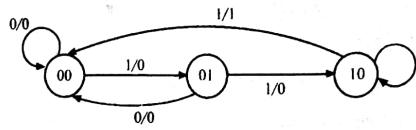
- (i) D -flip flop
- (ii) JK -flip flop

**Solution:**(a) There are three state, S_1 , S_2 , and S_3 . Let the state assignment be

$$S_1 = 00$$

$$S_2 = 01$$

$$S_3 = 10$$

Let the state be called AB . The state diagram now becomes,

Let us now draw the state transition table.

Present State A B	Input X	Next state		Output Z
		A'	B'	
0 0	0	0	0	0
0 0	1	0	1	0
0 1	0	0	0	0
0 1	1	1	0	0
1 0	0	1	0	0
1 0	1	0	0	1
1 1	0	-	-	-
1 1	1	-	-	-

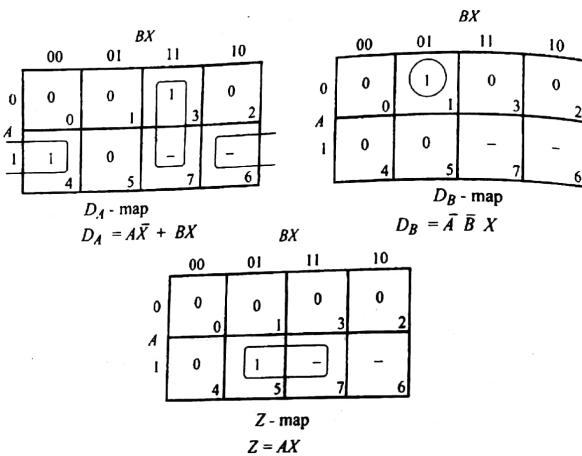
(i) We will now construct the evaluation table for implementation with D flip flop
The excitation table for a D -flip flop is shown below.

$Q \rightarrow Q^*$	D
0	0
0	1
1	0
1	1

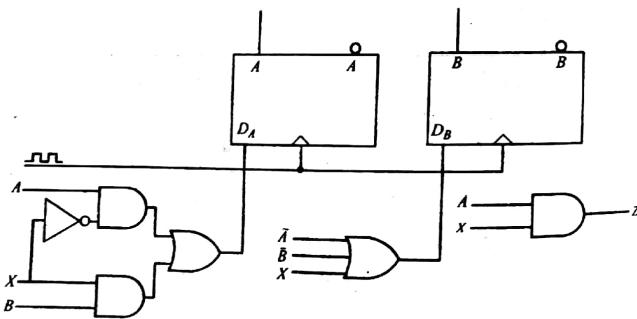
The excitation table for the required transition can now be written.

Row no.	Present state input			Next state		Flip flop inputs		Output Z
	A	B	X	A^*	B^*	D_A	D_B	
0	0	0	0	0	0	0	0	0
1	0	0	1	0	1	0	1	0
2	0	1	0	0	0	0	0	0
3	0	1	1	1	0	1	0	0
4	1	0	0	1	0	1	0	0
5	1	0	1	0	0	0	0	1
6	1	1	0	-	-	-	-	-
7	1	1	1	-	-	-	-	-

Let us now draw the Karnaugh maps for the D-flip flop inputs.



The implementation is as follows:



Cost of implementation: 9 input gates

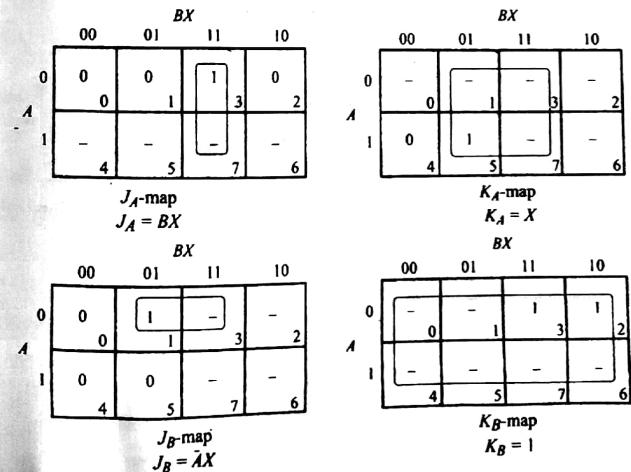
(ii) Next let us construct the excitation table for implementation with JK-flip flop. The JK excitation table is as follows

$Q \rightarrow Q'$	J	K
0 0	0	-
0 1	1	-
1 0	-	1
1 1	-	0

The excitation table for the machine is now drawn

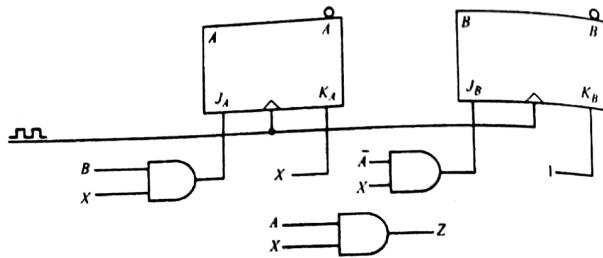
Cell no.	Present state		Input	Next state		Flip flop inputs		output
	A	B		A^*	B^*	J_A	K_A	
0	0	0	0	0	0	0	-	0
1	0	0	1	0	1	0	-	0
2	0	1	0	0	0	0	-	1
3	0	1	1	1	0	1	-	1
4	1	0	0	1	0	-	0	0
5	1	0	1	0	0	-	1	0
6	1	1	0	-	-	-	-	-
7	1	1	1	-	-	-	-	-

The Karnaugh maps can now be drawn for the flip flop inputs



As earlier, output $Z = AX$.

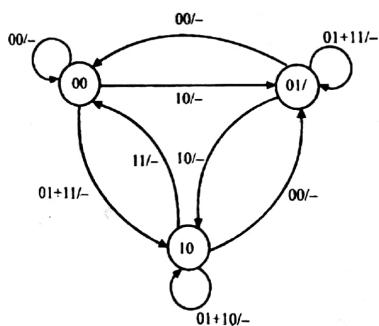
The implementation using JK flip flop can now be drawn.



Cost of implementation = 4 input gates. Compare the cost of implementation using D-flip flops which amounted to 9 input gates.

- (b) There are three states and let the state assignment be
 $P = 00$ $Q = 01$ $R = 10$ represented as AB . There is no output defined.

The state diagram now becomes:



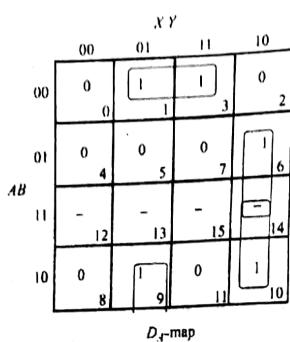
The transition table is generated next.

Cell no.	A	B	X	Y	A^*	B^*
0	0	0	0	0	0	0
1	0	0	0	1	1	0
2	0	0	1	0	0	1
3	0	0	1	1	1	0
4	0	1	0	0	0	0
5	0	1	0	1	0	1
6	0	1	1	0	1	0
7	0	1	1	1	0	1
8	1	0	0	0	0	1
9	1	0	0	1	1	0
10	1	0	1	0	1	0
11	1	0	1	1	0	0
12	1	1	0	0	-	-
13	1	1	0	1	-	-
14	1	1	1	0	-	-
15	1	1	1	1	-	-

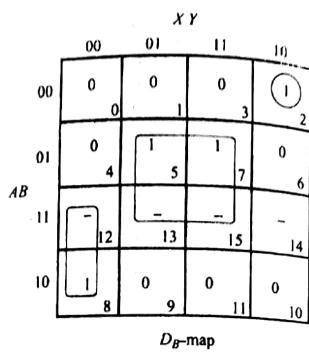
- (i) Let us consider implementation with D flip flop.
The excitation table is now drawn.

Cell no.	A	B	X	Y	A^*	B^*	D_A	D_B
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	1	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	1	0	1	0
4	0	1	0	0	0	0	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	0	1	0	1
8	1	0	0	0	0	1	0	1
9	1	0	0	1	1	0	1	0
10	1	0	1	0	1	0	0	1
11	1	0	1	1	0	0	0	0
12	1	1	0	0	-	-	-	-
13	1	1	0	1	-	-	-	-
14	1	1	1	0	-	-	-	-
15	1	1	1	1	-	-	-	-

The D maps are as follows:



$$D_A = \bar{A}\bar{B}Y + \bar{B}\bar{X}Y + BX\bar{Y} + AX\bar{Y}$$



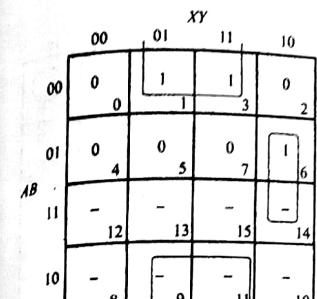
$$D_B = \bar{A}\bar{B}X\bar{Y} + A\bar{X}Y + BY$$

Cost of implementation is 28 input gates.

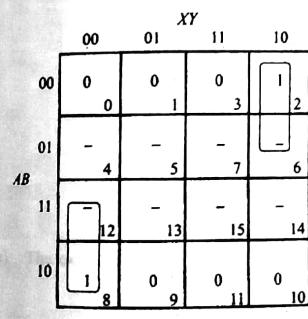
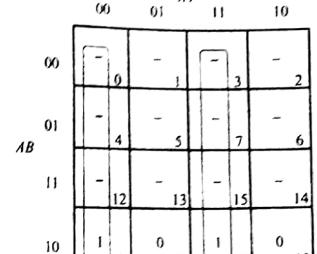
(ii) The excitation table for the system using JK flip flop is as follows:

Cell no.	A	B	X	Y	A^*	B^*	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	0	-	0	-
1	0	0	0	1	1	0	1	-	0	-
2	0	0	1	0	0	1	0	-	1	-
3	0	0	1	1	1	0	1	-	0	-
4	0	1	0	0	0	0	0	-	-	1
5	0	1	0	1	0	1	0	-	-	0
6	0	1	1	0	1	0	1	-	-	1
7	0	1	1	1	0	1	0	-	-	0
8	1	0	0	0	0	1	-	1	1	-
9	1	0	0	1	1	0	-	0	0	-
10	1	0	1	0	1	0	-	0	0	-
11	1	0	1	1	0	0	-	1	0	-
12	1	1	0	0	-	-	-	-	-	-
13	1	1	0	1	-	-	-	-	-	-
14	1	1	1	0	-	-	-	-	-	-
15	1	1	1	1	-	-	-	-	-	-

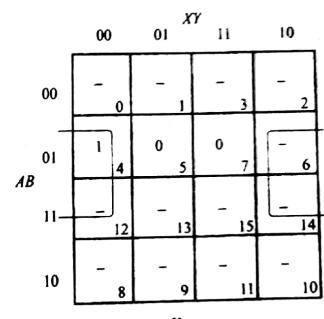
The Karnaugh maps for the flip flop inputs are now drawn.



$$J_A = \bar{B}Y + BX\bar{Y}$$



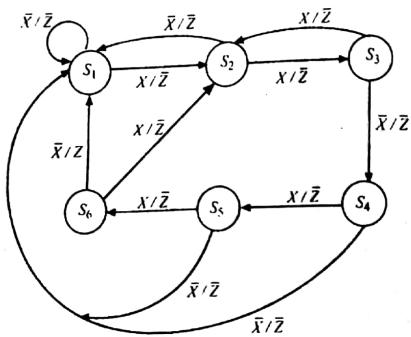
$$J_B = A\bar{X}\bar{Y} + \bar{A}XY$$



The expression can easily be implemented.

Cost of implementation = 23 input gates.

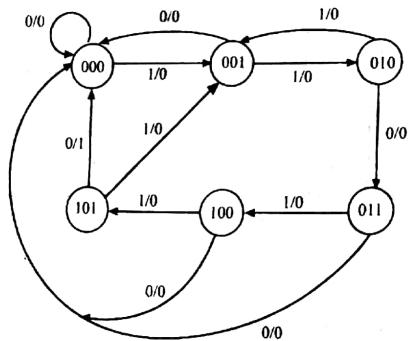
Implement the state diagram shown using (a) SR-flip flop (b) T-flip flop.



Solution

There are six states S_1 to S_6 and let them be assigned with states 000 to 110.

The state diagram now becomes,



The state transition table can now be drawn.

Cell no.	A	B	C	X	A' B' C'			Z
					A'	B'	C'	
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	0
2	0	0	1	0	0	0	0	0
3	0	0	1	1	0	1	0	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	0	1	0
6	0	1	1	0	0	0	0	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	0	0	0	0
9	1	0	0	1	1	0	1	0
10	1	0	1	0	0	0	0	1
11	1	0	1	1	0	0	1	0
12	1	1	0	0	-	-	-	-
13	1	1	0	1	-	-	-	-
14	1	1	1	0	-	-	-	-
15	1	1	1	1	-	-	-	-

(a) The excitation table for a SR-flip flop is shown below:

$Q \rightarrow Q'$	S	R
0 0	0	-
0 1	1	0
1 0	0	1
1 1	-	0

Using this, the excitation table for the system can be written as follows:

Cell no.	A	B	C	X	A^*	B^*	C^*	S_A	R_A	S_B	R_B	S_C	R_C	Z
0	0	0	0	0	0	0	0	0	-	0	-	0	-	0
1	0	0	0	1	0	0	1	0	-	0	-	1	0	0
2	0	0	1	0	0	0	0	0	-	0	-	0	1	0
3	0	0	1	1	0	1	0	0	-	1	0	0	1	0
4	0	1	0	0	0	1	1	0	-	-	0	1	0	0
5	0	1	0	1	0	0	1	0	-	0	1	1	0	0
6	0	1	1	0	0	0	0	0	-	0	1	0	1	0
7	0	1	1	1	1	0	0	1	0	0	1	0	1	0
8	1	0	0	0	0	0	0	0	1	0	-	0	-	0
9	1	0	0	1	1	0	1	-	0	0	-	1	0	0
10	1	0	1	0	0	0	0	0	1	0	-	0	1	1
11	1	0	1	1	0	0	1	0	1	0	-	-	0	0
12	1	1	0	0	-	-	-	-	-	-	-	-	-	-
13	1	1	0	1	-	-	-	-	-	-	-	-	-	-
14	1	1	1	0	-	-	-	-	-	-	-	-	-	-
15	1	1	1	1	-	-	-	-	-	-	-	-	-	-

We now need to plot the maps for the SR flip flop inputs.

CX			
00	01	11	10
0	0	1	3
AB	0	0	0
	4	5	7
	-	-	-
	12	13	15
0	8	-	9
8	-	0	11
0	0	0	0

S_A -map
 $S_B = BCX$

CX			
00	01	11	10
-	0	1	3
AB	-	-	-
	4	5	7
	-	-	-
	12	13	15
1	8	0	1
8	9	11	10
1	0	1	1

R_A -map
 $R_A = A\bar{X} + AC$

CX			
00	01	11	10
0	0	1	3
AB	-	0	2
	4	5	6
	-	-	-
	12	13	14
0	8	9	11
8	9	11	10
0	0	0	0

$S_B = \bar{A}\bar{B}CX$

CX			
00	01	11	10
-	0	0	2
AB	0	1	1
	4	5	6
	-	-	-
	12	13	14
-	8	9	11
8	9	11	10
-	0	0	0

$R_B = BX + BC$

CX			
00	01	11	10
0	1	0	0
AB	0	1	2
	4	5	6
	-	-	-
	12	13	14
0	8	9	11
8	9	11	10
0	0	0	0

$S_C = B\bar{C} + \bar{C}X + AX$

CX			
00	01	11	10
-	0	1	2
AB	0	1	1
	4	5	6
	-	-	-
	12	13	14
-	8	9	11
8	9	11	10
-	0	0	0

$R_C = \bar{A}C + CX$

CX			
00	01	11	10
0	0	1	2
AB	0	0	0
	4	5	6
	-	-	-
	12	13	14
0	8	9	11
8	9	11	10
0	0	0	0

Z -map
 $Z = AC\bar{X}$

Cost of implementation is 34 input gates.

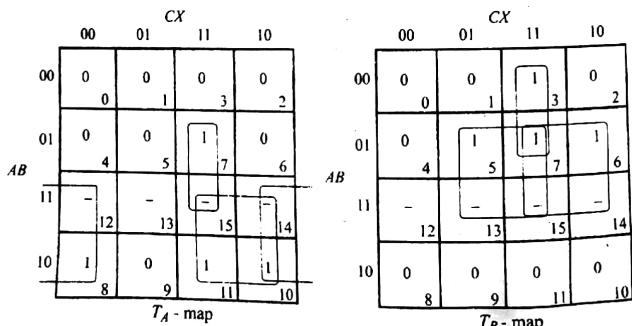
(b) Let us now implement using T-flip flop.

The excitation table for the T-flip flop is shown below.

$Q \rightarrow Q'$	T
0 0	0
0 1	1
1 0	1
1 1	0

The excitation table can be now written.

Cell no.	A	B	C	X	A^*	B^*	C^*	T_A	T_B	T_C
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	0	0	1
2	0	0	1	0	0	0	0	0	0	1
3	0	0	1	1	0	1	0	0	1	1
4	0	1	0	0	0	1	1	0	0	1
5	0	1	0	1	0	0	1	0	1	1
6	0	1	1	0	0	0	0	0	1	1
7	0	1	1	1	1	0	0	1	1	1
8	1	0	0	0	0	0	0	1	0	0
9	1	0	0	1	1	0	1	0	0	1
10	1	0	1	0	0	0	0	1	0	1
11	1	0	1	1	0	0	1	1	0	0
12	1	1	0	0	--	--	--	--	--	--
13	1	1	0	1	--	--	--	--	--	--
14	1	1	1	0	--	--	--	--	--	--
15	1	1	1	1	--	--	--	--	--	--



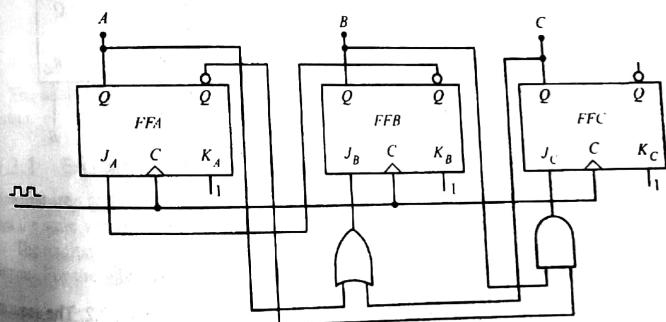
		CX			
		00	01	11	10
AB	00	0	1	1	1
	01	0	0	1	1
11	00	1	1	1	1
	11	-	-	-	-
10	00	1	1	1	1
	10	0	1	1	1

$$T_C = \bar{A}B + \bar{C}X + CX + \bar{A}C \text{ and } Z = AC\bar{X}$$

Cost of implementation is 32 input gates.

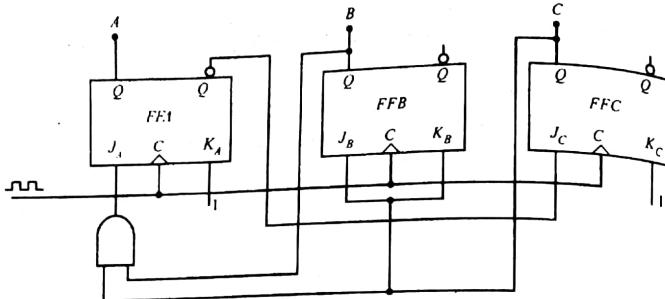
Exercise 7.1

Analyse the following synchronous sequential circuit:



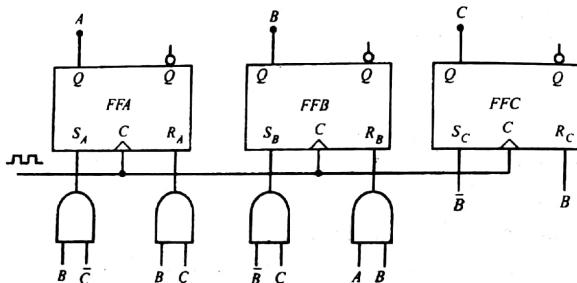
Exercise 7.2

Analyse the following synchronous sequential circuit:



◆ Exercise 7.3

Analyse the following synchronous sequential circuit.



7.3 Analysis of Clocked Synchronous Sequential Circuits

We had a glimpse of the analysis of synchronous sequential circuits in Section 7.2. The sequential circuits considered there were simple counters without inputs or decoded outputs. The counters were self-starting and the states themselves were the outputs. They were governed by the following equations.

$$Q^* = f_i(Q)$$

$$Y = Q$$

Analysis, which is essentially a reverse design procedure helps us to arrive at the present state next state table and consequently to draw the state diagram.

Let us take a typical example of a Mealy sequential machine and walk through the entire analysis procedure. Let us consider the analysis of the Mealy machine shown in Fig. 7.9.

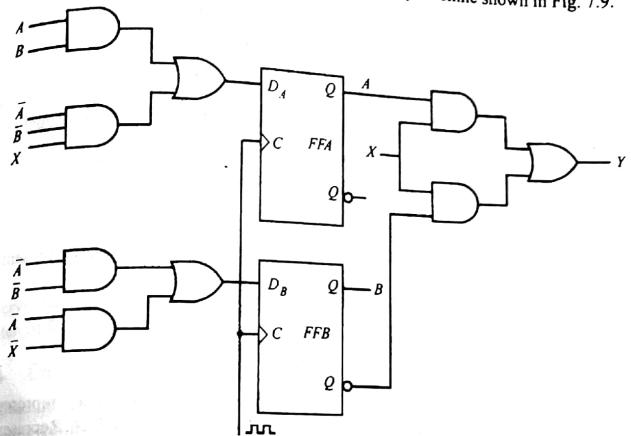


Fig. 7.9 Mealy machine example for analysis

The analysis is complete when we obtain the state diagram of this sequential synchronous circuit.

7.3.1 EXCITATION AND OUTPUT EXPRESSIONS

The first step is to write the algebraic Boolean expressions for the flip-flop inputs and the outputs. Let the state variables be the D flip-flop, FFA , output A and the D flip-flop, FFB output B .

The excitations to the flip-flops are precisely the Boolean expressions representing the flip-flop inputs. For the example in Fig. 6.10, the excitation expressions are

$$D_A = AB + X \bar{A} \bar{B} \quad (7.7)$$

$$D_B = \bar{A} \bar{B} + X \bar{A} \quad (7.8)$$

The output expression is

$$Y = XA + X \bar{B} \quad (7.9)$$

7.3.2 TRANSITION EQUATIONS

The characteristic equations as discussed in Section 6.1, of the flip-flops, present in the circuit are used to obtain the next state expressions from the excitation expressions.

For a D flip-flop, the characteristic equation is

$$Q^* = D \quad (7.10)$$

Thus, in the example of Fig. 7.9, the next states of the flip-flops are

$$A^* = D_A \quad (7.11)$$

$$B^* = D_B \quad (7.12)$$

The transition equations are obtained by substituting Equations 7.7 and 7.8 in Equations 7.11 and 7.12.

$$A^* = AB + X\bar{A}\bar{B} \quad (7.13)$$

$$B^* = \bar{A}\bar{B} + \bar{X}\bar{A} \quad (7.14)$$

Equations 7.13 and 7.14 give the next states as a function of the input and the present states i.e., they represent the equation.

$$Q^* = f_i(X, Q)$$

7.3.3 TRANSITION TABLES

The operation of sequential circuits are easy to comprehend if the next states are represented in tabular forms than in the form of algebraic expressions like Equations 7.13 and 7.14. Representation of the next state equations in tabular form is called a transition table. The next state equations need to be evaluated for each combination of the present state and the input in order to write the transition table.

Let us now evaluate Equations 7.13, 7.14, and 7.9 as shown in Fig. 7.10.

Row no.	A	B	X	B*		A*		Y								
				\bar{A}	\bar{B}	\bar{X}	$X\bar{A}$	$\bar{A}\bar{B}$	$X\bar{A}\bar{B}$	AB	A^*	B^*	$X\bar{A}$	$X\bar{B}$	Y	
0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	1	1	0	0	1	1	0	1	1	0	1	1	1
2	0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0
3	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
4	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
5	1	0	1	0	1	0	0	0	0	0	0	0	1	1	1	1
6	1	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0
7	1	1	1	0	0	0	0	0	1	1	0	1	0	1	0	1

Fig. 7.10 Evaluation of next state and output equations

Let us now write the transition table from Fig. 7.10. The transition table has three sections as shown in Fig. 7.11. The first section lists all possible states of the circuit. The middle section lists the next state for each possible present state and input. The last section lists the output for each possible present state and input.

Present state A B	Next state $A^* B^*$		Output Y	
	Input (X) $X = 0$	Input (X) $X = 1$	Input (X) $X = 0$	Input (X) $X = 1$
0 0	0 1	1 1	0	1
0 1	0 1	0 0	0	0
1 0	0 0	0 0	0	1
1 1	1 0	1 0	0	1

Fig. 7.11 Transition Table for Example Fig. 7.9

Observe that the transition table shown in Fig. 7.11 is simply the truth table of Fig. 7.10 written in a different form.

7.3.4 EXCITATION TABLES

Writing the transition table by evaluating the Boolean expressions for the next state and output can become cumbersome if the Boolean expressions are complicated. A simpler approach is to first construct the excitation table from which the transition table can be obtained. The excitation table also has three sections as shown in Fig. 7.12. The first section lists all possible states. The middle section lists the excitation at all possible present states for all possible inputs. The last section lists the output at all possible present states for all possible inputs. Since $Q^* = D$ for a D flip-flop, the excitation is the same as the next state and we can use Fig. 7.10 to write the excitation table. If any other types of flip-flops were being used in the design, we need to evaluate the flip-flop excitation or input expressions as a tabulation similar to Fig. 7.10 before constructing the excitation table. This will be illustrated using different examples later in this chapter.

Present state A B	Excitation $D_A D_B$		Output Y	
	Input (X) $X = 0$	Input (X) $X = 1$	Input (X) $X = 0$	Input (X) $X = 1$
0 0	0 1	1 1	0	1
0 1	0 1	0 0	0	0
1 0	0 0	0 0	0	1
1 1	1 0	1 0	0	1

Fig. 7.12 Excitation table for Example Fig. 7.9

It is easy to see that the present state and output sections will be the same for the transition table and excitation table of a given synchronous sequential circuit. The center section will change depending on the type of flip-flops used. For circuits using D flip-flops the entries in the center column will also be the same.

7.3.5 STATE TABLES

It is often convenient to label the states using alphanumeric symbols, assigning a distinct symbol to each state of the circuit. When the binary codes for the states are replaced with alphanumeric symbols in the transition table, we arrive at the state table.

Let us make symbolic state assignments as shown in Fig 7.13.

State	Symbol
0 0	a
0 1	b
1 0	c
1 1	d

Fig 7.13 Assignment of symbols to states

Applying table in Fig 7.13 to table in Fig 7.11, we obtain the state table as shown in Fig 7.14.

Present state	Next State		Output	
	Input (X)		Input (X)	
	X = 0	X = 1	X = 0	X = 1
a	b	d	0	1
b	b	a	0	0
c	a	a	0	1
d	c	c	0	1

Fig 7.14 State table for example of Fig. 7.9

In Mealy machine since the output is also a function of the inputs and the present state, the state table can be compactly written using two sections as shown in Fig. 7.15.

Present state	Next state, output (Y)	
	input (X)	
	X = 0	X = 1
a	b, 0	d, 1
b	b, 0	a, 0
c	a, 0	a, 1
d	c, 0	c, 1

Fig. 7.15 Compact state table for example of Fig. 7.9

7.3.6 STATE DIAGRAMS

A state diagram is a graphical representation of a state table. It consists of nodes representing states and directed branches representing the transitions. The inputs and outputs are also conveniently represented on the state diagram using the input/output (X/Y) notation. A section of a state diagram is shown in Fig. 7.16.

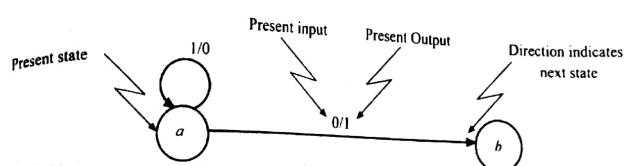


Fig. 7.16 Section of a state diagram to illustrate input/output notation

With reference to Fig. 7.16, let the circuit be in state 'a'. The input/output designation says that if the present state is 'a' an input 0 takes it to next state 'b' with an output of 1 whereas an input 1 retains it in the same state 'a' with an output 0 during the next clock pulse.

The state diagram for table in Fig. 7.14 or table in Fig. 7.15 is shown in Fig. 7.17.

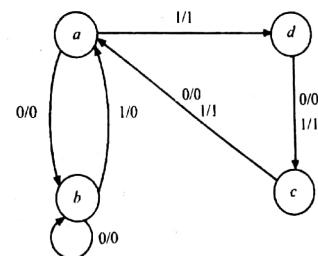
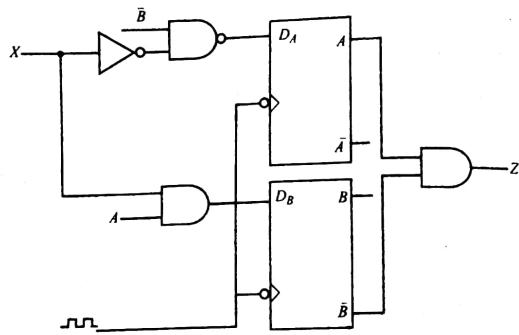


Fig. 7.17 State diagram for example in Fig. 7.9

The state diagram in Fig. 7.17 describes the operation of the Mealy synchronous sequential circuit of Fig. 7.9.

Draw the state diagram for the sequential circuit shown.



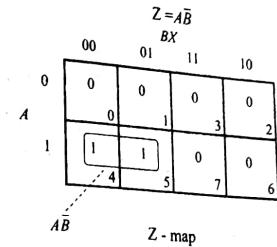
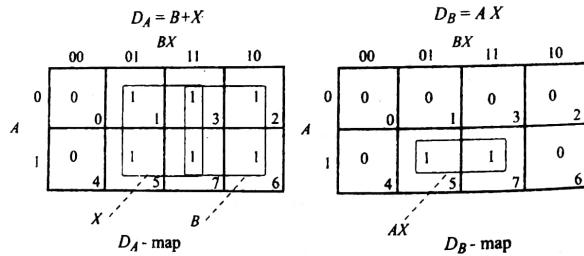
Solution: Let us begin by writing the flip flop equations.

$$D_A = \overline{B} \bar{X} = B + X$$

$$D_B = AX \quad \text{and} \quad Z = A \cdot \bar{B}$$

Since there are two flip flops there could be four possible states.

Let us back-construct the Karnaugh maps from the flip flop equations.



Let us write the excitation table from the maps. We know for a D -flip flop,

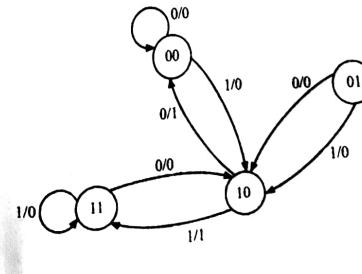
$$Q^* = D$$

$$A^* = D_A$$

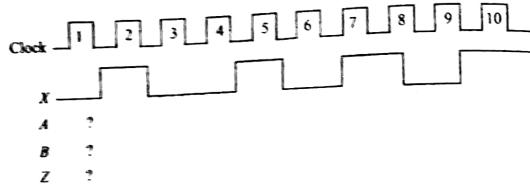
$$B^* = D_B$$

Cell no.	A	B	X	A^*	B^*	D_A	D_B	Z
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	0
2	0	1	0	1	0	1	0	0
3	0	1	1	1	0	1	0	0
4	1	0	0	0	0	0	0	1
5	1	0	1	1	1	1	1	1
6	1	1	0	1	0	1	0	0
7	1	1	1	1	1	1	1	0

We can now write the state diagram as follows:

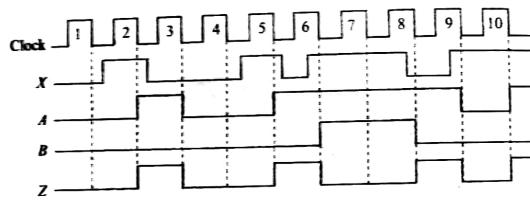


Write the timing diagram for Example 7.10 for the input shown



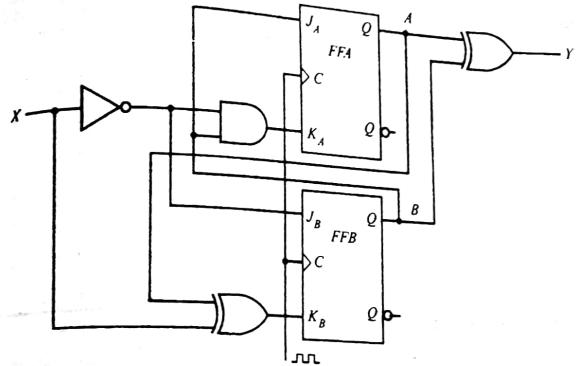
Solution

Let us complete the timing diagram using the excitation table obtained in Example 7.10.



A and B change at the falling edge of the clock due to the bubble at the clock terminal in Example 7.10, whereas Z is simply $A \bar{B}$.

Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown.



Solution: The excitation expressions or flip-flop inputs are

$$J_A = B$$

$$K_A = B\bar{X}$$

$$J_B = \bar{X}$$

$$K_B = A \oplus X$$

The output expression is

$$Y = A \oplus B = A\bar{B} + \bar{A}B$$

Clearly, this is a Moore machine since $Y = f(Q)$

Since it is cumbersome to write the transition table from the transition or next state equations, let us first construct the excitation table. Before this, we need to evaluate the flip-flop excitation expression as shown in Fig. 7.18.

The transition table is constructed next from the excitation table as shown in Fig. 7.20.

A	B	X	\bar{A}	\bar{B}	\bar{X}	$B\bar{X}$	$A \oplus X$	J_i	K_i	J_b	K_b	$Y = A \oplus B$
0	0	0	1	1	1	0	0	0	0	1	0	0
0	0	1	1	1	0	0	1	0	0	0	1	0
0	1	0	1	0	1	1	0	1	1	1	0	1
0	1	1	1	0	0	0	1	1	0	0	1	1
1	0	0	0	1	1	0	1	0	0	1	1	1
1	0	1	0	1	0	0	0	0	0	0	0	1
1	1	0	0	0	1	1	1	1	1	1	1	0
1	1	1	0	0	0	0	0	1	0	0	0	0

Fig. 7.18 Truth table of excitation and output expressions for Example 7.12

Now, let us construct the excitation table as shown in Fig. 7.19.

Present state	Excitation $J_i K_i, J_b K_b$				Output Y	
	For input		For input			
	A	B	$X = 0$	$X = 1$		
0 0	0	0	1, 0, 1, 0	0, 0, 0, 1	0 0	
0 1	1	1	1, 1, 1, 0	1, 0, 0, 1	1 1	
1 0	0	1	0, 0, 1, 1	0, 0, 0, 0	1 1	
1 1	1	1	1, 1, 1, 1	1, 0, 0, 0	0 0	

Fig. 7.19 Excitation table for Example 7.12

Present state	Next state $A^* B^*$		Output Y	
	For input		For input	
	A	B	$X = 0$	$X = 1$
0 0	0	1	0 1	0 0
0 1	1	1	1 1	1 0
1 0	1	0	1 1	1 0
1 1	1	1	0 0	1 1

Fig. 7.20 Transition table for Example 7.12

Let the states be labeled as follows:

$$00 = a$$

$$01 = b$$

$$10 = c$$

$$11 = d$$

The state table is now shown in Fig. 7.21.

Present state	Next state		Output	
	For input		For input	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	b	a	0	0
b	d	c	1	1
c	d	c	1	1
d	a	d	0	0

Fig. 7.21 State tables for Example 7.12

The state diagram drawn from table in Fig. 7.21 is shown in Fig. 7.22.

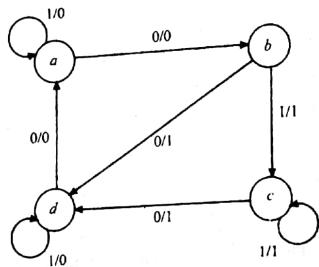
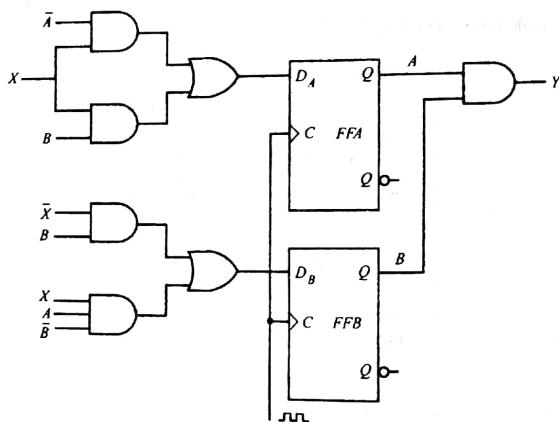


Fig. 7.22 State diagram for Example 7.12

EXERCISE 7.12
Construct the excitation table, transition table, state table and state diagram for the synchronous sequential circuit shown.



Solution: Let us begin by writing the excitation expressions which are the flip-flop input expressions.

$$D_A = \bar{A}X + BX$$

$$T_B = B\bar{X} + A\bar{B}X$$

The output expression is

$$Y = AB$$

This is also a Moore machine since $Y = f(Q)$.

Let us now evaluate the excitation and output expressions as shown in Fig. 7.23.

A	B	X	\bar{A}	\bar{B}	\bar{X}	$\bar{A}X$	BX	$A\bar{B}$	$A\bar{B}X$	$B\bar{X}$	D_A	T_B	$Y = AB$
0	0	0	1	1	1	0	0	0	0	0	0	0	0
0	0	1	1	1	0	1	0	0	0	0	1	0	0
0	1	0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	1	1	0	0	0	0	1	0
1	0	0	0	1	1	0	0	1	0	0	0	0	0
1	0	1	0	1	0	0	0	1	1	0	0	0	1
1	1	0	0	0	1	0	0	0	0	1	0	1	1
1	1	1	0	0	0	0	1	0	0	0	0	1	1

Fig. 7.23 Evaluation of excitation and output expressions

We will now construct the excitation table as shown in Fig. 7.24.

<i>Present state</i> A	<i>state</i> B	<i>Excitation D_A, T_B</i>		<i>Output Y</i>	
		<i>For input</i>	<i>For input</i>	<i>For input</i>	<i>For input</i>
0	0	0, 0	1, 0	0	0
0	1	0, 1	1, 0	0	0
1	0	0, 0	0, 1	0	0
1	1	0, 1	1, 0	1	1

Fig. 7.24 Excitation table for Example 7.13

The transition table is constructed from the excitation table as shown in Fig. 7.25.

Present state		Next state $A^* B^*$		Output Y	
		For input		For input	
A	B	$X = 0$	$X = 1$	$X = 0$	$X = 1$
0	0	00	10	0	0
0	1	00	11	0	0
1	0	00	01	0	0
1	1	00	11	1	1

Fig. 7.25 Transition table for Example 7.13

Consider present state $AB = 00$. The next state is $A^* B^*$. Here, A^* depends on the D input which is 0 for $X = 0$ and 1 for $X = 1$. Since $A^* = D$ for a D flip flop, $A^* = 0$ for $X = 0$ and $A^* = 1$ for $X = 1$. Now B^* depends on the T input which is 0 for both $X = 0$ and $X = 1$ and hence $B^* = B$ (there is no toggle) for both $X = 0$ and $X = 1$. Thus, the next state for present state $AB = 00$ is $A^* B^* = 00$ for $X = 0$ and $A^* B^* = 10$ for $X = 1$.

The next state for all the other states are similarly filled in table shown in Fig. 7.25.

Let us label the states as 00 = a , 01 = b , 10 = c and 11 = d .

By substituting these symbols for the states in the transition table, we can write the state table as shown in Fig. 7.26.

Present state		Next state		Output Y	
		For input		For input	
$X = 0$	$X = 1$	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	a	c	0	0	0
b	a	d	0	0	0
c	a	b	0	0	0
d	a	d	1	1	1

Fig. 7.26 State table for Example 7.13

The state diagram is shown in Fig. 7.27.

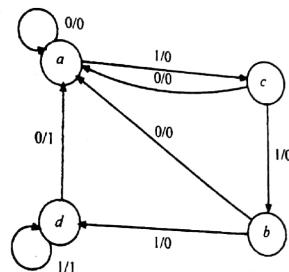
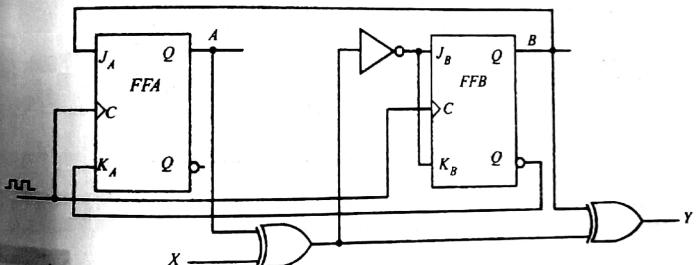


Fig. 7.27 State diagram for Example 7.13

Analyse the given synchronous sequential circuit.



Solution: The excitation equations are

$$\begin{aligned} J_A &= B & J_B &= \overline{A \oplus X} \\ K_A &= \bar{B} & K_B &= \overline{A \oplus X} \end{aligned}$$

and the output equation is

$$Y = A \oplus B \oplus X$$

380 An Illustrative Approach to Logic Design

These expressions are now evaluated is shown in Fig. 7.28.

A	B	X	$A \oplus X$	$A \oplus B \oplus X$	J_A	K_A	J_B	K_B
0	0	0	0	0	0	1	1	1
0	0	1	1	1	0	1	0	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	1	0	0	0
1	0	0	1	1	0	1	0	0
1	0	1	0	0	0	1	1	1
1	1	0	1	0	1	0	0	0
1	1	1	0	1	1	0	1	1

Fig. 7.28 Evaluation of excitation and output expressions

Excitation table is shown in Fig. 7.29.

Present state	Excitation $J_A K_A, J_B K_B$				Output Y	
	For input		For input			
	$X = 0$	$X = 1$	$X = 0$	$X = 1$		
0 0	01, 11	01, 00	0	1		
0 1	10, 11	10, 00	1	0		
1 0	01, 00	01, 11	1	0		
1 1	10, 00	10, 11	0	1		

Fig. 7.29 Excitation table for Example 7.14

Transition table is shown in table Fig. 7.30.

Present state	Next state $A^* B^* f$				Output Y	
	For input		For input			
	$X = 0$	$X = 1$	$X = 0$	$X = 1$		
0 0	01	00	0	1		
0 1	10	11	1	0		
1 0	00	01	1	0		
1 1	11	10	0	1		

Fig. 7.30 Transition table for Example 7.14

Let the states be symbolized as $00 = a, 01 = b, 10 = c$ and $11 = d$.

The state table is constructed as shown in Fig. 7.31.

Present state	Next state		Output Y	
	For input		For input	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	b	a	0	1
b	c	d	1	0
c	a	b	1	0
d	d	c	0	1

Fig. 7.31 State table of Example 7.14

The state diagram is shown in Fig. 7.32.

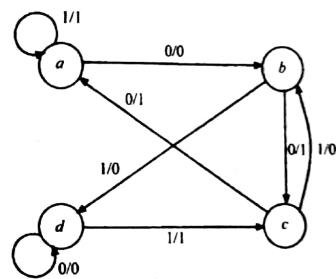


Fig. 7.32 State diagram of Example 7.14

Analyse the synchronous sequential circuit shown in Fig. 7.33.

Solution: Let us write the excitation and output expressions.

$$T_a = XB + \bar{A}B$$

$$T_b = X + \bar{A}B$$

$$Y_1 = \bar{A}X$$

$$Y_2 = BX$$

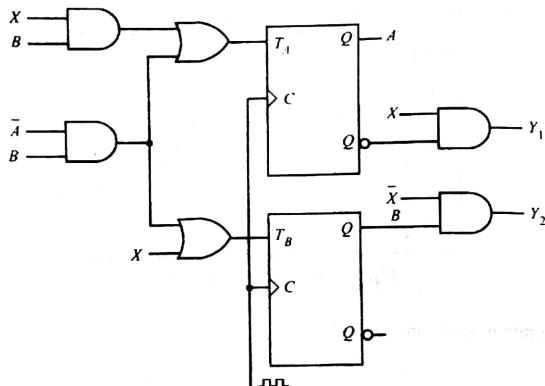


Fig. 7.33 Circuit for Example 7.9

Let us evaluate these expressions as in table shown in Fig. 7.34.

A	B	X	\bar{A}	\bar{X}	XB	\bar{AB}	$XB + \bar{AB}$	$X + \bar{A}B$	\bar{AX}	$B\bar{X}$
0	0	0	1	1	0	0	0	0	0	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	1	1	0	1	1	1	0	1
0	1	1	1	0	1	1	1	1	1	0
1	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	1	0	0	0	0	0	1
1	1	1	0	0	1	0	1	1	0	0

Fig. 7.34 Evaluation of excitation and output expressions

The excitations table is shown in Fig. 7.35.

Present state A B	Excitation T_A, T_B		Output $Y_1 Y_2$	
	For input		For input	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
0 0	00	01	00	10
0 1	11	11	01	10
1 0	00	01	00	00
1 1	00	11	01	00

Fig. 7.35 Excitation table for Example 7.15

The transition table is shown in Fig. 7.36.

Present state A B	Next state $A' B'$		Output $Y_1 Y_2$	
	For input		For input	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
0 0	00	01	00	10
0 1	10	10	01	10
1 0	10	11	00	00
1 1	11	00	01	00

Fig. 7.36 Transition table for Example 7.15

Let us assign $00 = a, 01 = b, 10 = c, 11 = d$
The state table is shown in Fig. 7.37.

Present state	Next state		Output $Y_1 Y_2$	
	For input		For input	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
a	a	b	00	10
b	c	c	01	10
c	c	d	00	00
d	d	a	01	00

Fig. 7.37 State table for Example 7.15

The state diagram is shown in Fig. 7.38.

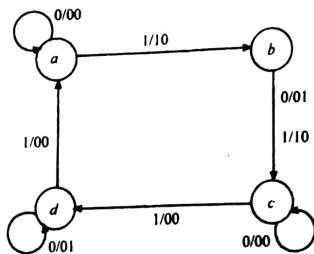
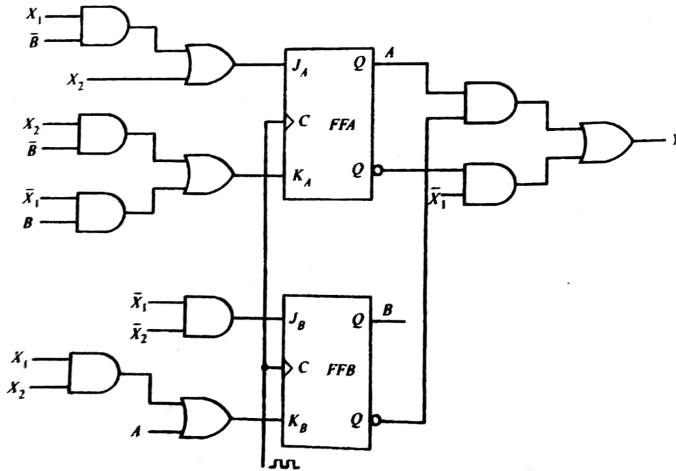


Fig. 7.38 State diagram of Example 7.15

Exercise 7.15

Analyse the given synchronous sequential circuit.



Solution: The excitation and output expressions are

$$\begin{aligned} J_A &= X_1 \bar{B} + X_2 & K_A &= X_2 \bar{B} + \bar{X}_1 B \\ J_B &= \bar{X}_1 \bar{X}_2 & K_B &= X_1 X_2 + A & Y &= A \bar{B} + \bar{X}_1 \bar{A} \end{aligned}$$

Let us evaluate these expressions as in Fig. 7.39.

A	B	X_1	X_2	\bar{A}	\bar{B}	\bar{X}_1	X_2	$X_1 \bar{B}$	$\bar{X}_2 \bar{B}$	$\bar{X}_1 B$	$\bar{X}_1 \bar{X}_2$	$X_1 X_2$	$A \bar{B}$	$\bar{X}_1 \bar{A}$	J_A	K_A	J_B	K_B	Y
0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	1	0
0	0	0	1	1	1	1	0	0	1	0	0	0	0	1	1	1	0	0	1
0	0	1	0	1	1	0	1	1	0	0	0	0	0	1	1	0	1	0	0
0	0	1	1	1	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0
0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	1	0	1	0	0
0	1	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	1	0
0	1	0	1	1	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1
0	1	0	1	1	0	0	1	0	0	1	0	0	0	1	1	1	0	0	1
0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	1	0	0	1	0	0	1	0	0	0	1	1	1
1	0	0	1	0	1	1	0	0	0	0	0	0	1	0	1	1	0	0	1
1	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	0	1
1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	1
1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 7.39 Evaluation of excitation and output expressions

The excitation table is shown in Fig. 7.40.

Present state	Excitation $J_A K_A, J_B K_B$				Output Y					
	For inputs $X_1 X_2$		For inputs $X_1 X_2$							
	A	B	00	01	10	11	00	01	10	11
0 0	00, 10	11, 00	10, 00	11, 01	1	1	0	0		
0 1	01, 10	11, 00	00, 00	10, 01	1	1	1	1	1	1
1 0	00, 11	11, 01	10, 01	11, 01	1	1	1	1	0	0
1 1	01, 11	11, 01	00, 01	10, 01	0	0	0	0	1	0

Fig. 7.40 Excitation table for Example 7.16

The transition table is shown in Fig. 7.41.

Present state		Next state $A^* B^*$				Output $Y_1 Y_2$			
		For inputs $X_1 X_2$		For inputs $\bar{X}_1 \bar{X}_2$		For inputs $X_1 X_2$		For inputs $\bar{X}_1 \bar{X}_2$	
A	B	00	01	10	11	00	01	10	11
0	0	01	10	10	10	1	1	0	0
0	1	01	11	01	10	1	1	0	0
1	0	11	00	10	00	1	1	1	1
1	1	00	00	10	10	0	0	0	0

Fig. 7.41 Transition table for Example 7.16

Let us assign $00 = a$, $01 = b$, $10 = c$ and $11 = d$

The state table is shown in Fig. 7.42.

Present state	Next state								Output	
	For inputs $X_1 X_2$				For inputs $\bar{X}_1 \bar{X}_2$				Output	
	00	01	10	11	00	01	10	11	0	1
a	b	c	c	c	1	1	0	0	0	0
b	b	d	b	c	1	1	0	0	0	0
c	d	a	c	a	1	1	1	1	1	1
d	a	a	c	c	0	0	0	0	0	0

Fig. 7.42 State table for Example 7.16

The state diagram is shown in Fig. 7.43.

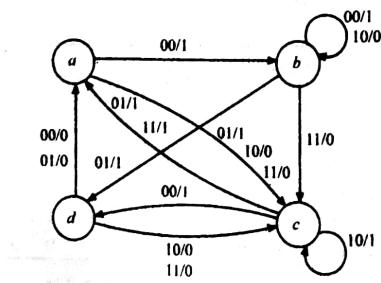


Fig. 7.43 State diagram of Example 7.16

Exercise 7.4

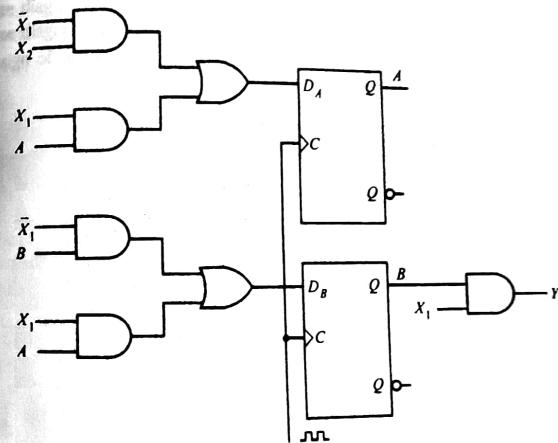
Construct the excitation table, transition table, state table and state diagram of a synchronous sequential circuit built using two positive edge triggered flip-flops A and B. The system inputs are x_1 and x_2 and the output is y . The flip-flop inputs and circuit output are given by

$$J_A = BX_1 + \bar{B}\bar{X}_2 \quad J_B = \bar{A}X_1$$

$$K_A = \bar{B}X_1\bar{X}_2 \quad K_B = A + X_1\bar{X}_2Y = AX_1X_2 + B\bar{X}_1\bar{X}_2$$

Exercise 7.5

Analyse the following synchronous sequential circuit with inputs X_1 and X_2 and output Y .



◆ Exercise 7.6

Analyse the given synchronous sequential circuit with input X and output Y .

