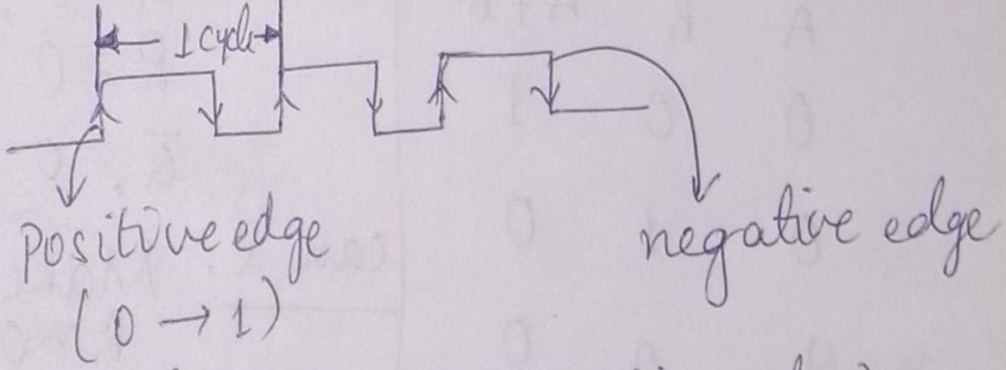
Flip-flops.

* Memory element → It can store 1 bit.
* Clock signal



Something which goes from 0 → 1 (Positive edge)

1 cycle ⇒ T/t seconds (milliseconds)

$$t = \frac{1}{f}$$

Cycle is also called Duration.

$T = t_1 + t_2$ (If $t_1 = t_2$, Square wave/ square clock signal)

t_1 → width of +ve half

$t_1 \neq t_2$ (need not be).

→ Digital holds 0V/5V (0 or 1 value).

* Clock wave - is a square or an assymmetrical square wave produced by clock generator.

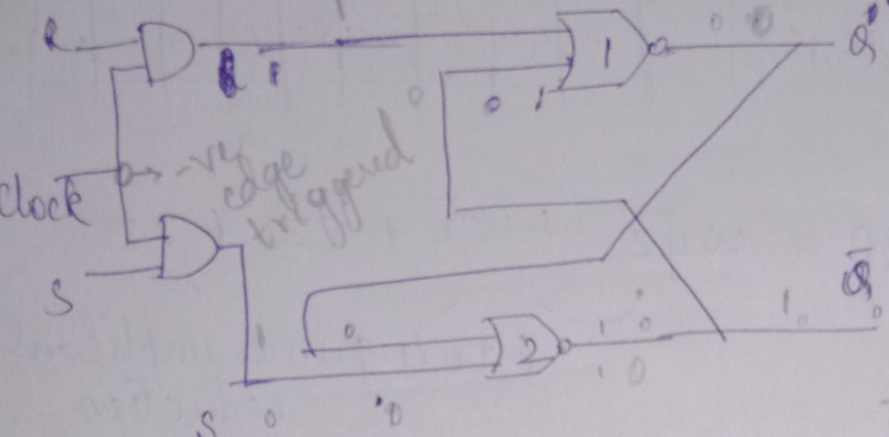
* All the Sequential ckts need clock signal for operation.

S-R (or) R-S Flipflop: (present i/p's, prev. o/p's) ***

(Basic Latch)

Set ↓ Reset ↓ goes back to 0.

F/F ≡ Latch



Back to back (or) Feedback connection

fig-①

NOR		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

case 1. Assume $Q=0$, $\bar{Q}=1$

$R=0$, $S=1$

$\bar{Q}=0$, $\therefore Q=1$

case 2. Make $S=0$ (Prev. latest value $\bar{Q}=0$, $Q=1$)

$R=0, S=0$

$\bar{Q}=0, Q=1$

No change in o/p.

case 3: $S=0$, Make $R=1$.

$\bar{Q}=0$, $Q=0$.

case 4: $S=1$, $R=1$

$\bar{Q}=1, Q=0$.

New, $\bar{Q}=0, Q=0$.

* (1,1) neglected.

S	R	Q_{t+1} (Next state)	$\overline{Q_{t+1}}$
0	0	No change	P.S
0	1	0	1
1	0	1	0
1	1	X	X

Q_{t+1} → Next state

Forbidden state

* On this basic latch, other flipflocks,
  - D
  - JK
  - T

  } flipflops are designed.

D → Delay
T → Toggle
JK → Set (J), Reset (K)

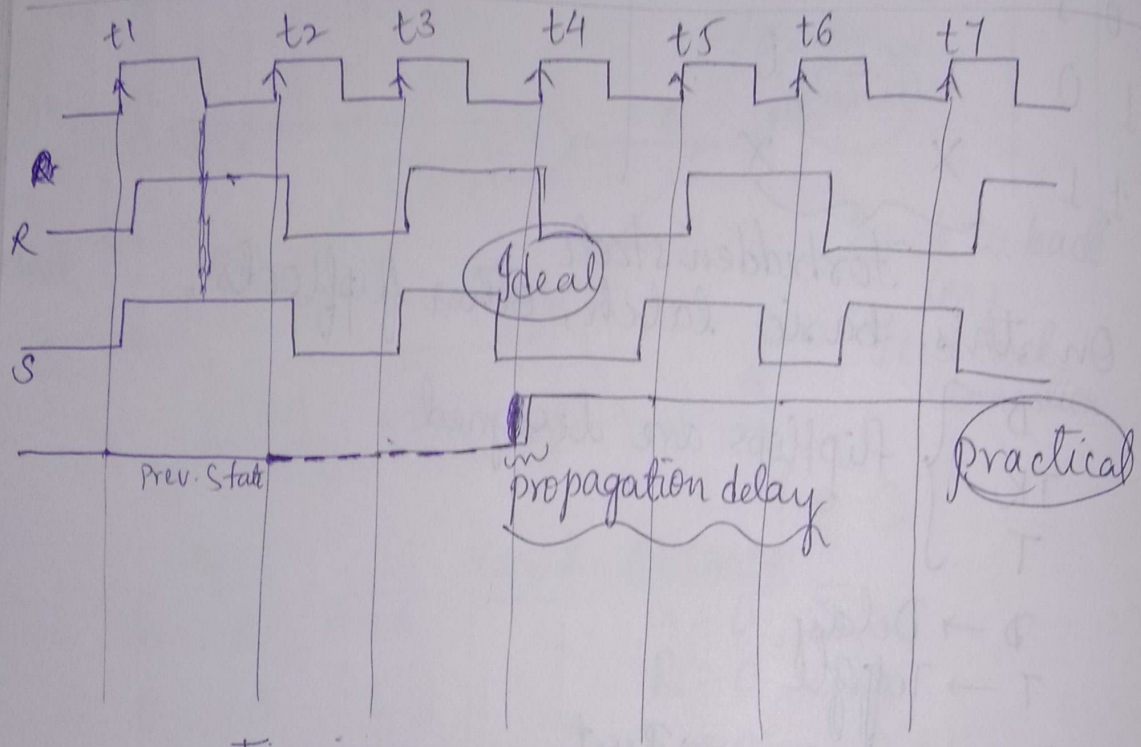
* JK f/f overcomes the last state of SR flipflop.
  ↓ most preferred
  problems of
* In JK f/f, it is no more forbidden. (used instead)

Gate SR with clock:

fig-①

Clock	S	R	Q_{t+1}	$\overline{Q_{t+1}}$
0	X	X	X	X
1	0	0	Noch.	P.S
1	0	1	0	1
1	1	0	1	0
1	1	1	X	X

* Edge triggered:



Timing Diagram ------⇒ Forbidden.

(Should have clock +ve / -ve edge triggered)