Logic diagram

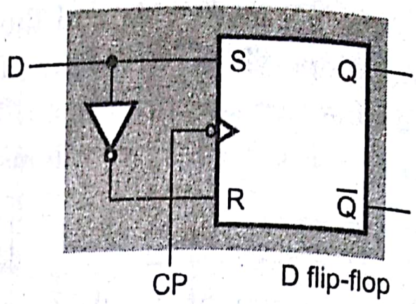


Fig. 4.42 SR to D flip-flop conversion

4.12.2 SR Flip-Flop to JK Flip-Flop

The excitation table for above conversion is as shown in Table 4.9.

Inputs		Present state	Next state	Flip-flop inputs	
J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Table 4.9

K-map simplification

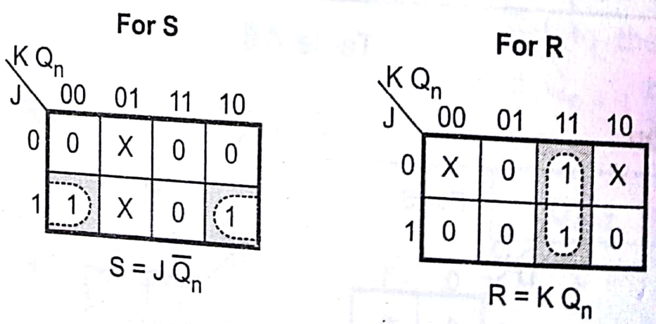


Fig. 4.43

Logic diagram

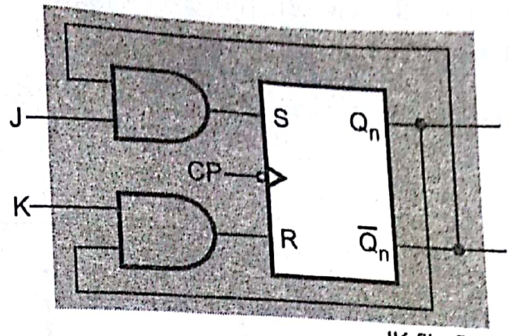


Fig. 4.44 SR to JK flip-flip conversion

4.12.3 SR Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in the Table 4.10.

Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

Table 4.10

K-map simplification

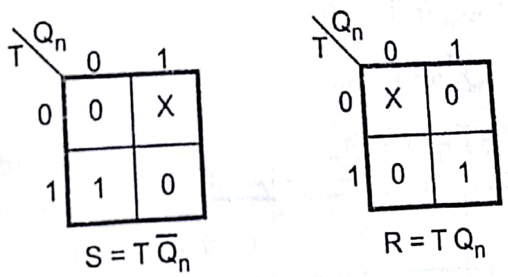


Fig. 4.45

Logic diagram

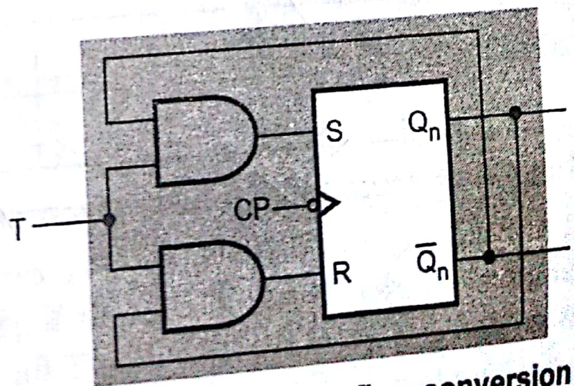


Fig. 4.46 SR to T flip-flop conversion

If we apply clock pulses to the circuit, the circuit output will toggle from 0 to 1 to 0. Thus, we can build 1-bit counter using SR Flip-flop by converting it to T flip-flop.

Example 4.3 : *Prepare the truth table for the circuit of Fig. 4.47 and show that it acts as a T-type flip-flop.*

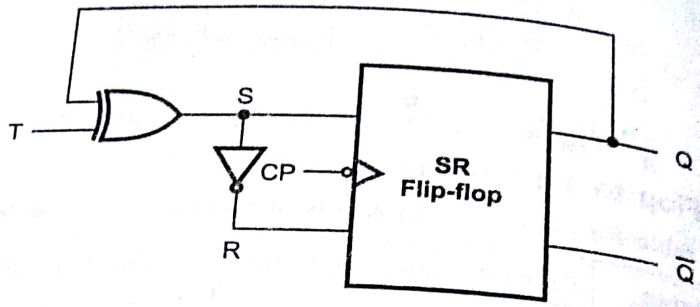


Fig. 4.47

Solution : For SR flip-flop,

$$Q_{n+1} = S + \overline{R}\,Q_n \quad \text{... Characteristics equation}$$

$$= S + S\,Q_n \quad \because R = \overline{S}$$

$$= S(1 + Q_n)$$

$$= S$$

We have, $S = Q_n \oplus T$

$$\therefore \quad Q_{n+1} = Q_n \oplus T$$

$$= T\overline{Q}_n + \overline{T}\,Q_n \quad \text{... characteristic equation of T flip-flop}$$

C_p	T	Q_n	$S = Q_n \oplus T$	$R = \overline{S}$	$Q_{n+1} = S$
↓	0	0	0	1	0
↓	0	1	1	0	1
↓	1	0	1	0	1
↓	1	1	0	1	0

Table 4.11 Truth table for the given circuit

Looking at column 1 and column 5 of the table 4.11 we can conclude that when T = 0, the output does not change and when T = 1, the output toggles. Thus, the given circuit acts as a T flip-flop. This is another way of implementing T flip-flop using SR flip-flop.

4.12.4 JK Flip-Flop to T Flip-Flop

The excitation table for above conversion is as shown in Table 4.12.

Input	Present state	Next state	Flip-flop inputs	
T	Q_n	Q_{n+1}	J_A	K_A
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

Table 4.12

K-map simplification

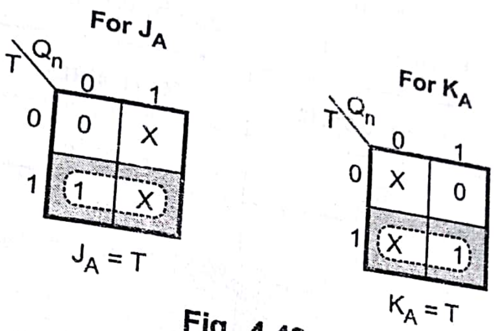


Fig. 4.48

Logic diagram

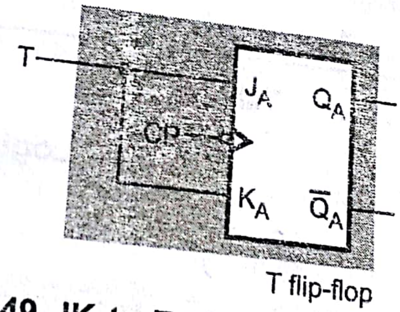


Fig. 4.49 JK to T flip-flop conversion

4.12.5 JK Flip-Flop to D Flip-Flop

The excitation table for above conversion is as shown in the Table 4.13.

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

Table 4.13

Input	Present state	Next state	Flip-flop input
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Table 4.14

K-map simplification

For D

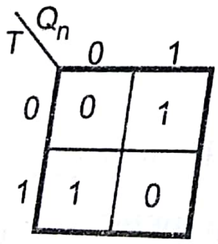


Fig. 4.52

$$D = \bar{T}Q_n + T\bar{Q}_n$$

$$= T \oplus Q_n$$

Logic diagram

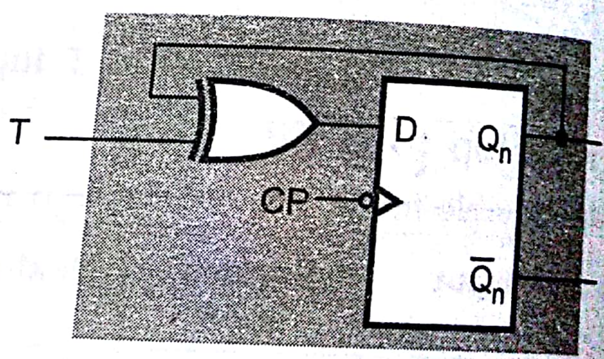


Fig. 4.53 D to T flip-flop conversion

Example 4.4 : *Analyze the circuit and prove that it is equivalent to T flip-flop.*

Solution : To analyze the circuit means to derive the truth table for it.

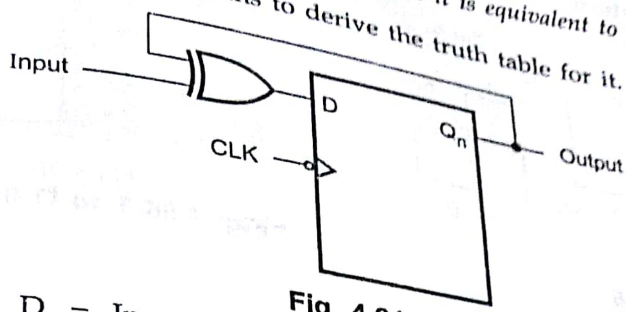


Fig. 4.64

We have, $D = \text{Input} \oplus Q_n$

CLK	Input	Q_n	$D = \text{input} \oplus Q_n$	Q_{n+1}	
↓	0	0	0	0	When input is 0 output does not change
↓	0	1	1	1	
↓	1	0	1	1	When input is 1 output toggles
↓	1	1	0	0	

Table 4.15 Truth table for given circuit

In the above circuit, output does not change when input is 0 and it toggles when input is 1. This is the characteristics of T flip-flop. Hence, the given circuit is T flip-flop constructed using D flip-flop.

4.12.7 T Flip-Flop to D Flip-Flop

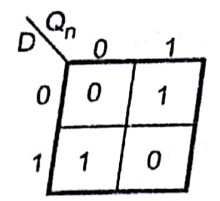
The excitation table for above conversion is as shown in the Table 4.16.

Input	Present state	Next state	Flip-flop input
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 4.16

K-map simplification

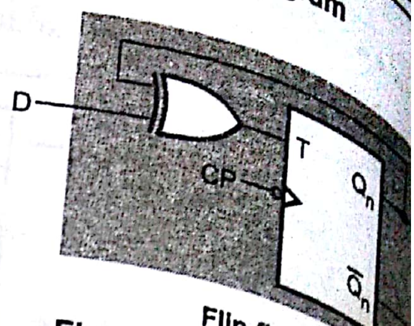
For T



$T = D\,\overline{Q}_n + \overline{D}\,Q_n$

Fig. 4.55

Logic diagram



Flip-flop conversion

Fig. 4.56 T to D flip-flop co

$$T = D\,\overline{Q}_n + \overline{D}\,Q_n$$

4.12.8 JK Flip-Flop to SR Flip-Flop

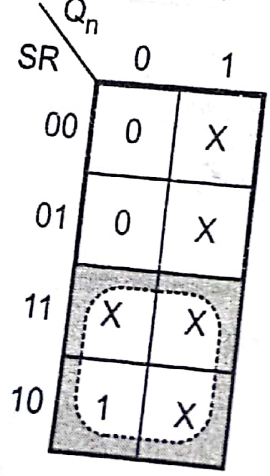
The excitation table for above conversion is as shown in Table 4.17.

Inputs		Present state Q_n	Next state Q_{n+1}	Flip-flop inputs	
S	R			J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X 1	X	X
1	1	1	X 1	X	X

Table 4.17 Excitation table for JK to SR conversion

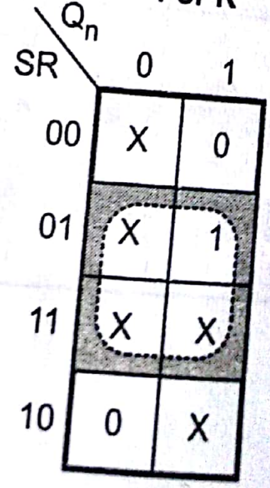
K-map simplification

For J



J = S

For K



K = R

Fig. 4.57

Logic diagram

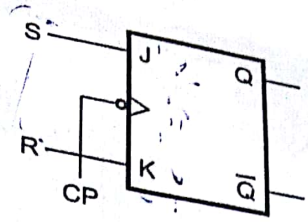


Fig. 4.58 JK to SR

4.12.9 D Flip-Flop to SR Flip-Flop

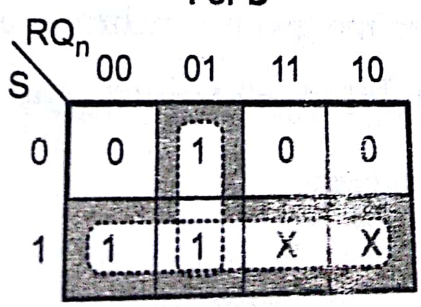
The excitation table for above conversion is as shown in the Table 4.18.

Inputs		Present state	Next state	Flip-flop input
S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	X	X
1	1	1	X	X

Table 4.18 Excitation table for D to SR conversion

K-map simplification

For D



$$D = \overline{R}\,Q_n + S$$

Fig. 4.59