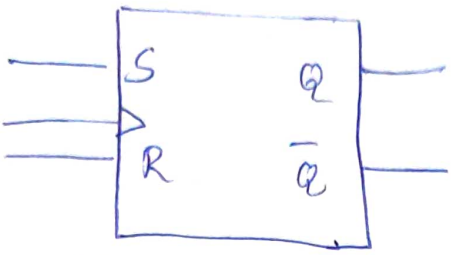
Logic Circuit

S R



Graphical Symbol

① Function Table.
Characteristic Table.
Truth Table

CLK	S	R	Q	$\bar{Q}$
	0	0	P.S	
	0	1	0	1
	1	0	1	0
	1	1	Forbidden state	x x

Characteristic Equation Q_{t+1}

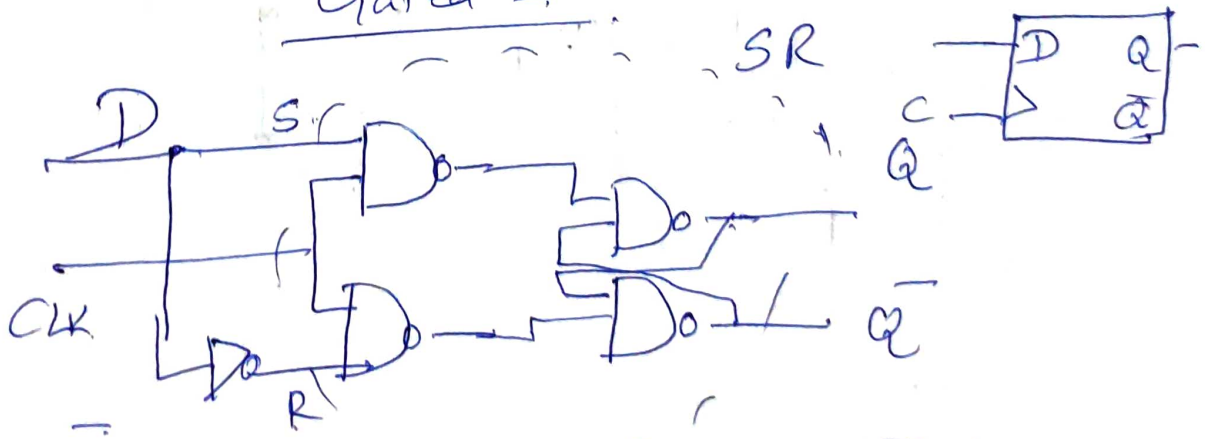
S	R	P.S Q_t	N.S Q_{t+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

Basic Latch

S \ RQ_t	00	01	11	10
0	0	1	0	0
1	1	1	x	x

$$Q_{t+1} = S + \bar{R} Q_t$$

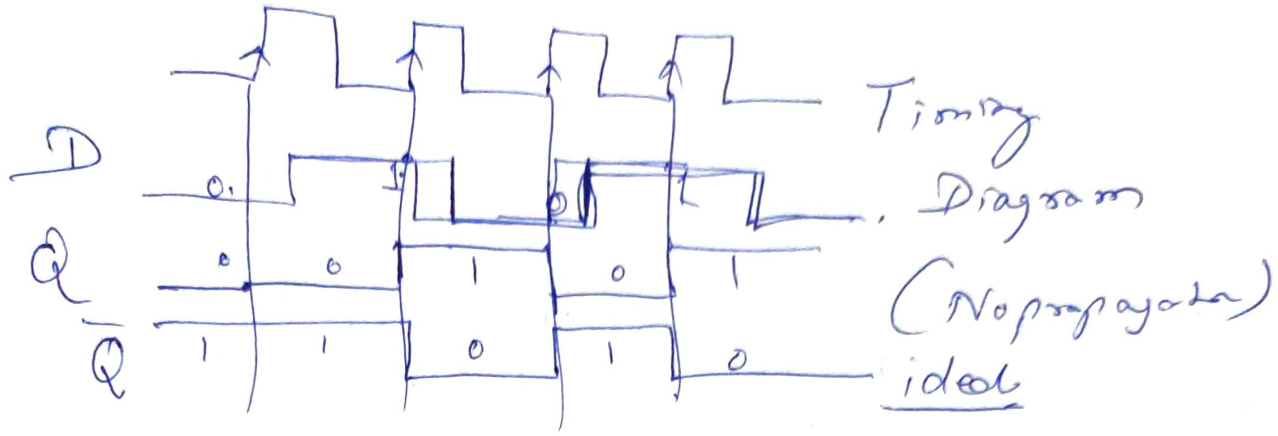
Gated D



CLK	D	Q	$\bar{Q}$
1	0	0	1
1	1	1	0
0	x	P.S	

Q Follows D

Delay



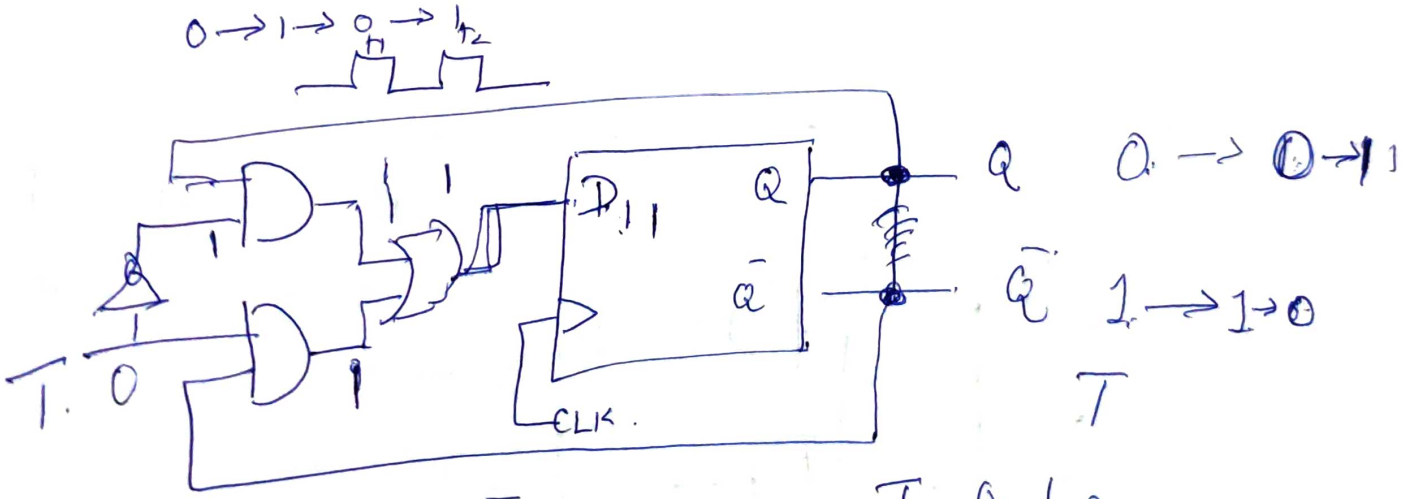
Characteristic Equation

i/p	P.S	N.S.
D	Q_t	Q_{t+1}
0	0	0
0	1	0
1	0	1
1	1	1

D \ Q_t	0	1
0	0	0
1	1	1

$$Q_{t+1} = D.$$

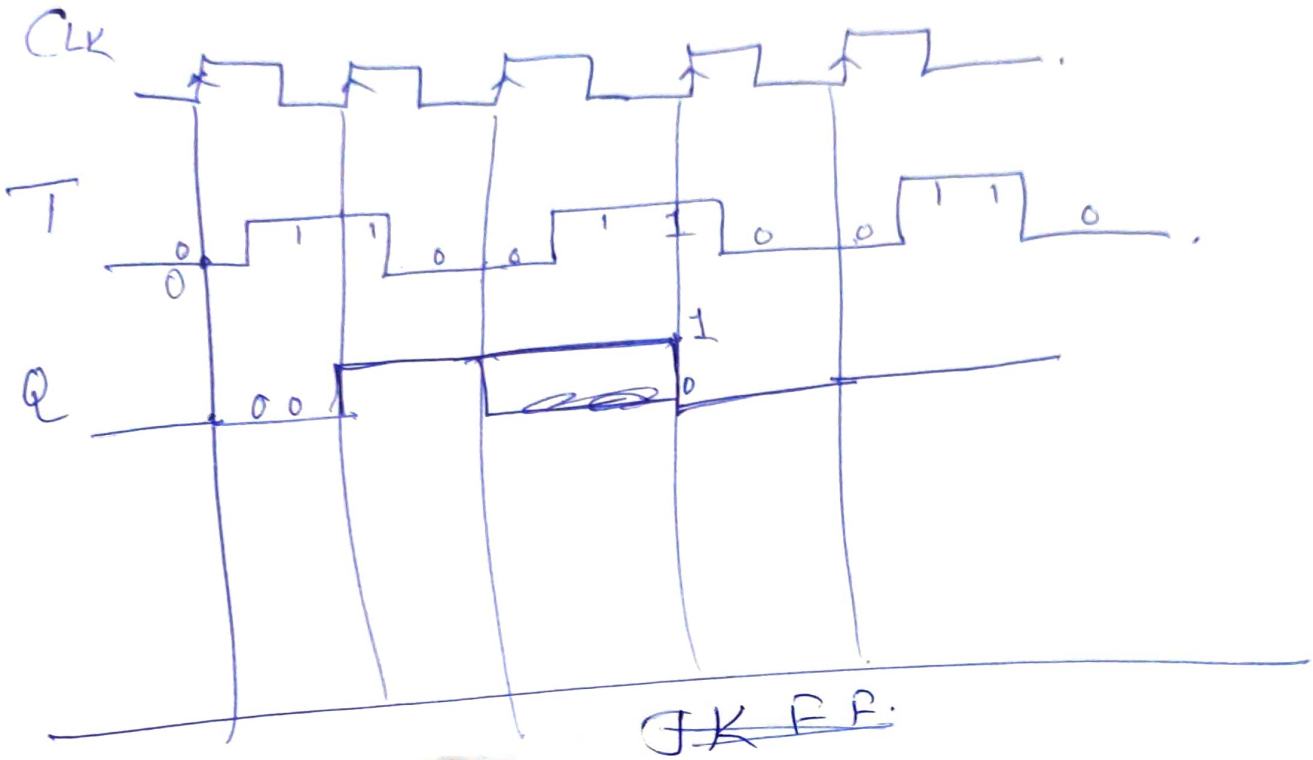
T F.F Toggle.



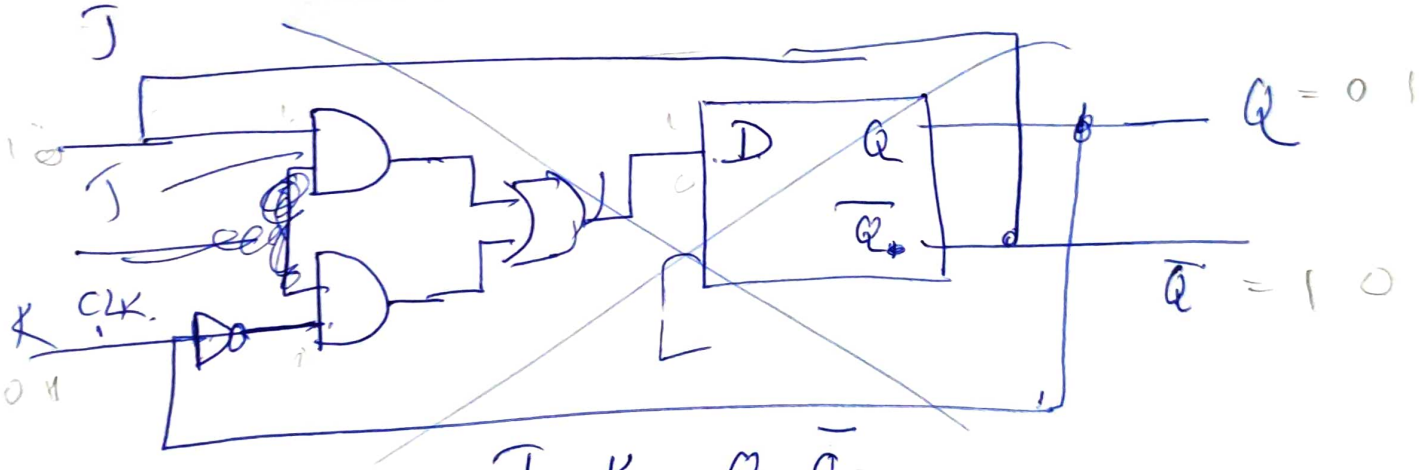
T	Q_{t+1}
0	Q_t
1	$\bar{Q}_t$

T	Q_t	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{t+1} = T\bar{Q}_t$$

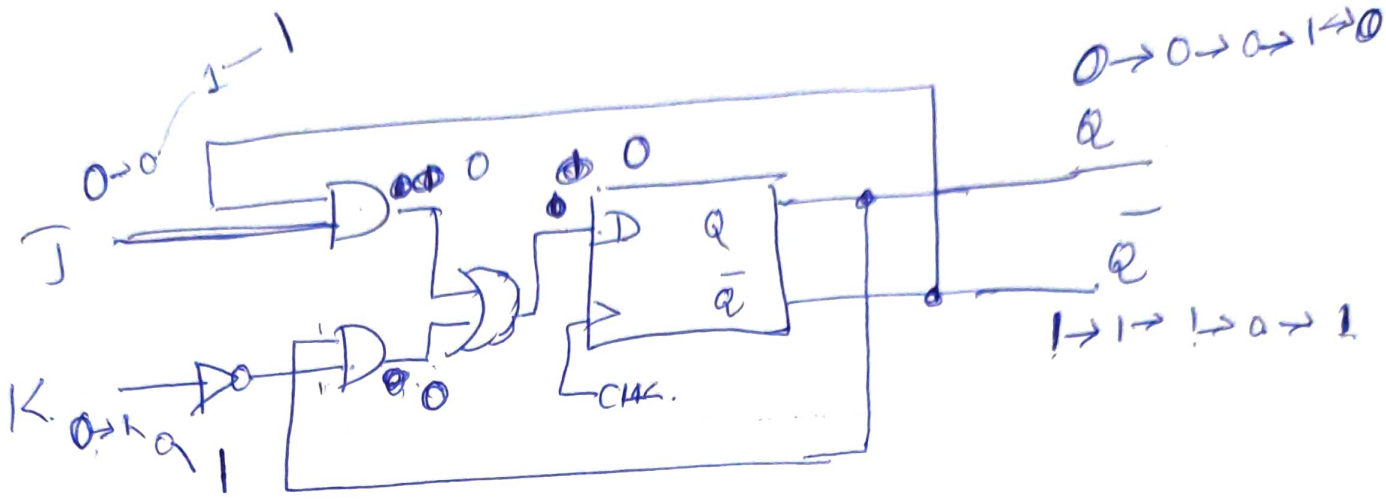


~~JK FF.~~



J	K	Q	$\bar{Q}$
0	0	P.S	
0	1	0	1
1	0	1	0
1	1	toggle	

JK FF



J	K	Q	$\bar{Q}$
0	0	P. S.	
0	1	0	1
1	0	1	0.5
1	1	0	1 toggles
		1	
		1	0

The last state of JK table is called as Toggle state (equivalent to TFFs.)