Excitation Table of all the FF are nothing but inputs required to make a transition from present state to next state

Shift Registers

1) Register can store information temporary.
   ↳
2) Register with capability to shift is called shift register

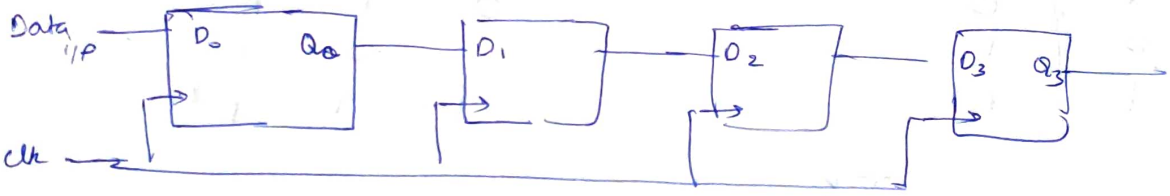
left shift → x 2

right shift → ÷ 2

MSB ← LSB is left shift

MSB → LSB is right shift

~~data~~ SISO [serial In serial out]

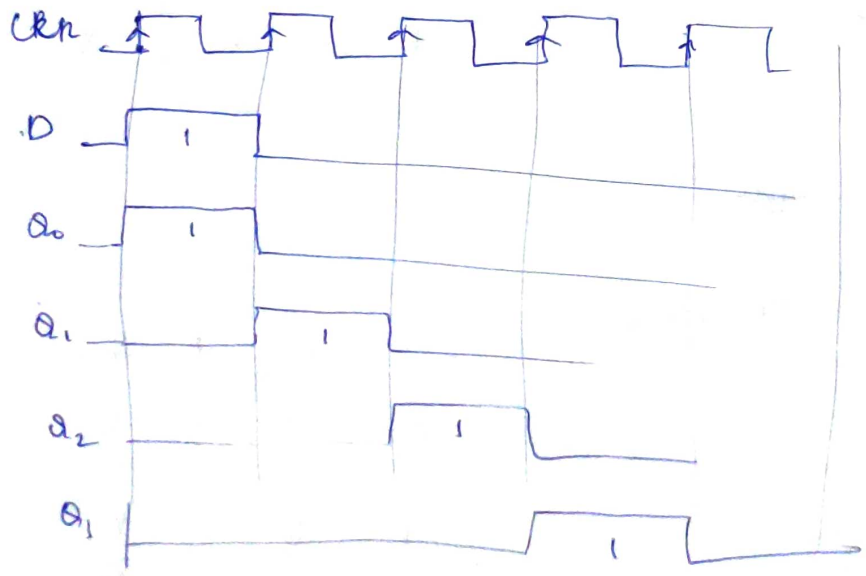


data is 1 for 1 clock cycle

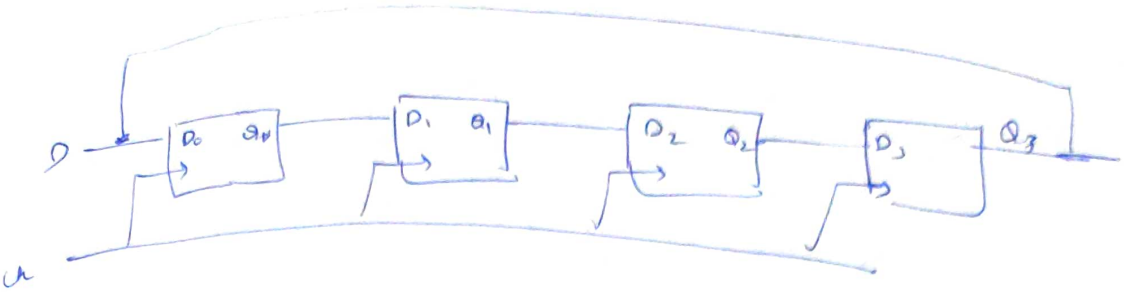
at Clk 1, $Q_0 = 1$

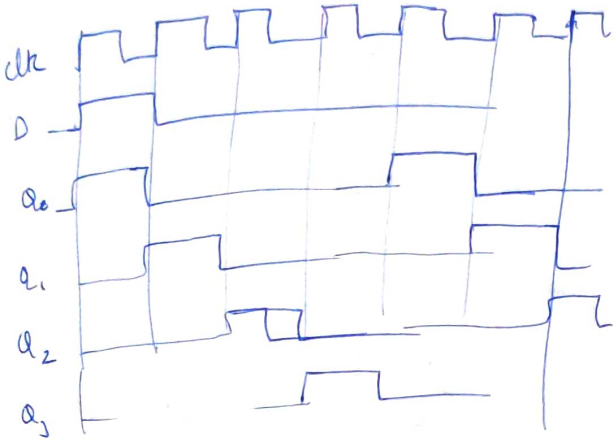
at clk = 2, Q_0 is shifted to D_1 & so on

at 4th pulse $Q_3 = 1$



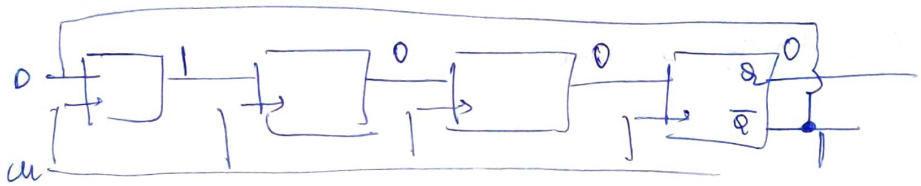
Ring counter





clk	D	Q_0	Q_1	Q_2	Q_3
1	1	1	0	0	0
1	0	0	1	0	0
1	0	0	0	1	0
1	0	0	0	0	1
1	0	1	0	0	0

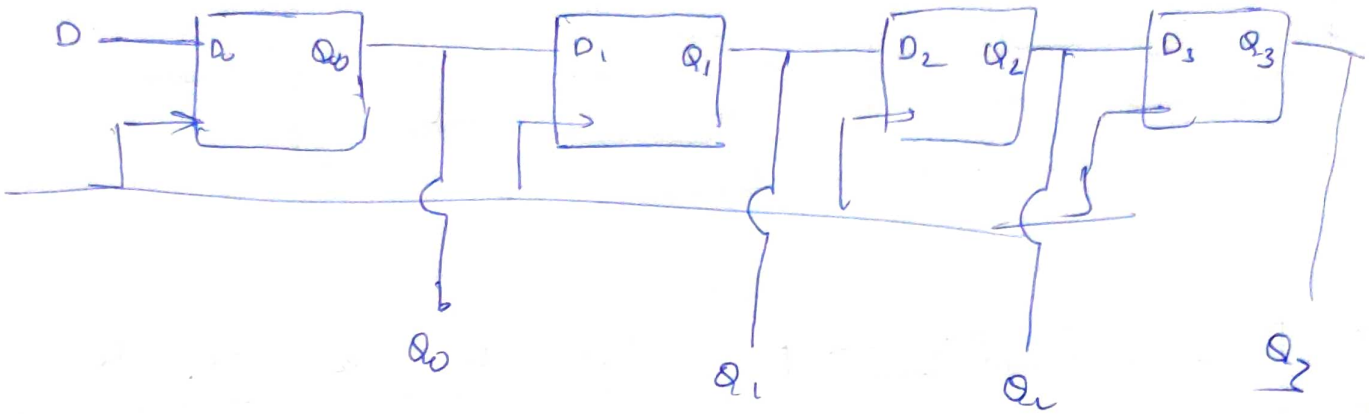
Twisted Ring Counter (Johnson)



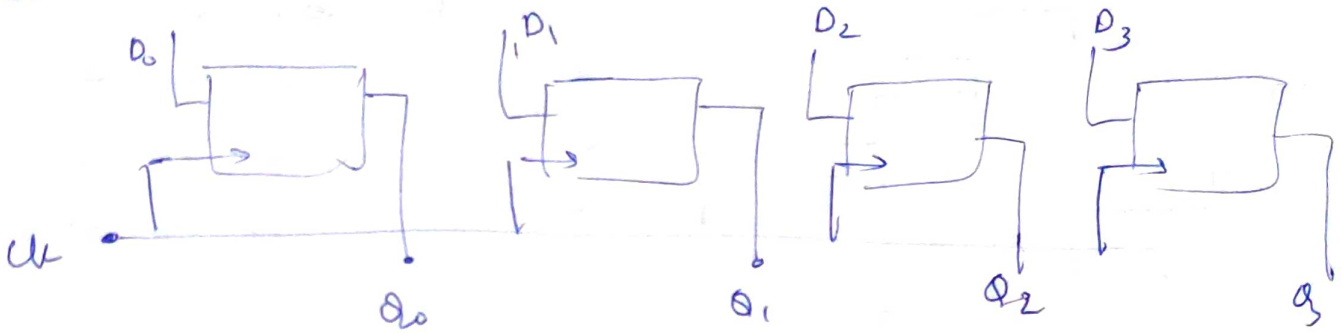
clk	D	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
1	1	1	0	0	0	1
1	0	0	1	0	0	1
1	0	0	0	1	0	1
1	0	0	0	0	1	0
1	0	0	0	0	0	1
1	1	1	0	0	0	1

8 bit

SIPO



PIPO



PISO

with SISO

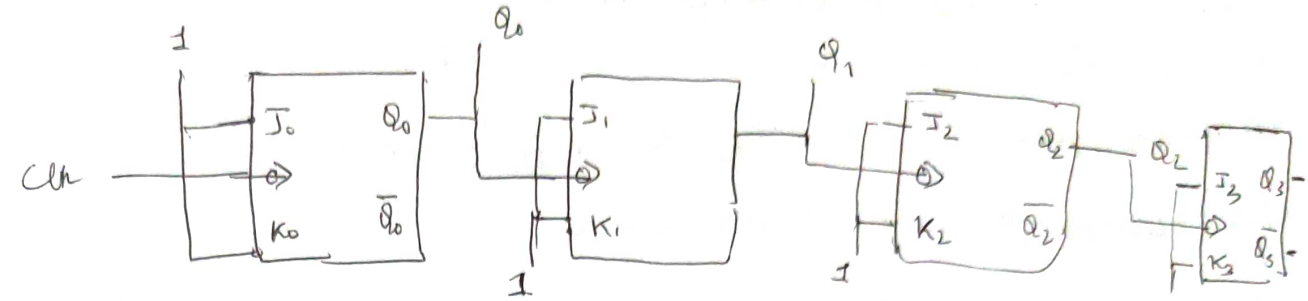
→ ring counter / swing counter

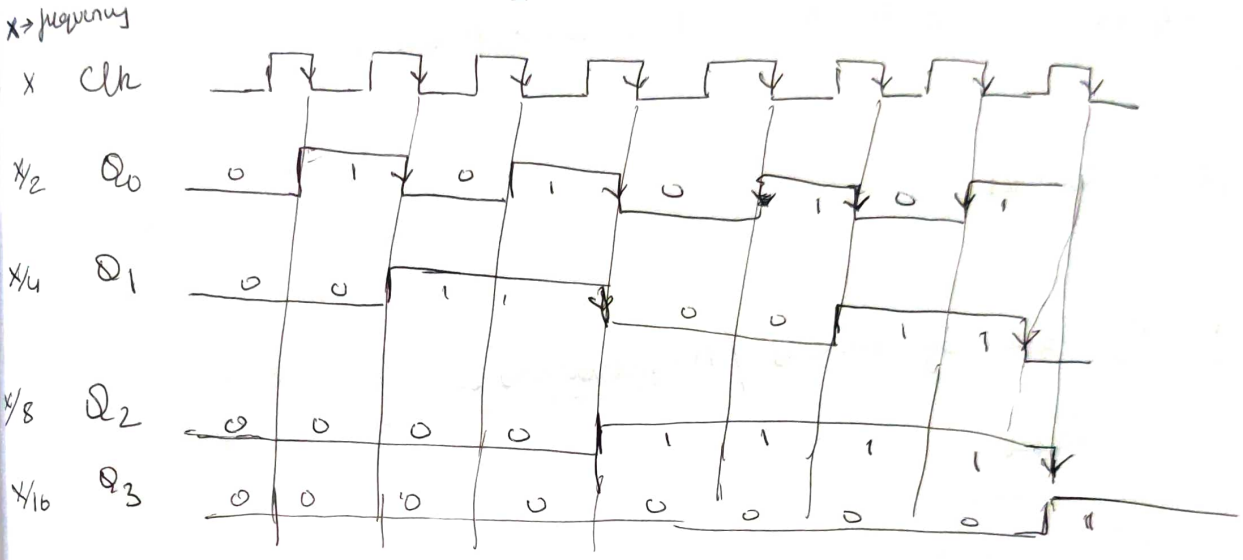
Shift reg

used in multiplication / division

CISC → complex instruction set

A Synchronous Counter





The 3 bit up counter is converted to 4 bit binary up counter by adding 4th flipflop J_3 K_3.

#	Q_3	Q_2	Q_1	Q_0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0

Properties :-

(i) Period of clk is 10ms

$$F = \frac{1}{10 \times 10^{-3}} = 100\ Hz = x$$

(ii) Frequency Divider circuit

Down Counter

The same ckt can be converted to down counter initially all o/p will be 1, 1, 1. The clock is connected from $\bar{Q}_0$ to $J_1 K_1$ to $Q \bar{Q}_1$ in $J_2 K_2$

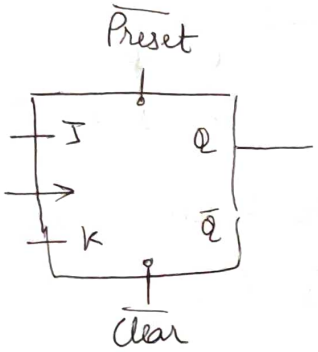
This becomes a 3 bit Down Counter.

All outputs are held to one if it counts down to 1, 1, 1

⇒ Mod divider ckt

Q)

what diff b/w Synchronous / Asynchronous :-

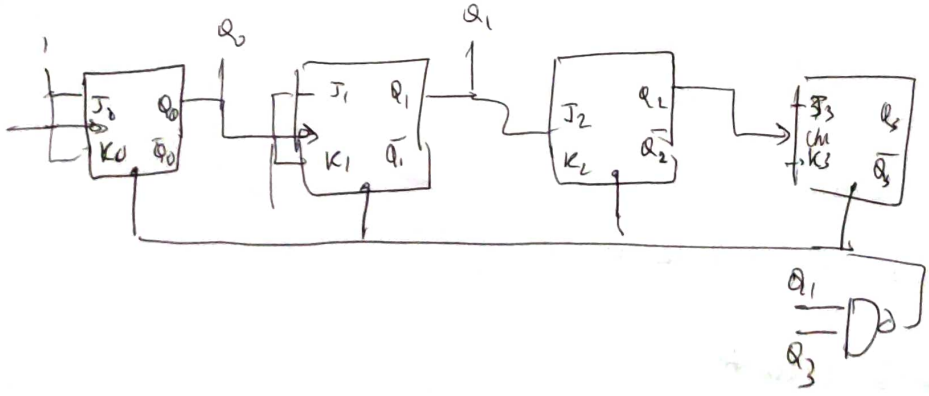


Preset and clear are Asynchronous input they are preset & clear. without i/p J & K and clk, the output Q has been set to 1 by connecting $\overline{preset}$ to 0.

o/p Q can set to 0 by enabling $\overline{clear}$ to 0.

Reset Synchronization

TRUNCATE



Modulo Counters [Unit-5]

It counts from 0 to n-1

* If n = 8 , 3 bit Binary ~~count~~ up counter counting 0 to 7

n = 6 It counts from 0 to 5 & next state will be zero

Asynchronous Counters

- 3bit up count & down counts
- modulo counter
- 4bit down / up counter

The same 3 bit counter can start from any other state, with 1 clock pulse $q_0 = 1$ $q_1 = 1$ $q_2 = 0$ then continuous clk is fed counts from 0 to 7. and Resets to 0

Parallel loading / ~~Preset~~

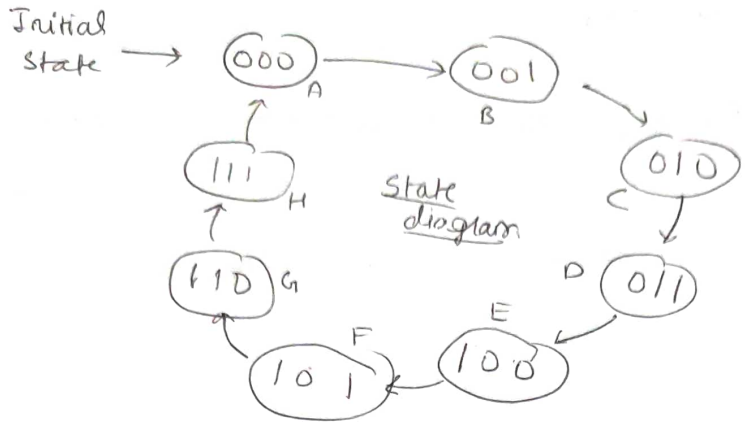
$J_0 = 1$, $K_0 = 0$, 1 clk pulse is fed q_0 becomes 1

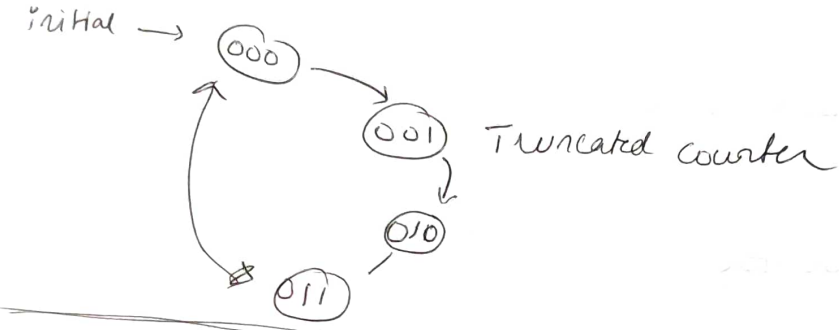
If at same time $J_1 = 0$, $J_2 = 0$, $q_0 = 1$, $\bar{q}_0 = 0$

Then the continuous clk is fed & initial state is from 2 - 7 and resets at all zeros.

De Synchronous counter

given diagram draw counter





→ state assignment

SYNCHRONOUS

Q) Design & modulate synchronous RF. Draw ckt, timing diagram, design, function table

Previous state			Next state			Excitation Table		
Q_2	Q_1	Q_0	Q_{2+1}	Q_{1+1}	Q_{0+1}	J_2K_2	J_1K_1	J_0K_2
0	0	0	0	0	1	0 X	0 X	1 X
0	0	1	0	1	0	0 X	1 X	X 1
0	1	0	0	1	1	0 X	X 0	1 X
0	1	1	1	0	0	1 X	X 1	X 1
1	0	0	1	0	1	X 0	0 X	1 X
1	0	1	1	1	0	X 0	1 X	X 1
1	1	0	1	1	1	X 0	X 0	1 X
1	1	1	0	0	0	X 1	X 1	X 1

WKT

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J_2 =

Q_1Q_0 / $\bar{Q}_2$	00	01	11	10
$\bar{Q}_2$	0	0	(1)	0
Q_2	X	X	X	X

$J = Q_1 Q_0$

K_2

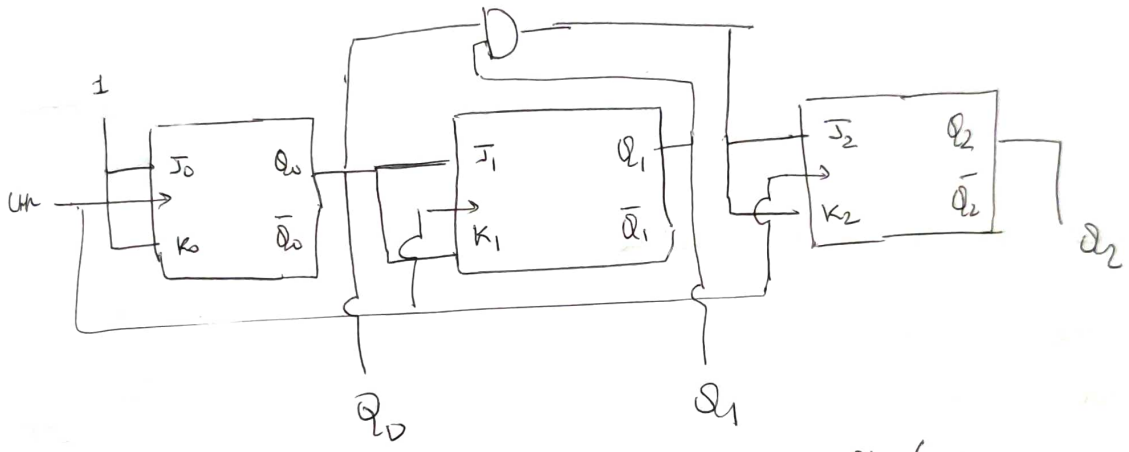
Q_1Q_0 / Q_2	00	01	11	10
0	X	X	(X)	1
1	0	0	(1)	0

$K_2 = Q_1 Q_0$

J_1 =

X	X	1	0
X	X	1	0

$J_1 = Q_0$ $\quad K_1 = Q_0$



Q) design a counter to count 2, 3, 0, 6, 7, 1

PS				NS				J_3K_3	J_2K_2	J_1K_1	J_0K_0
Q_3	Q_2	Q_1	Q_0	Q_{3+1}	Q_{2+1}	Q_{1+1}	Q_{0+1}	excitation table			
m_2 0	0	1	0	0	0	1	1	0	X		
m_3 0	0	1	1	0	0	0	0	0	X		
m_0 0	0	0	0	1	0	0	0	1	X		
1	0	0	0	0	1	1	0	X	1		
0	1	1	0	0	0	0	1	0	X		
0	0	0	1	0	0	1	0	0	X		

J_3

Q_3 / $Q_2Q_1Q_0$	000	001	011	010	110	111	101	100
0	(1) 0	0 1	0 3	0 2	X 6	X 7	X 5	X 4
1	X 12	X 13	X 15	X 14	X 10	X 11	X 9	X 8

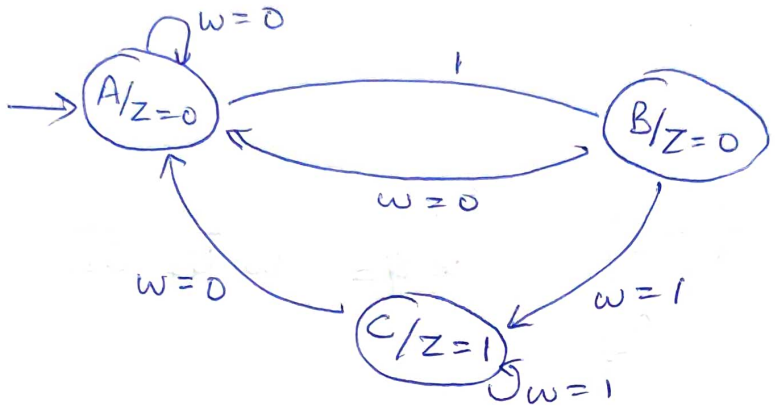
Unit-5

Sequential circuit

1) Moore circuits [Basic steps]

The o/p will depend on state & the i/p and the output is changed in next state.

eg



State Diagram

Sequence

			A		B	A	B	C	C	A	B	C	A
i/p	w	0		1		0	1		1	0	1	1	0
o/p	Z	0		0		0	0		1	0	0	1	0

State ~~diagram~~ Table

Present state PS	Next state NS		Output Z
	w=0	w=1	
A	A	B	0
B	A	C	0
C	A	C	1

state assignment

3 states, 2 digits (unique)

A = 00 B = 01 C = 10

	PS		NS				O/P
			w = 0		w = 1		
	Q_2	Q_1	Q_{2t+1}	Q_{t+1}	Q_{2t+1}	Q_{t+1}	Z
A	0	0	0	0	0	1	0
B	0	1	0	0	1	0	0
			0	0	1	0	1
C	1	0					
	1	1	x	x	x	x	x

//

state assignment (different form)

consider Q_2 & Q_{2t+1} ↑ Q_1 Q_{t+1} ↑

	PS		NS		Z		
w	Q_2	Q_1	Q_{2t+}	Q_{t+1}		D_2	D_1
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	0	0	1	0	0
0	1	1	x	x	x	x	x
1	0	0	0	1		0	1
1	0	1	1	0		1	0
1	1	0	1	0		1	0
1	1	1	x	x	x	x	x

Q_2 & Q_1 are O/P of 2 flip flops

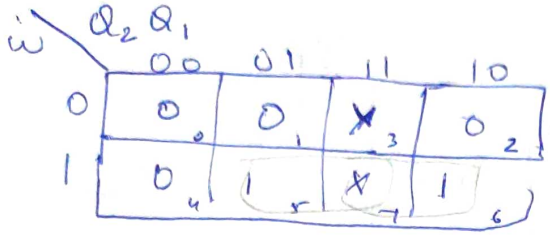
we will choose D-flip flop

excitation Table

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

equation for D_2 & D_1 using K-map

D_2

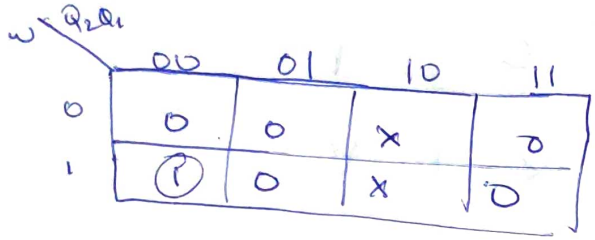


consider x

$D_2 = wQ_1 + wQ_2$

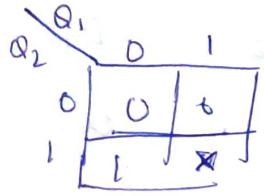
$\boxed{D_2 = w[Q_1 + Q_2]}$

D_1

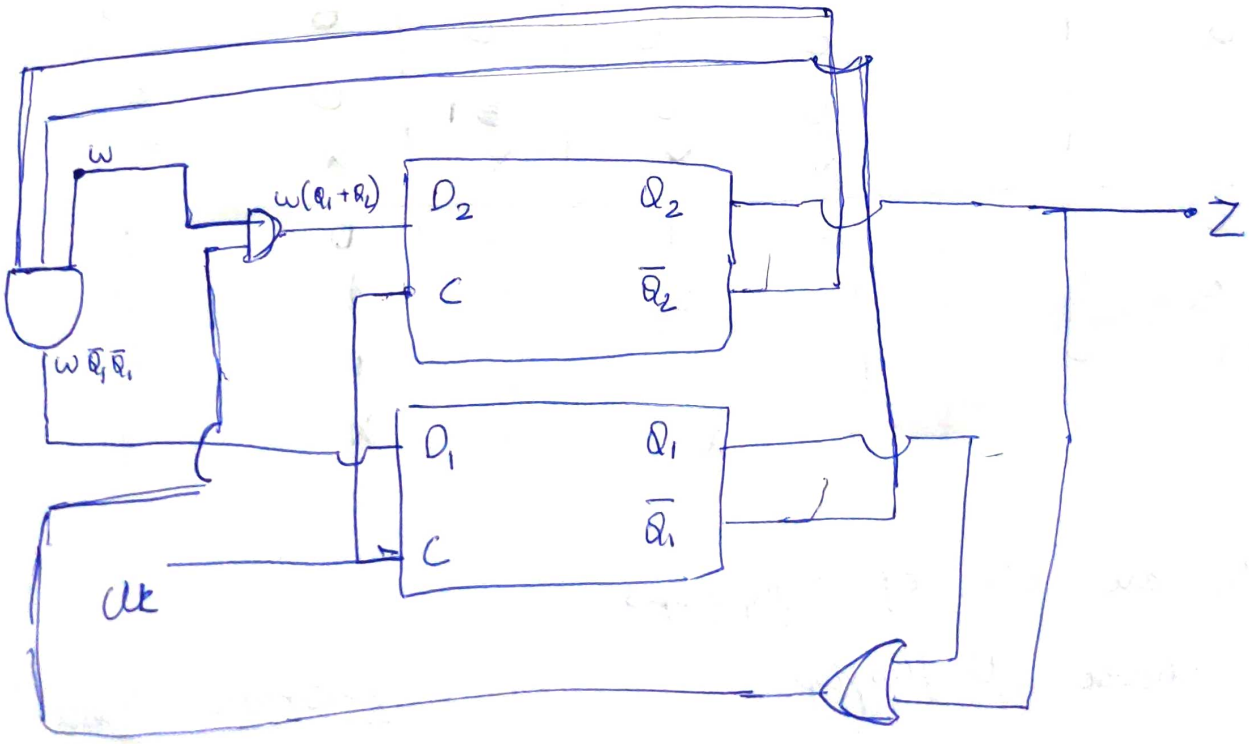


$\boxed{D_1 = w\,\bar{Q}_2\,\bar{Q}_1}$

Z



$\boxed{Z_2 = Q_2}$



w	Q_2	Q_1	Q_{t+1}	Q_{t+1}	J_2	K_2	J_1	K_1
0	0	0	0	0	0	X	0	X
0	0	1	0	0	1	X	X	1
0	1	0	0	0	X	1	0	X
0	1	0	X	X	X	X	X	X
1	0	0	0	1	0	X	1	X
1	0	1	1	0	1	X	X	1
1	1	0	1	0	X	0	0	X
1	1	1	X	X	X	X	X	X

excitation Table

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J_2

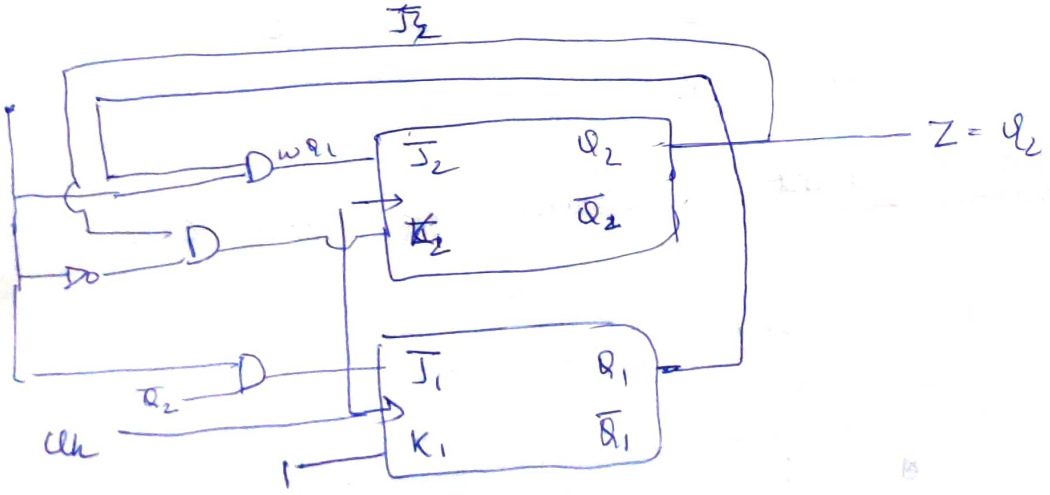
w \ Q_2Q_1	00	01	11	10
0	0	0	X	X
1	0	1	X	X

$J_2 = wQ_1$

$K_2 = \bar{w} Q_2$

$J_1 = w \bar{Q}_2$

$K_1 = 1$

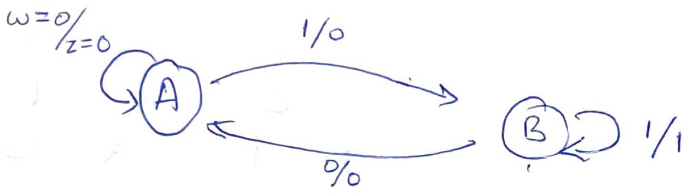


Mealy

O/P depends on present value of I/P and also on present state i/p & also on present state.

	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w	0	1	0	1	1	0	1	1	1	0	1
Z	0	0	0	0	1	0	0	1	1	0	0
	A	B	A	B	B	A	A	B	B	A	

i/p/o/p = w/z = 0/0 & 1/1 & 1/0



It reduces number of states

State Table

PS	NS		O/P	
	w=0	w=1	w=0	w=1
0 A	A	B	0	0
1 B	A	B	0	1

State Assignment [2 states 1 digit A=0, B=1]

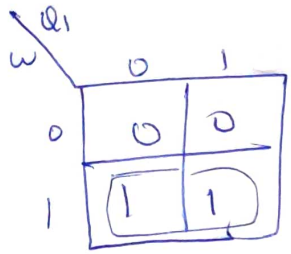
PS	NS		O/P	
	w=0	w=1	w=0	w=1
Q_1	Q_{t+1}	Q_{t+1}	Z	Z
A 0	0	1	0	0
B 1	0	1	0	1

only 1 flip flop

PS		NS	Z	D	J_1 K_1
w	Q_1	Q_{t+1}			
0	0	0	0	0	0 X
0	1	0	0	0	X 1
1	0	1	0	1	1 X
1	1	1	1	1	X 0

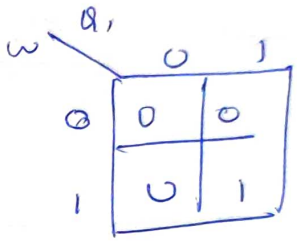
with D-flipflop

D_1

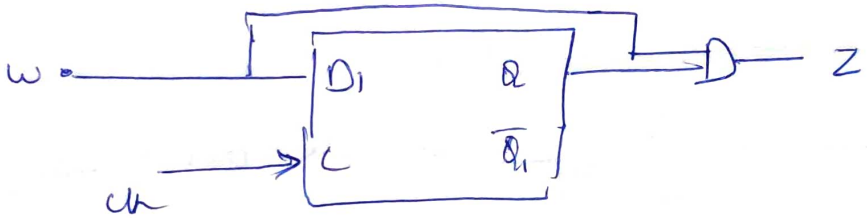


$D_1 = w$

Z

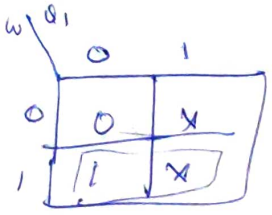


$Z = w Q_1$



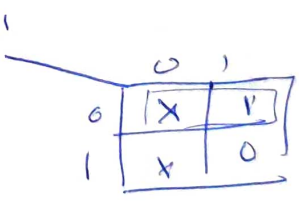
11y for JK flip flop

J_1

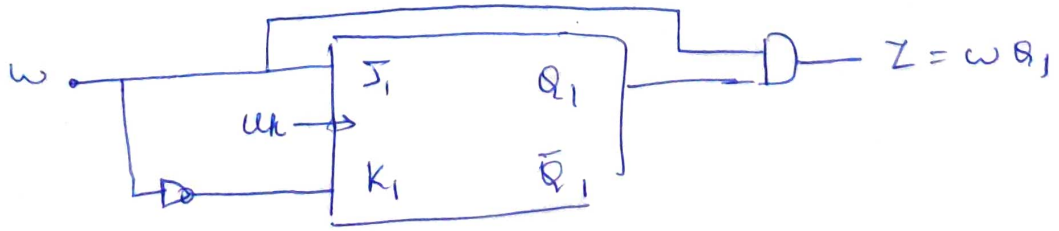


$J_1 = w$

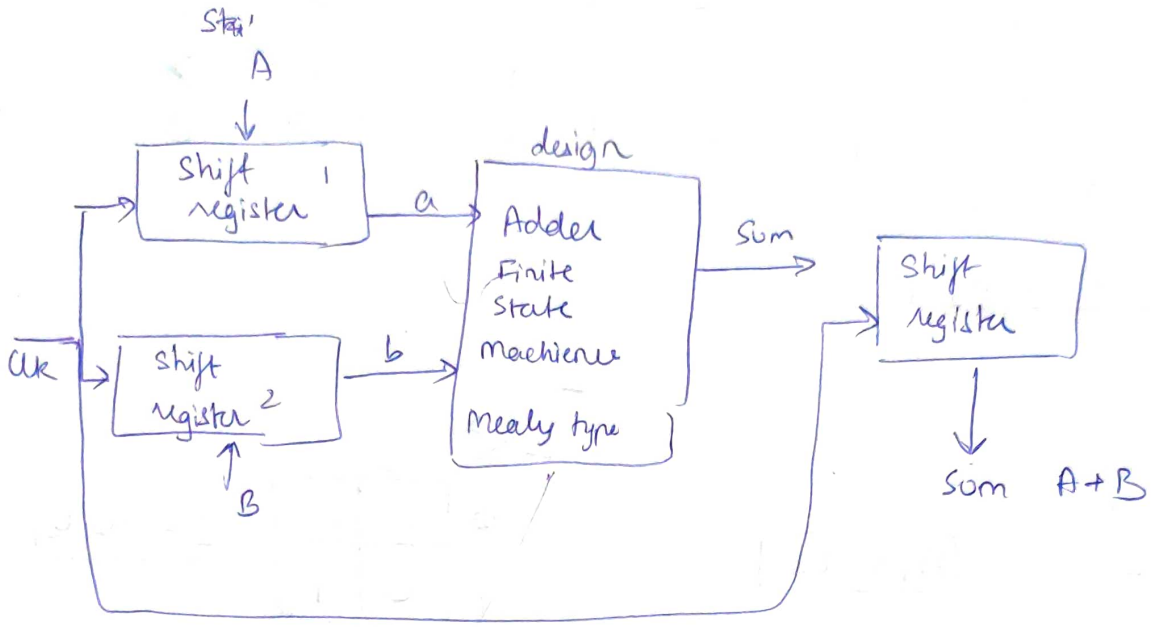
K_1

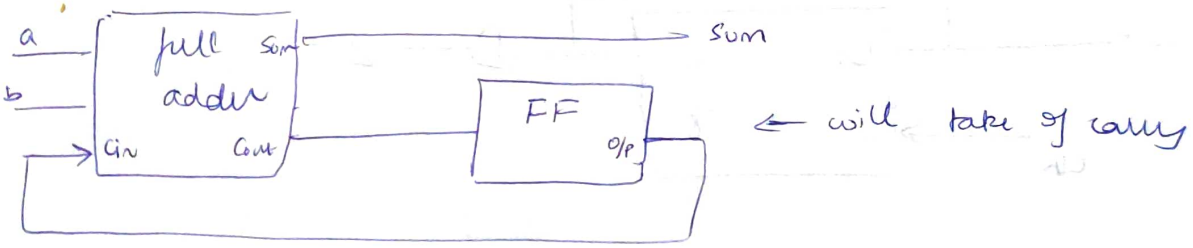


$K_1 = \bar{w}$



Serial adder . sequential type Addition binary.





Full adder Function Table

	Cin	a	b	Sum	carryout (C_o)		
S_0	0	0	0	0	0	S_0	$C_{in}=0$
S_0	0	0	1	1	0	S_0	
S_0	0	1	0	1	0	S_0	
S_0	0	1	1	0	1	S_1	
S_1	1	0	0	1	0	S_0	$C_{in}=1$
S_1	1	0	1	0	1	S_1	
S_1	1	1	0	0	1	S_1	
S_1	1	1	1	1	1	S_1	

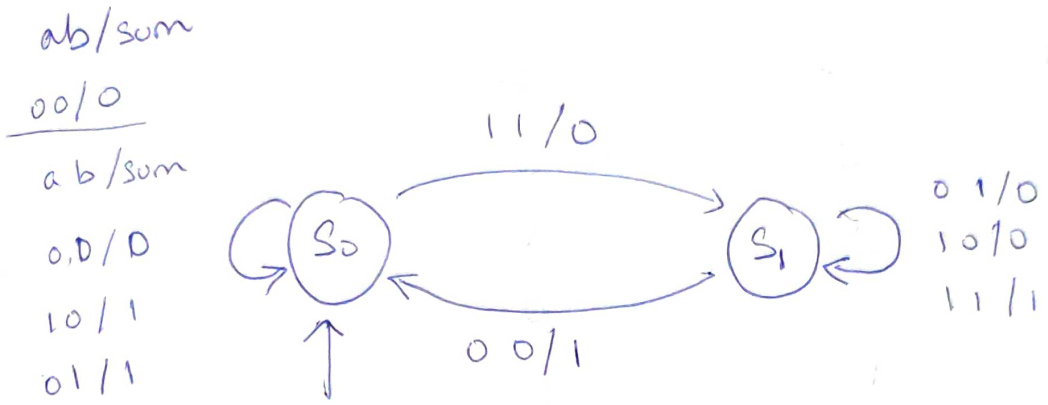
state diagram

1 case: $C_{in} = 0$

S_0

case 2: $C_{in} = 1$

S_1



FSM → finite state machine

FSM remains in S_0 when ab = 01, 10, 01

FSM $S_0 \rightarrow S_1$ when ab = 11

FSM remain in S_1 when ab = 01, 10, 11

FSM $S_1 \rightarrow S_0$ when 00

State Table → only (S_0 | S_1)

PS	NS ab				OP - Sum ab			
	00	01	10	11	00	01	10	11
S_0 0	S_0	S_0	S_0	S_1	0	1	1	0
S_1 1	S_0	S_1	S_1	S_1	1	0	0	1

State assignment Table → only values

0	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1

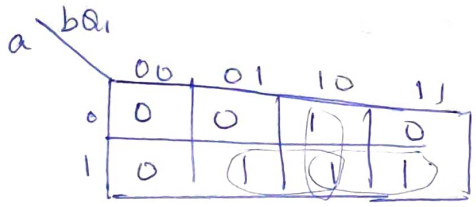
Design FF

PS (states)			NS	D_1
a	b	Q_1	Q_{1t+1}	
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

eg:

D - K-map

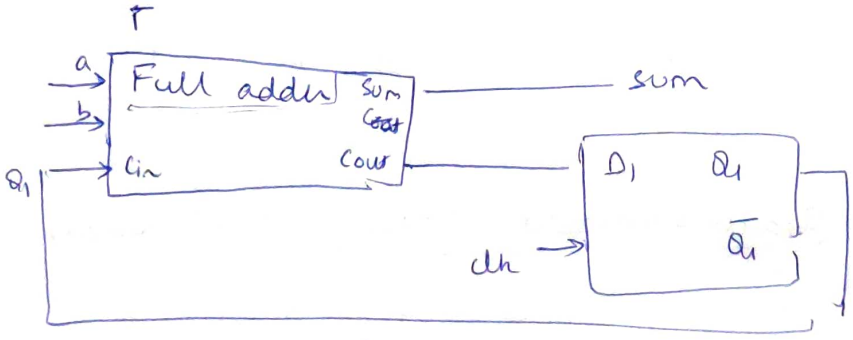
D

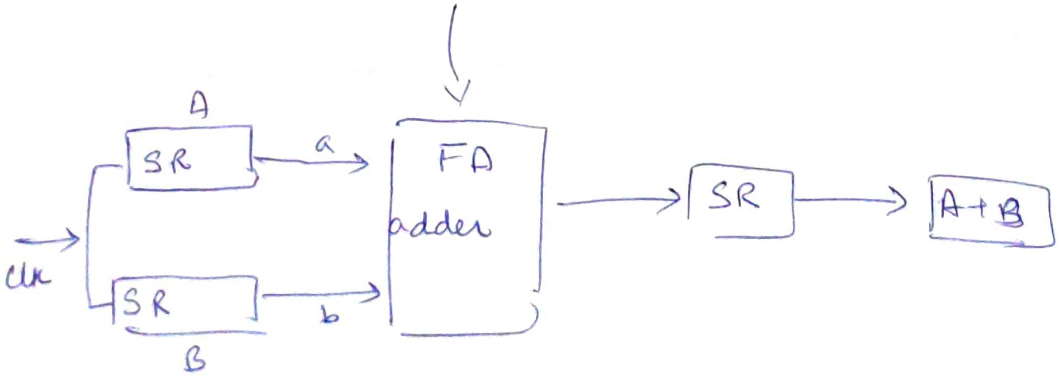


$D = bQ_1 + aQ_1 + ab$

equ same as carry out of Full adder

Adder FSM





carry look ahead adder / carry save adder

Ripple carry adder propagates carry from one stage to another stage. Delay so to overcome we need fast adder

NC - no carry
CP → carry propagate

Full adder

A	B	Cin	Sum	Cout	
0	0	0	0	0	NC
0	0	1	1	0	NC
0	1	0	1	0	NC
0	1	1	0	1	CP
1	0	0	1	0	NC
1	0	1	0	1	CP
1	1	0	0	1	carry generate
1	1	1	1	1	carry generate

when A & B = 1

Refer to figure in book

C →
P → propagate
G → generate

$P_i = A_i \oplus B_i$

$G_i = A_i B_i$

carry generated when A = 1 & B = 1

$$Sum = P_i + C_i$$

$$C = G_i + P_i + C_i$$

→ fast adder equation