

CHAPTER 13

Wave-Shaping Circuits

Learning Objectives

After completing this chapter, you will learn the following:

- RC and RL low-pass and high-pass circuits.
- RC and RL integrator and differentiator circuits.
- Different types of diode-based clipping circuits.
- Basic clamping circuit, its limitations and practical clamping circuit.
- Bistable, monostable and astable multivibrator circuits configured around discrete semiconductor devices.
- Schmitt trigger circuit and its applications.
- Multivibrator circuits configured around digital integrated circuits.
- Multivibrator circuits configured around timer IC 555.

The topics discussed in this chapter include basic linear and non-linear wave shaping circuits like the RC and RL integrator, RC and RL differentiator, clipping circuits, clamping circuits and multivibrator circuits. Though a clamping circuit is not a wave-shaping circuit in the true sense, it has been chosen to be discussed here because the concepts relevant to the operation of clamping circuits are similar to those that explain the operation of RC wave-shaping and clipping circuits. A clamper circuit acts on an AC waveform, sinusoidal or non-sinusoidal, and gives it a DC level though it does not alter the wave shape. It is an important building block of voltage-multiplying circuits. Keeping in view the scope of the present text, a separate chapter on clamping circuits would not be justified.

13.1 Basic RC Low-Pass Circuit

Figure 13.1 shows the basic RC low-pass circuit comprising a single-section RC circuit with output taken across the capacitor. The output voltage is given by

$$V_o = \left(\frac{X_C}{\sqrt{R^2 + X_C^2}} \right) \times V_i \quad (13.1)$$

Qualitatively, since the output is taken across the capacitor and the reactance of a capacitor is inversely proportional to the frequency, the output voltage will fall with increase in frequency (Figure 13.2). That is how

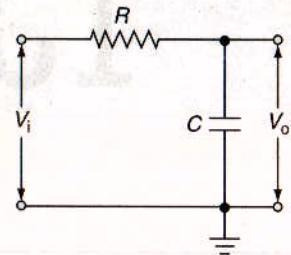


Figure 13.1 | RC low-pass circuit.

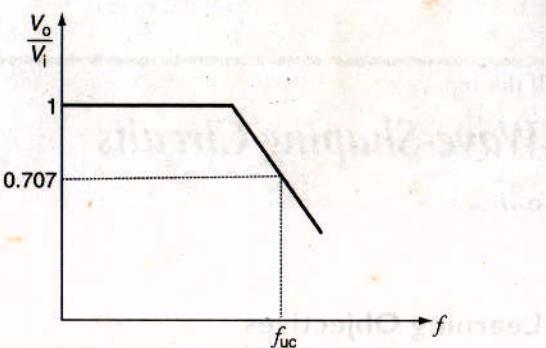


Figure 13.2 | Frequency response of a RC low-pass circuit.

an RC network of the type shown in Figure 13.1 behaves as a low-pass circuit. The upper 3 dB cut-off frequency is the frequency at which output amplitude is 0.707 times (or 3 dB below) the nominal maximum amplitude. The nominal maximum output amplitude is same as the input amplitude; therefore, the ratio (V_o/V_i) equals 0.707 at 3 dB cut-off frequency.

The ratio (V_o/V_i) becomes 0.707 when the resistance (R) equals capacitive reactance (X_C). Therefore, the cut-off frequency (f_{uc}) is given by

$$f_{uc} = \frac{1}{2\pi RC} \quad (13.2)$$

We will now study the behavior of this circuit toward step and pulse inputs.

Step Input

For a step input (V_i) of Figure 13.3(a), the output voltage (V_o), which is also voltage across C , rises exponentially towards the final value of V with a time constant (RC). The output voltage (V_o) is given by

$$V_o = V(1 - e^{-t/RC}) \quad (13.3)$$

This expression is valid only when the capacitor is initially fully discharged. If the capacitor were initially charged to a voltage V_o less than V , then the exponential charging equation would be

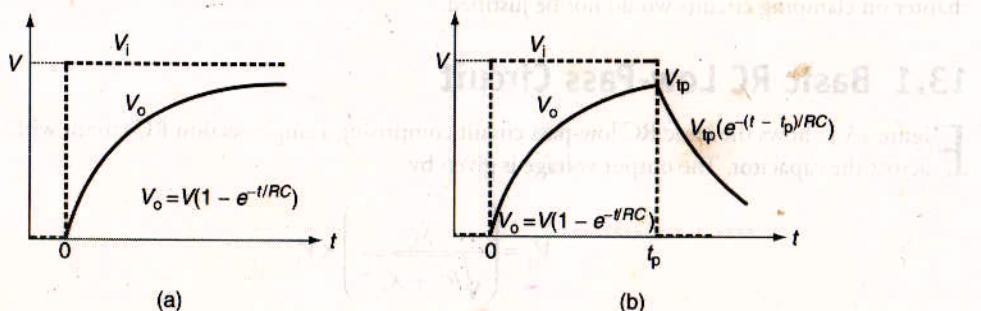


Figure 13.3 | (a) Step response of low-pass circuit; (b) pulse response of low-pass circuit.

$$V_o = V - (V - V_o)e^{-t/RC} \quad (13.4)$$

If this input step occurs at time $t = t_1$, then the following equation represents the charging process:

$$V_o = V[1 - e^{-(t-t_1)/RC}] \quad (13.5)$$

Pulse Input

For the pulse input of Figure 13.3(b), output (V_o) during the high time of the pulse is given by

$$V_o = V(1 - e^{-t_p/RC}) \quad (13.6)$$

At $t = t_p$, the amplitude of the output voltage is given by

$$V_o(t = t_p) = V(1 - e^{-t_p/RC}) = V_{tp} \quad (13.7)$$

The output (V_o) during the low time of the pulse is given by

$$V_o = V_{tp}(e^{-(t-t_p)/RC}) \quad (13.8)$$

We are often interested in knowing the quality with which the leading and the trailing edges will be passed through the RC low-pass circuit. Such a situation arises particularly in the analysis of high-frequency amplifiers where the amplifier input has a finite capacitance and this capacitance along with source resistance constitutes a low-pass RC network. We will see that the capability of the network to pass fast transitions depends upon the upper 3 dB cut-off frequency of the network.

The quality with which this network reproduces fast transitions is expressed by the magnitude of the rise time (t_r) which is the time taken by the output to change from 10% to 90% of the impressed transition or step. From the exponential charging relationship, it can be verified that

$$t_r = 2.2 RC \quad (13.9)$$

The relationship between the upper 3 dB cut-off frequency (f_{uc}) and the rise time (t_r) is given by

$$f_{uc} = \frac{0.35}{t_r} \quad (13.10)$$

where f_{uc} is specified in MHz and t_r is specified in μs . This expression indicates that higher the upper 3 dB cut-off frequency, smaller is the rise time. Therefore, for faithful reproduction of fast transitions, f_{uc} should be as high as possible.

13.2 RC Low-Pass Circuit as Integrator

If the circuit shown in Figure 13.1 is an integrator circuit, the output voltage V_o should be integral of the input voltage (V_i), that is,

$$V_o = K \int V_i dt$$

where K is a constant. In the given RC circuit, if the product RC is much larger than the time period (T) of the applied input, the capacitor voltage (or the output voltage in the present case) would change by only a very small amount as the input goes through a complete cycle. In such a case, it is not wrong to assume that whole of input voltage (V_i) appears across the resistor (R) only. As a result current (I_i) can be expressed as

$$I_i = \frac{V_i}{R}$$

The output voltage (V_o) across the capacitor is given by

$$V_o = \frac{1}{C} \int I_i dt = \frac{1}{C} \int \frac{V_i}{R} dt = \frac{1}{RC} \int V_i dt \quad (13.11)$$

Therefore, output voltage (V_o) is integral of input voltage (V_i) provided that the time constant is much larger than the time period of the input signal, that is, $RC \gg T$. In fact, if $RC \geq 15T$ integration is near ideal.

EXAMPLE 13.1

Refer to Figure 13.4. Determine the amplitude of V_o at the time of input pulse going low and also 1 ms after it has gone low.

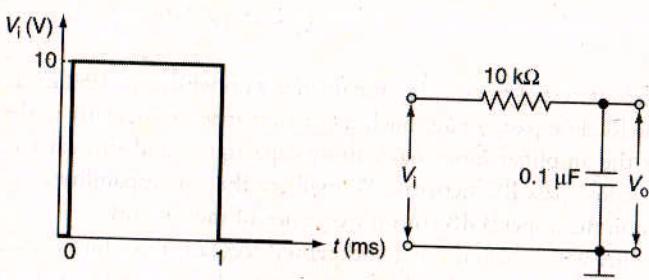


Figure 13.4 | Example 13.1.

Solution

1. The time constant $= R \times C = 10 \times 10^3 \times 0.1 \times 10^{-6} = 10^{-3} \text{ s} = 1 \text{ ms}$.
2. Coincidentally, the time constant equals the pulse width. The output V_o will be 63.1% of the final value of 10 V, that is, $V_o = 6.31 \text{ V}$ at the time of pulse going high to low.
3. In general, the charging process is governed by the expression

$$V_o = V(1 - e^{-t/RC})$$

For $t = RC$, output voltage V_o is 63.1% of the final voltage (V).

4. When the input pulse goes low, the capacitor starts discharging as per

$$V_o = V'(e^{-(t-t_p)/RC})$$

Here, $V' = 6.31 \text{ V}$ and $t_p = 1 \text{ ms}$. Again V_o will be 36.9% of (V') 1 ms after the capacitor starts discharging as 1 ms happens to be equal to circuit time constant. Therefore, the output voltage after 1 ms $= 0.369 \times 6.31 \text{ V} = 2.33 \text{ V}$.

5. The output waveform is shown in Figure 13.5.

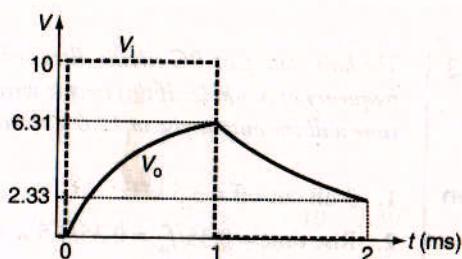


Figure 13.5 | Solution to Example 13.1.

EXAMPLE 13.2

How will the circuit of Figure 13.6(a) respond to a 10 V step input of Figure 13.6(b)? In what time will the output rise from 1 V to 9 V?

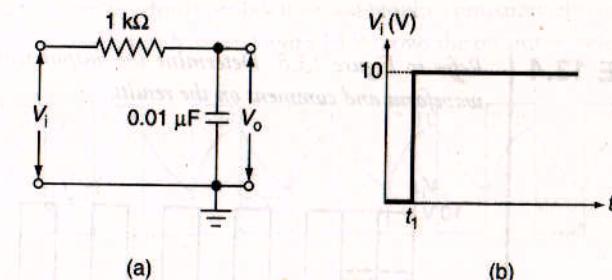


Figure 13.6 | Example 13.2.

Solution

1. Circuit time constant $= RC = 10^3 \times 0.01 \times 10^{-6} = 10 \mu\text{s}$.
2. The response is governed by the equation
$$V_o = 10(1 - e^{-t/10\mu\text{s}})$$

$$= 10(1 - e^{-10^5 t})$$
3. For $t = 10 \mu\text{s}$, $V_o = 10(1 - e^{-1}) = 0.631 \times 10 = 6.31 \text{ V}$.
4. The output voltage (V_o) is shown in Figure 13.7.
5. The time taken for the output voltage (V_o) to rise from 1 V to 9 V is equal to the rise time (t_r):
$$t_r = 2.2RC = 2.2 \times 10^3 \times 0.01 \times 10^{-6} = 22 \mu\text{s}$$

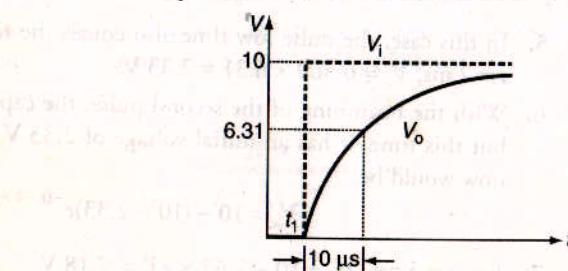


Figure 13.7 | Solution to Example 13.2.

EXAMPLE 13.3

The basic low-pass RC circuit discussed in the previous examples has 3 dB cut-off frequency of 3.5 kHz. If this circuit were fed at the input with a 20 V step, in what time will the output rise to 12.6 V starting from the time of receiving the step?

Solution

1. $3 \text{ dB cut-off} = 3.5 \text{ kHz}$.
 2. $\text{Rise time} = 0.35/f_{uc} = 0.35/3.5 \times 10^3 = 10^{-4} \text{ s}$.
 3. Therefore, $2.2 \text{ RC} = 10^{-4}$, which gives $\text{RC} = 10^{-4}/2.2 = 45.5 \mu\text{s}$.
 4. The output will rise to 12.6 V (which is 63% of the final value of 20 V) in $45.5 \mu\text{s}$ (=time constant).

EXAMPLE 13.4

Refer to Figure 13.8. Determine the output waveform (V_o) for 10 cycles of input waveform and comment on the results.

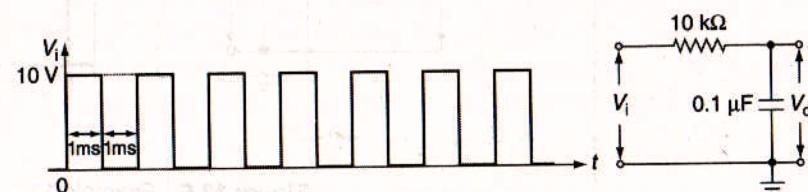


Figure 13.8 | Example 13.4

Solution

- With the leading edge of the first cycle, the capacitor starts charging and charging is governed by the following equation, $V_o = 10(1 - e^{-t/RC})$.
 - The time constant = $RC = 10 \times 10^3 \times 0.1 \times 10^{-6} = 10^{-3}$ s = 1 ms.
 - Since the pulse high time equals the time constant (= 1 ms), the output will rise to 6.31 V at the end of the first pulse.
 - The capacitor starts discharging from the time instant of the trailing edge of the first pulse and the discharge equation is given by

$$V = 6.31(e^{-(t - 10^{-3})/RC})$$

5. In this case, the pulse low time also equals the time constant. Therefore, at $t = 2 \text{ ms}$, $V_o = 0.369 \times 6.31 = 2.33 \text{ V}$.

6. With the beginning of the second pulse, the capacitor starts charging again but this time, it has an initial voltage of 2.33 V and the charging equation

$$V = 10 - (10 - 2.33)e^{-(t - 2 \times 10^{-3})/10^{-1}}$$

8. For $t = 4$ ms, $V_o = 7.18 \times 0.369 = 2.65$ V.

9. Similarly, at $t = 5$ ms,

$$V_o = 10 - (10 - 2.65) \times e^{-1} = 10 - 7.35 \times e^{-1} = 7.3 \text{ V}$$

10. At $t = 6$ ms, $V_o = 7.3 \times 0.369 = 2.69 \text{ V}$.

11. At $t = 7$ ms, $V_o = 10 - (10 - 2.69) \times e^{-1} = 10 - 7.31 \times e^{-1} = 7.31 \text{ V}$.

12. At $t = 8$ ms, $V_o = 7.31 \times 0.369 = 2.70 \text{ V}$.

13. At $t = 9$ ms, $V_o = 10 - (10 - 2.70) \times e^{-1} = 10 - 7.30 \times e^{-1} = 7.31 \text{ V}$.

14. At $t = 10$ ms, $V_o = 7.31 \times 0.369 = 2.70 \text{ V}$.

15. In the subsequent cycles, the output will swing between 2.70 V and 7.31 V. It is clear from the above calculations that the steady state is achieved after four cycles. It can be verified that if the circuit time constant is much smaller than the input waveform time period, the steady state would be arrived at very quickly, most likely in the first cycle itself. If the time constant is much larger than the input waveform period, it would require comparatively larger number of cycles to reach steady state. Figure 13.9 shows the output waveform.

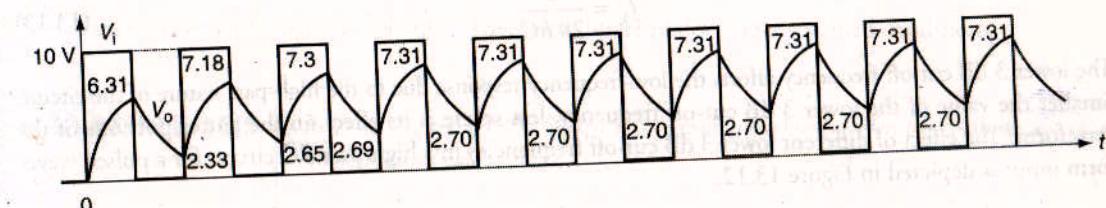


Figure 13.9 | Solution to Example 13.4

13.3 Basic RC High-Pass Circuit

Figure 13.10 shows the basic RC high-pass circuit. The operation of this circuit can be explained on lines similar to the description of RC low-pass circuit. The output voltage (V_o) is given by

$$V_o = \left(\frac{R}{\sqrt{R^2 + X_C^2}} \right) \times V_i \quad (13.12)$$

Since the reactance of a capacitor is inversely proportional to the frequency, it would increase with decrease in frequency. Consequently, the output voltage falls with decrease in frequency of the input waveform thus lending the circuit of Figure 13.10 its high-pass characteristics as shown in Figure 13.11. The frequency where the ratio V_o/V_i falls to 0.707 of its maximum value is known as the lower 3 dB cut-off frequency. Expression for lower 3 dB cut-off frequency can be computed as follows:

At the lower 3 dB cut-off frequency (f_L),

$$\frac{V_o}{V_i} = \frac{R}{\sqrt{R^2 + X_C^2}} = 0.707$$

Therefore at f ,

$$R = X$$

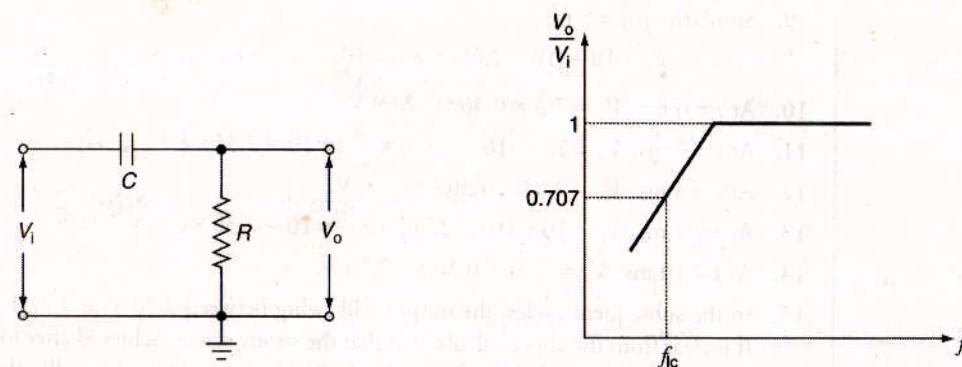


Figure 13.10 | RC high-pass circuit.

Figure 13.11 | Frequency response of high-pass circuit.

The lower 3 dB cut-off frequency is given by

$$f_c = \frac{1}{2\pi RC} \quad (13.13)$$

The lower 3 dB cut-off frequency affects the low-frequency response due to the high-pass nature of the circuit. Smaller the value of the lower 3 dB cut-off frequency, less severe is its effect on the flatter portions of the waveform. The effect of different lower 3 dB cut-off frequencies in a high-pass RC circuit for a pulsed waveform input is depicted in Figure 13.12.

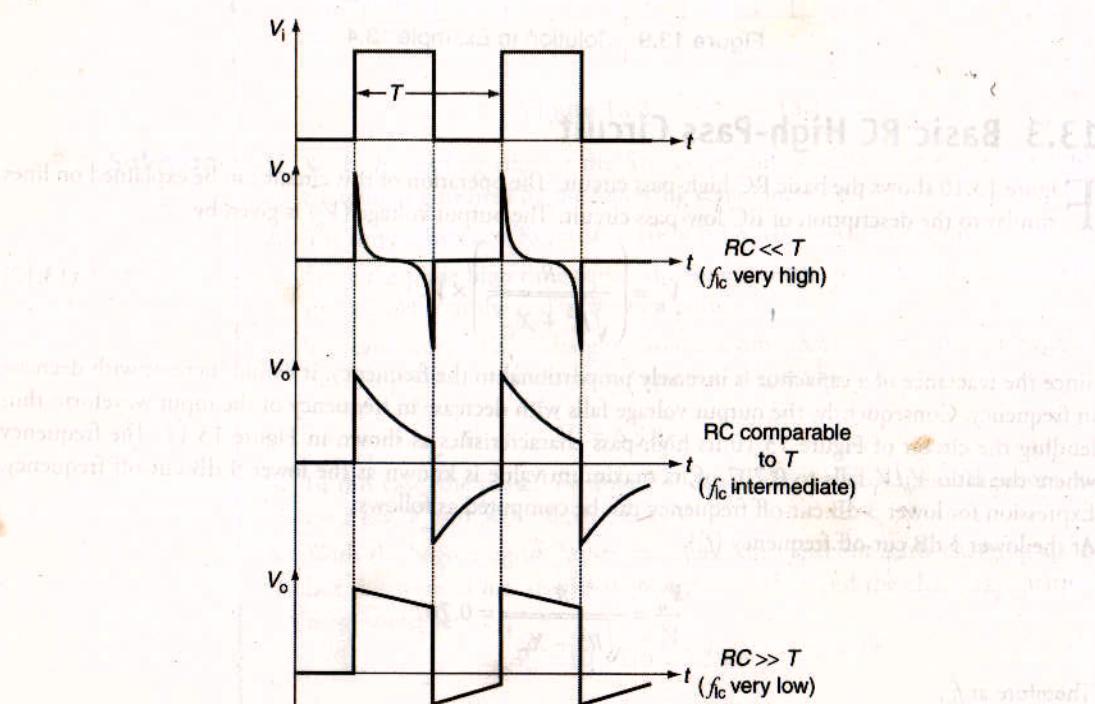


Figure 13.12 | Effect of lower 3 dB cut-off frequency on pulsed waveform input.

13.4 RC High-Pass Circuit as Differentiator

A differentiator circuit is the one in which the output response is proportional to the differential of the input excitation. In other words, the output is proportional to the slope of the input. In the case of the RC circuit of Figure 13.10 where the output is taken across R , if the time constant (RC) is much smaller than the input waveform time period, it is safe to assume that whole of input (V_i) appears across (C) only as the input goes through one complete cycle. The current (I_i) flowing in the circuit is given by

$$I_i = C \frac{dV_i}{dt}$$

The output voltage (V_o) is given by

$$V_o = I_i \times R$$

$$V_o = RC \frac{dV_i}{dt} \propto \frac{dV_i}{dt} \quad (13.14)$$

This explains why RC high-pass circuit behaves as a differentiator under specified conditions.

EXAMPLE 13.5

Refer to Figure 13.13. Sketch the output waveform preferably without doing any mathematical calculations.

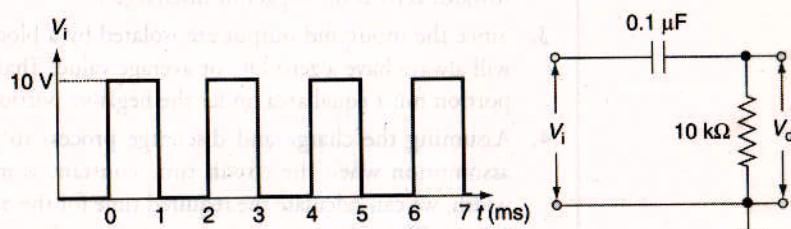


Figure 13.13 | Example 13.5.

Solution

1. The output waveform is shown Figure 13.14. The waveform is self-explanatory. The fact that the circuit time constant is 1 ms and so are the high and low times of the input waveform, all voltage levels can be determined without doing any calculations.

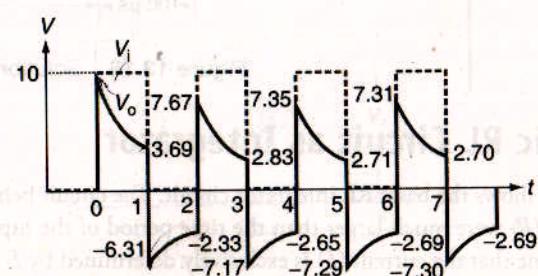


Figure 13.14 | Solution to Example 13.5.

EXAMPLE 13.6

A 100 μs pulse is applied to the RC high-pass circuit of Figure 13.15. Sketch the response waveform. Also calculate the time taken by output pulse to go to near zero after the input pulse goes low.

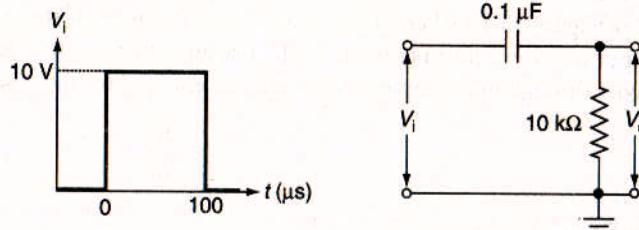


Figure 13.15 | Example 13.6.

Solution

1. The output voltage at the time of termination of input pulse, that is, at $t = 100 \mu\text{s}$ can be calculated from

$$10 - 10(1 - e^{-10^4/RC}) = 10e^{-10^4/10^3} = 10/e^{0.1} = 9 \text{ V}$$
2. As the input pulse goes to zero, the output goes to -1 V as the voltage across capacitor cannot change instantaneously. The output then gradually rises towards zero as the capacitor discharges.
3. Since the input and output are isolated by a blocking capacitor, the output will always have a zero DC or average value. That is, area under the positive portion must equal area under the negative portion.
4. Assuming the charge and discharge process to be linear which is a valid assumption when the circuit time constant is much larger than the pulse width, we can calculate the required time for the output to decay to zero to be 1.9 ms. The response waveform is shown in Figure 13.16.

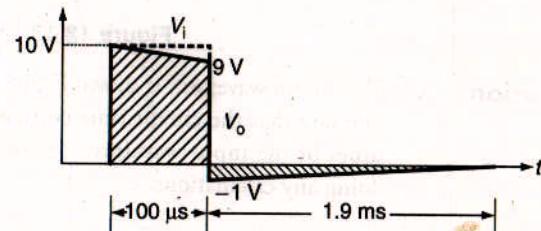


Figure 13.16 | Solution to Example 13.6.

13.5 Basic RL Circuit as Integrator

Figure 13.17 shows the basic RL integrator circuit. The circuit behaves as an integrator circuit, if the time constant (L/R) were much larger than the time period of the input waveform. If it were so, it would be justified to assume that the current (I_i) is exclusively determined by L as the input goes through one complete cycle. That is,

$$I_i = \frac{1}{L} \int V_i dt$$

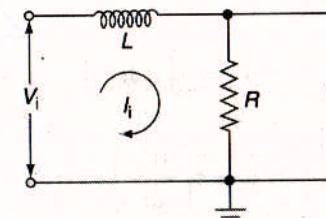


Figure 13.17 | Basic RL integrator.

As the output voltage (V_o) is equal to $V_o = I_i \times R$, therefore

$$V_o = \frac{R}{L} \int V_i dt$$

$$V_o \propto \int V_i dt \quad (13.15)$$

13.6 Basic RL Circuit as Differentiator

Figure 13.18 shows the basic RL differentiator circuit. If the time constant (L/R) were much smaller than the input waveform time period, the current (I) very quickly reaches the steady state and the transient portion takes negligible time. It can thus be assumed that the current (I_i) is exclusively determined by R . That is,

$$I_i = \frac{V_i}{R}$$

As the output voltage (V_o) is equal to

$$V_o = L \frac{dI_i}{dt}$$

Therefore V_o is given by

$$V_o = \frac{L}{R} \frac{dV_i}{dt}$$

$$V_o \propto \frac{dV_i}{dt} \quad (13.16)$$

We can see that the results obtained in the case of RL circuits are analogous to those obtained in the case of RC circuits. In general, for a simple integrator circuit (RL or RC),

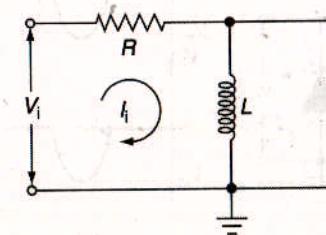


Figure 13.18 | RL differentiator circuit.

$$V_o = \frac{1}{\tau} \int V_i dt \quad (13.17)$$

and for differentiator circuit (RL or RC)

$$V_o = \tau \left(\frac{dV_i}{dt} \right) \quad (13.18)$$

where τ is the time constant which is equal to RC (for RC circuit) or L/R (for RL circuit).

13.7 Diode Clipper Circuits

Diode-based clipper circuits can be used for clipping or removing whole or part of positive or negative portions of bidirectional waveforms. This class of wave-shaping circuits is also called non-linear wave-shaping circuits as one or more than one element has non-linear current-voltage characteristics. Four basic diode-based clipper circuits are shown in Figures 13.19(a)–(d). The non-linear element in the circuits of Figure 13.19 is the diode. In the following paragraphs, we will study the response of each of these circuits to a sinusoidal input. Diodes are assumed to be ideal. That is, the cut-in voltage of the diodes is zero.

1. The input and output waveforms for the clipping circuit of Figure 13.19(a) are shown in Figure 13.20(a). The figure is self-explanatory. The circuit configuration is similar to that of a half-wave rectifier circuit. During the positive and negative half cycles of the input waveform, the diode is respectively forward- and reverse-biased. The positive half cycles therefore appear across the output.

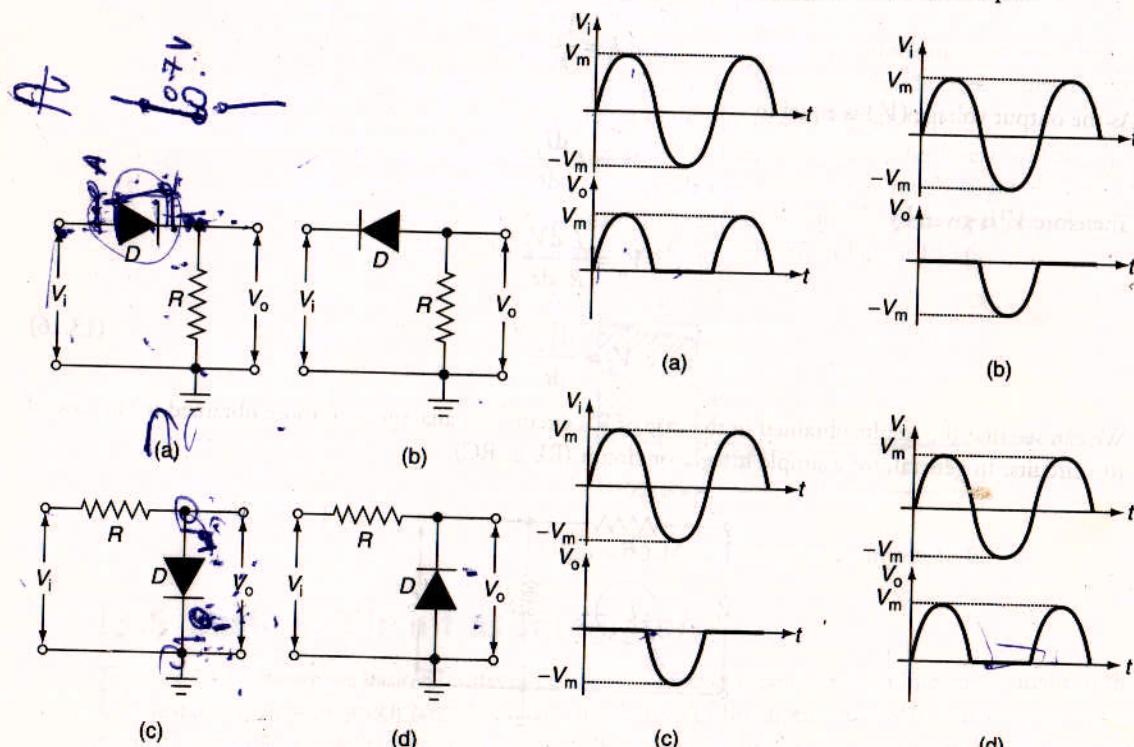


Figure 13.19 | Basic clipper circuits.

Figure 13.20 | Input and output waveforms for the clipper circuits of Figure 13.19.

2. Similarly the output waveform for the circuit of Figure 13.19(b) is shown in Figure 13.20(b). The circuit is again a half-wave rectifier circuit that allows negative half cycles to appear across the output. The diode in this case is forward-biased during negative half cycles of the input waveform.
3. For the clipping circuit of Figure 13.19(c), the diode is forward-biased during positive half cycles and reverse-biased during negative half cycles. The output is therefore clipped to zero during positive half cycles and the negative half cycles are allowed to appear across the output as the diode is then reverse-biased.
4. For the circuit of Figure 13.19(d), the negative half cycles would be clipped to zero.

In case the diodes used in the circuits of Figure 13.19 were non-ideal, the output waveforms would be similar to those shown in Figure 13.20 except that the diode would have a cut-in voltage of 0.7 V for silicon diodes and 0.3 V for germanium diodes instead of zero as assumed in the case of ideal diodes. The waveforms for clipping circuits of Figure 13.19 with silicon diodes are shown in Figure 13.21. The other important issue is that of choice of resistance (R). In the case of non-ideal diodes, the forward-biased resistance of the diode (R_f) is not zero and also the reverse-biased resistance of the diode (R_r) is not infinite. In such a situation, it is desirable that resistance (R) is so chosen that it satisfies the condition $R_f \ll R \ll R_r$. The optimum value of R is given by geometric mean of R_f and R_r . That is

$$R = \sqrt{R_f \times R_r} \quad (13.19)$$

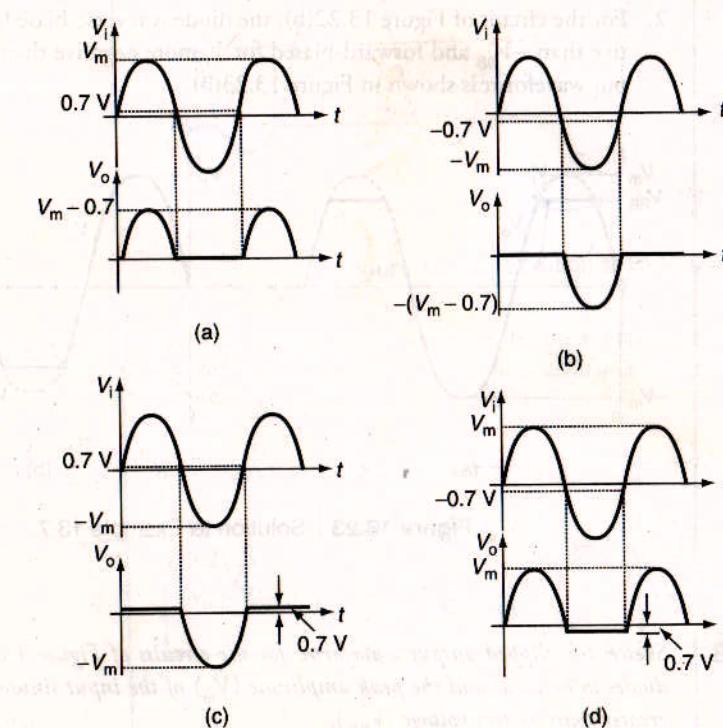


Figure 13.21 | Output waveforms for clipper circuits of Figure 13.19 when the diodes are non-ideal.

EXAMPLE 13.7

Sketch the output waveform for the clipping circuits of Figure 13.22. Assume the diodes to be ideal and the peak amplitude (V_m) of the input sinusoidal signal to be greater than the battery voltage (V_{BB}).

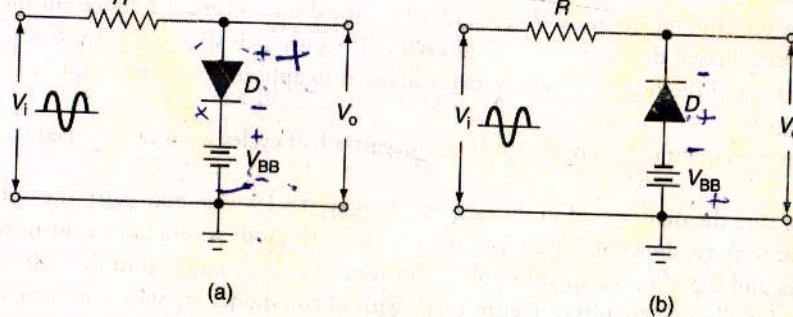


Figure 13.22 | Example 13.7.

Solution

- In the case of the circuit shown in Figure 13.22(a), the diode gets forward-biased when the input exceeds V_{BB} and thus the output remains clamped at V_{BB} as long as input remains greater than V_{BB} . For $V_i < V_{BB}$, the diode is reverse-biased and the output is same as the input. The output waveform is shown in Figure 13.23(a).
- For the circuit of Figure 13.22(b), the diode is reverse-biased for V_i less negative than $-V_{BB}$ and forward-biased for V_i more negative than $-V_{BB}$. The output waveform is shown in Figure 13.23(b).

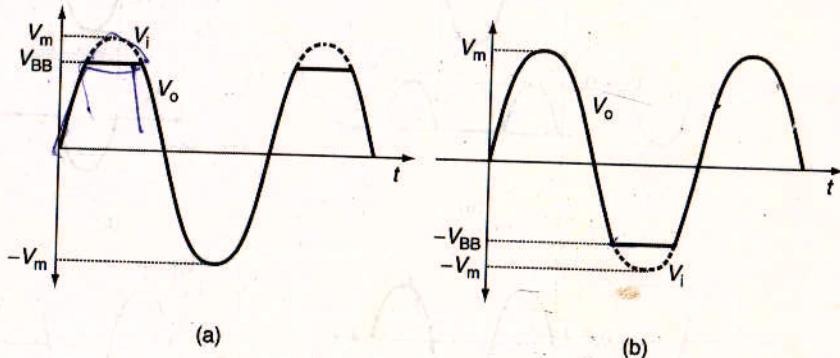


Figure 13.23 | Solution to Example 13.7.

EXAMPLE 13.8

Sketch the clipped output waveforms for the circuits of Figure 13.24. Assume the diodes to be ideal and the peak amplitude (V_m) of the input sinusoidal signal to be greater than battery voltage (V_{BB}).

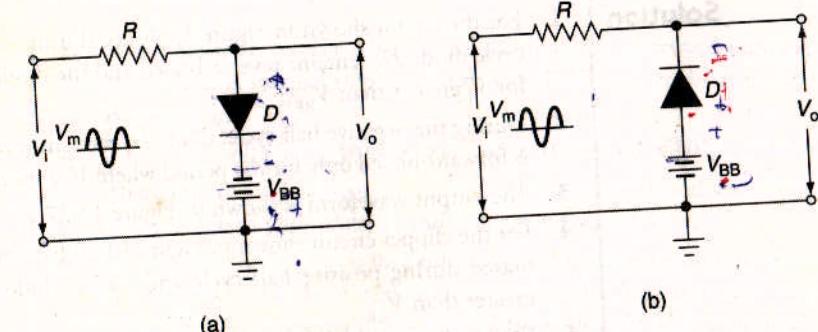


Figure 13.24 | Example 13.8.

Solution

- For the circuit shown in Figure 13.24(a), the diode is forward-biased for all input voltages except for the period when V_i is more negative than the battery voltage ($-V_{BB}$) where it is reverse-biased. Figure 13.25(a) shows the output waveform.
- For the circuit shown in Figure 13.24(b), the diode is forward-biased for V_i less than or equal to battery voltage (V_{BB}) and reverse-biased for V_i greater than V_{BB} . Figure 13.25(b) shows the output waveform.

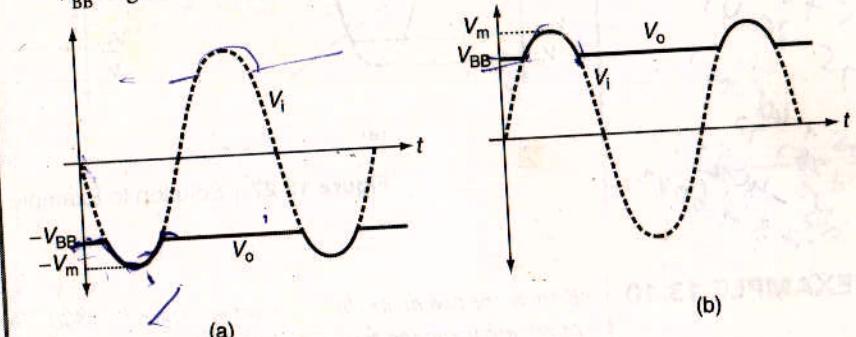


Figure 13.25 | Solution to Example 13.8.

EXAMPLE 13.9

Sketch the clipped output waveforms for the double-diode circuits of Figures 13.26(a) and (b). Assume diodes D_1 and D_2 to be ideal and the forward-biased voltage drops of the Zener diodes to be zero.

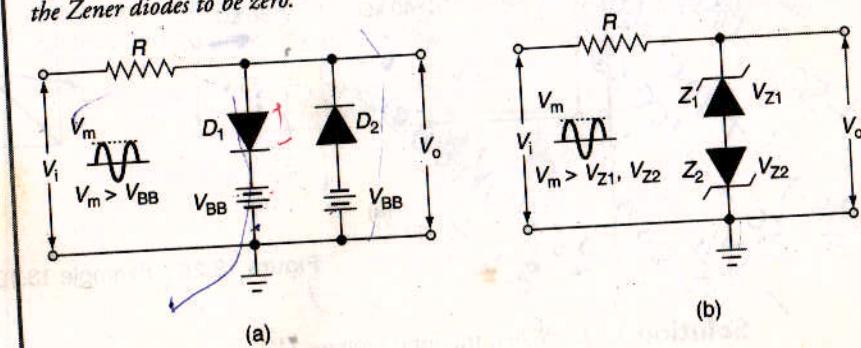


Figure 13.26 | Example 13.9.

Solution

- For the circuit shown in Figure 13.26(a), during the whole of positive half-cycle diode D_2 remains reverse-biased and the diode D_1 gets forward-biased for V_i greater than V_{BB} .
- During the negative half cycle, diode D_1 remains reverse-biased and diode D_2 is forward-biased only for the period where V_i is more negative than $-V_{BB}$.
- The output waveform is shown in Figure 13.27(a).
- For the clipper circuit shown in Figure 13.26(b), Zener diode Z_2 is forward-biased during positive half cycle and Zener diode Z_1 breaks down for V_i greater than V_{Z1} .
- During the negative half cycle, Zener diode Z_1 is forward-biased and Zener diode Z_2 breaks down for V_i more negative than $-V_{Z2}$.
- The output waveform is shown in Figure 13.27(b).

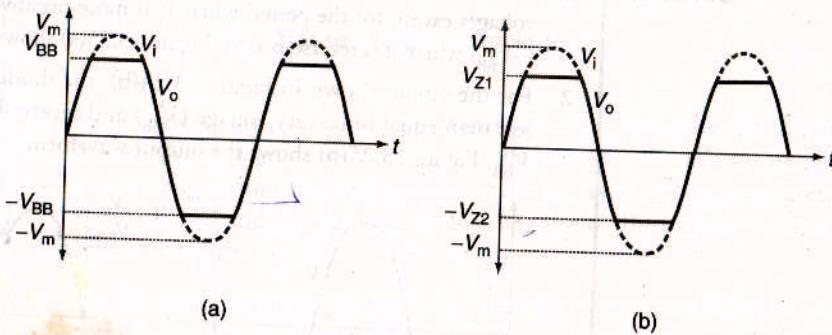


Figure 13.27 | Solution to Example 13.9.

EXAMPLE 13.10

Refer to the two diode clipper circuit of Figure 13.28(a). The input to this circuit is a linear ramp varying from 0 to 100 V as shown in Figure 13.28(b). Plot the output waveform. The diodes can be assumed to be ideal.

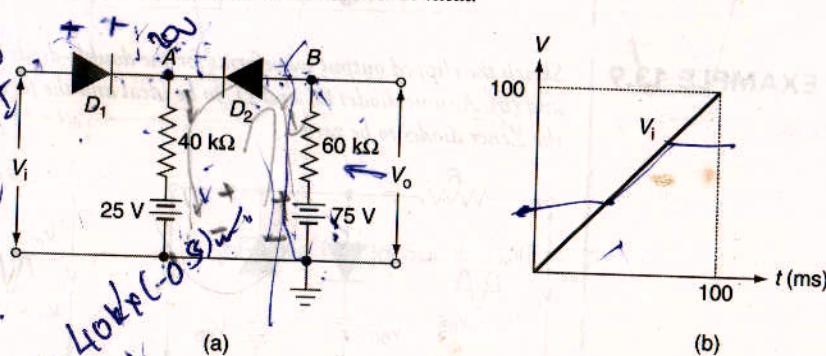


Figure 13.28 | Example 13.10.

Solution

- When the input voltage (V_i) is less than the potential at node A, the diode D_1 is reverse-biased.

- When diode D_1 is reverse-biased and the diode D_2 is forward-biased, potential at node A is equal to potential at node B. The potential at nodes A and B is equal to $[75 - \{(75 - 25)/(60 \times 10^3 + 40 \times 10^3)\} \times 60 \times 10^3] = 45 \text{ V}$
- Therefore, for V_i less than 45 V, diode D_1 is reverse-biased and diode D_2 is forward-biased with nodes A and B at a potential of 45 V.
- As V_i exceeds 45 V, D_1 gets forward-biased and from then onwards, potential at A is same as V_i . Diode D_2 remains forward-biased as long as V_i does not exceed 75 V. Thus, for V_i greater than 45 V and less than 75 V, V_o is same as V_i .
- As V_i exceeds 75 V, D_2 is also reverse-biased. From then onwards, the output is constant at 75 V.
- The input and output waveforms are shown in Figure 13.29.

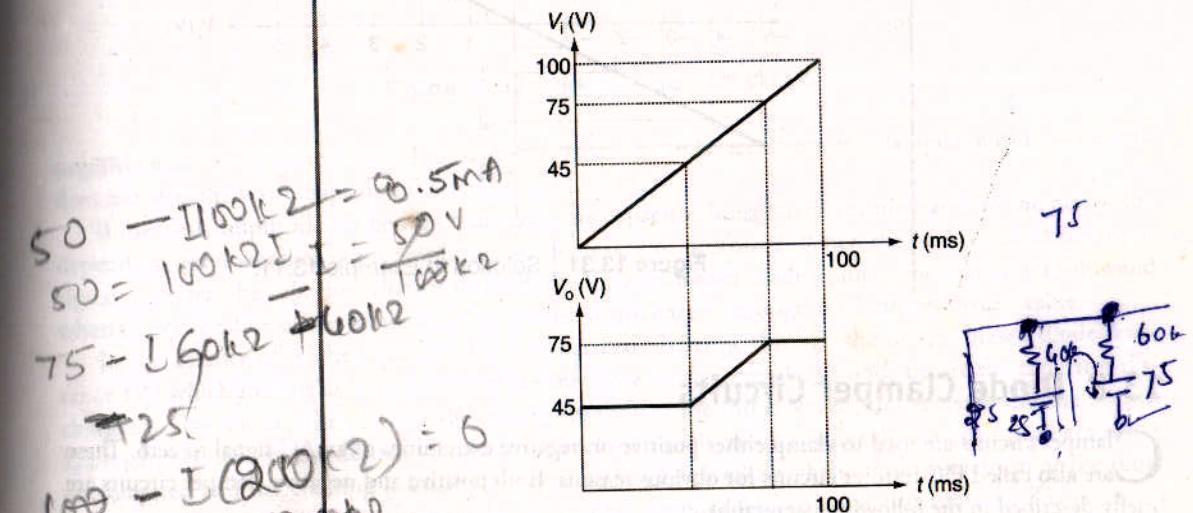


Figure 13.29 | Solution to Example 13.10.

EXAMPLE 13.11

Draw the transfer characteristics (i.e., V_o versus V_i) for the two diode clipper circuit of Figure 13.30. Assume the diodes to be ideal.

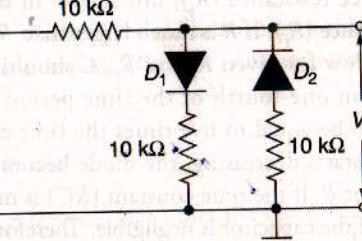


Figure 13.30 | Example 13.11.

Solution

- As V_i increases in the positive direction, D_1 is forward-biased and D_2 is reverse-biased. V_o in this case is always equal to $V_i/2$.
- For negative values of V_i , diode D_2 is forward-biased and diode D_1 is reverse-biased. Again the output is $V_i/2$.
- The transfer characteristics are shown in Figure 13.31.

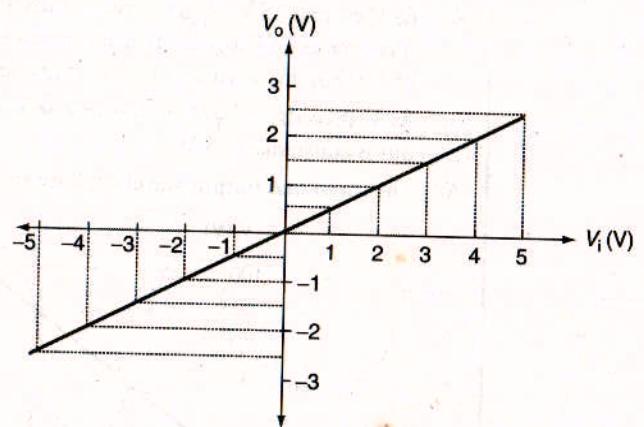


Figure 13.31 | Solution to Example 13.11.

13.8 Diode Clammer Circuits

Clammer circuits are used to clamp either positive or negative extremities of an AC signal to zero. These are also called DC restorer circuits for obvious reasons. Both positive and negative clammer circuits are briefly described in the following paragraphs.

Negative Clammer

Figure 13.32(a) shows the negative clammer circuit, which clamps the positive peaks of the AC signal to zero. Figure 13.32(b) shows the clamped output waveform for a given sinusoidal input. The circuit functions as follows. As the input V_i rises towards the positive peak V_m from zero in the first quarter of the cycle, capacitor (C) charges to V_m through the forward-biased diode. The overall charging resistance is sum of source resistance (R_s), not shown in the figure, and the parallel combination of R and diode's forward resistance (R_f). If R is much larger than R_f then the capacitor C charges with a time constant of $[(R_s + R_f) \times C]$. Now for given R_s and R_f , C should be such that it charges to V_m in a time which in no case is greater than one-fourth of the time period of the input waveform. The total charging time may be considered to be equal to five times the time constant.

When the input starts decreasing, the diode becomes reverse-biased. The capacitor now tends to discharge through resistor R . If the time constant (RC) is much larger than the time period of the input waveform, the discharge of the capacitor is negligible. Therefore, the voltage across the capacitor remains constant at the maximum value of the input signal. The output at any instant of time is then equal to algebraic sum of input voltage and voltage across the capacitor. Thus, all positive peaks (V_m) are clamped to zero and all

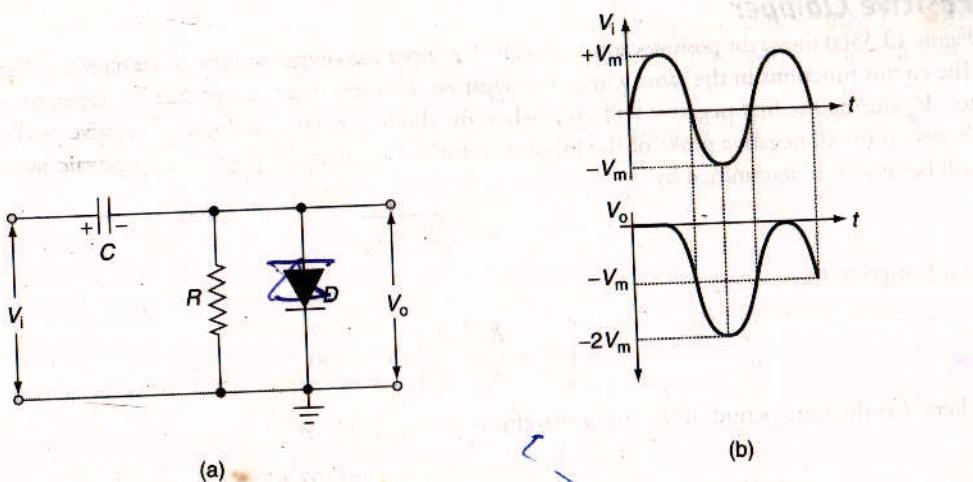


Figure 13.32 | Negative clammer circuit.

negative peaks ($-V_m$) go to $-2V_m$. The clamping circuit as can be seen from the clamped output waveform, does not alter the wave shape, it only changes the DC level.

If the peak amplitude of the input changes, the capacitor must charge or discharge to the new value depending upon whether input amplitude has increased or decreased. When the peak value of the input signal increases, the capacitor charges through the forward-biased diode again to the new larger value and when the peak value of the input signal decreases, it discharges through R to the new lower value.

In the absence of R , the capacitor will be forced to discharge through the reverse-biased diode resistance (R_f) which may be as large as $100 \text{ M}\Omega$. Therefore, it may even be seconds before the capacitor discharges to new lower value, in case the peak amplitude of the input waveform decreases and the output again gets clamped to the desired voltage. As R is chosen to be much smaller than R_f , this problem is not encountered and the clamping is usually restored within a few cycles of the input waveform at the most even after the input undergoes a step change in peak amplitude. The optimum value of R is given by geometric mean of R_f and R_s . That is,

$$R = \sqrt{R_f \times R_s} \quad (13.20)$$

It may be mentioned here that the clamping circuit will function even in the absence of R provided that the peak input amplitude remains constant. In the event of peak input amplitude decreasing, one has to wait for a sufficiently long time depending upon $R_f \times C$ time constant before normal clamping operation is restored.

After having calculated the value of R for a given diode, C should be so chosen that it does not discharge appreciably during the time the diode remains reverse-biased. The time constant when the diode is reverse-biased is given by

$$\left[R_s + \frac{R_f \times R}{R_f + R} \right] \times C \quad (13.21)$$

The time constant of the discharge circuit should at least be 100 times the reverse-biased time period. It is more appropriate to choose C to meet extremely slow discharge requirement rather than fast charging requirement through R_f . R_f is usually so small that C chosen by the discharge criterion almost always satisfies the charge criterion.

Positive Clammer

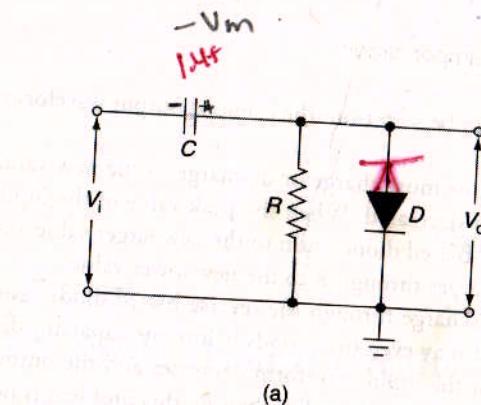
Figure 13.33(a) shows the positive clamper circuit. The input and output waveforms are shown in Figure 13.33(b). The circuit functions in the same way as the negative clamper circuit except that the capacitor would charge to $-V_m$ during the first negative half cycle when the diode gets forward-biased. Negative peaks are clamped to zero as for all negative peaks of the input waveform, the output (V_o) given by algebraic sum of V_i and V_c will be zero. R is determined by

$$R = \sqrt{R_f \times R_s} \quad (13.22)$$

and C is given by

$$\left(R_s + \frac{R_f \times R}{R_f + R} \right) \times C \geq 100 T \quad (13.23)$$

where T is the time period of the input waveform.



(a)

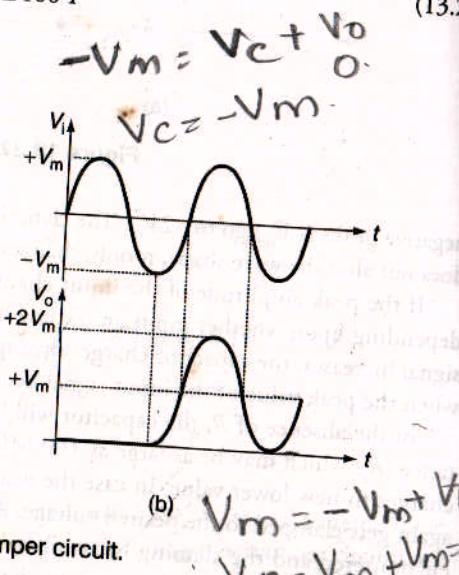


Figure 13.33 | Positive clamper circuit.

EXAMPLE 13.12

For the clamping circuit of Figure 13.34(a) and the input waveform of Figure 13.34(b), plot the output waveform for the first five cycles. Comment on the results obtained. (Assume the diodes to be ideal.)

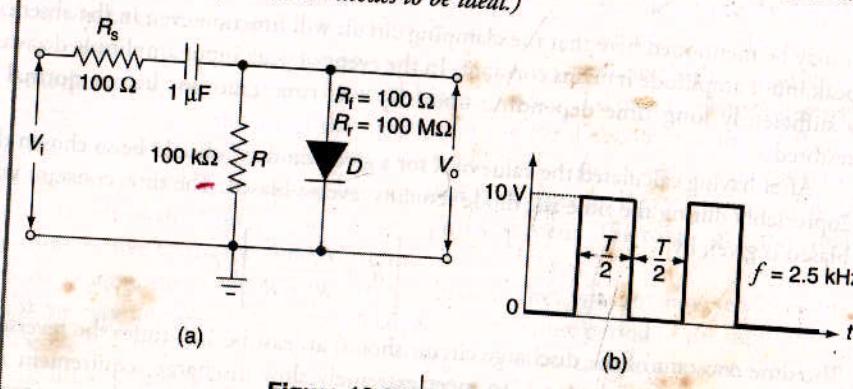


Figure 13.34 | Example 13.12.

Solution

- As the input goes from 0 to +10 V, the diode gets forward-biased. As the voltage across the capacitor cannot change instantaneously, the output voltage (V_o) abruptly rises to only +5 V due to the potential divider arrangement of R_s ($= 100 \Omega$) and R_f ($= 100 \Omega$).
- The capacitor then starts charging towards +10 V with a time constant $(R_f + R_s) \times C$.
- The time constant $= (100 + 100) \times 10^{-6} = 200 \mu\text{s}$.
- The time period of input waveform $= 400 \mu\text{s}$ (for $f = 2.5 \text{ kHz}$).
- Therefore, during the first cycle, when the diode is forward-biased the capacitor would exponentially charge as per the following equation:

$$V_c = 10(1 - e^{-t/(200 \times 10^{-6})})$$

- For $t = 200 \mu\text{s}$, $V_c = 10(1 - e^{-1}) = 6.3 \text{ V}$.
- This gives, $V_o = (10 - 6.3)/2 = 1.85 \text{ V}$.
- When the input drops to zero, the diode gets reverse-biased and the output drops to -6.3 V (= capacitor voltage) as the value of R_f is much larger than R_s .
- For the second half of the first cycle, when the input is zero, the output remains equal to the capacitor voltage of -6.3 V . Here, it is assumed that the capacitor does not discharge through R during this time which is quite valid as the time constant (RC) equal to 100 ms is 500 times the half cycle time of 200 μs .
- The output returns to $+1.85 \text{ V}$ as the input goes to $+10 \text{ V}$ again with the beginning of the second cycle. The capacitor will start charging exponentially. At the end of the HIGH time of the second cycle, the capacitor voltage $V_c = 10 - (10 - 6.3)e^{-1} = 8.64 \text{ V}$.
- This gives, $V_o = (10 - 8.64)/2 = 0.68 \text{ V}$.
- When the input drops to zero, the output drops to -8.64 V . The output waveform progresses in the same fashion for the subsequent cycles.

- As shown in Figure 13.35, the output is nearly clamped in the fifth cycle. From then onwards, the output has the positive extremities of the input waveform clamped to zero.

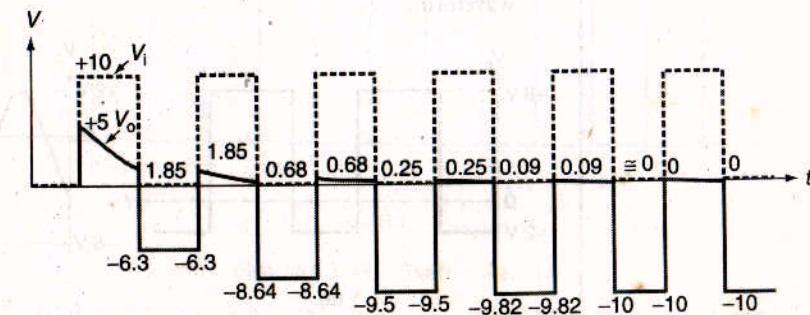


Figure 13.35 | Solution to Example 13.12.

EXAMPLE 13.13

Sketch the steady-state clamped output waveforms for the circuits shown in Figures 13.36(a)–(c). Assume a zero forward-biased voltage drop for diodes.

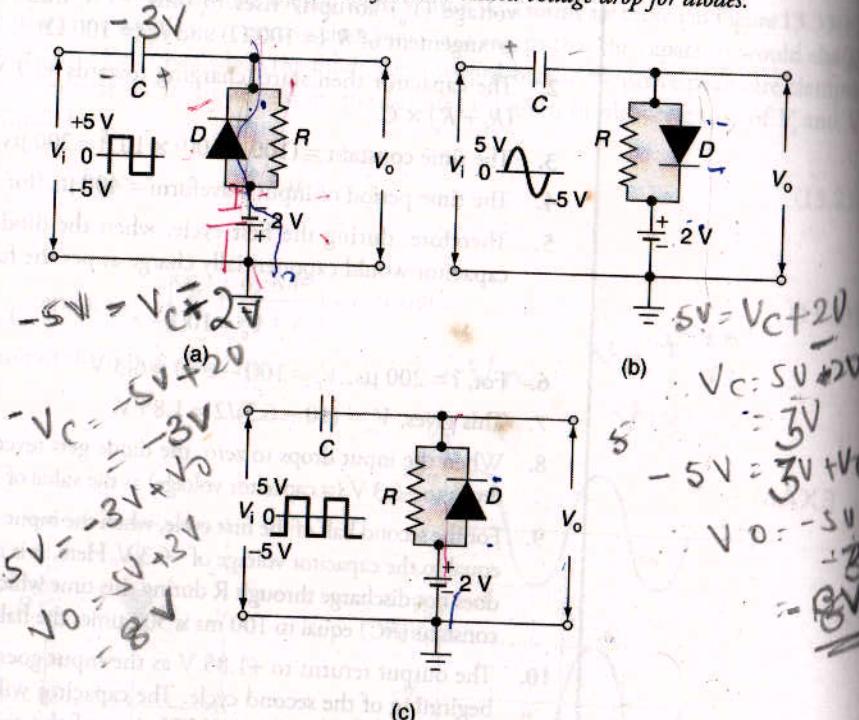


Figure 13.36 | Example 13.13.

Solution

- Refer to Figure 13.36(a): In the absence of the 2 V battery, the negative extremities of the input waveform would be clamped to zero. In the presence of the battery the waveform will be clamped to -2 V. Figure 13.37(a) shows the clamped waveform.
- Refer to Figure 13.36(b): In this case, the positive peaks instead of being clamped to zero are clamped to +2 V. Figure 13.37(b) shows the clamped waveform.

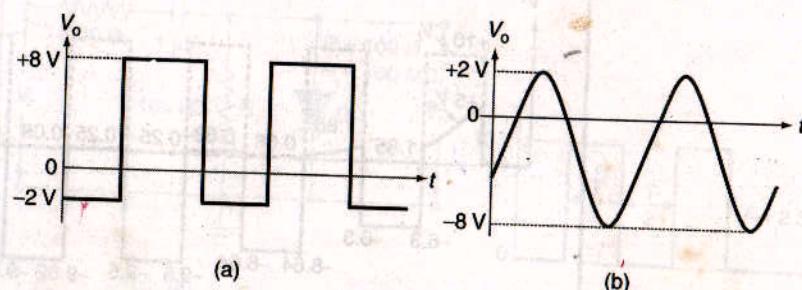


Figure 13.37 | Solution to Example 13.13.

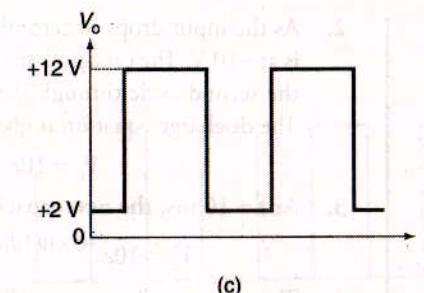


Figure 13.37 | Continued.

- Refer to Figure 13.36(c): The circuit is similar to the one shown in Figure 13.36(a) except that the polarity of battery has been reversed. As a result, the negative peak is clamped to +2 V. Figure 13.37(c) shows the waveform.

EXAMPLE 13.14

Refer to the clamping circuit of Figure 13.38(a). The input waveform to this circuit is shown in Figure 13.38(b) for the first six cycles. Sketch the clamped output waveform for the first six cycles.

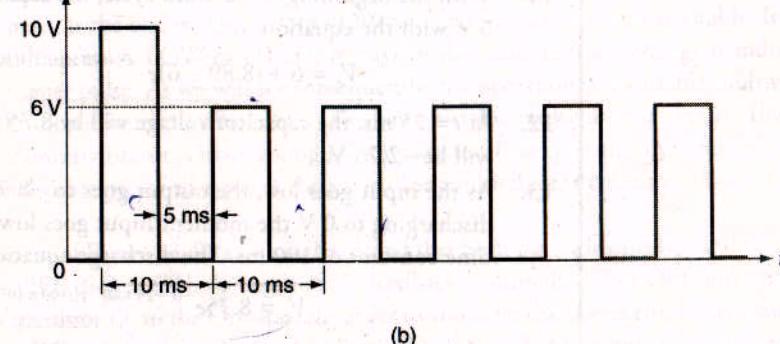
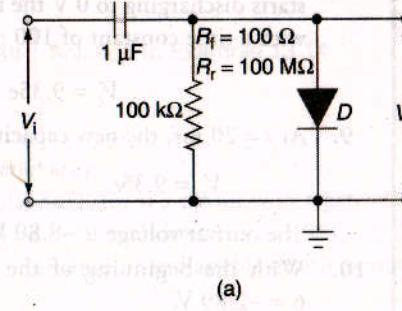


Figure 13.38 | Example 13.14.

Solution

- With $C = 1 \mu\text{F}$ and $R_f = 100 \Omega$, the capacitor (C) would charge to 10 V in about half a millisecond (100 μs being the charging time constant) during the 5 ms high time of the first cycle.