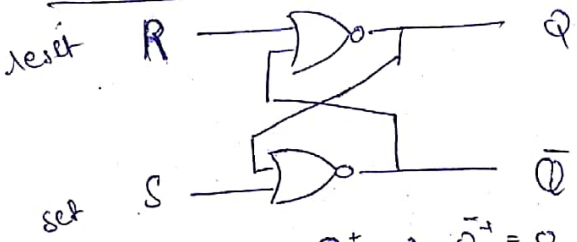
Flip-Flops

Basic storage element is a latch

- NOR S-R latch



S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$ (memory state)
0	1	0	1
1	0	1	0
1	1	forbidden state	

when $S = R = 1$ $Q^+ = 0$ $\bar{Q}^+ = 0$ (Not possible)

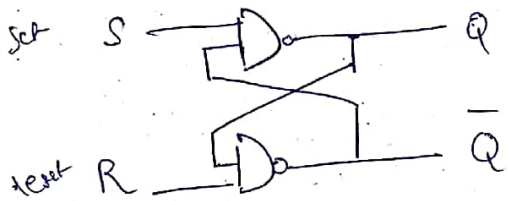
but if $S=0$ $R=0$ applied

wrt Q: $Q^+ = 1$ $\bar{Q}^+ = 0$

wrt $\bar{Q}$: $Q^+ = 0$ $\bar{Q}^+ = 1$

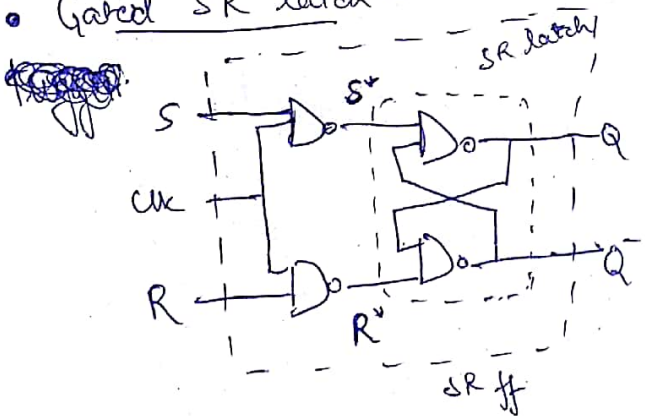
} for same input 2 different o/ps ∴ forbidden state

- NAND S-R latch



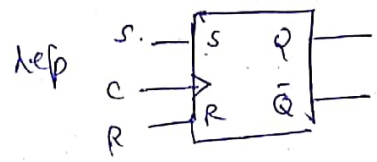
S	R	Q	$\bar{Q}$
0	0	forbidden state	
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$ (memory state)

- Gated SR latch (NAND)



$S^* = \bar{S} + \overline{Clk}$

$R^* = \bar{R} + \overline{Clk}$



Truth table :-

Clk	S	R	Q	$\bar{Q}$	Q_{n+1}
0	x	x	memory state		Q_n
1	0	0	memory state		Q_n
1	0	ϕ	0	1	0
1	ϕ	0	1	0	1
1	1	1	forbidden state		Invalid

Q_{n+1} → next state

Q_n → previous state

characteristic table :-

CLK = 1

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

Q_{n+1}

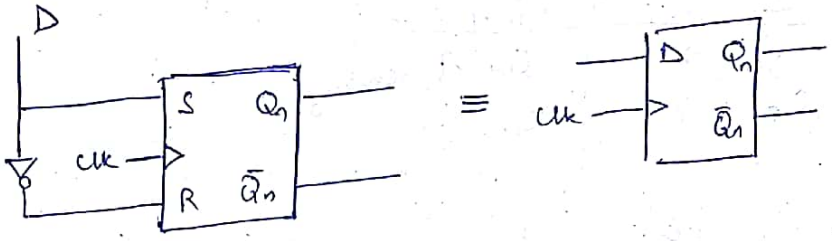
Q \ SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

$Q_{n+1} = S + Q_n \bar{R}$

excitation table :-

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

• D flip flop



truth table

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

Char table

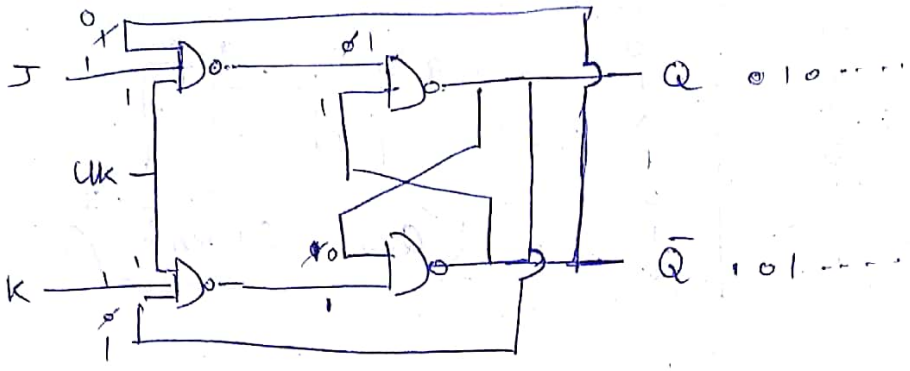
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$Q_{n+1} = D$

Excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

JK flip flop



Clk = 1 $\bar{J}$ = 1 K = 1

assume Q = 0 Q = 0, 1, 0 ...

$\bar{Q}$ = 1 $\bar{Q}$ = 1, 0, 1 ...

racing very fastly

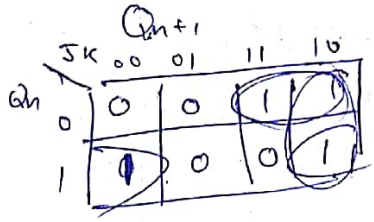
$\bar{Q}_{n+1} = Q_n$

truth table :

Clk	J	K	Q_{n+1}	
0	X	X	Q_n	} memory
1	0	0	Q_n	} memory
1	0	1	0	
1	1	0	1	
1	1	1	$\bar{Q}_n$ (toggle)	

characteristic table :

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



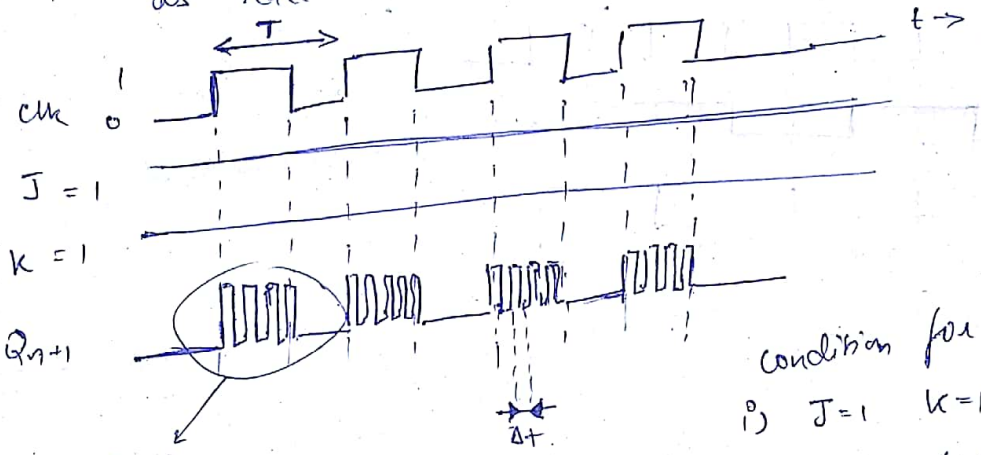
$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

excitation table

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Race around condition

due to the feed-back the value of Q & $\bar{Q}$ keeps on changing / toggling uncontrolled, this condition is known as race around condition



condition for racing

i) J = 1 K = 1

ii) delay of generation & propagation < T/2

iii) $\Delta t << T$

condition to overcome racing

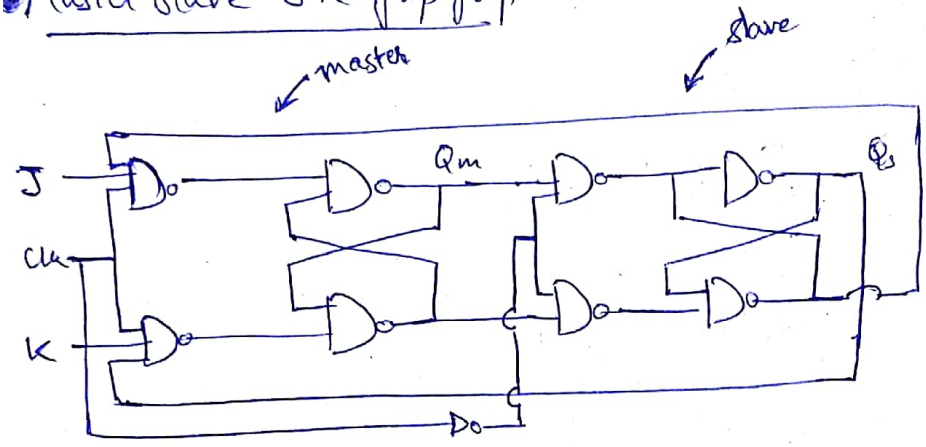
i) T/2 < pro delay of FF

ii) edge trig → { in edge trig, there is not enough time for the circuit to race.

iii) Master - slave

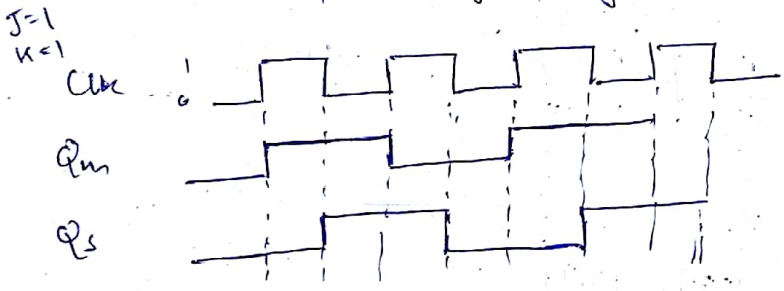
(A) (Same as -ve edge trig)

Master slave JK flip flop

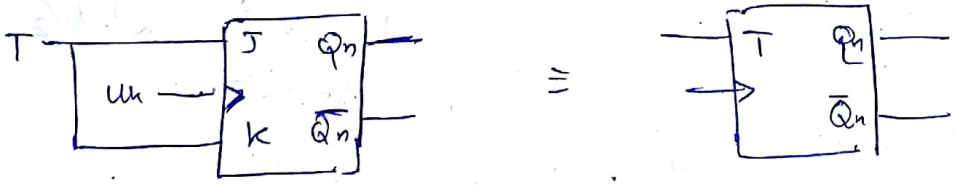


the feedback is given back to master but the clk is low at that time ∴ no change is noticed ∴ eliminating race around condition.

O/p change only 1 in clock cycle



T- flip flop



truth table:

Clk	T	Q_{n+1}	
0	X	Q_n	memory
1	0	Q_n	memory
1	1	$\bar{Q}_n$	toggle

Char. table

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excit. table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_n \ T	0	1
0	0	1
1	1	0

$Q_{n+1} = Q_n \oplus T$

---

flip flop Conversion

Steps :
1. Id avail & required ff
2. Make char table for required ff
3. Make excitation table for avail ff
4. Write boolean exp for avail ff
5. Draw the circuit

eg → JK (avail) to D (required) ff

Step 1

Step 2

Q_n	D	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

Step 3

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 4

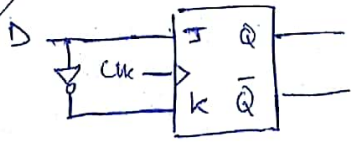
Q_n \ D	J
0	1
X	X

Q_n \ D	K
X	X
1	0

$J = D$

$K = \bar{D}$

Step 5



- T to D ff

req - D ff
avail - T ff

Q_n	D	Q_{n+1}	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_n \ D	$\bar{D}$	D
$\bar{Q}_n$	0	1
Q_n	1	0

$T = Q_n \oplus D$

- SR to JK ff

req - JK
avail - SR

Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	x
0	0	1	0	0	x
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	x	0
1	0	1	0	0	1
1	1	0	1	x	0
1	1	1	0	0	1

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

S

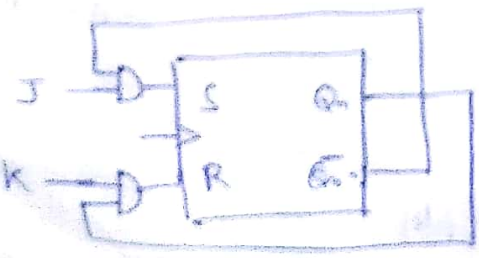
Q_n \ JK	$\bar{J}\bar{K}$	$\bar{J}K$	JK	$J\bar{K}$
$\bar{Q}_n$	0	0	1	1
Q_n	x	0	0	x

R

Q_n \ JK	$\bar{J}\bar{K}$	$\bar{J}K$	JK	$J\bar{K}$
$\bar{Q}_n$	x	x	0	0
Q_n	0	1	1	0

$S = \bar{Q}_n J$

$R = Q_n K$



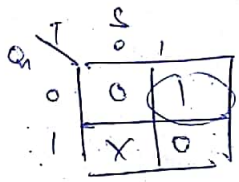
eg SR to T ff

req - T

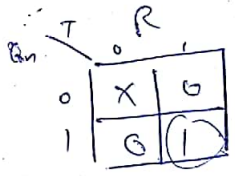
avail - SR

Q_n	T	Q_{n+1}	S	R
0	0	0	0	x
0	1	1	1	0
1	0	1	x	0
1	1	0	0	1

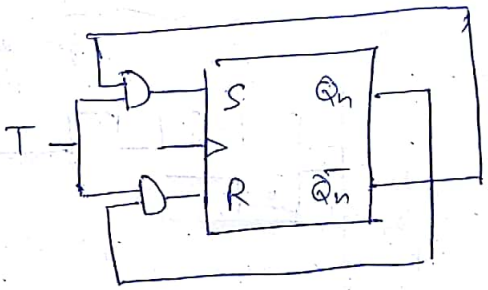
Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0



$S = \bar{Q}_n T$



$R = Q_n T$

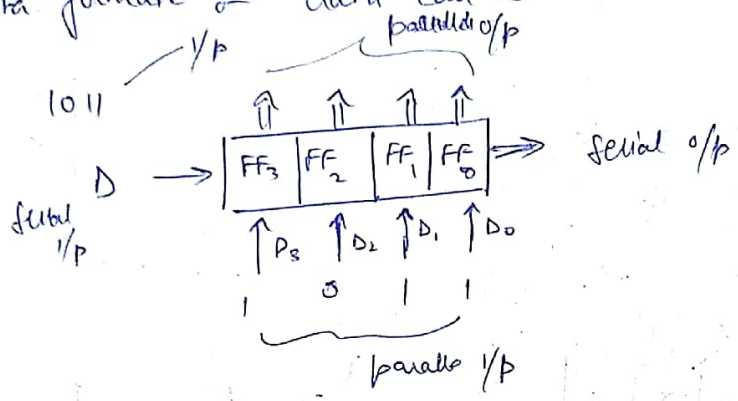


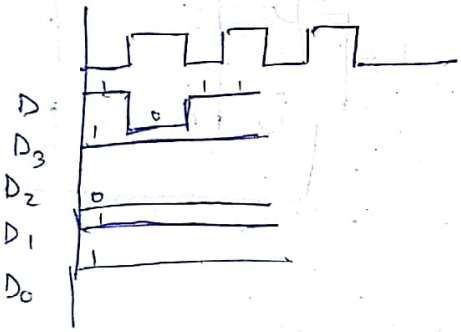
Registers

> group of ff is known as register
> n-bit register will consist of n f.f

data formate :- data can be entered in ⊢ serial form
                                        ⊢ parallel form

eg 1011





Classification of Register :-

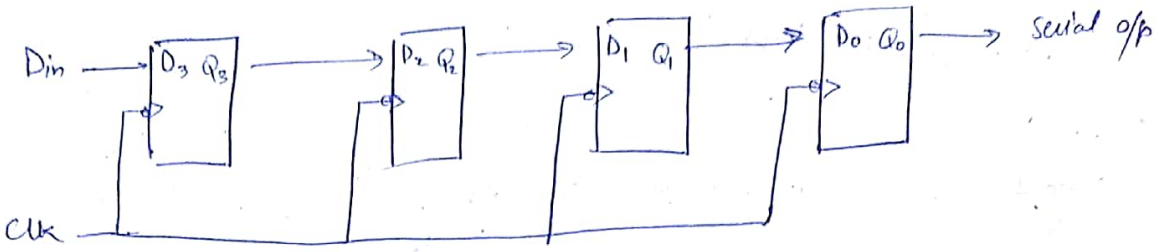
i) depending on I/p & O/p :-

- SISO
- SIPO
- PISO
- PIPO

ii) Applications.

- shift reg
- storage reg.

Shift reg. (SISO)



i/p = 1111

Clk	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1