

* Bipolar Junction Transistor :-

Transistor is a three terminal device such as base, Emitter & Collector, which can be operated in three configurations Common base, Common Emitter & Common collector.

→ The amplification in the transistor is achieved by passing i/p current signal from a region of low resistance to a region of a high resistance. This concept of transfer of resistance has given the name Transfer-Resistor (Transistor).

→ Two types of transistors :-

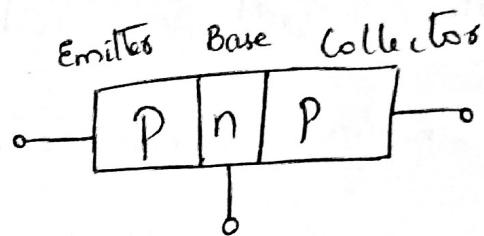
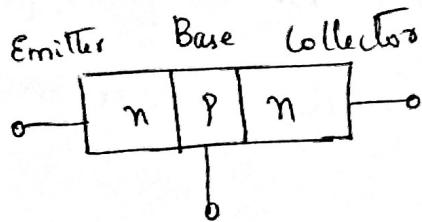
* Unipolar junction transistor (current conduction is only due to 1 type of charge carriers ie, majority carriers)

* Bipolar junction transistor (current conduction because of both the types of charge carriers holes & electrons)

→ There are two types of BJT's

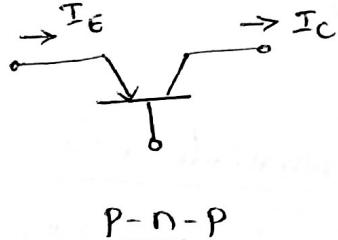
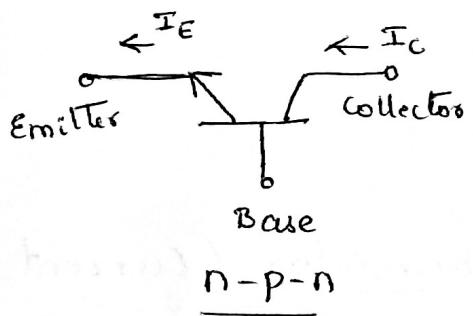
* n-p-n type

* p-n-p type



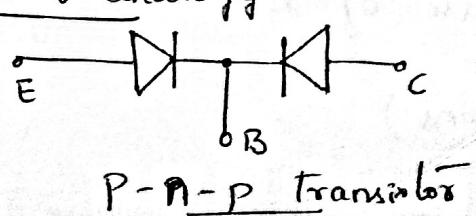
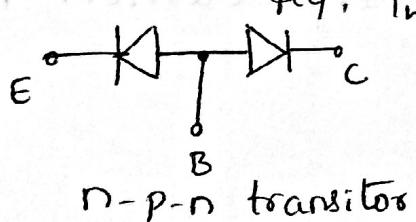
→ The middle region of each transistor type is called base & it is very thin & lightly doped.

Emitter & collector are heavily doped. But doping level in emitter is slightly greater than that of collector.



* Diode Equivalent Transistor :-

The transistor can be considered as two p-n junction diodes connected back to back as shown below:-
fig: Two transistor analogy



• One junction is b/w the emitter & the base which is called as emitter-base junction or simply the emitter junction J_E .

→ The other junction is b/w the base & collector & is called collector-base junction or simply collector junction J_C .

* Unbiased transistor :-

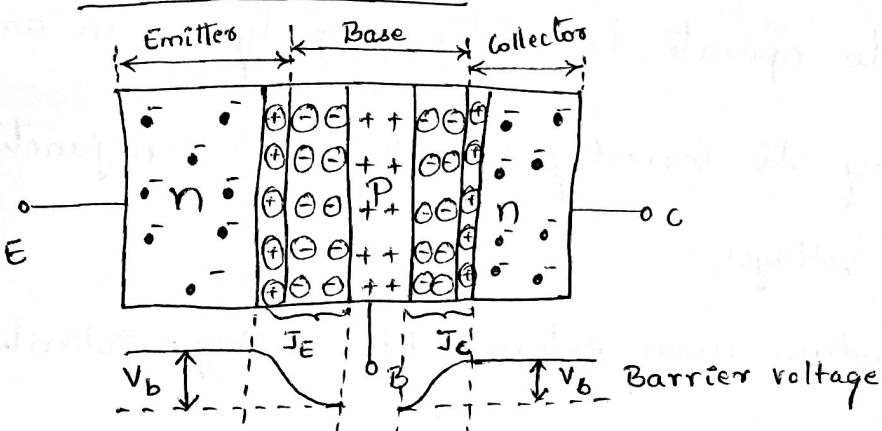


Fig: Unbiased npn transistor
(a)

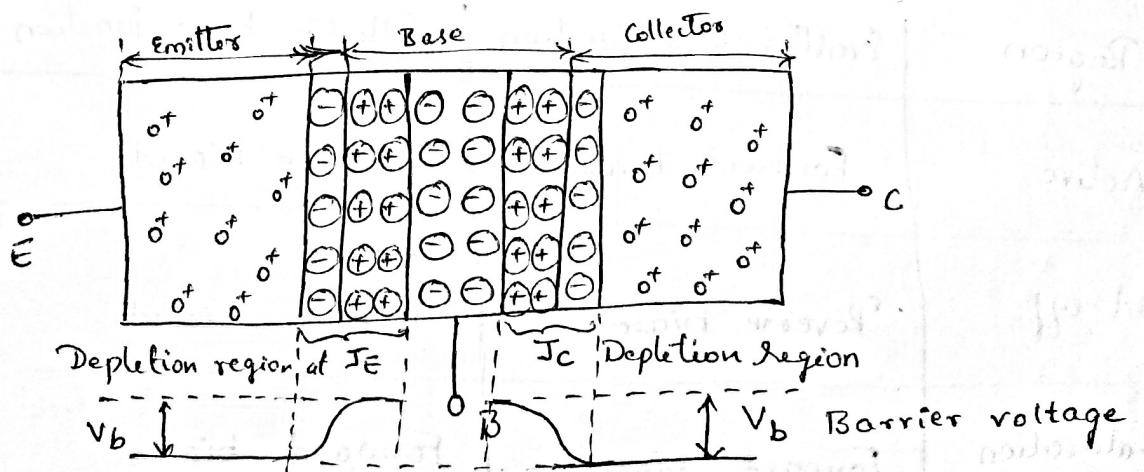


Fig: Unbiased pnp transistor

* Unbiased Transistor means a transistor with no external voltage (biasing) is applied. Therefore there will be no current flowing from any of the transistor terminals.

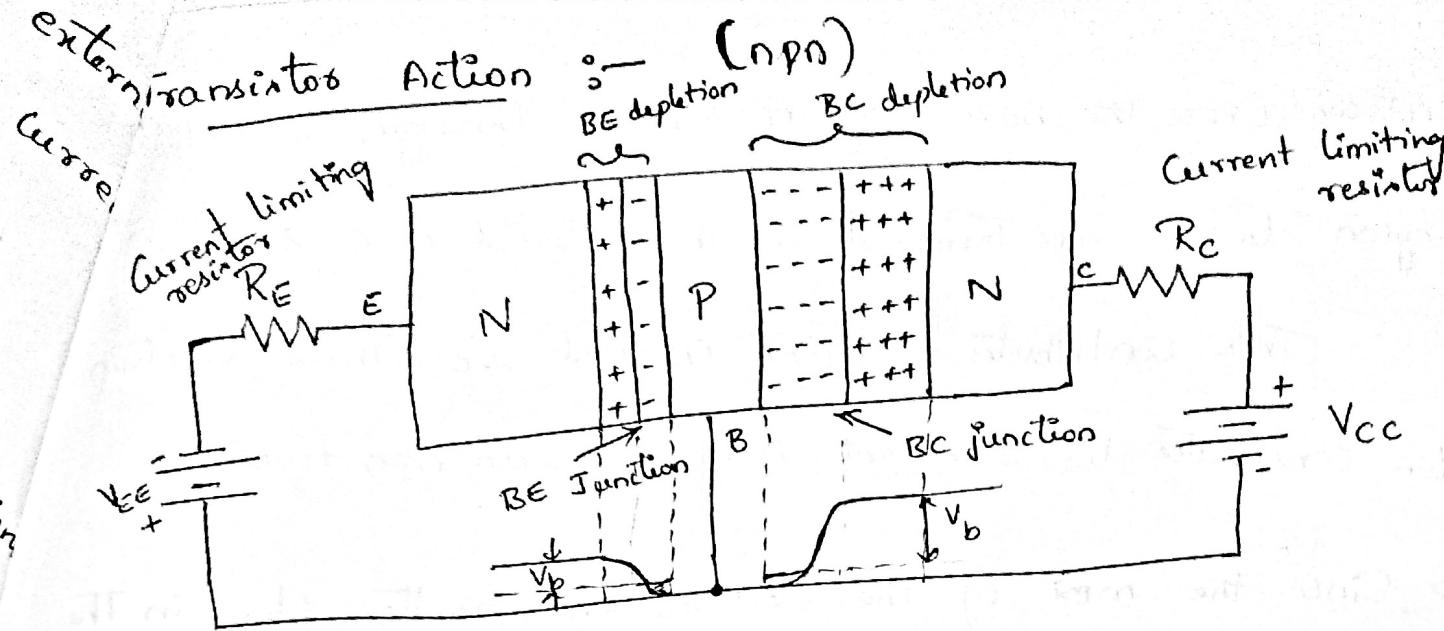
Since transistor is like two p-n junction diodes connected back to back, there are depletion regions at the junction emitter junction & collector junction as shown in the fig (a) & (b)

* Biased transistor :-

→ In order to operate transistor properly as an amplifier it is necessary to correctly bias the two p-n junctions with external voltages.

Depending upon external bias voltage polarities used the transistor works in one of the three regions :-

Region	Emitter base junction	Collector base junction
* Active	Forward biased	Reverse biased
* Cut-off	Reverse biased	Reverse biased
* Saturation	Forward biased	Forward biased



→ The base to emitter junction is fwd biased by the dc source V_{EE} . Thus the depletion region at this junction is reduced.

The collector to base junction is reverse biased increasing the depletion region at collector to base junction as shown above.

→ The fb EB junction causes the electrons in the n-type emitter to flow towards the base. This constitutes the emitter current I_E . As these electrons flow through the p-type base they tend to combine with holes in p-region.

→ Due to light doping, very few of the electrons injected into the base from the emitter recombine with holes to contribute base current I_B & the remaining large no of

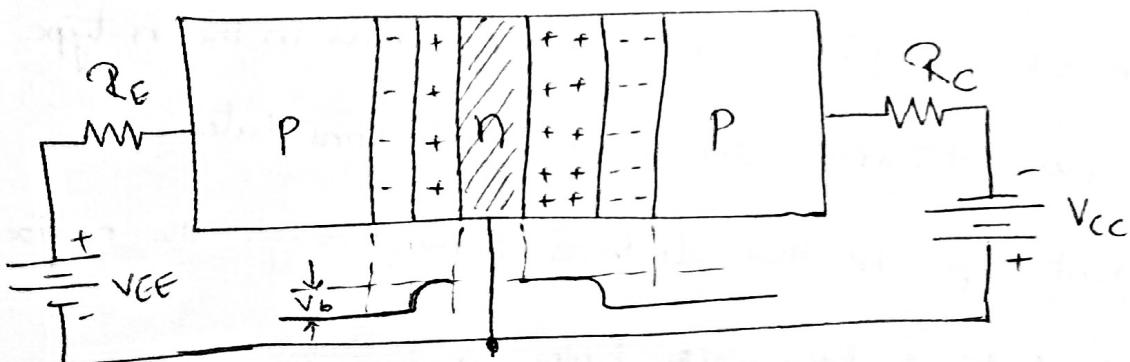
electrons from the base region & move through the collector region to the +ve terminal of the external d.c. source. ^{PA}
 This contributes collector current I_C . Thus electron flow constitutes the dominant current in an n-p-n transistor.

→ Since the most of the electrons from emitter flow in the collector ~~out~~ & very few combine with holes in the base. Thus the collector current is larger than the base current.

The relationship b/w these current is given by,

$$I_E = I_C + I_B$$

* Working principle of p-n-p transistors :-

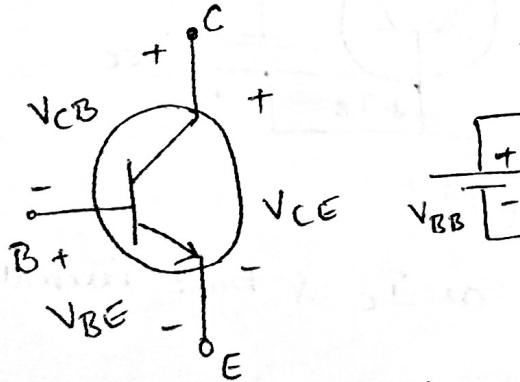


→ The fwd biased EB junction Causes the holes in the p-type emitter to flow towards the base. This constitutes the emitter current I_E .

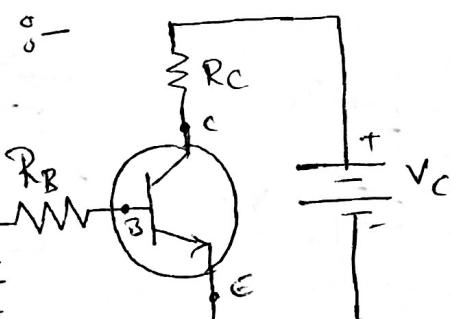
As these holes flow through the n-type base they tend to combine with electrons in the n-region (base). As the base is very thin & lightly doped very few of the holes injected into the base from the emitter recombine with electrons to constitute base current I_B .

→ The remaining large no. of holes cross the depletion region & move through the collector region to the -ve terminal of the external d.c source. This constitutes Collector Current, I_C . Thus the hole flow constitutes the dominant current in an pnp transistor.

* Transistor voltages :-



NPN transistor voltage & polarities

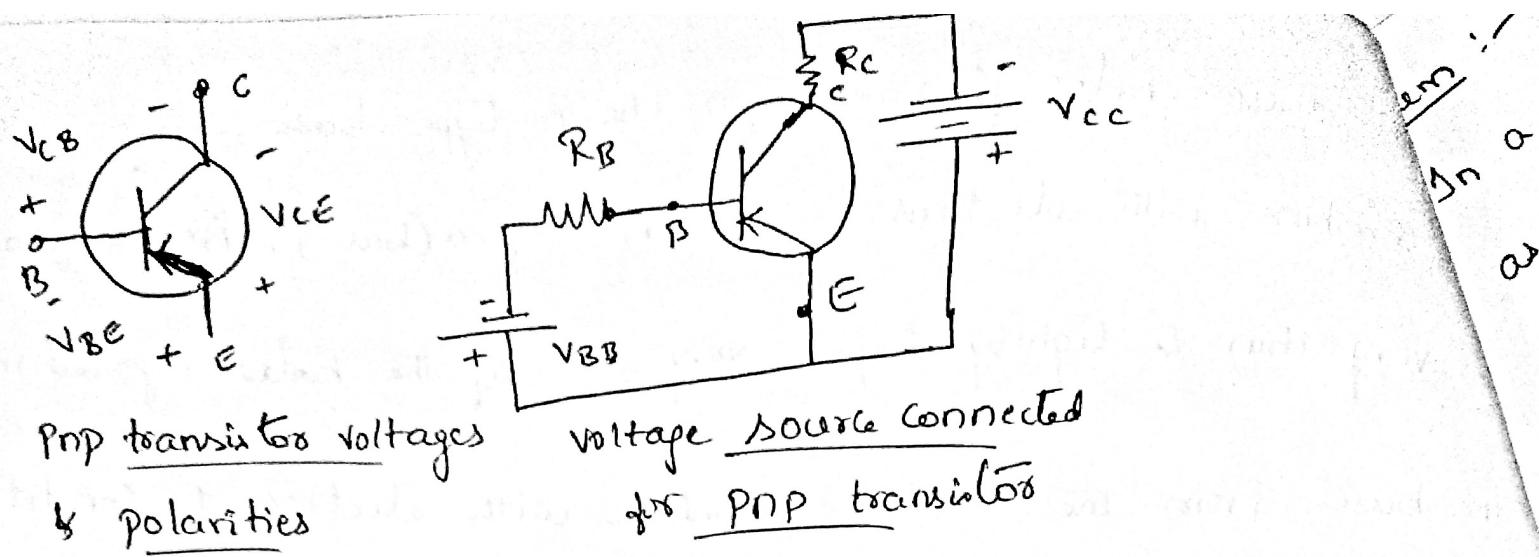


Voltage source connections

* The -ve terminals of both the supply voltages are connected to emitter terminal of transistor.

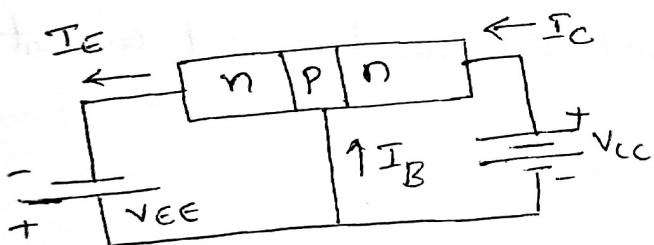
* To make CB junction reverse biased, the supply voltage V_{CC} is always much larger than V_{BB} .

* The voltage sources are connected to the transistor with series resistors. These resistors are called as current limiting resistors.

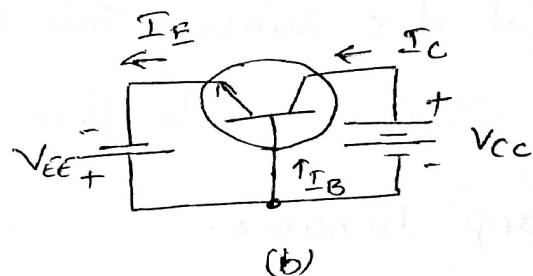


* The source voltage +ve terminals are connected at the emitter terminal with V_{CC} larger than V_{BB} to keep collector base junction reverse biased.

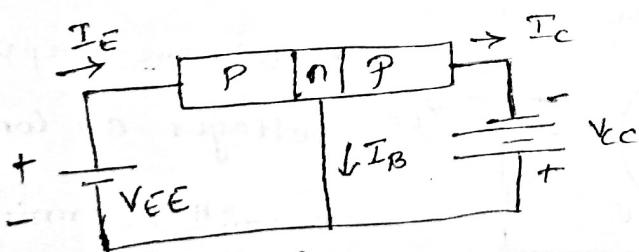
Transistor Currents :-



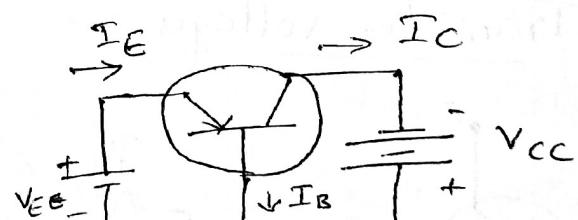
(a)



(b)



(c)



(d)

* The collector current is indicated as I_C & base current as I_B & emitter current as I_E .

* For both npn & pnp transistors,

$$I_E = I_C + I_B$$

blem :-

In a certain transistor, the emitter current is 1.02 times as large as the collector current. If the emitter current is 12 mA, find the base current.

Soln:- $I_E = 12 \text{ mA}$, $I_E = 1.02 I_C$

$$1.02 I_C = 12 \text{ mA}$$

$$I_C = \frac{12 \times 10^{-3}}{1.02} = \underline{\underline{11.765 \text{ mA}}}$$

$$\therefore I_E = I_C + I_B$$

$$I_B = I_E - I_C = 12 \times 10^{-3} - 11.765 \times 10^{-3} \\ = \underline{\underline{235 \text{ nA}}}$$

→ Actually there is one more current component flows inside the transistor called as reverse saturation current (I_{CBO}).

→ This reverse saturation current flows across the reverse biased collector junction when emitter is open circuited.

→ Hence the collector current is constituted by two components namely the current due to injected charge carriers from emitter to collector crossing the base & current due to reverse saturation current.

\therefore we have,

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

$$= \alpha_{dc} (1 + \beta_{dc}) I_B + I_{CBO}$$

→ Almost all of I_E crosses to the collector & only small portion flows out of the base terminal.

→ α_{dc} is the emitter-to-collector current gain

or the ratio of collector current to emitter current

i.e., $\alpha_{dc} = \frac{I_C}{I_E}$ typical value of $\alpha = 0.9$ to 0.99

or $\alpha_{dc} = \frac{I_C - I_{CBO}}{I_E}$

→ β_{dc} is the base-to-collector current gain or the ratio of collector current to base current i.e.,

$\beta_{dc} = \frac{I_C}{I_B}$ typical value of $\beta = 0$ to 300

B+5C

\rightarrow Relationship between $\alpha + \beta$:-

$$\text{W.K.T } \beta = \frac{I_C}{I_B}$$

$$I_E = I_C + I_B \quad \& \quad I_B = I_E - I_C$$

$\therefore \beta = \frac{I_C}{I_E - I_C}$
 Dividing the numerators & denominators of RHS of above

Eqn by I_E , we get

$$\beta = \frac{I_C/I_E}{I_E/I_E - I_C/I_E}$$

$$\therefore \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$\text{W.K.T , } \alpha = \frac{I_C}{I_E}$$

$$\therefore \alpha = \frac{I_C}{I_B + I_C}$$

Dividing the numerators & denominators of RHS of above

Eqn by I_B , we get, $\alpha = \frac{I_C/I_B}{I_B/I_B + I_C/I_B}$

$$\therefore \boxed{\alpha = \frac{\beta}{1+\beta}}$$

Problems :-

① A transistor has $I_B = 100 \mu A$ & $I_C = 2mA$. Find

(i) β (ii) α (iii) I_E (iv) If I_B changes by $+25 \mu A$ & changes by $+0.6mA$. Find the new value of β .

Soln:- Given $I_B = 100 \mu A$ & $I_C = 2mA$

$$(i) \beta = \frac{I_C}{I_B} = \frac{2m}{100 \mu} = \underline{\underline{20}}$$

$$(ii) \alpha = \frac{\beta}{1+\beta} = \frac{20}{1+20} = \underline{\underline{0.952}}$$

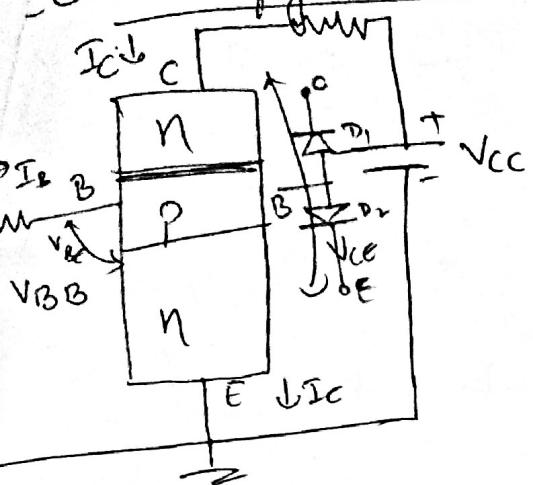
$$(iii) I_E = I_B + I_C = 100 \mu + 2m \\ = \underline{\underline{2.1mA}}$$

$$(iv) \text{ New } I_B = 100 \mu + 25 \mu \\ = \underline{\underline{125 \mu A}}$$

$$I_C = 2m + 0.6m \\ = \underline{\underline{2.6mA}}$$

$$\therefore \text{ New } \beta = \frac{I_C}{I_B} = \frac{2.6m}{125 \mu} = \underline{\underline{20.8}}$$

E Configuration :- i/p char



* The ckt arrangement is as shown in the fig.

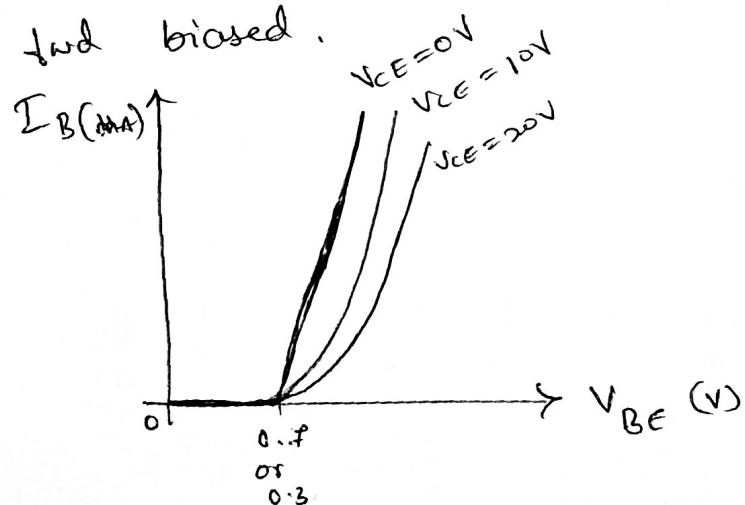
* V_{BB} & V_{CC} are biasing potential.

→ I_B & V_{BE} are i/p Current & voltage respectively

& I_C & V_{CE} are o/p current & voltage respectively.

* The i/p char is plotted for I_B vs. V_{BE} for different values of V_{CE} .

* The i/p char is same as diode fwd char $\therefore D_2$ is fwd biased.



$$W_{eff} = \frac{W_B - W_A}{const}$$

But when reverse voltage V_{CE} is increased, the base will be at lower potential w.r.t V_{CB} \therefore of this width of base depletion layer ~~that~~ generating more to base (lightly doped)
 N.E. + $V_{CE} = V_{CB} + V_{BE}$

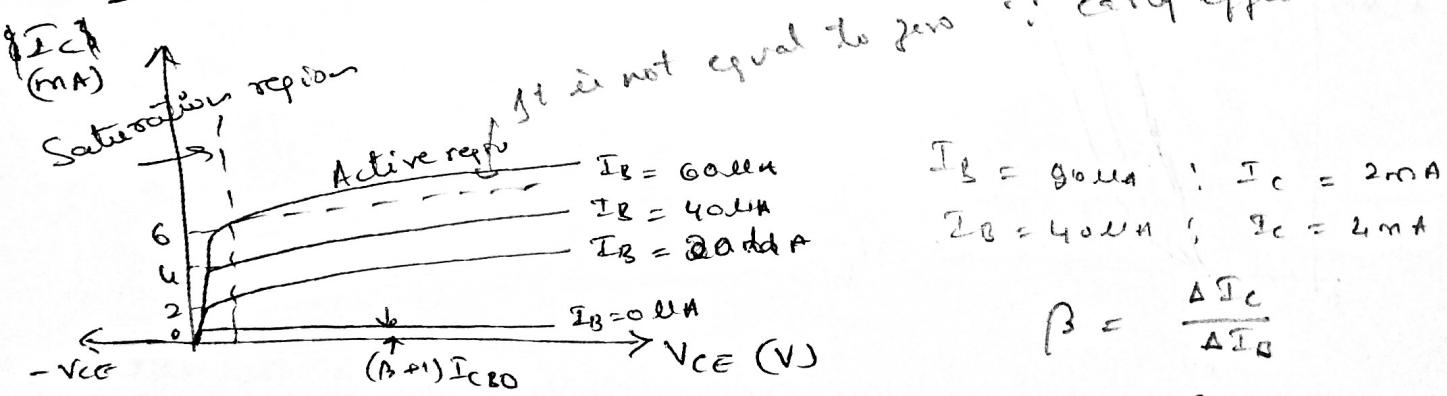
* $\therefore \uparrow V_{CE}, V_{CB} \uparrow \& V_{BE} \text{ Const}$

* ∵ the width of the depletion region @ emitter-base junction is very small whereas width of the depletion region at the collector-base is very large.

As a result, the width of base region ↓ which in turn reduces the i_p Current (I_B). ∵ of this for const values of V_{CE} , the curve shifts to the right side. This effect is called as "early effect".

→ Op chara :-

It is graphical representation of I_C v/s V_{CE} for diff values of I_B



$$\rightarrow I_C = \beta I_B + (B+1) I_{CBO}$$

when $I_B = 0$

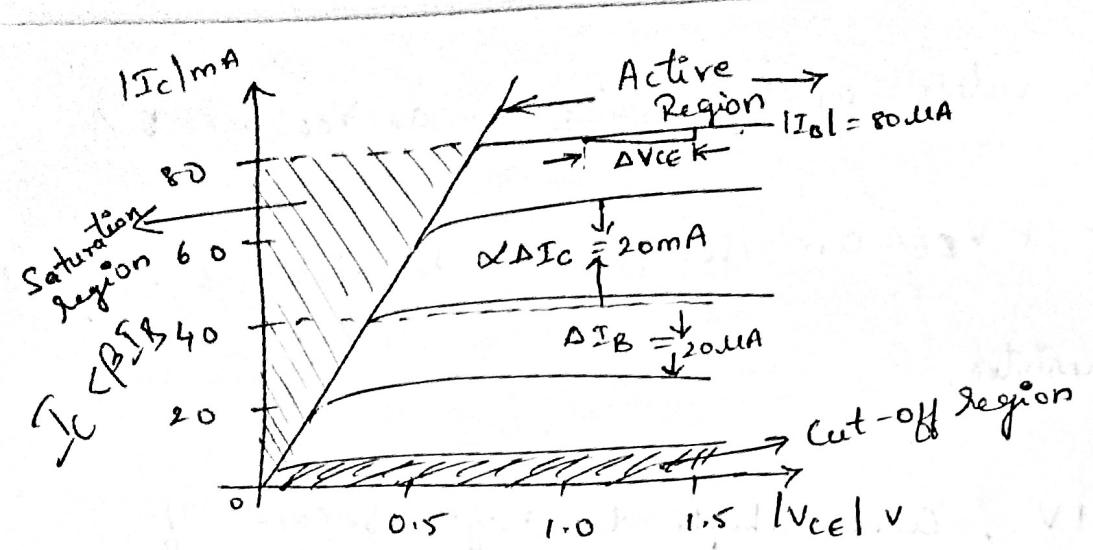
$$I_C = (B+1) I_{CBO}$$

When the base current $I_B = 0\text{mA}$, the transistor operates in the cut-off region.

- i) For a fixed value of V_{BE} , $I_B \downarrow$ as V_{CE} increases.
- ii) voltages V_{BE} & V_{CE} are the same for npn transistor & they are reverse for pnp transistor.
- iii) For $V_{BE} > 1V$, curve shifts to right because of early effect.

Procedure for plotting O/P characteristics

- ① Adjust the V_{BE} to set I_B at fixed value say 20mA.
- ② ↑ V_{CE} in steps of 0.5V & measure I_C , make sure that the base current remains constant at fixed value.
- ③ Continue ↑ V_{CE} till we get sufficient readings to plot a smooth curve.
- ④ Adjust I_B to new value say 30mA & repeat the steps ② & ③
- ⑤ Repeat ④ for more values of I_B .
- ⑥ Plot the graph of I_C versus V_{CE} for different values of I_B .



* This chara shows the relation b/w the collector current (I_c) & collector-emitter voltage (V_{CE}) for various fixed values of I_B . This char is often called as Collector chara.

* The value of β_{dc} of the transistor can be found at any point on the chara by taking the ratio of I_c to I_B at that point i.e., $\beta_{dc} = \frac{I_c}{I_B}$.

* From the O/p chara, we can see that change in ΔV_{CE} causes the little change in ΔI_c for constant base current I_B . Thus the o/p dynamic resistance is high in CE configuration.

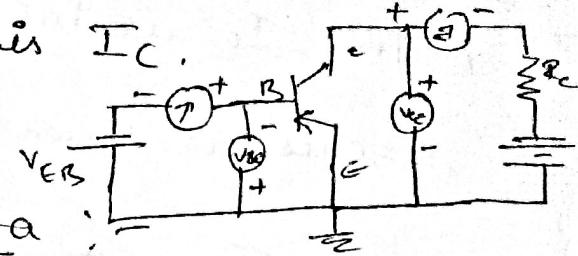
$$\therefore r_o = \frac{\Delta V_{CE}}{\Delta I_c} / I_B = \text{Constant}$$

or $\Delta I_B = 0$

$C \rightarrow R_B$

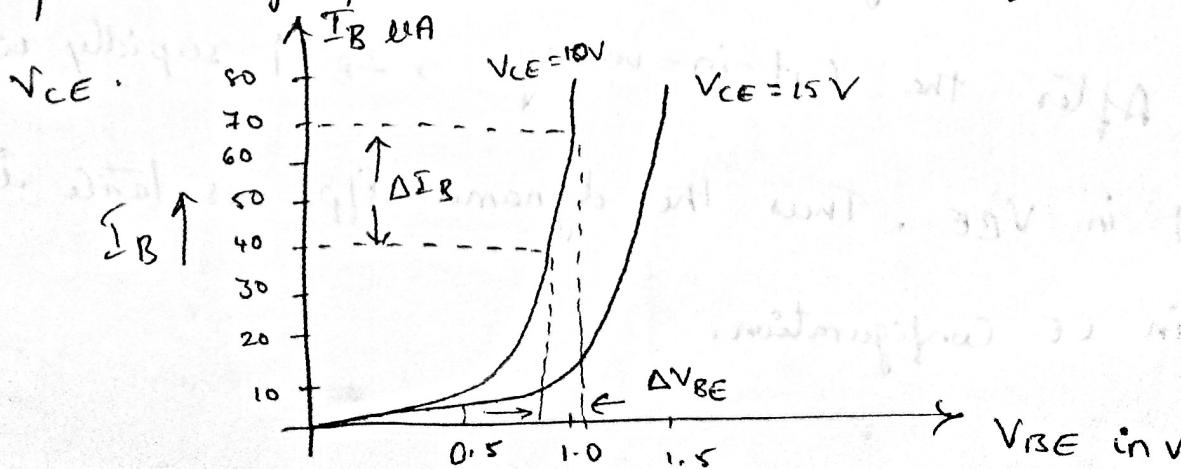
The i/p v_{tg} in the CE configuration is the base-emitter voltage (V_{BE}) & the o/p v_{tg} is the collector-emitter voltage (V_{CE})

& the i/p current is I_B & o/p current is I_C .



* Procedure for plotting i/p chara:

1. Adjust the collector supply voltage V_{CC} to set V_{CE} at a fixed value say 10V.
2. ↑ I_B in steps of 5mA & measure V_{BE} make sure that V_{CE} remains constant at fixed value.
3. Continue ↑ I_B till we get sufficient readings to plot a smooth curve.
4. Adjust V_{CE} to new value say 15V & repeat the steps (2) & (3)
5. plot the graph I_B versus V_{BE} for different values of V_{CE} .



- * It is the curve b/w an i/p voltage V_{BE} & i/p current I_B at constant collector-emitter voltage V_{CE} .
- * The I_B is taken along y-axis & V_{BE} is taken along x-axis as shown above graph.

From the chara it is observed that :-

- The i/p resistance is the ratio of change in base emitter v/tg (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage V_{CE} .

It is given by,

$$r_{in} = \left| \frac{\Delta V_{BE}}{\Delta I_B} \right| \quad |V_{CE} \text{ constant}|$$

(600Ω to 4kΩ)

- As the i/p to a transistor in the CE configuration is b/w the base to emitter junction the CE i/p chara resembles a family of forward biased diode curves.

After the cut-in voltage, $I_B \uparrow$ rapidly with small ↑ in V_{BE} . Thus the dynamic i/p resistance is small in CE Configuration.

① If a transistor $\alpha = 0.99$, $I_B = 100\text{mA}$ determine I_C

soltu :- $\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = \underline{\underline{99}}$

$\therefore I_C = \beta I_B = 99 \times 100 \times 10^{-6} = \underline{\underline{9.9\text{mA}}}$

② Calculate I_C , I_E & β_{dc} for a transistor that has

$\alpha_{dc} = 0.90$ & $I_B = 50\text{mA}$

soltu :- $I_C = \frac{\alpha I_B}{1-\alpha} = \frac{0.90 \times 50\text{mA}}{1-0.90} = \underline{\underline{0.45\text{mA}}}$

$I_C = \alpha I_E$

$I_E = \frac{I_C}{\alpha} = \frac{0.45\text{mA}}{0.90} = \underline{\underline{500\text{mA}}}$

$\beta = \frac{\alpha}{1-\alpha} = \frac{0.90}{1-0.90} = \underline{\underline{9}}$

③ Calculate α & β of a transistor if I_C is 2mA & $I_B = 30\text{mA}$
also determine new I_B to give $I_C = 7\text{mA}$?

soltu :- $I_C = \beta I_B$

$\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3}}{30 \times 10^{-6}} = \underline{\underline{66.66}}$

$$I_E = I_C + I_B = 2m + 30 \times 0.1 = 2.030 \underline{mA}$$

$$I_C = \alpha I_E$$

$$\alpha = \frac{I_C}{I_E} = \frac{2m}{2.03m} = \underline{\underline{0.98}}$$

New value of I_B

$$I_C = \beta I_B$$

$$7mA = 66.66 I_B$$

$$I_B = \frac{7m}{66.66} = \underline{\underline{105 \mu A}}$$

- ④ Consider a transistor that has $I_C = 3mA$ & $I_E = 3.03mA$. Calculate new current levels when the transistor is replaced with a new device that has $\beta = 75$. Assume I_B constant.

Soln: $I_C = \alpha_{dc} I_E$

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{3m}{3.03m} = 0.99$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.99}{1-0.99} = 99$$

$$I_B = \frac{I_C}{\beta} = \frac{3m}{99} = \underline{\underline{30 \mu A}}$$

New value of $\beta = 75$

$$\therefore I_C' = \beta I_B = 75 \times 30 \mu A = \underline{\underline{2.25mA}}$$

$$\alpha' = \frac{\beta}{1+\beta} = \frac{75}{1+75} = \underline{\underline{0.98}}$$

$$\therefore I_E' = \frac{I_C'}{\alpha'} = \frac{2.25 \times 10^{-3}}{0.98} = \underline{\underline{2.24mA}}$$

Given $I_E = 2.5 \text{ mA}$, $\alpha = 0.98$ & $I_{CBO} = 10 \text{ nA}$. Calculate I_B & I_C .

Soln:- $I_C = \alpha I_E + I_{CBO}$

$$= 0.98 \times 2.5 \text{ mA} + 10 \text{ nA}$$

$$= \underline{\underline{2.46 \text{ mA}}}$$

$$I_B = \frac{I_C}{\beta} = \frac{I_C(1-\alpha)}{\alpha} = \frac{2.46 \times 10^{-3} (1-0.98)}{0.98}$$

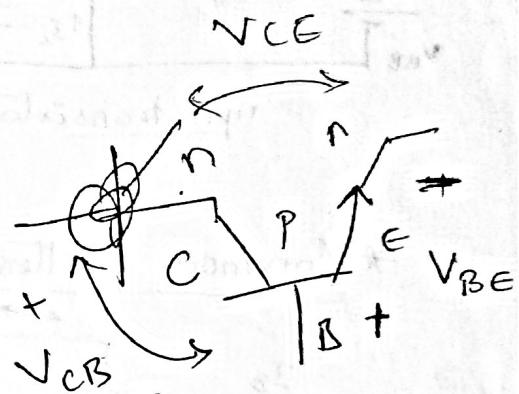
$$= \underline{\underline{50.2 \text{ nA}}}$$

* Transistor Configurations :-

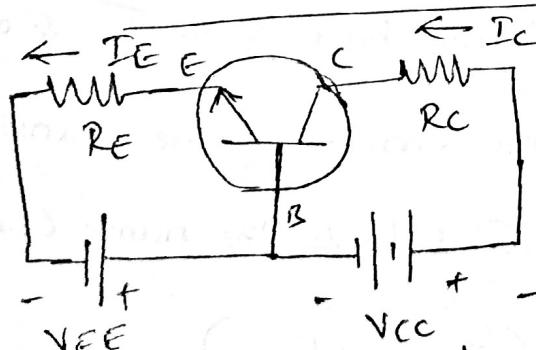
→ Common Base Configuration

→ Common Collector

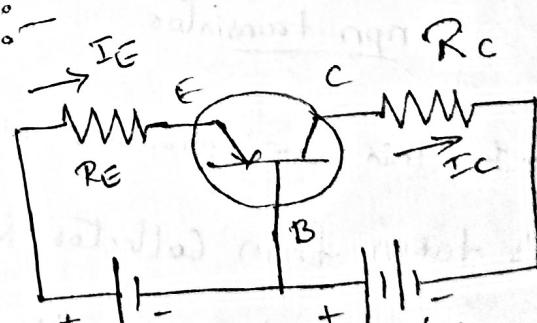
→ Common Emitter



* Common Base Configuration :-



n-p-n transistor

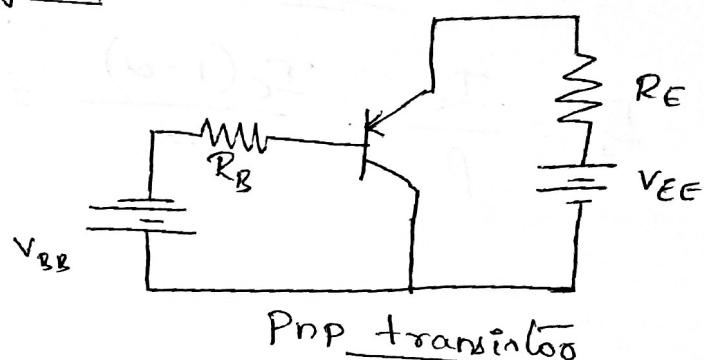
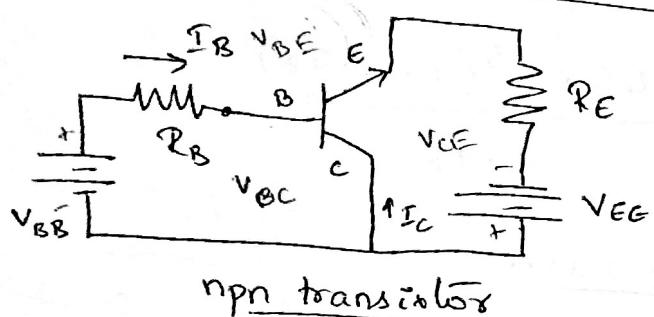


p-n-p transistor

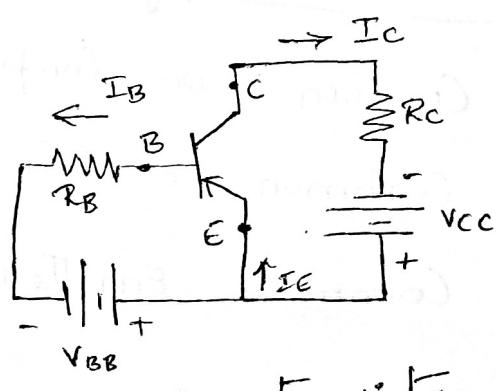
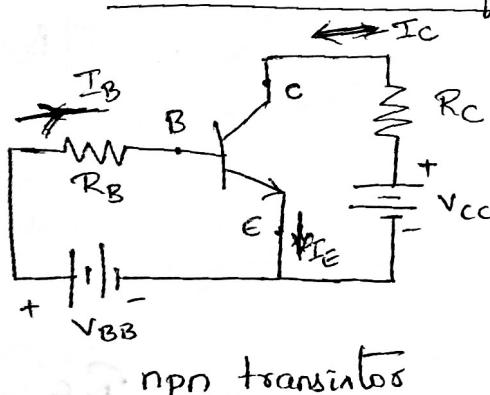
* Configuration i/p is applied b/n emitter & base & o/p taken from the collector & base.

Base of the transistor is common to both i/p & o/p hence named as Common base Configuration.

* Common Collector configuration:-



* Common Emitter Configuration :-



→ In this Configuration i/p is applied b/n base & emitter & o/p is taken from collector & emitter. Here emitter of the transistor is common to both i/p & o/p circuits & hence the name Common emitter Configuration.

$$V_{BE} = (I_B, V_{CE})$$

i/p current } independent
& o/p v/tg } variables
v/tg } dependent
i/p v/tg & o/p v/tg } variables

$$I_C = (V_{CE}, I_B)$$

10 Relation b/w α_{dc} & β_{dc} :-

$$\alpha_{dc} = \frac{I_C}{I_E} \quad \& \quad \beta_{dc} = \frac{I_C}{I_B}$$

w.r.t., $I_E = I_C + I_B \quad \text{--- (1)}$

\therefore by I_C

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{\beta + 1}{\beta}$$

$$\boxed{\alpha = \frac{\beta}{1 + \beta}} \quad \text{--- (2)}$$

$$\alpha(1 + \beta) = \beta$$

$$\alpha + \alpha\beta = \beta$$

$$\therefore \alpha = \beta - \alpha\beta$$

$$\alpha = \beta(1 - \alpha)$$

$$\boxed{\therefore \beta = \frac{\alpha}{1 - \alpha}} \quad \text{--- (3)}$$

$$I_E = I_C + I_B \quad \text{--- ①}$$

$$I_C = \alpha I_E + I_{CBO} \quad \text{--- ②}$$

$$\therefore I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$= \alpha I_C + \alpha I_B + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{I_{CBO}}{1 - \alpha}$$

Let $\frac{\alpha}{1 - \alpha} = \beta$

$$\frac{1}{1 - \alpha} = \beta + 1$$

$$\begin{aligned} \text{RHS} &= \frac{\alpha}{1 - \alpha} + 1 \\ &= \frac{\beta + 1 - \alpha}{1 - \alpha} \end{aligned}$$

$$\therefore I_C = \beta I_B + \left(\frac{1}{1 - \alpha}\right) I_{CBO}$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

$$\alpha = \frac{1}{1 - \alpha}$$

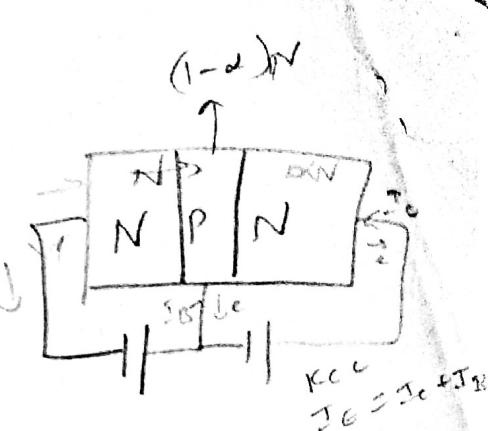
$$\alpha_e = \frac{I_C}{I_E} = \frac{I_C - I_{CBO}}{I_E}$$

$$\beta_e = \frac{I_C}{I_B}$$

$\beta_e = \frac{I_C}{I_B}$

$$\beta_e = \frac{I_C}{I_E}$$

$$\therefore \beta_e = \frac{\beta + 1 - \alpha}{\beta + 1} = \frac{\alpha}{\beta + 1}$$



$$\alpha \rightarrow 2.1 \text{ to } 5.1$$

$$95.1 \text{ to } 98$$

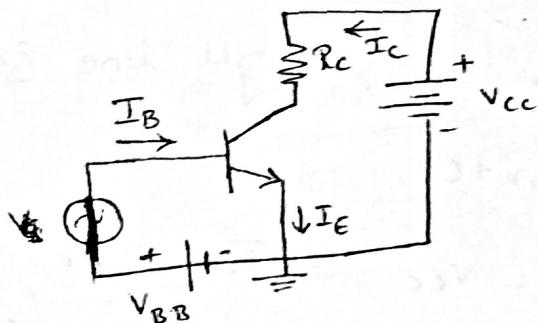
$$0.95 \text{ to } 0.98$$

Unit - 2

DC load line & Bias Point

Since dc biasing is essentially required for proper operation of the transistor, if the transistor is used as an amplifier then the device should be operated in active region, similarly if the device is required to be operated as an electronic switch then it should be operated in saturation & cut-off region.

* Operating & DC load line :-



* Consider the Common emitter ckt as shown in the fig.

* The transistor base emitter junction is forward biased by external dc voltage V_{BB} & collector base junction reverse biased by V_{CC}.

By applying KVL to the OIP ckt:-

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad \text{--- (1)}$$

$$\therefore V_{CC} = I_C R_C + V_{CE} \quad \text{--- (2)}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \quad \text{--- (3)}$$

$$\text{or } I_C = \frac{-V_{CE}}{R_C} + \frac{V_{CC}}{R_C}$$

$$\therefore I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad \text{--- (4)}$$

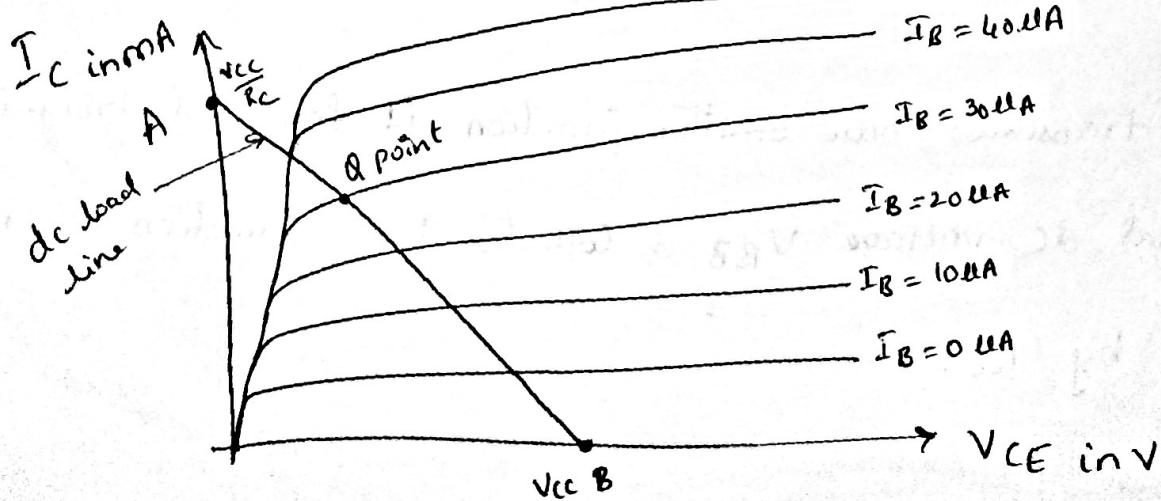
Eqn (4) represents a straight line with a slope of $(-1/R_C)$

Compare Eqn (4) with straight line Eqn

$$y = mx + c$$

\therefore (i) when $V_{CE} = V_{CC}$; $I_C = 0$ & (to find pt B)

(ii) when $V_{CE} = 0$; $I_C = \frac{V_{CC}}{R_C}$ (to find pt A)



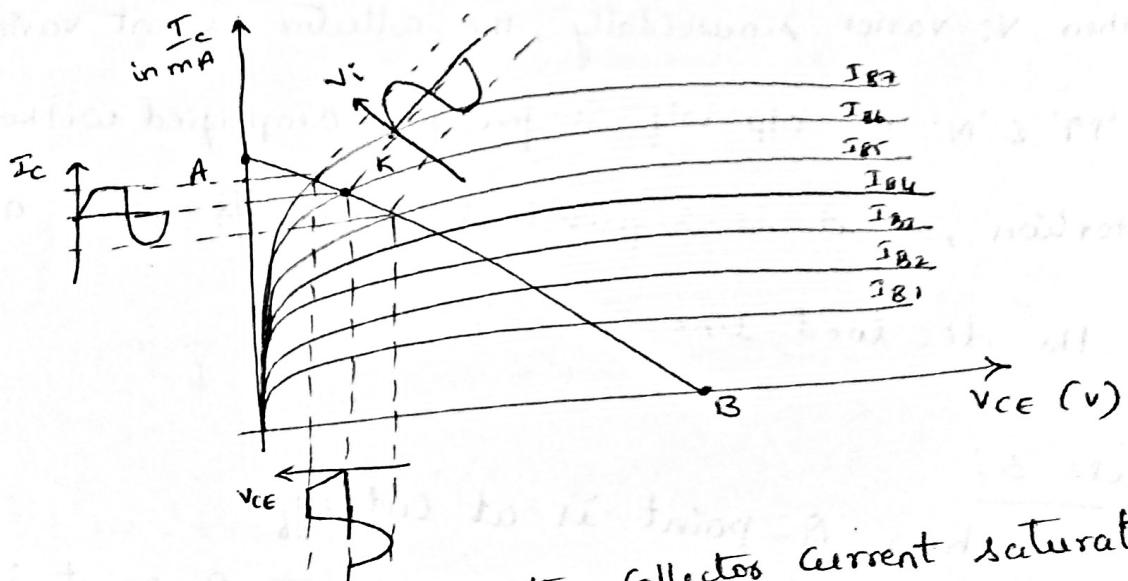
The intersection pt on the load line is called operating point or Q-point, usually Q-point is set typically near the middle of DC load line for faithful amplification.

* Selection of operating point (Q-point) :-

Case 1 :-

When Q-point is at saturation.

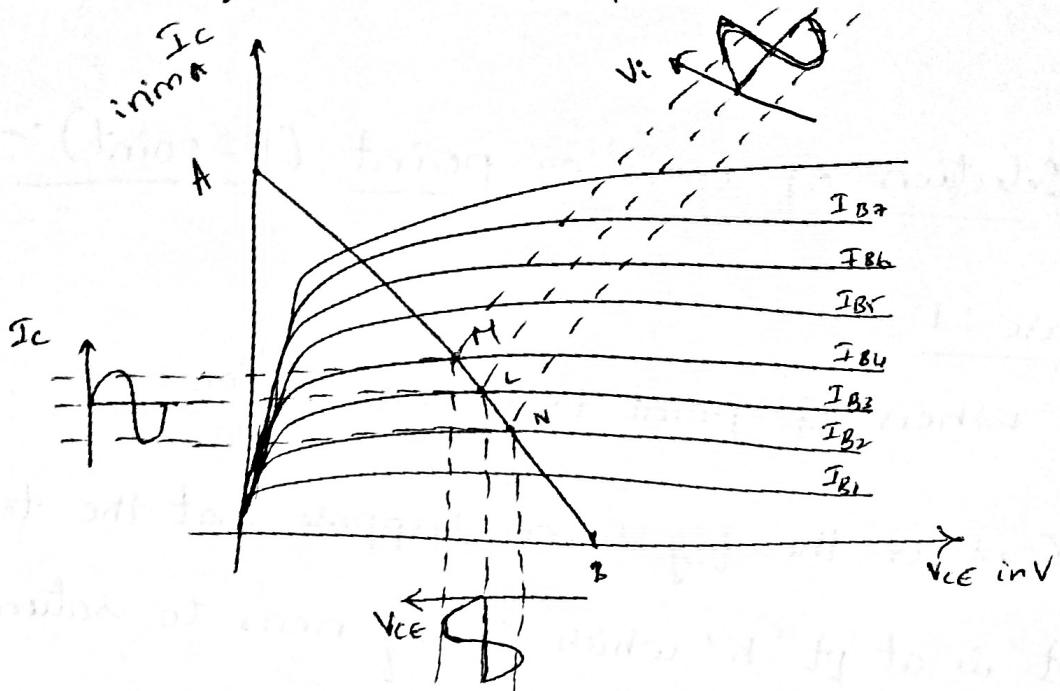
Consider the fig shown suppose that the transistor Q pt is at pt 'K' which is very near to saturation.



* From fig Vi is maximum, the collector current saturates & is shown by a clipped top indicating distortion is present across op, the I_c & V_{CE} swing are asymmetrical w.r.t variation of V_i .

Case 2:— When Q-point is at middle of active region

Consider the fig shown suppose the transistor 'Q' point is at the middle of load line (Point 'L').

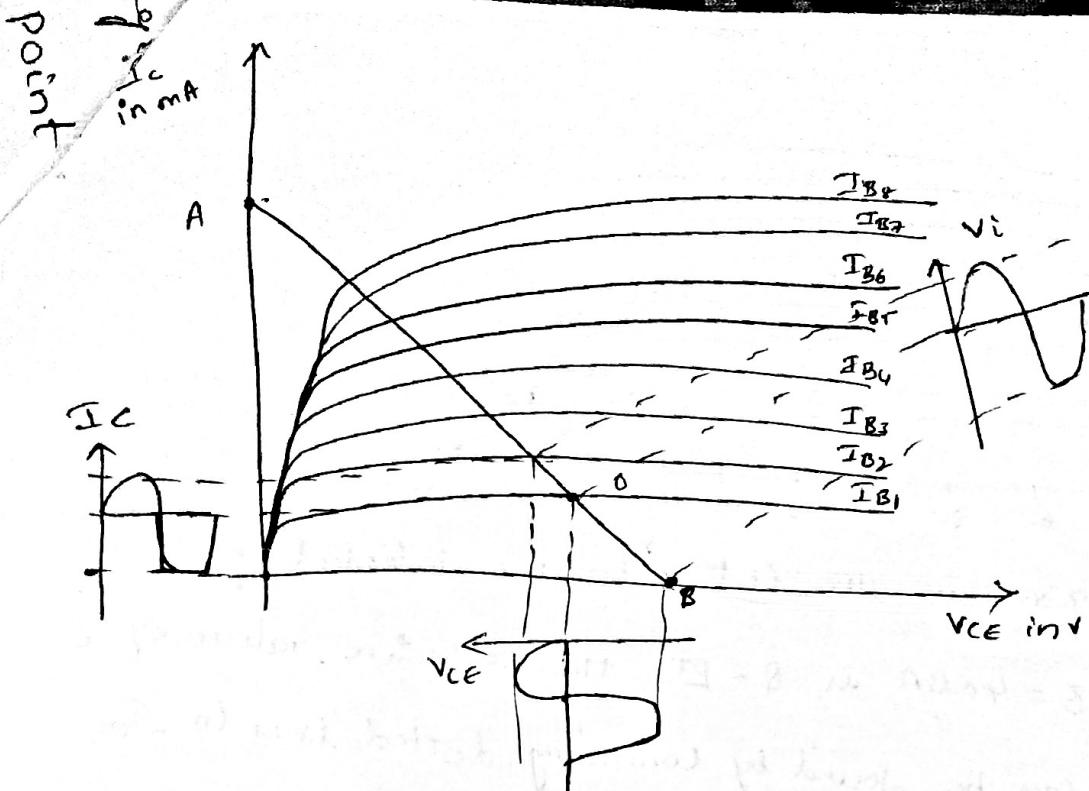


* When V_i varies sinusoidally, the collector current varies b/n pts 'M' & 'N' the o/p w/f is faithfully amplified without any distortion, so it is required to select Q-point at middle of the dc-load line.

Case 3:

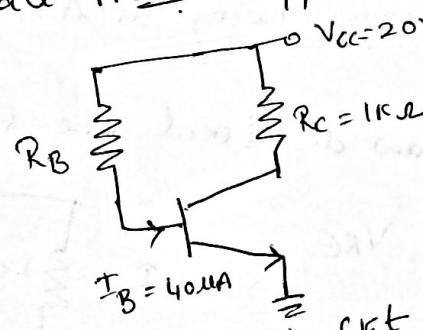
when Q-point is at cut-off

consider the fig shown, suppose the Q-point is at cutoff (point O), when V_i varies sinusoidally, during the half cycle the collector current amplifies faithfully but during -ve half cycle of V_i the collector current becomes zero & distorts the o/p signal.



Problems:-

- ① Determine the Q-point for the ckt shown below & also calculate max o/p voltage swing?



Soln:- Applying KVL to o/p ckt
 $V_{CC} = I_C R_C + V_{CE}$ — ①

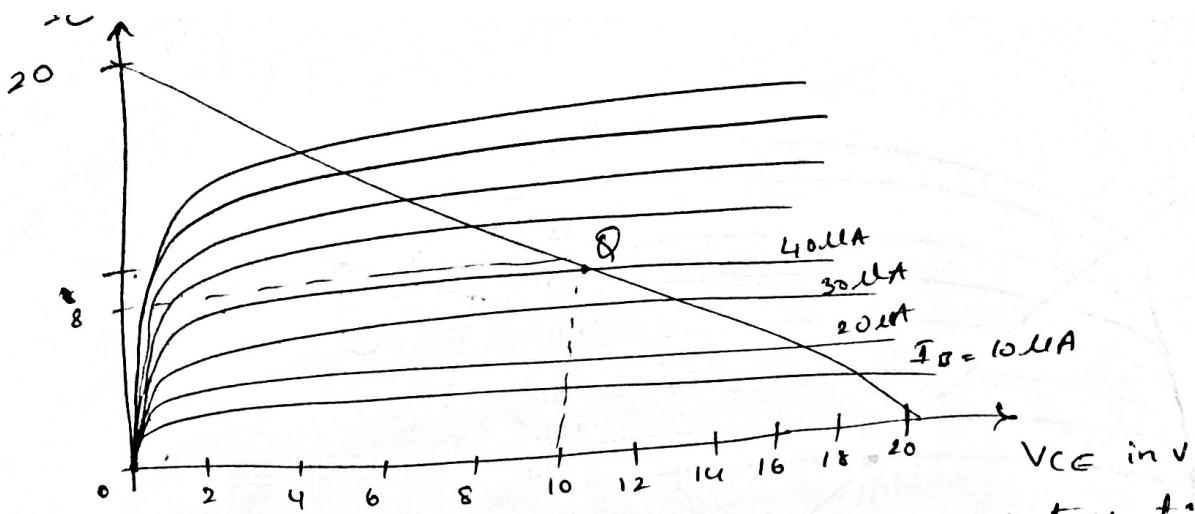
let us find point 'A', substitute $V_{CE} = 0$ in Eqn ①

$$\therefore I_C = \frac{V_{CC}}{R_C} = \frac{20}{1k} = 20 \text{ mA}$$

$I_{C\text{max}}$ is 20mA & is pt A

To find pt 'B' substitute $I_C = 0$ in Eqn ①

$$\therefore V_{CC} = V_{CE} = 20V \text{ & is pt 'B'}$$



Since I_B is given in the Ckt, so the intersection of load line at $I_B = 40\text{mA}$ in Q-pt, the respective values of I_C & V_{CE} at Q-pt can be found by connecting dotted lines to I_C & V_{CE} .

From above intersection we get $I_C = 8\text{mA}$ & $V_{CE} = 10\text{V}$

\therefore max op voltage swing in $\Delta V_{CE} \approx \pm 10\text{V}$

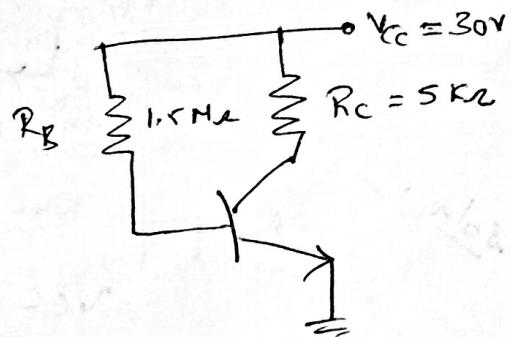
- ② For the Ckt shown draw dc load line & mark Q-pt
assume $\beta = 100$, neglect V_{BE}

$$V_{CC} = I_C R_C + V_{CE}$$

Soln:-

$$\text{pt 'A'} : - V_{CE} = 0$$

$$I_{C(\text{max})} = \frac{V_{CC}}{R_C} = \frac{30}{5K} = 6\text{mA}$$



$$\text{pt 'B'} : - I_C = 0$$

$$V_{CC} = V_{CE} = 30\text{V}$$

* Types of Biasing :-

In order to make biasing circuit simple & economical, more stable, single supply is used for biasing.

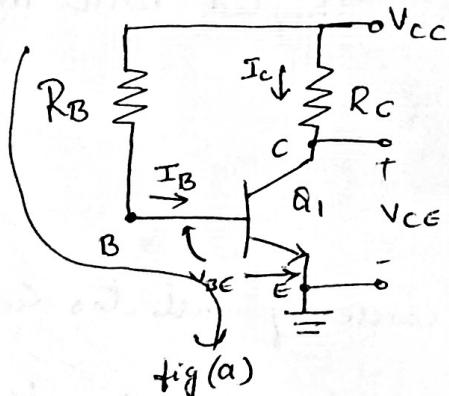
These are three different types of biasing circuits used in transistors, which employ single power supply namely :-

(a) Fixed bias (or) base resistor bias

(b) collector to base bias (or) biasing with f/b resistor

(c) voltage divider bias or self bias.

* Base Bias :-



→ The transistor bias arrangement shown in the fig known as base bias method.

→ In this method, a large resistance R_B is connected b/w the base & +ve end of supply for NPN transistor & -ve terminal of supply is grounded.

→ The base current I_B can be determined by supply voltage V_{CC} & base resistor R_B .

Since R_B & V_{CC} are constant, the base current also remains constant & fixed in value so called as fixed bias.

* To determine I_B , Apply KVL to base ckt

$$\text{ie, } V_{CC} = I_B R_B + V_{BE}$$

$$\therefore I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$V_{CC} - I_C R_C - V_{CE} = 0 \\ V_{CE} = V_{CC} - I_C R_C$$

* The transistor collector current can be found from the

relation , $I_C = \beta I_B$ where $\beta = h_{FE}$

* Advantages :-

→ The biasing ckt is very simple.

→ Single power supply is used.

→ By changing R_B the Q-pt can be shifted within active region.

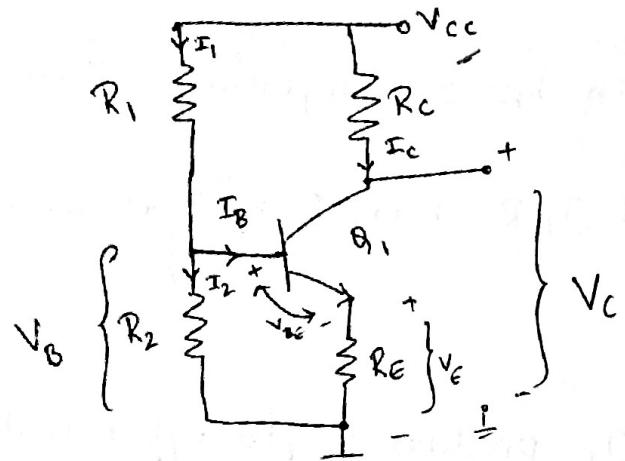
Disadvantages :-

→ It provides poor stabilization because if collector current

↑ due ↑ in temp , $I_C \uparrow$ & transistor is pushed to saturation.

→ There are strong chances of thermal run away. Hence this method is rarely used.

* Voltage divider bias :-



* A voltage divider bias Ckt is shown in the fig this is the most widely used biasing Ckt & provides good bias stability.

* In this method, two resistors R_1 & R_2 are connected across the supply voltage V_{CC} , which in turn provides biasing.

This biasing Ckt is called voltage divider bias because the supply voltage V_{CC} is divided by the voltage divider network formed by R_1 & R_2 .

The voltage drop across R_2 fwd biases base-emitter junction, this causes the base current & hence collector current to flow in the zero signal conditions.

The voltage divider bias Ckt are normally designed to have the voltage divider current I_2 in R_2 very much larger than I_B .

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_E = I_E R_E$$

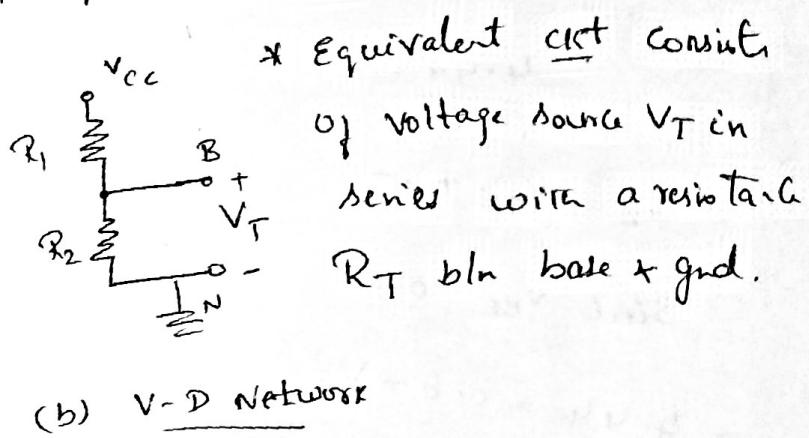
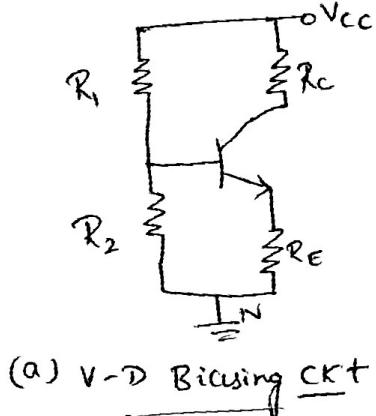
$$V_C = V_{CC} - I_C R_C$$

* Voltage divider bias (Accurate Analysis (Or) Exact analysis):-

(Or)
Precise circuit analysis :-

→ In accurate analysis the base current I_B is considered in the analysis of the Ckt.

→ The voltage divider Ckt consisting of R_1 & R_2 must be replaced with its Thvenin equivalent Ckt.



* Consider the fig (b) V-D netw, where V_T is voltage across R_2 . Using voltage division rule we get,

$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} \quad \text{--- (1)}$$

V_T is the thvenin's v_{tg}.

To find R_T we have to connect V_{CC} pt to ground as shown in the fig (c).

* voltage gain (∞) voltage amplification is given by The ratio of change in o/p voltage to the change in i/p voltage

$$\text{ie, } A_V = \frac{\Delta V_{CE}}{\Delta V_B} \quad \text{--- (3)}$$

$$A_V = -\frac{\beta \Delta I_B R_C}{\Delta V_B} \quad \text{--- (4)}$$

$$\text{let } R_C = 12\text{k}\Omega \text{ & } \beta = 50$$

$$\text{also } \Delta V_B = \pm 20\text{mV} \text{ results in } \Delta I_B = \pm 5\text{mA}$$

Substitute the values in Eqn (4),

$$\therefore A_V = \frac{-50 \times (\pm 5\text{mA}) \times 12\text{k}}{\pm 20\text{mV}}$$

$$A_V = -150$$

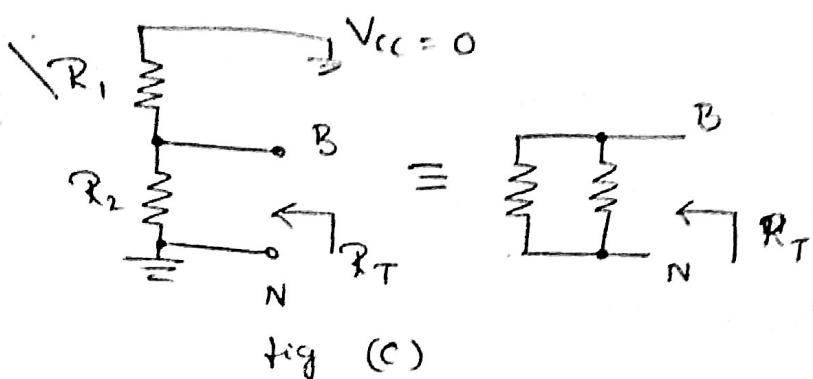
$$\underline{|A_V| = 150}$$

$$\therefore \text{From Eqn (3), } \Delta V_{CE} = A_V \Delta V_B$$

$$\underline{\Delta V_{CE} = -150 \Delta V_B}$$

i.e., change in o/p voltage = -150 times change in i/p voltage

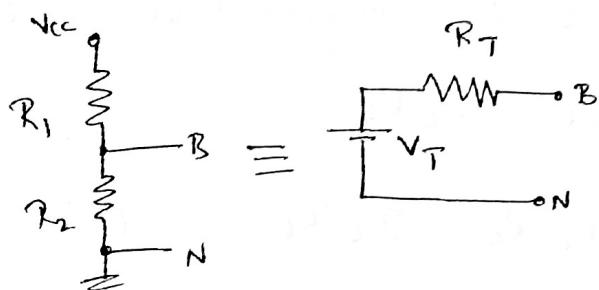
* The -ve sign in A_V implies, i/p & o/p voltages of CE configuration are 180° out of phase.



$\therefore R_T$ is the equivalent resistance b/w B & N

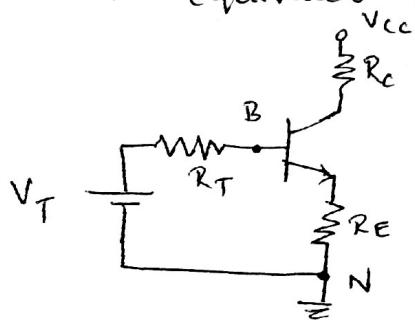
$$R_T = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad \text{--- (2)}$$

* The Thévenin Equivalent ckt of voltage divider n/w of fig(b) b/w the pt B & N is show in the fig(d).



fig(d) : Thévenin Equivalent of V-D n/w

Now let us replace the voltage divider n/w in fig (a) with its Thévenin Equivalent ckt.



fig(e)

\therefore Applying KVL to the B-E ckt

$$V_T = R_T I_B + V_{BE} + I_E R_E \quad \text{--- (3)}$$

$$\text{But } I_E = I_B + I_C$$

$$= I_B + \beta I_B$$

$$\therefore I_E = I_B (1 + \beta)$$

Using this relation in Eqn ③ we have

$$V_T = R_T I_B + V_{BE} + (1+\beta) I_B R_E$$

$$V_T - V_{BE} = I_B [R_T + (1+\beta) R_E]$$

$$\therefore I_B = \frac{V_T - V_{BE}}{R_T + (1+\beta) R_E} \quad \text{--- } ④$$

Once I_B is known, the I_C is obtained by,

$$I_C = \beta I_B \quad \text{--- } ⑤$$

V_{CE} can be obtained by applying KVL to CE cut

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\therefore V_{CE} = \underline{V_{CC} - I_C R_C - I_E R_E} \quad \text{--- } ⑥$$

$$I_C \approx I_E$$

$$\left. \begin{aligned} I_C &= (\beta + 1) I_B \\ I_E &= I_C \end{aligned} \right\}$$

② A voltage divider bias Ckt has $V_{CC} = 18V$, $R_1 = 33k\Omega$, $R_E = 1k\Omega$, $R_C = 1.2k\Omega$, $\beta = 50$. Taking $V_{BE} = 0.7V$, find I_C , V_{CE} & V_C . Draw the DC load line & locate the Q-point.

Soln: - Since ' β ' is given I_B can be calculated. Hence we can use exact or accurate analysis.

$$V_T = \frac{V_{CC}R_2}{R_1+R_2} = \frac{18 \times 12k}{33k + 12k} = \underline{\underline{4.8V}}$$

$$R_T = \frac{R_1 R_2}{R_1 + R_2} = \frac{33k * 12k}{33k + 12k} = \underline{\underline{8.8k\Omega}}$$

$$I_B = \frac{V_T - V_{BE}}{R_T + (1+\beta)R_E} = \frac{4.8 - 0.7}{8.8k + (1+50)(1k)} = \underline{\underline{0.0686mA}}$$

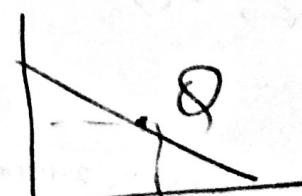
$$I_C = \beta I_B = 50 \times 0.0686mA = \underline{\underline{3.43mA}}$$

$$I_E = I_B + I_C = \underline{\underline{3.5mA}}$$

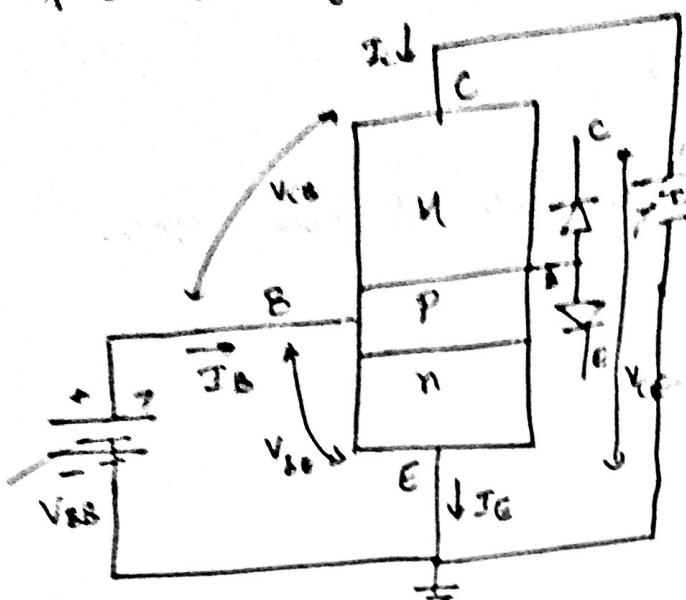
$$V_E = I_E R_E = 3.5mA \times 1k = \underline{\underline{3.5V}}$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C - I_E R_E \\ &= 18V - 3.43mA \times 1.2k - 3.5mA \times 1k \end{aligned}$$

$$= \underline{\underline{10.38V}}$$



\rightarrow CE Configuration :



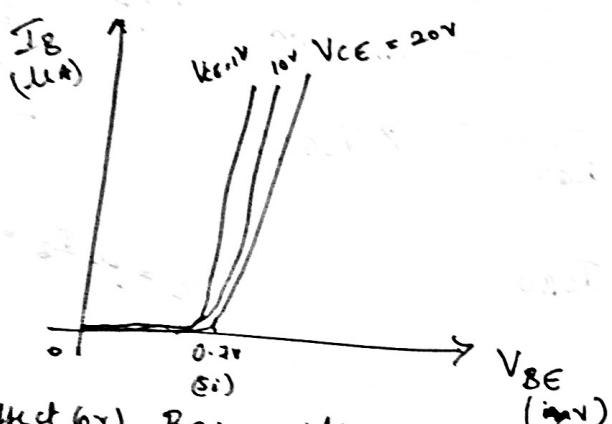
V_{BS} & V_{CC} \rightarrow Biasing potential

V_{BE} & I_S are the voltage & current respectively

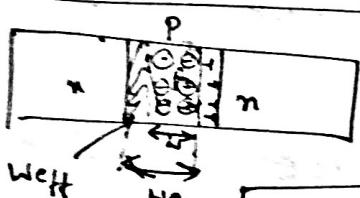
V_{CE} & I_C are the O/P

For plotting the i/p char,

the i_p I_B & i_p voltage V_{BE} for diff values of V_{CE} are plotted.



Early effect (or) Base width modulation :-



$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CE} = V_{CB} + V_{BE} \text{ (at saturation)}$$

$$W_{CH} = W_B - N$$

depletion region base region

As a result more penetration in

$$\text{If } V_{CE} \uparrow = V_{CB} \uparrow = n \uparrow$$

as $n \uparrow$; $W_{eff} \downarrow$ as N_B (const)

as $W_{eff} \downarrow$ less the conduction takes place at base region.

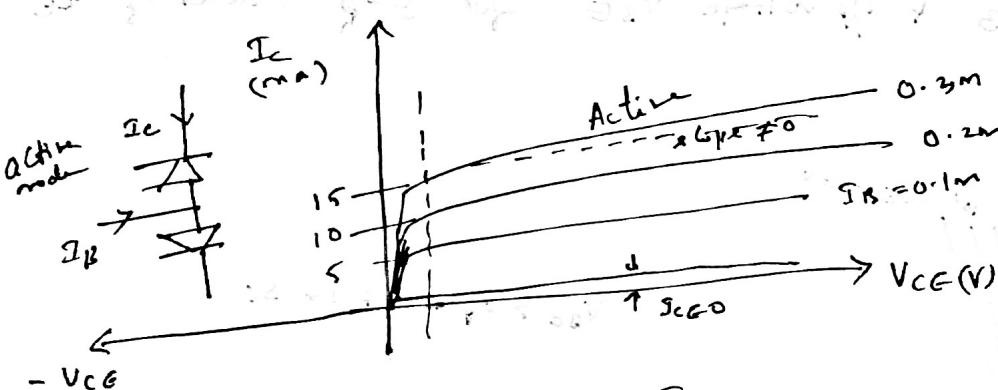
$\therefore I_B \downarrow$

$$\therefore V_{CE} \uparrow = I_B \downarrow$$

$$(or) V_{CE} \downarrow = I_B \uparrow$$

O/p char: i.e., O/p Current v/s o/p voltage for diff I_C v/s V_{CG}

values of I_B .



$$I_B = 0.1\text{mA} ; I_{Cmax} = 10\text{mA}$$

$$I_B = 0.2\text{mA} ; I_{Cmax} = 20\text{mA}$$

$$\therefore \beta = \frac{\Delta I_C}{\Delta I_B} = \frac{10 - 5}{0.2 - 0.1} = 50$$

$$I_P = 50$$

$$\text{w.r.t. } I_C = \beta I_B + (1 + \beta) I_{CBO}$$

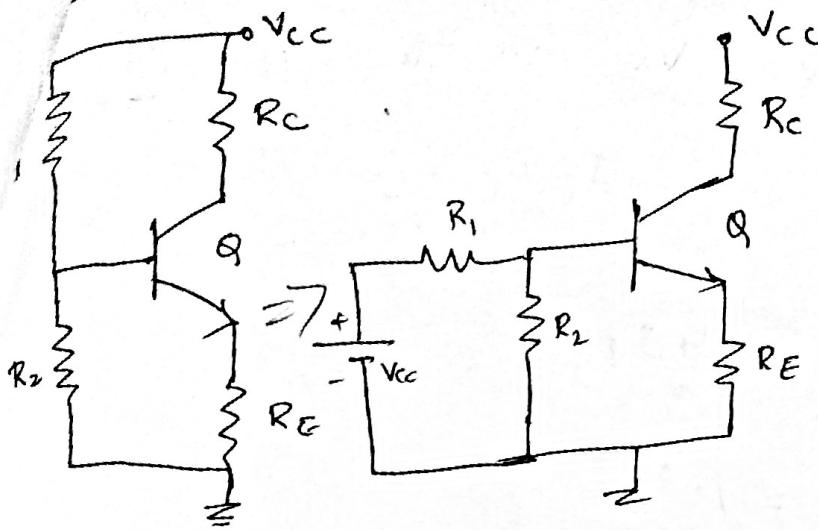
$$I_C = \beta I_B + I_{CBO}$$

$$I_B = 0$$

$$\therefore I_C = (1 + \beta) I_{CBO} \rightarrow \text{Small Current} = I_{CBO} = \text{leaking current}$$

Cutoff

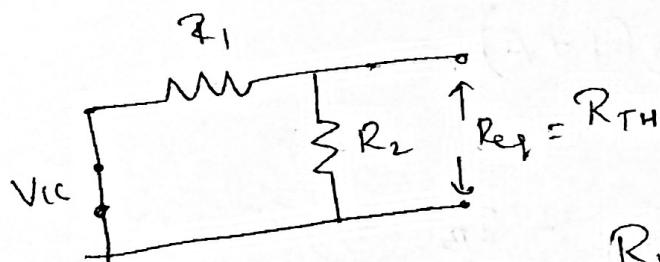
slope $\neq 0 \dots I_C$ depends on V_{CE} due to early effect



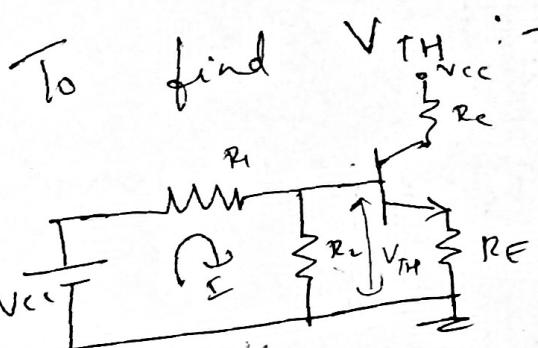
R_{TH}

V_{TH}

To find R_{TH} short V_{CC}



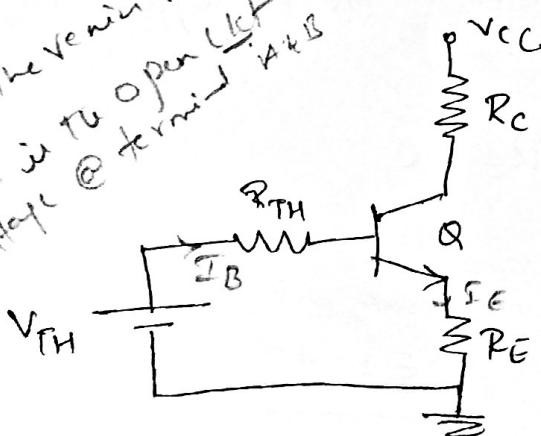
$$R_{TH} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$



$$I = \frac{V_{CC}}{R_1 + R_2}$$

$$\therefore V_{TH} = IR_2 = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$$

The Thévenin voltage
'i.e.' is the open circuit
voltage @ terminal A & B



$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$I_E = I_C + I_B$$

$$I_C = \beta I_B$$

$$\begin{aligned} V_{CC}, \Sigma R_1, \Sigma R_2 &\neq 0 \\ V_{CC}, \Sigma (R_1 + R_2) &\neq 0 \\ \Sigma &= \frac{V_{CC}}{R_{TH}} \\ \therefore V_{TH} &= I_B R_2 \end{aligned}$$

Thévenin's Theorem:
Any combination of batteries
& resistances can be replaced by
a single voltage source 'E'
& a single resistor 'R'.
To find 'E' at terminals
short V_{CC} & all
sources V_{CC} replaced by
current I .
To find 'R'
short V_{CC} & all
sources V_{CC} replaced by
open circuit
 $\Sigma R_1 + \Sigma R_2 = 0$

To find I_B apply KVL to the i/p $\underline{C_{K_F}}$

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

Since $I_E = I_C + I_B$

But $I_C = \beta I_B$

$$\therefore I_E = \beta I_B + I_B$$

$$\underline{I_E = I_B(1+\beta)}$$

$$\therefore V_{TH} - I_B R_{TH} - V_{BE} - I_B(1+\beta) R_E = 0$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta+1)R_E}$$

Once I_B is known I_C can be found by

$$I_C = \beta I_B$$

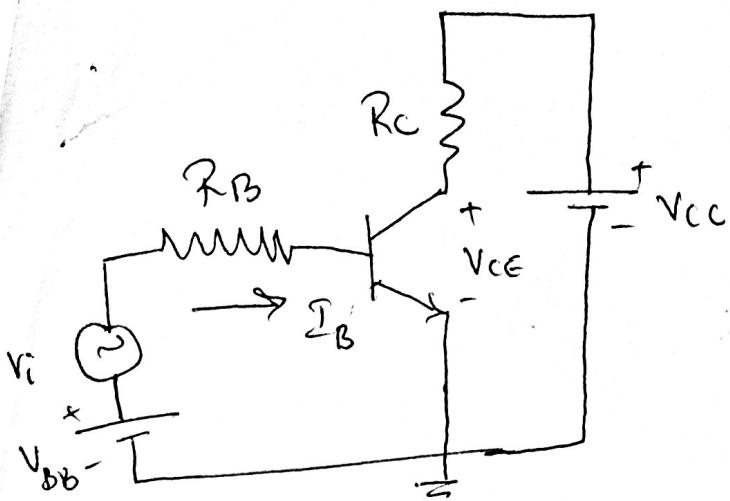
To find V_{CE} :- Apply KVL to the o/p $\underline{C_{K_F}}$

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

~~Since $I_E \ll I_C$~~

$$\therefore V_{CE} = \underline{\underline{V_{CC} - I_C(R_C + R_E(1+\beta)) I_B}}$$

Voltage amplification in BJT:-



As i/p voltage $\propto I_B$
 $I_B \propto V_{BE}$ across R_C there is
 drop in V_{CE} due to i/p
 phase off ie I_B
 'phase off' out of plane

* V_i is the ac voltage (signal) to be amplified. It is connected in B-E Ckt.

Let the i/p voltage change by an amount ΔV_B .

\therefore the base current changes by ΔI_B & collector

current changes by,

$$\Delta I_C = \beta \Delta I_B \quad \text{--- (1)}$$

Apply KVL to the C-E Ckt,

$$\therefore V_{CC} - I_C R_C - V_{CE} = 0$$

Change in o/p voltage V_{CE} is given by,

$$\Delta V_{CE} = -\Delta I_C R_C$$

$$\Delta V_{CE} = -\beta \Delta I_B R_C \quad \text{--- (2)}$$

$$\therefore V_{CC} = 0$$

* voltage gain (A_v) voltage amplification is given by the ratio of change in o/p voltage to the change in i/p voltage.

$$\text{ie, } A_v = \frac{\Delta V_{CE}}{\Delta V_B} \quad \rightarrow \textcircled{3}$$

$$A_v = -\frac{\beta \Delta I_B R_C}{\Delta V_B} \quad \rightarrow \textcircled{4}$$

$$\text{let } R_C = 12\text{k}\Omega \quad \& \quad \beta = 50$$

$$\text{also } \Delta V_B = \pm 20\text{mV} \text{ results in } \Delta I_B = \pm 5\text{mA}$$

Substitute the values in Eqn \textcircled{4},

$$\therefore A_v = \frac{-50 \times (\pm 5\text{mA}) \times 12\text{k}}{\pm 20\text{mV}}$$

$$\boxed{A_v = -150}$$

$$\underline{|A_v| = 150}$$

$$\therefore \text{From Eqn } \textcircled{3}, \Delta V_{CE} = A_v \Delta V_B$$

$$\underline{\Delta V_{CE} = -150 \Delta V_B}$$

i.e., change in o/p voltage = -150 times change in i/p voltage.

* The -ve sign in A_v implies, i/p & o/p voltages of CE configuration are 180° out of phase.