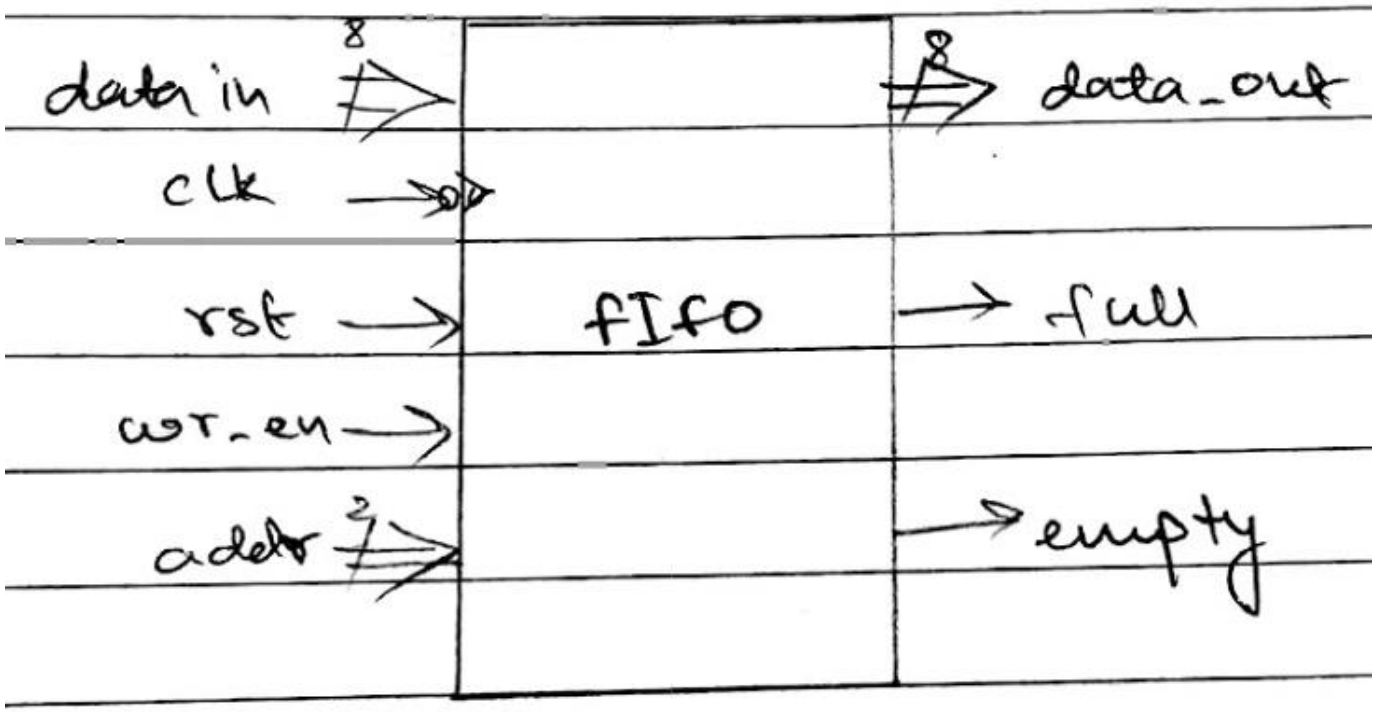
Class	:	BE - 8
Roll No	:	42410
Assignment No	:	3
Assignment Name	:	FIFO
Date of Performance	:	3-10 to 10-10

BLOCK DIAGRAM:



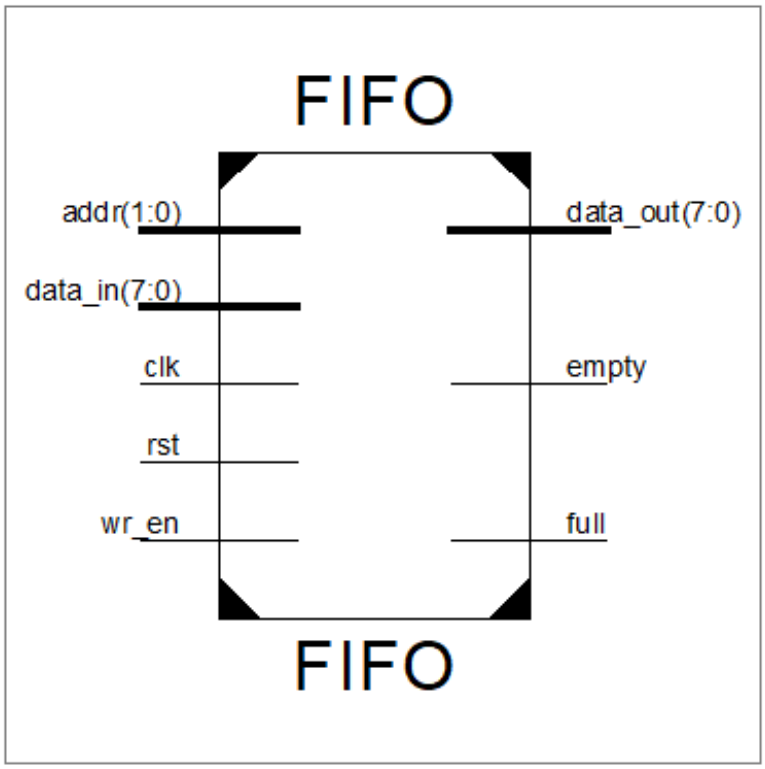
Function Table:

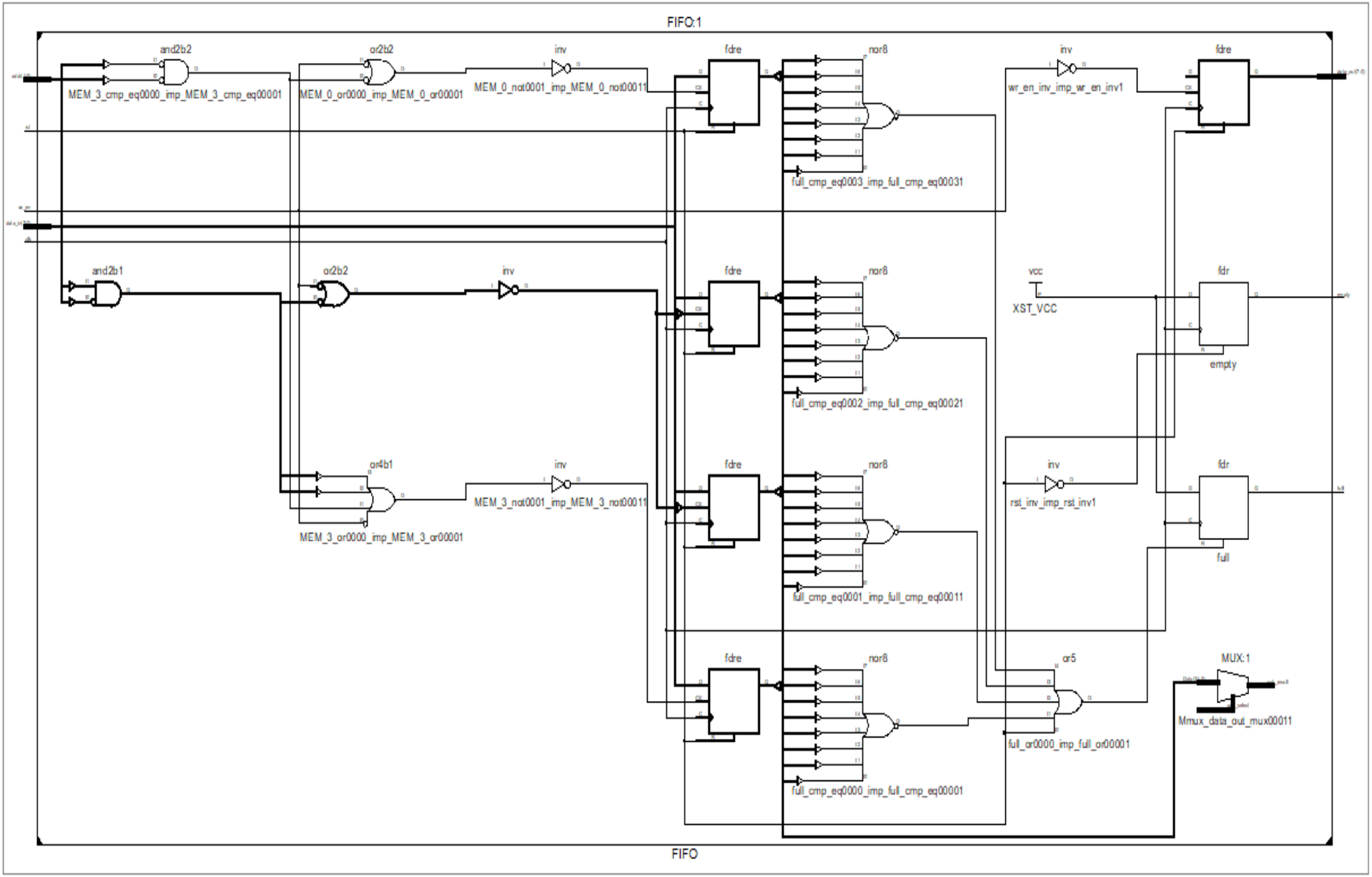
rst	CLK	wr_en	addr	data_out	full	Empty
1	x	x	X	$(00)_H$	0	1
0	↓	1	$(00)_2$	NA	0→1	0
0	↓	0	↓ $(11)_2$	data_in	0	0

MAIN VHDL PROGRAM:

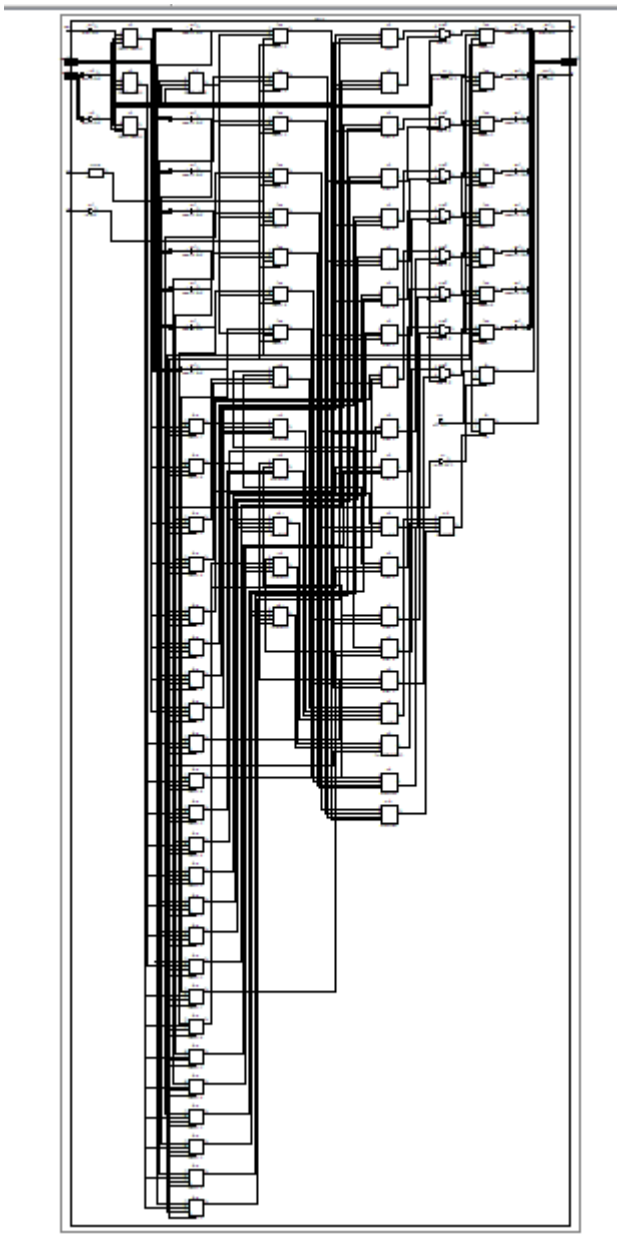
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;
entity FIFO is
   Port
    (
         data_in : in  STD_LOGIC_VECTOR (7 downto 0);
       rst : in  STD_LOGIC;
       clk : in  STD_LOGIC;
       wr_en : in  STD_LOGIC;
         addr : in  STD_LOGIC_VECTOR (1 downto 0);
       data_out : out  STD_LOGIC_VECTOR (7 downto 0);
       empty : inout  STD_LOGIC;
       full : inout  STD_LOGIC);
end FIFO;
architecture FIFO_ARCH of FIFO is
   TYPE MEMORY IS ARRAY(0 TO 3) OF STD_LOGIC_VECTOR(7 DOWNTO 0);
   SIGNAL MEM : MEMORY:=(X"00",X"00",X"00",X"00");
   CONSTANT all_zeros : MEMORY :=(others => (others=>'0'));
begin
   PROCESS(data_in,rst,clk,wr_en,addr,empty,full)
   BEGIN
      IF rst='1' THEN
         data_out<=X"00";
         MEM<=(X"00",X"00",X"00",X"00");
         empty<='1';
         full<='0';
      ELSIF FALLING_EDGE(clk) THEN
         IF (MEM(0)/=X"00") AND (MEM(1)/=X"00") AND (MEM(2)/=X"00") AND (MEM(3)/=X"00") THEN
            empty<='0';
            full<='1';
         ELSE
            empty<='0';
            full<='0';
         END IF;
         IF wr_en='1' THEN   --WRITE
            CASE addr IS
               WHEN "00" => MEM(0)<=data_in;
               WHEN "01" => MEM(1)<=data_in;
               WHEN "10" => MEM(2)<=data_in;
               WHEN OTHERS => MEM(3)<=data_in;
            END CASE;
         ELSE              --READ
            CASE addr IS
               WHEN "00" => data_out<=MEM(0);-- MEM(0)<=X"00";
               WHEN "01" => data_out<=MEM(1);-- MEM(1)<=X"00";
               WHEN "10" => data_out<=MEM(2);-- MEM(2)<=X"00";
               WHEN OTHERS => data_out<=MEM(3);-- MEM(3)<=X"00";
            END CASE;
         END IF;
      END IF;
   END PROCESS;
end FIFO_ARCH;
```

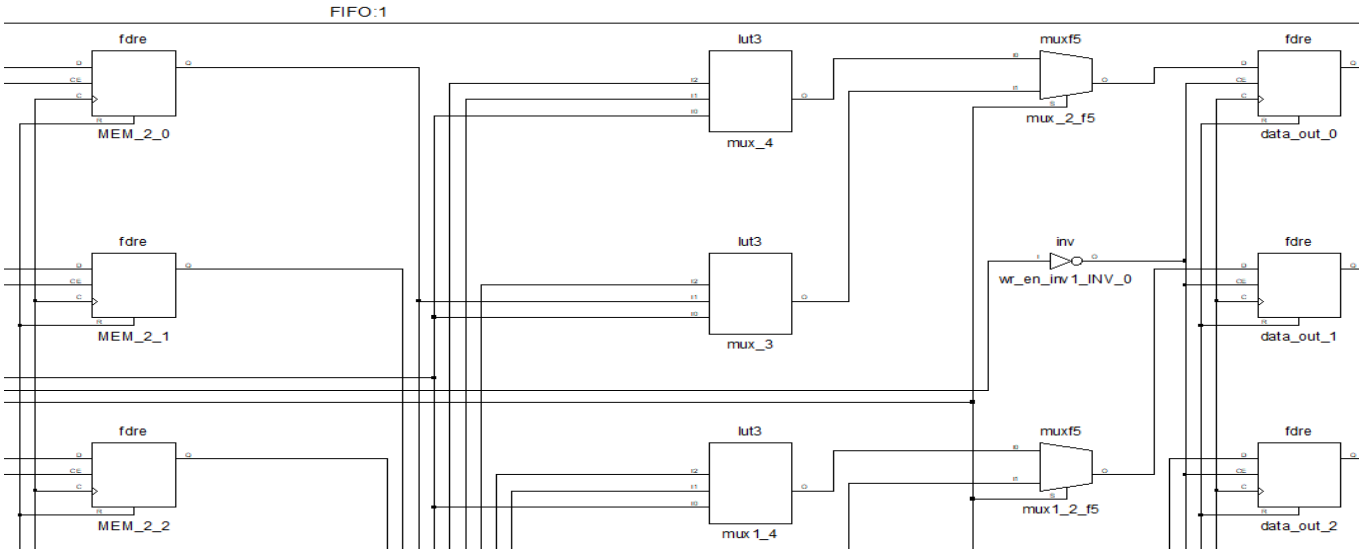
RTL SCHEMATIC




FIFO:1
and2b2
MEM_3_cmp_eq0000_imp_MEM_3_cmp_eq00001
or2b2
MEM_0_or0000_imp_MEM_0_or00001
inv
MEM_0_not0001_imp_MEM_0_not00011
fdre
nor8
full_cmp_eq0003_imp_full_cmp_eq00031
inv
wr_en_inv_imp_wr_en_inv1
fdre
and2b1
or2b2
inv
fdre
nor8
full_cmp_eq0002_imp_full_cmp_eq00021
vcc
XST_VCC
fdr
empty
or4b1
MEM_3_or0000_imp_MEM_3_or00001
inv
MEM_3_not0001_imp_MEM_3_not00011
fdre
nor8
full_cmp_eq0001_imp_full_cmp_eq00011
inv
rst_inv_imp_rst_inv1
fdr
full
fdre
nor8
full_cmp_eq0000_imp_full_cmp_eq00001
or5
full_or0000_imp_full_or00001
MUX:1
Mmux_data_out_mux00011
FIFO

TECHNOLOGY SCHEMATIC





SYNTHESIS REPORT:

A) Device Utilisation Summary

```
=========================================================================
*                      Final Report                     *
=========================================================================
Final Results
RTL Top Level Output File Name     : FIFO.ngr
Top Level Output File Name         : FIFO
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 23

Cell Usage :
# BELS                             : 41
#      GND                         : 1
#      INV                         : 1
#      LUT2                        : 1
#      LUT3                        : 20
#      LUT4                        : 8
#      LUT4_L                      : 2
#      MUXF5                       : 8
# FlipFlops/Latches                : 42
#      FDC_1                       : 1
#      FDCE_1                      : 40
#      FDP_1                       : 1
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 22
#      IBUF                        : 12
#      OBUF                        : 10
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                29  out of   2448     1%
 Number of Slice Flip Flops:      41  out of   4896     0%
 Number of 4 input LUTs:          32  out of   4896     0%
 Number of IOs:                   23
 Number of bonded IOBs:           23  out of    158    14%
    IOB Flip Flops:               1
 Number of GCLKs:                 1  out of     24     4%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

B) TIMMING REPORT

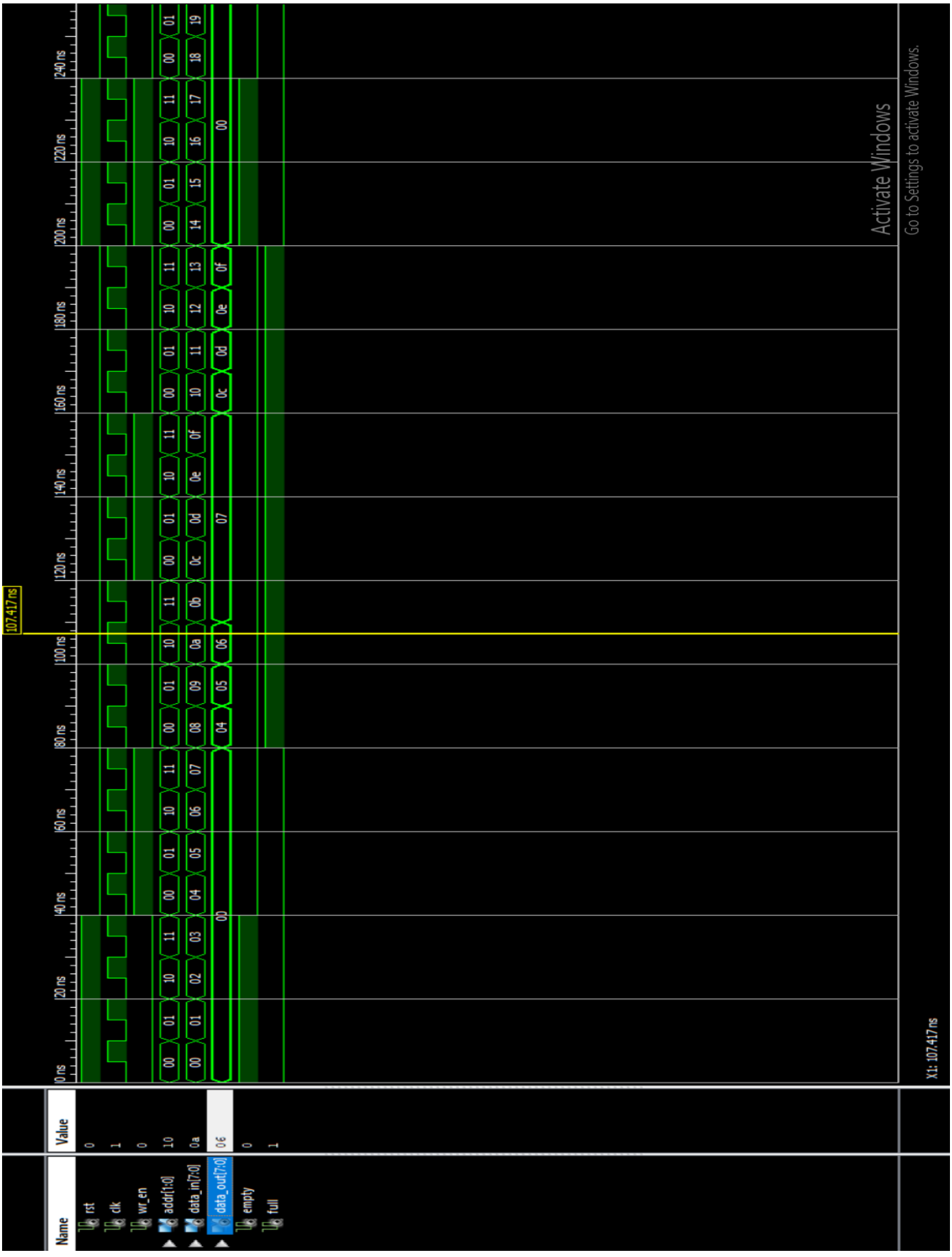
```
================================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
    FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
    GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 42    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
rst                                | IBUF                   | 42    |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 4.085ns (Maximum Frequency: 244.801MHz)
   Minimum input arrival time before clock: 3.933ns
   Maximum output required time after clock: 4.040ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

TEST BENCH PROGRAM

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

ENTITY FIFO_tb IS
END FIFO_tb;

ARCHITECTURE behavior OF FIFO_tb IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT FIFO
   PORT(
        data_in : IN  std_logic_vector(7 downto 0);
        rst : IN  std_logic;
        clk : IN  std_logic;
        wr_en : IN  std_logic;
                    addr : in  STD_LOGIC_VECTOR (1 downto 0);
        data_out : OUT  std_logic_vector(7 downto 0);
        empty : INOUT  std_logic;
        full : INOUT  std_logic
       );
   END COMPONENT;


  --Inputs
  signal data_in : std_logic_vector(7 downto 0) := X"FF";
  signal rst : std_logic := '1';
  signal clk : std_logic := '0';
  signal wr_en : std_logic := '0';
      signal addr :  STD_LOGIC_VECTOR (1 downto 0):="00";

      --BiDirs
  signal empty : std_logic;
  signal full : std_logic;

      --Outputs
  signal data_out : std_logic_vector(7 downto 0);

  -- Clock period definitions
  constant clk_period : time := 10 ns;

BEGIN

      -- Instantiate the Unit Under Test (UUT)
  uut: FIFO PORT MAP (
        data_in => data_in,
        rst => rst,
        clk => clk,
        wr_en => wr_en,
                     addr => addr,
        data_out => data_out,
        empty => empty,
```

```
      full => full
     );

  -- Clock process definitions
  clk_process :process
  begin
          clk <= '0';
          wait for clk_period/2;
          clk <= '1';
          wait for clk_period/2;
  end process;


  -- Stimulus process
  stim_procDIN: process
  begin
    data_in<= data_in +1;
          wait for 10 ns;
  end process;

     stim_procRST: process
  begin
          rst<= '1';
          wait for 40 ns;
    rst<= '0';
          wait for 160 ns;
     end process;

     stim_procWREN: process
  begin
          wait for 40 ns;
          wr_en<=NOT(wr_en);
  end process;

     stim_procADDR: process
  begin
          wait for 10 ns;
          addr<= addr+1;
  end process;
END;
```

ISIM WAVEFORMS



PIN LOCKING REPORT

```
# PlanAhead Generated physical constraints

NET "data_in[7]" LOC = P165;     #sw4-0
NET "data_in[6]" LOC = P167;     #sw4-1
NET "data_in[5]" LOC = P163;     #sw4-2
NET "data_in[4]" LOC = P164;
NET "data_in[3]" LOC = P161;
NET "data_in[2]" LOC = P162;
NET "data_in[1]" LOC = P160;
NET "data_in[0]" LOC = P153;     #sw4-7
NET "data_out[7]" LOC = P179;   #sw3-0
NET "data_out[6]" LOC = P180;   #sw3-1
NET "data_out[5]" LOC = P177;
NET "data_out[4]" LOC = P178;
NET "data_out[3]" LOC = P152;
NET "data_out[2]" LOC = P168;
NET "data_out[1]" LOC = P171;
NET "data_out[0]" LOC = P172;   #sw3-7
NET "clk" LOC = P132;
NET "reset" LOC = P204;          #k0
NET "enr" LOC = P184;        #sw2-6
NET "enw" LOC = P194;        #sw2-7
NET "fifo_empty" LOC = P199;#sw1-6
NET "fifo_full" LOC = P196;  #sw1-7
```

Conclusion:

Thus, we have:

1) Modeled a 4-bit ALU using Behavioral Modeling Style.
2) Observed following Schematics: **RTL** & **Technology Schematics** generated **Post-Synthesis**.
3) Interpreted **Device utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers & D FFs used out of the available device resources.
4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
5) Written a TESTBENCH to verify the functionality of 4-bit ALU & verified the functionality as per the TRUTH-TABLE, by observing ISIM Waveforms.
6) Used Plan Ahead Editor for pin-locking.
7) Prototyped the FPGA **XC3S250EPQ208-5** to realize 4-bit ALU & verified its operation by giving suitable input combinations