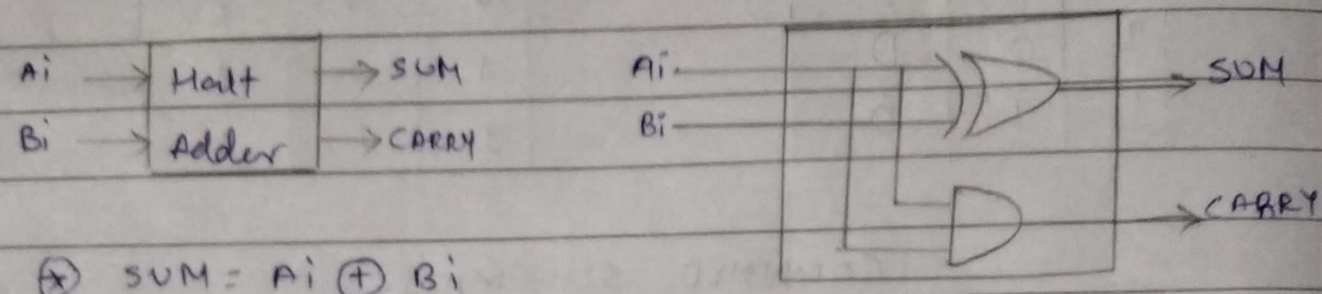
| | | |
|---|---|---|
| Class | : | BE - 8 |
| Roll. No | : | 42410 |
| Assignment No. | : | 1.f |
| Assignment Name | : | Half Adder |
| Date of Performance | : | 21-11-2020 |

(+) (L-f) Half Adder :- Also Includes Assignment 2

F = 90 nm

+ Symbol :-

Gate-level Schematic




(*) SUM = Ai ⊕ Bi

CARRY = Ai · Bi

TRUTH TABLE

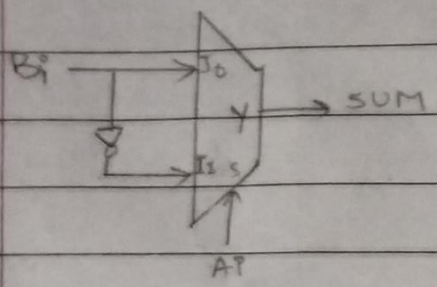
| Ai | Bi | SUM | CARRY |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

(+) Approach TG → MUX → LOGIC GATE

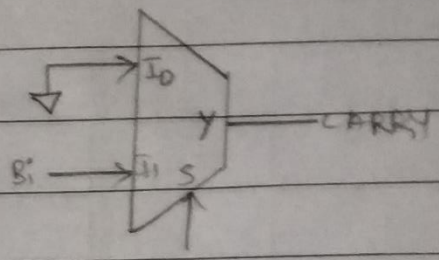
(i) (ii)

## ⊛ Assignment:- 1.f (continued...)

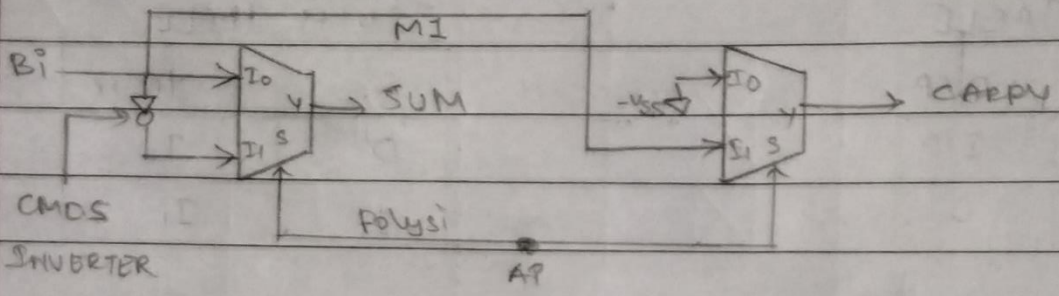
MUX-1 (EX-OR GATE)



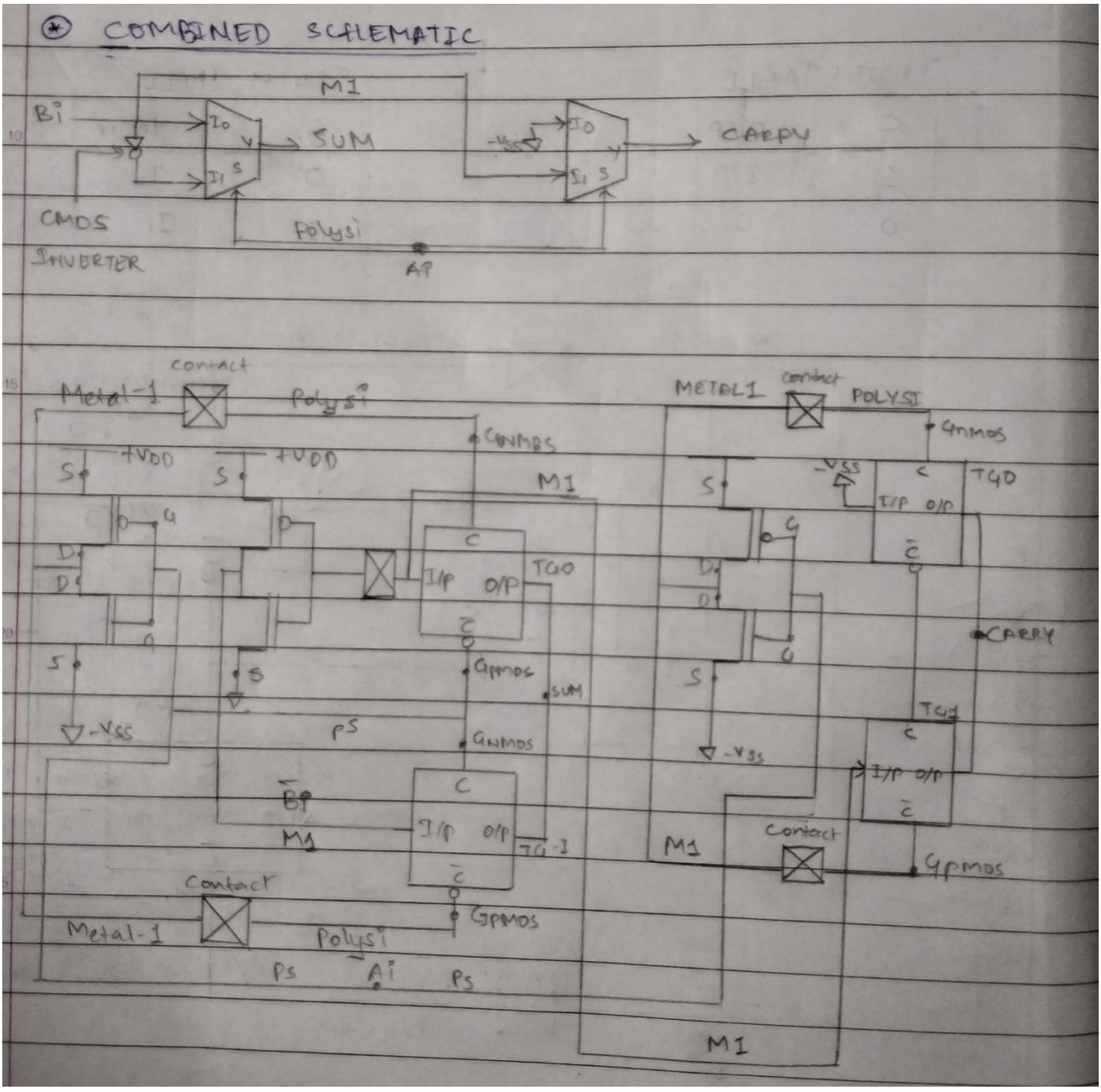

MUX-2 (AND GATE)



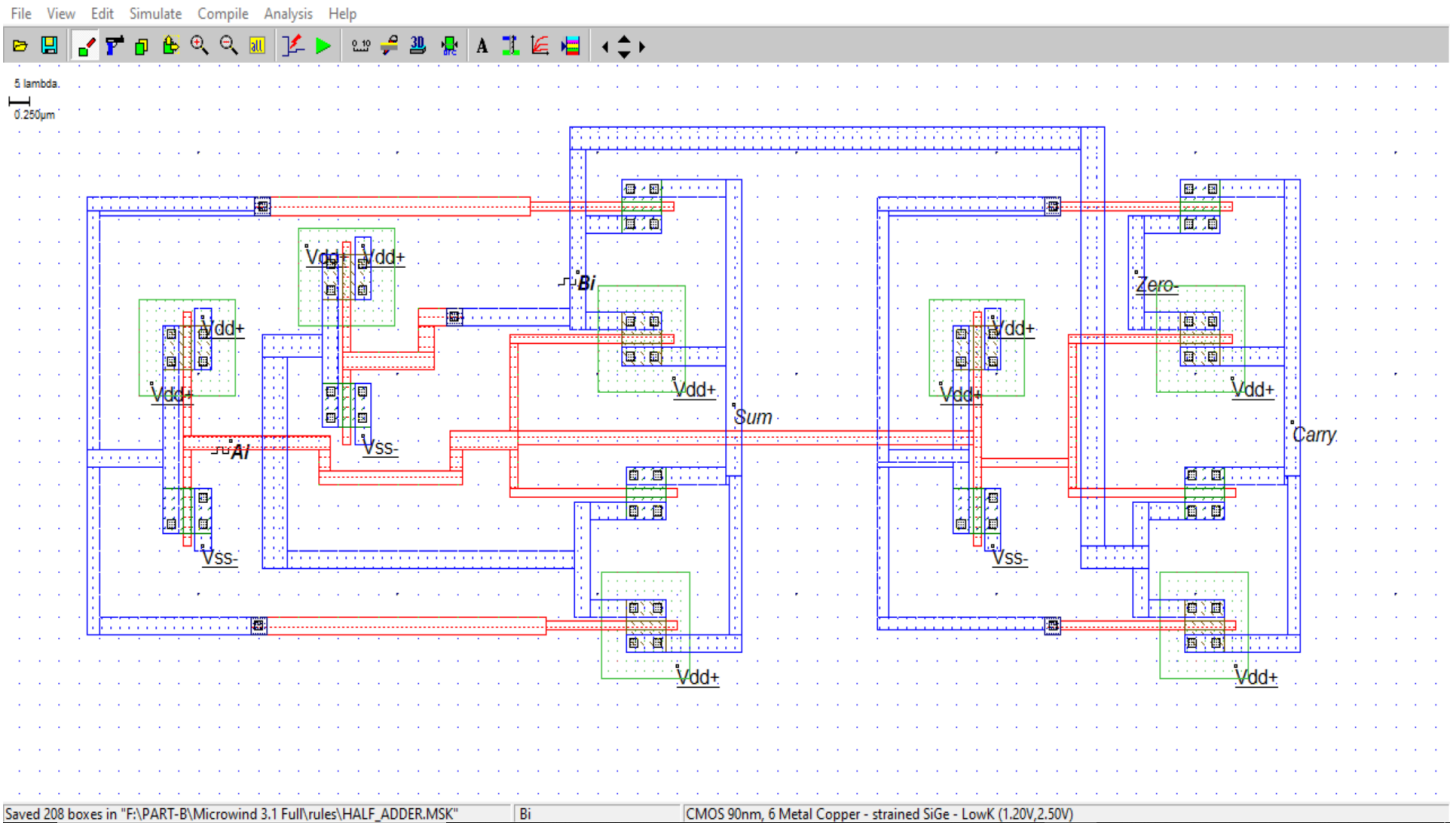

## ⊛ COMBINED SCHEMATIC



**BLOCK DIAGRAM**

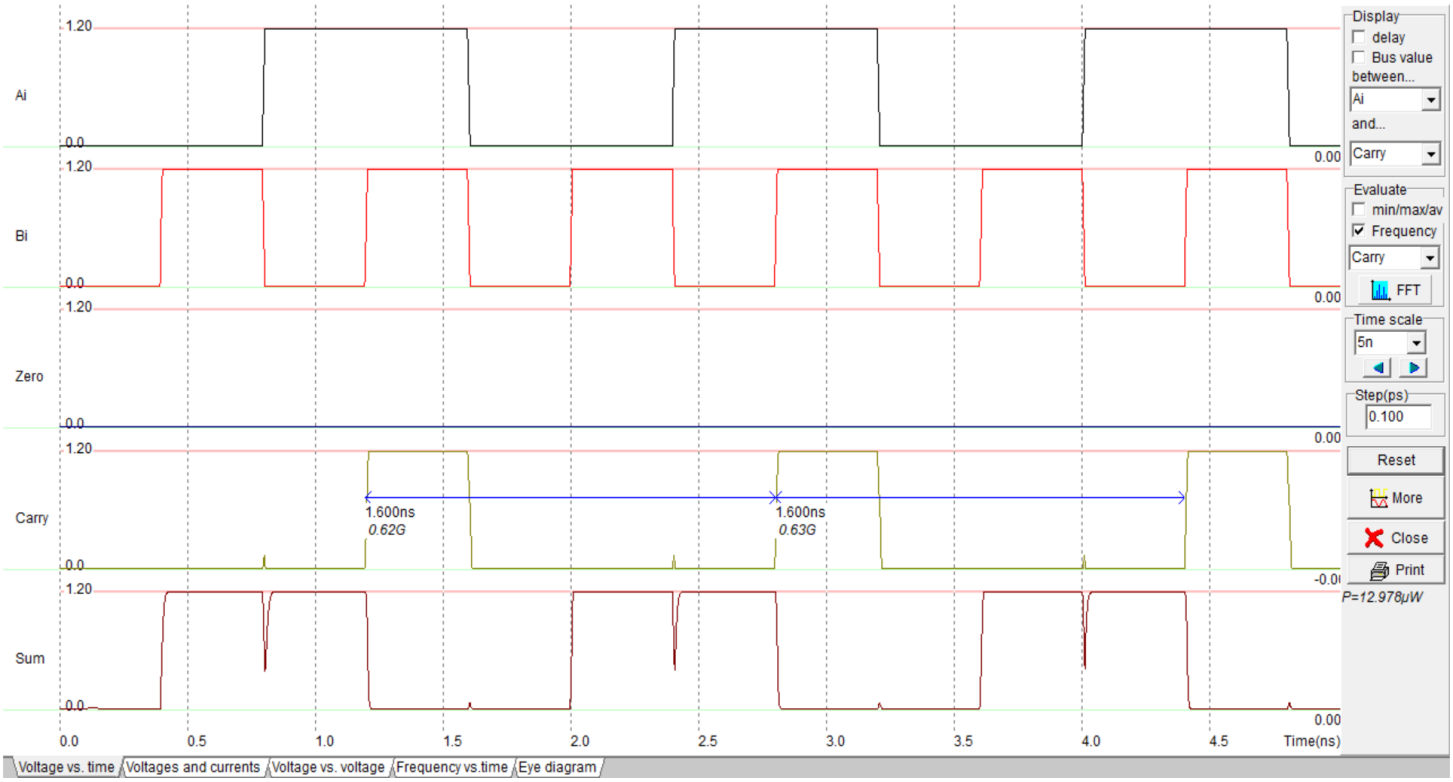


# LAYOUT

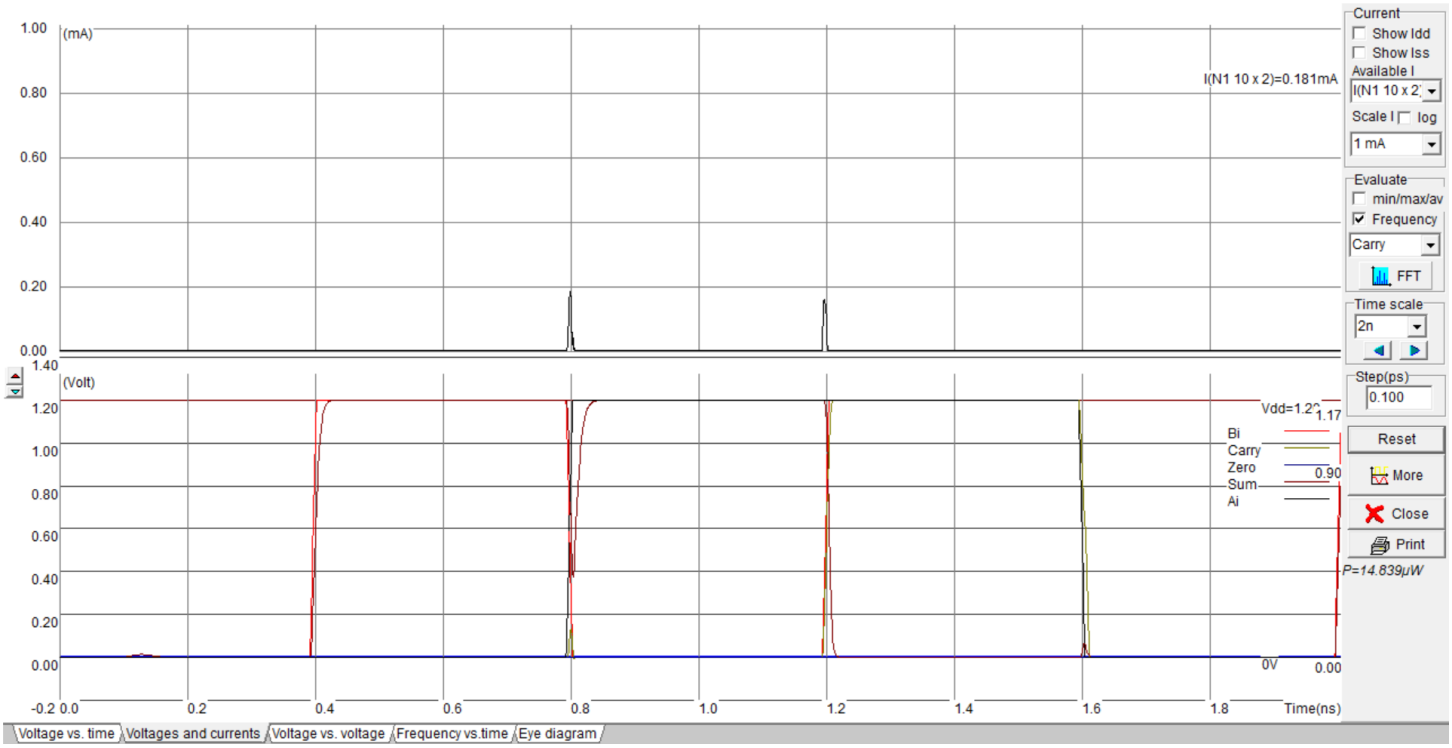

File View Edit Simulate Compile Analysis Help
5 lambda.
0.250µm
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Vss-
Vss-
Vss-
Bi
Al
Sum
Carry
Zero-
Saved 208 boxes in "F:\PART-B\Microwind 3.1 Full\rules\HALF_ADDER.MSK"
Bi
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

WAVEFORMS

1. V vs T Waveform



V out, I out Waveform




**Conclusions:**

Thus, we have:

1) Drawn the LAYOUT for Half adder by using an EX-OR gate and an AND gate constructed by Multiplexers in 90 nm Foundry.
2) Simulated the LAYOUT to observe waveforms.
3) Verified its functionality as per TRUTH-TABLE.