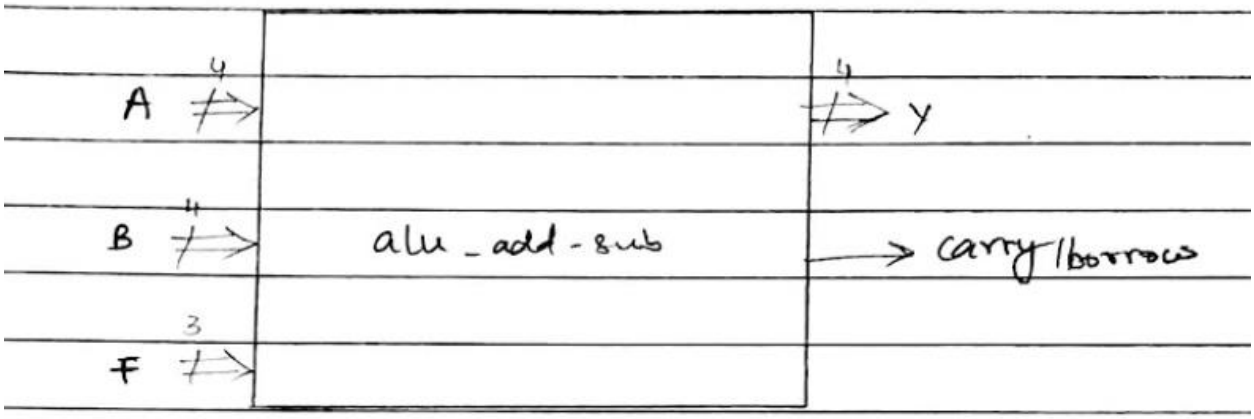
TITLE PAGE

Class	:	BE-08
Roll No.	:	42410
Assignment No.	:	01
Assignment Name	:	4 -bit ALU (Arithmetic Logic Unit)
Date of Performance	:	

Block Diagram:



A, B : 4 bit operands

f : 3 bit function bus

Y : 4 bit sum / difference logic O/P

carry_borrow : carry or borrow

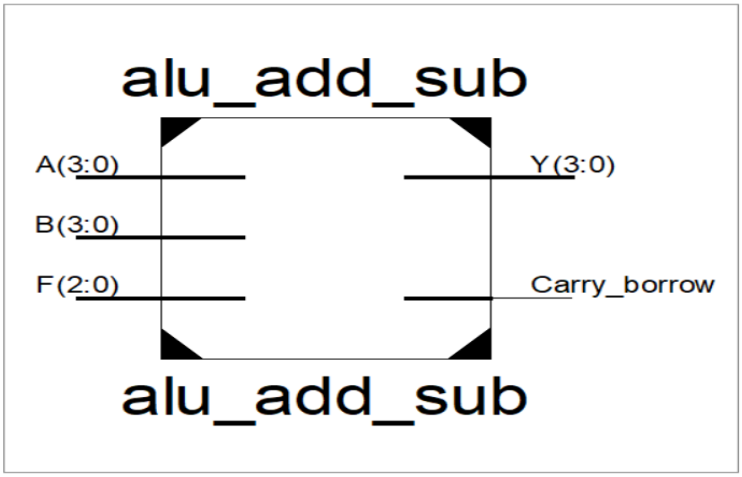
Truth Table:

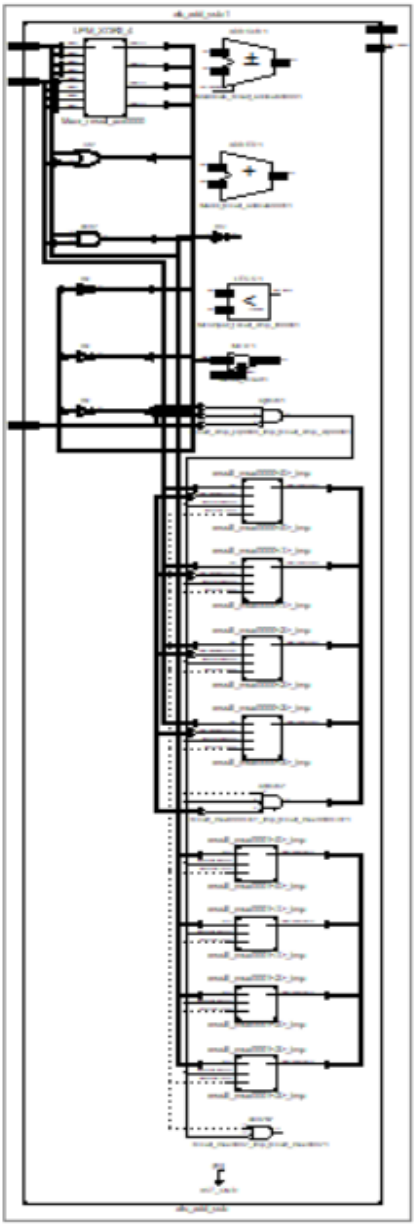
function Bus			operations
f(2)	f(1)	f(0)	
0	0	0	$A \cdot B$
0	0	1	$\overline{A \cdot B}$
0	1	0	$A+B$
0	1	1	$\overline{A+B}$
1	0	0	$A \oplus B$
1	0	1	$\overline{A \oplus B}$
1	1	0	A add B
1	1	1	A − B

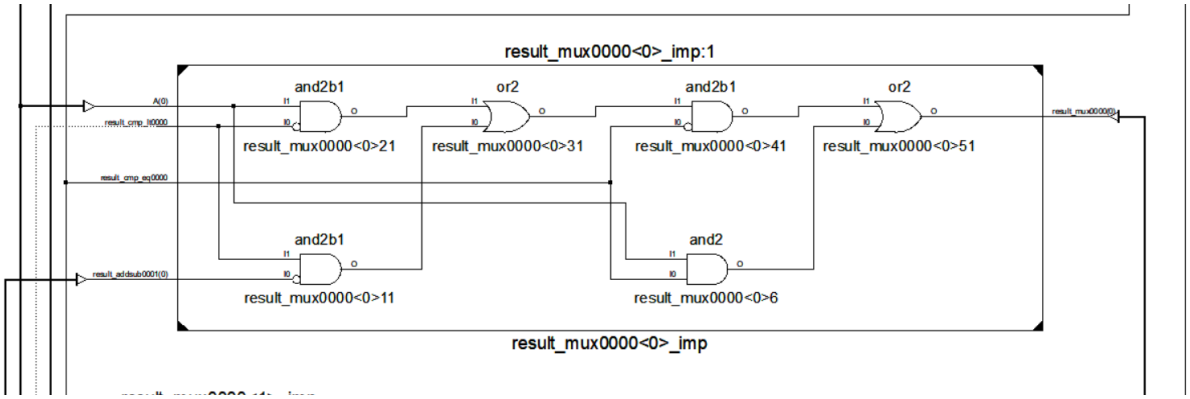
MAIN VHDL PROGRAM

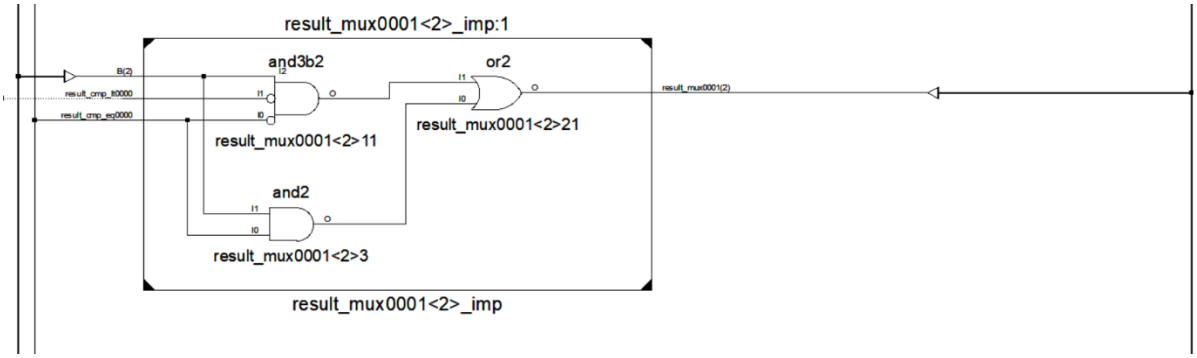
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
use IEEE.NUMERIC_STD.ALL;

entity alu_add_sub is
   Port ( A : in  STD_LOGIC_VECTOR (3 downto 0);
        B : in  STD_LOGIC_VECTOR (3 downto 0);
        F : in  STD_LOGIC_VECTOR (2 downto 0);
                        Carry_borrow : out STD_LOGIC;
        Y : out  STD_LOGIC_VECTOR (3 downto 0));
end alu_add_sub;

architecture alu_add_sub_arch of alu_add_sub is
signal result: std_logic_vector(4 downto 0):="00000";
begin
                PROCESS(A,B,F)
                        BEGIN
                                CASE F IS
                                        WHEN "000" =>
                                                result <= '0' & (A AND B);
                                        WHEN "001" =>
                                                result <= '0' & (A NAND B);
                                        WHEN "010" =>
                                                result <= '0' & (A OR B);
                                        WHEN "011" =>
                                                result <='0' & (A NOR B);
                                        WHEN "100" =>
                                                result <= '0' & (A XOR B);
                                        WHEN "101" =>
                                                result <= '0' & (A XNOR B);
                                        WHEN "110" =>
                                                result<=('0'& A )+('0'& B );
                                        WHEN  OTHERS =>
                                                if a<b then
                                                        result<=not(('0'& A)+('0' & not(B)+1))+1;
                                                else
                                                        result<=('0'& A )-('0'& B );
                                                end if;
                                END CASE;
                END PROCESS;

                                Y <= result(3 downto 0);
                Carry_borrow <= result(4);
end alu_add_sub_arch;
```

RTL SCHEMATIC

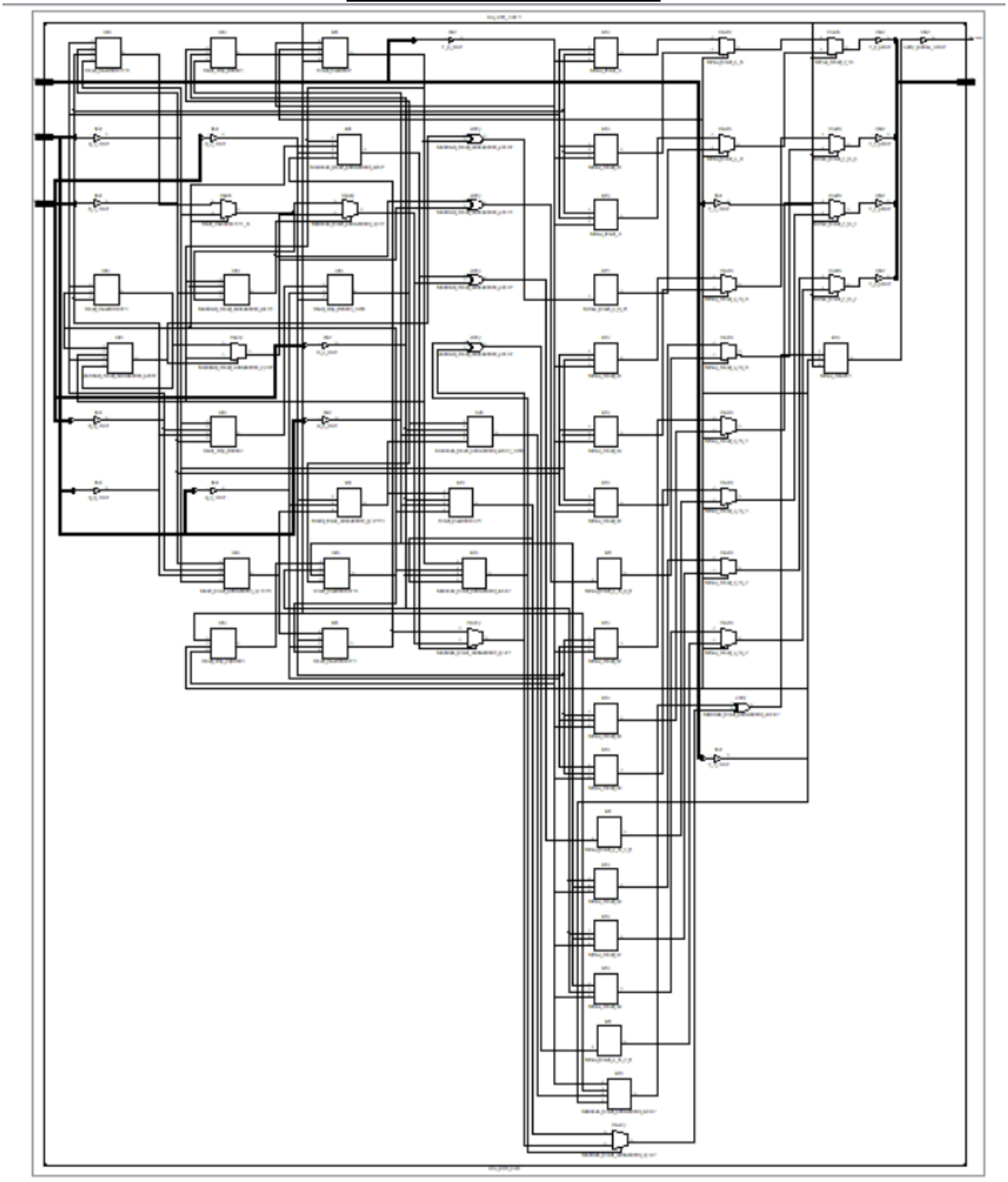


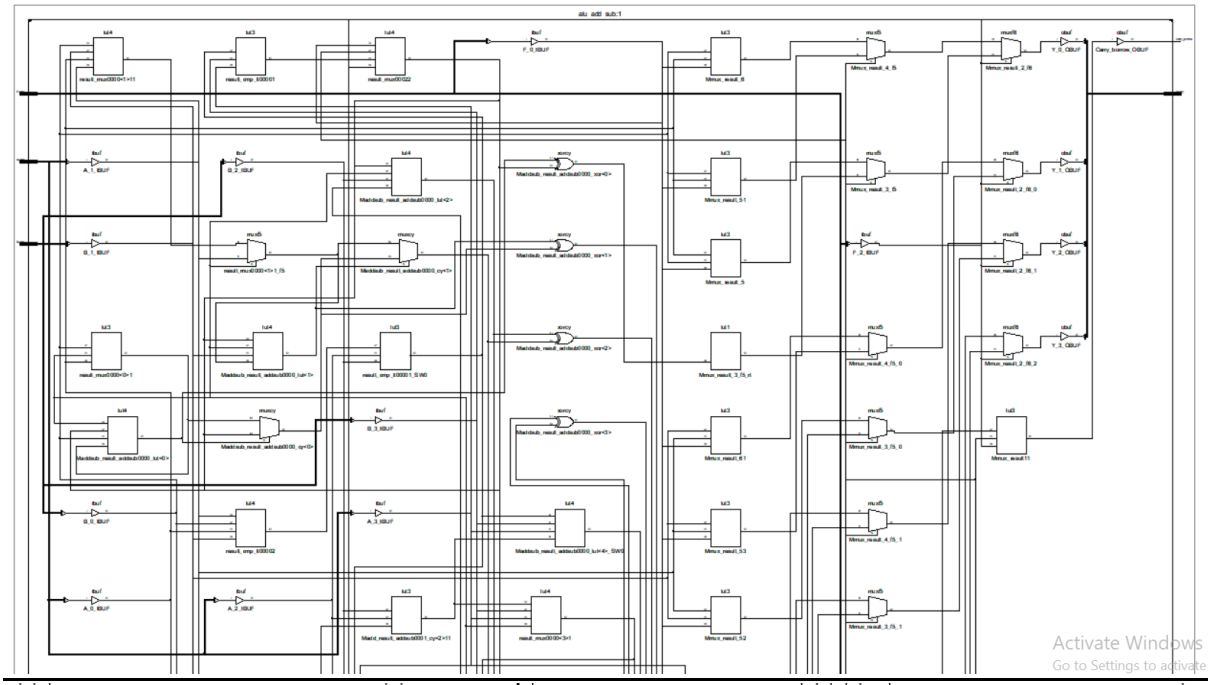


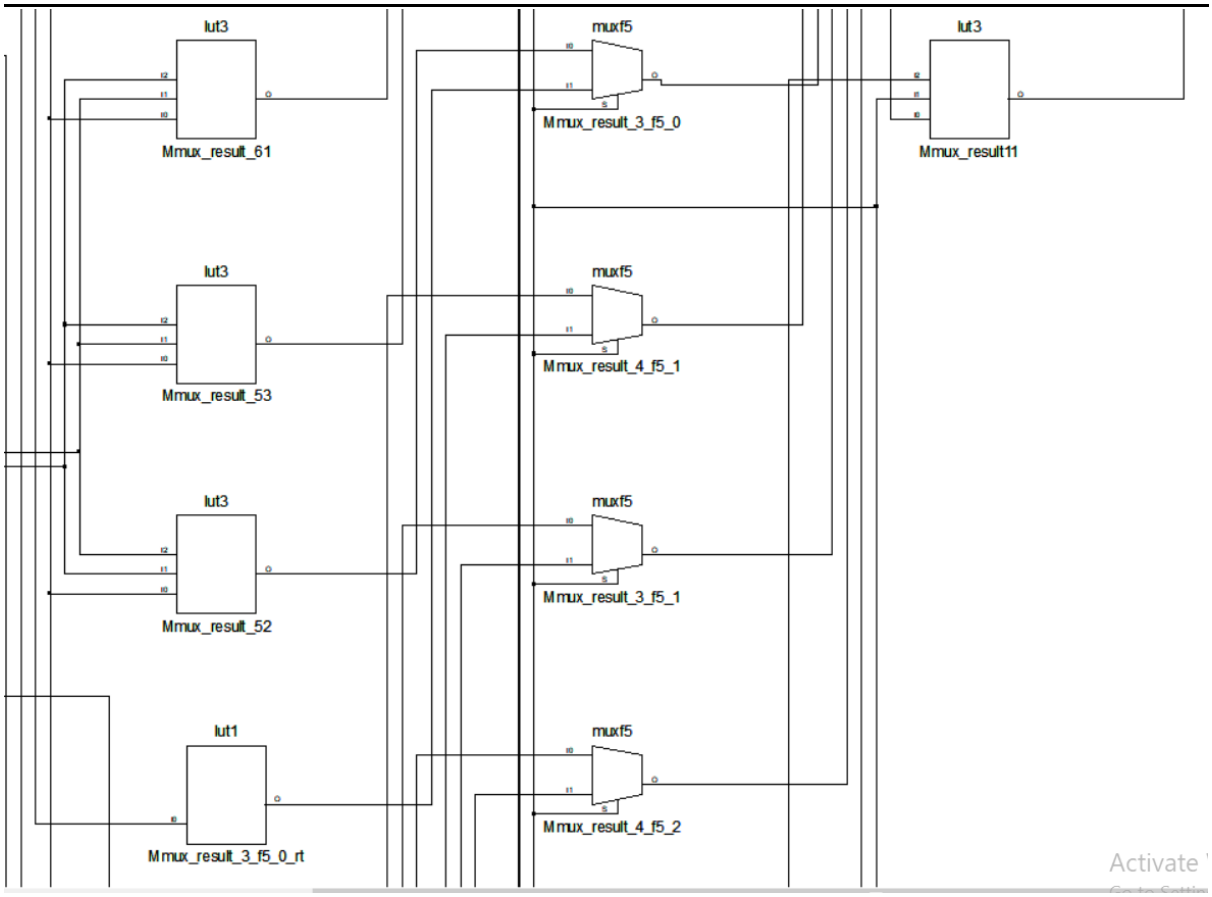

result_mux0000<0>_imp:1
and2b1
or2
and2b1
or2
A(0)
result_cmp_lt0000
result_cmp_eq0000
result_addsub0001(0)
result_mux0000<0>21
result_mux0000<0>31
result_mux0000<0>41
result_mux0000<0>51
result_mux0000(0)
and2b1
and2
result_mux0000<0>11
result_mux0000<0>6
result_mux0000<0>_imp


result_mux0001<2>_imp:1
and3b2
or2
B(2)
result_cmp_lt0000
result_cmp_eq0000
result_mux0001(2)
result_mux0001<2>11
result_mux0001<2>21
and2
result_mux0001<2>3
result_mux0001<2>_imp

TECHNOLOGY SCHEMATIC




alu_add_sub:1


lut3
Mmux_result_61
muxf5
Mmux_result_3_f5_0
lut3
Mmux_result11
lut3
Mmux_result_53
muxf5
Mmux_result_4_f5_1
lut3
Mmux_result_52
muxf5
Mmux_result_3_f5_1
lut1
Mmux_result_3_f5_0_rt
muxf5
Mmux_result_4_f5_2

SYNTHESIS REPORT

a) Device Utilisation Summary

```
=========================================================================
*                  Final Report                         *
=========================================================================
Final Results
RTL Top Level Output File Name     : alu_add_sub.ngr
Top Level Output File Name         : alu_add_sub
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 16

Cell Usage :
# BELS                             : 57
#      LUT1                        : 4
#      LUT3                        : 18
#      LUT4                        : 13
#      MUXCY                       : 4
#      MUXF5                       : 9
#      MUXF6                       : 4
#      XORCY                       : 5
# IO Buffers                       : 16
#      IBUF                        : 11
#      OBUF                        : 5
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                 19  out of   2448     0%
 Number of 4 input LUTs:           35  out of   4896     0%
 Number of IOs:                    16
 Number of bonded IOBs:            16  out of    158    10%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

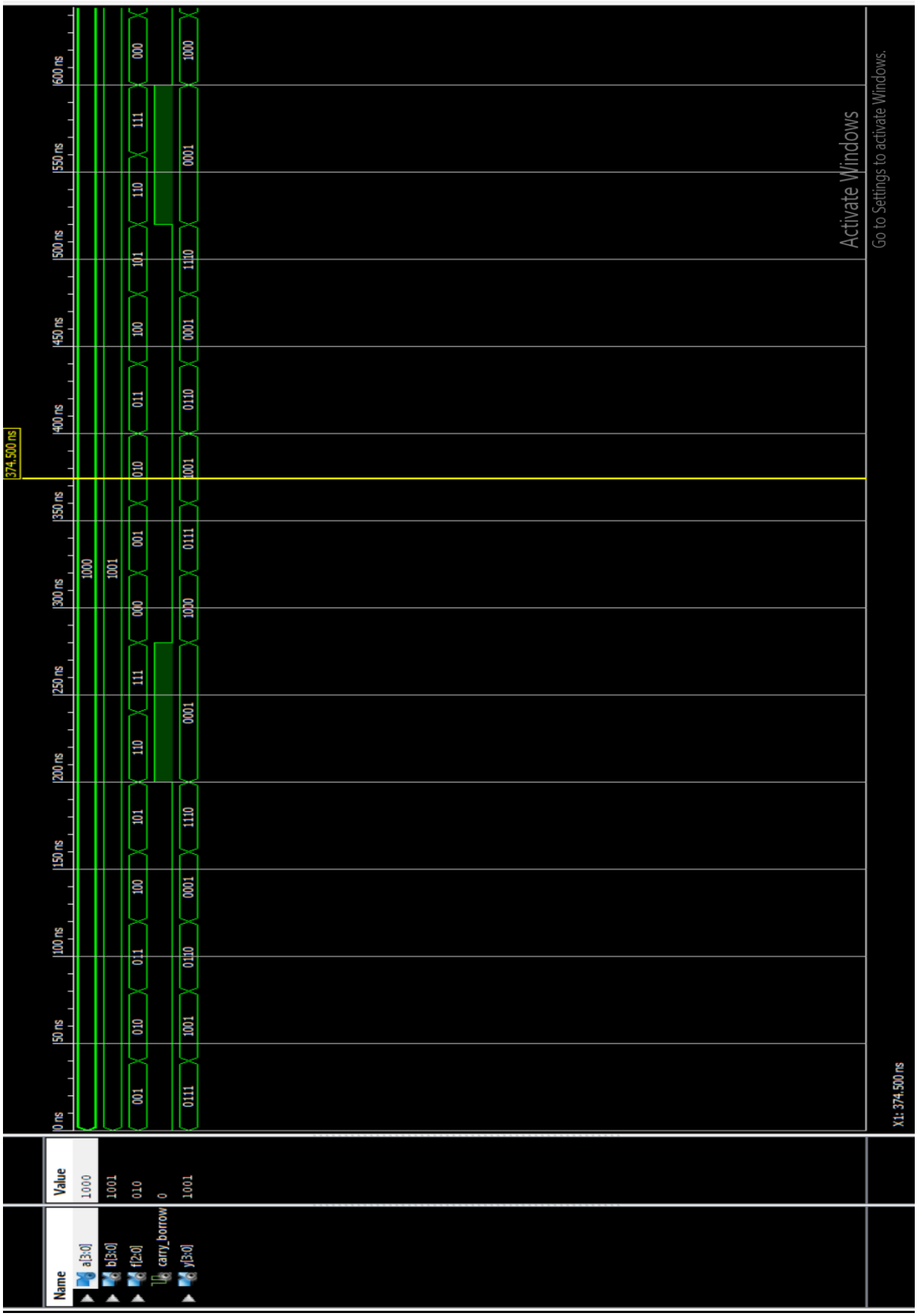
b) Timing Report

```
=========================================================================
====
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 13.714ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

TESTBENCH PROGRAM

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use ieee.std_logic_unsigned.all;

ENTITY alu_add_sub_tb IS
END alu_add_sub_tb;

ARCHITECTURE alu_add_sub_arch OF alu_add_sub_tb IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT alu_add_sub
PORT(
A : IN  std_logic_vector(3 downto 0);
B : IN  std_logic_vector(3 downto 0);
F : IN  std_logic_vector(2 downto 0);
Carry_borrow : OUT  std_logic;
Y : OUT  std_logic_vector(3 downto 0)
);
END COMPONENT;

--Inputs
signal A : std_logic_vector(3 downto 0) := "1000";
signal B : std_logic_vector(3 downto 0) := "1001";
signal F : std_logic_vector(2 downto 0) := (others => '0');

--Outputs
signal Carry_borrow : std_logic;
signal Y : std_logic_vector(3 downto 0);
-- No clocks detected in port list. Replace <clock> below with
-- appropriate port name
BEGIN
-- Instantiate the Unit Under Test (UUT)
uut: alu_add_sub PORT MAP (
A => A,
B => B,
F => F,
Carry_borrow => Carry_borrow,
Y => Y
);
stim_proc: process
begin
F <= F+1;
wait for 40 ns;
end process;

END;
```

ISIM WAVEFORMS



UCF FILE

```
# PlanAhead Generated physical constraints

NET "A[3]" LOC = P205;
NET "A[2]" LOC = P206;
NET "A[1]" LOC = P203;
NET "A[0]" LOC = P200;
NET "B[3]" LOC = P192;
NET "B[2]" LOC = P193;
NET "B[1]" LOC = P189;
NET "B[0]" LOC = P190;
NET "F[2]" LOC = P179;
NET "F[1]" LOC = P180;
NET "F[0]" LOC = P177;
NET "Y[3]" LOC = P165;
NET "Y[2]" LOC = P167;
NET "Y[1]" LOC = P163;
NET "Y[0]" LOC = P164;
```

CONCLUSION:

Thus, we have:

1)Modelled 4-Bit ALU Interfacing using Behavioural Modelling Style.
2)Observed following Schematics: **RTL & Technology Schematics** generated **Post-Synthesis.**
3)Interpreted **Device Utilisation Summary** in terms of LUTs , SLICES , IOBs , Multiplexers & D FFs used out of the available device resources.
4)Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
5)Written a TESTBENCH to verify the functionality of 4-Bit ALU Interfacing & verified the functionality as per the TRUTH-TABLE, by observing ISIM Waveforms.
6)Used PlanAhead Editor for pin-locking.
7)Prototyped the FPGA **XC3S250EPQ208-5** to realize 4-Bit ALU Interfacing & verified its operation by giving suitable input combinations.