Class	:	BE - 8
Roll. No	:	42410
Assignment No.	:	B.1 (b, c)
Assignment Name	:	CMOS NAND and AND Gate
Date of Performance	:	12-11-2020

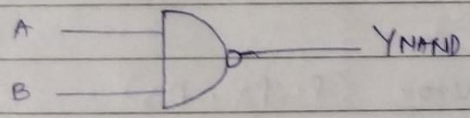
(1.b) CMOS 2i/p NAND Gate

(1.c) CMOS 2i/p AND Gate

F = 90nm

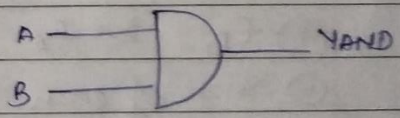
SYMBOLS: —

2i/p NAND GATE:



$Y_{NAND} = \overline{A \cdot B}$

2i/p AND GATE:



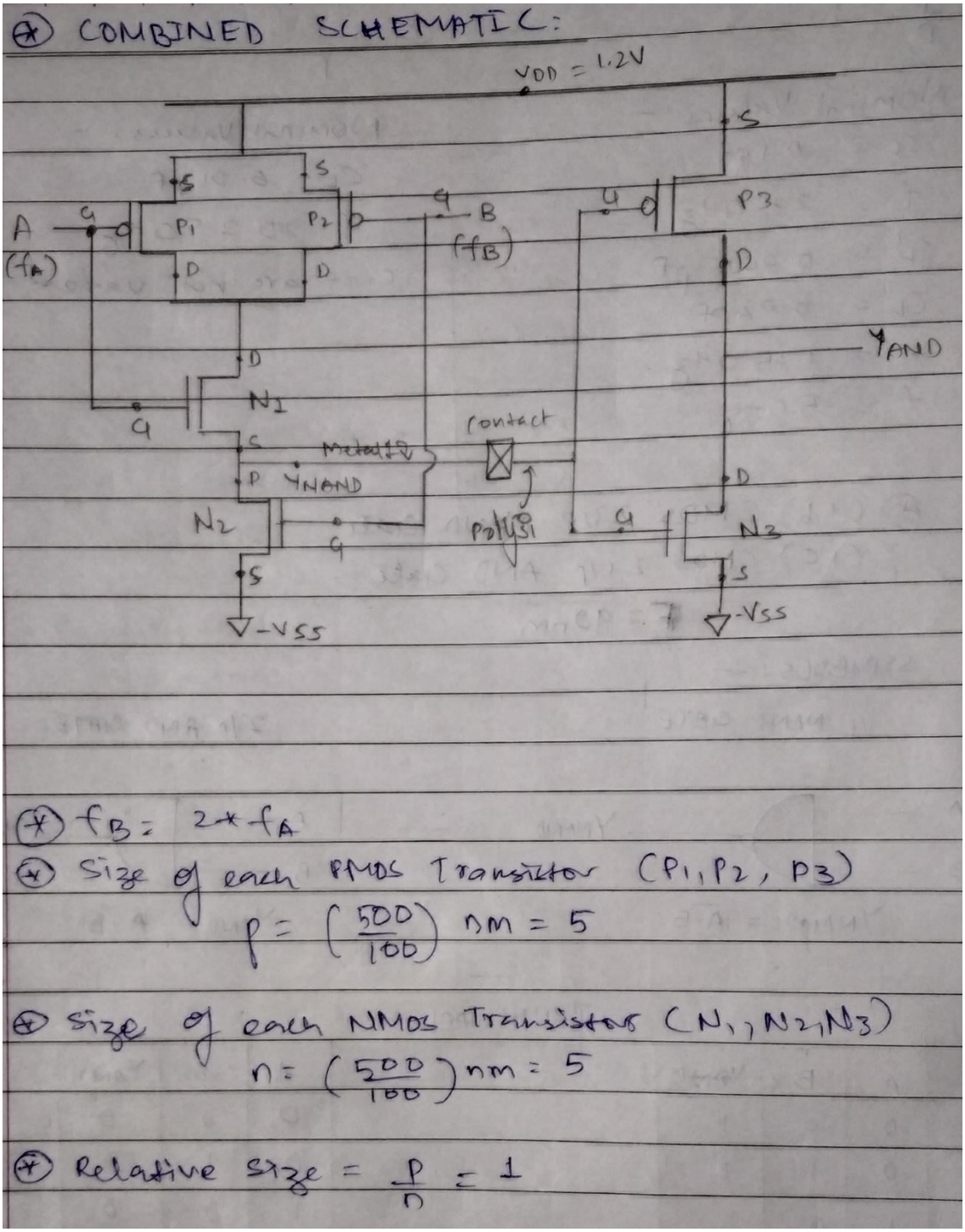
$Y_{AND} = A \cdot B$

TRUTH TABLES

A	B	YNAND
0	0	1
0	1	1
1	0	1
1	1	0

A	B	YAND
0	0	0
0	1	0
1	0	0
1	1	1

Block Diagram



* $f_B = 2 * f_A$
* Size of each PMOS Transistor (P_1, P_2, P_3)

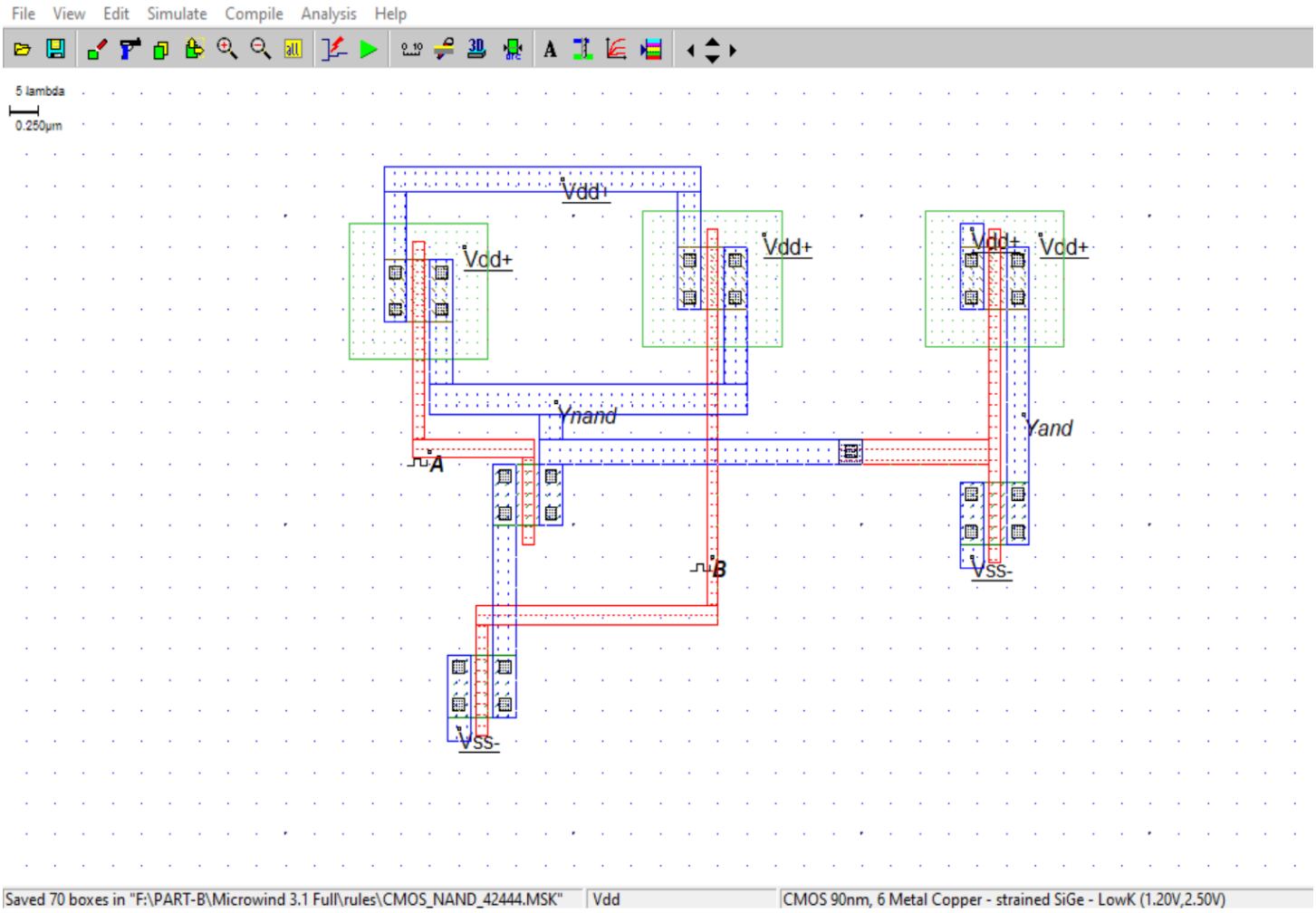
$$p = \left(\frac{500}{100}\right) nm = 5$$

* Size of each NMOS Transistor (N_1, N_2, N_3)

$$n = \left(\frac{500}{100}\right) nm = 5$$

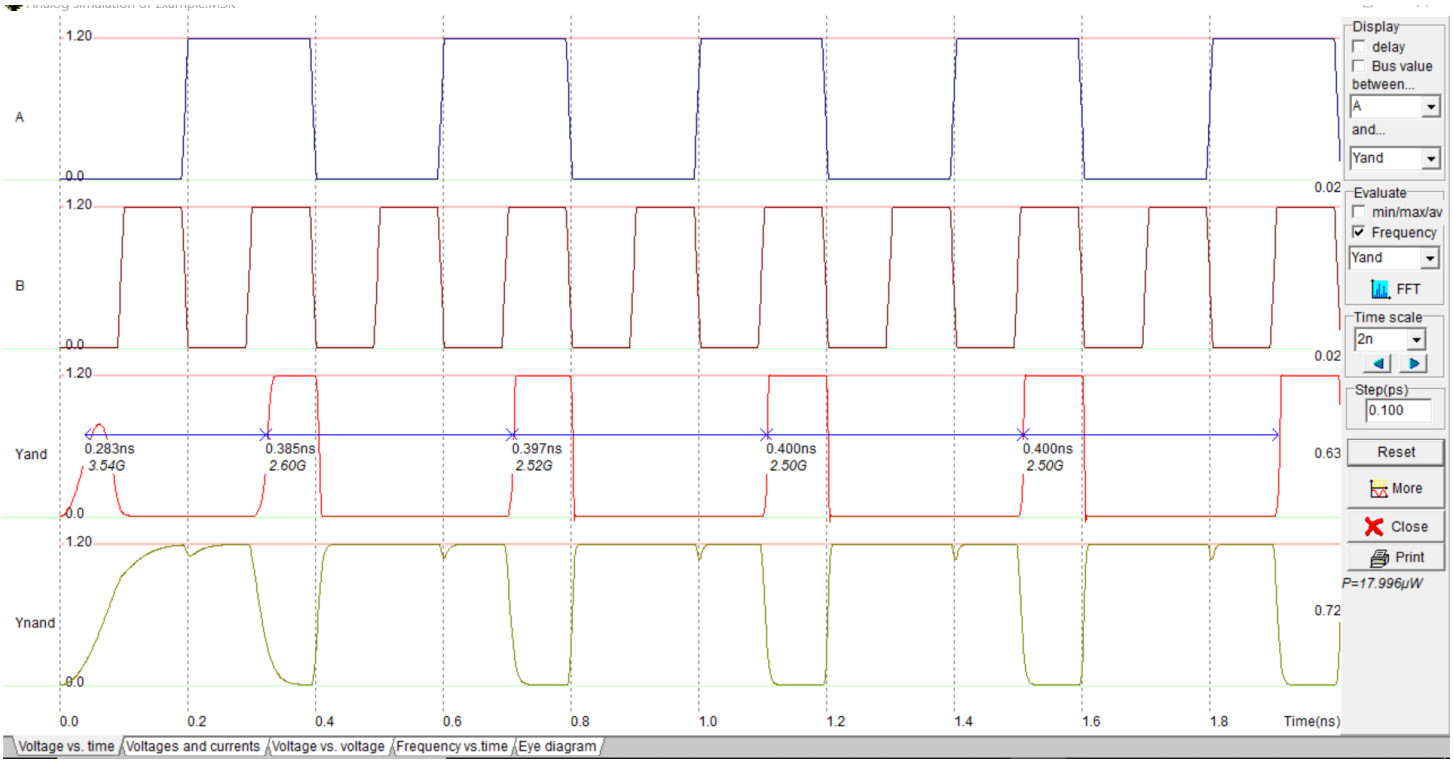
* Relative size $= \frac{p}{n} = 1$

LAYOUT


File View Edit Simulate Compile Analysis Help
5 lambda
0.250µm
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Ynand
Yand
A
B
Vss-
Vss-
Saved 70 boxes in "F:\PART-B\Microwind 3.1 Full\rules\CMOS_NAND_42444.MSK"
Vdd
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

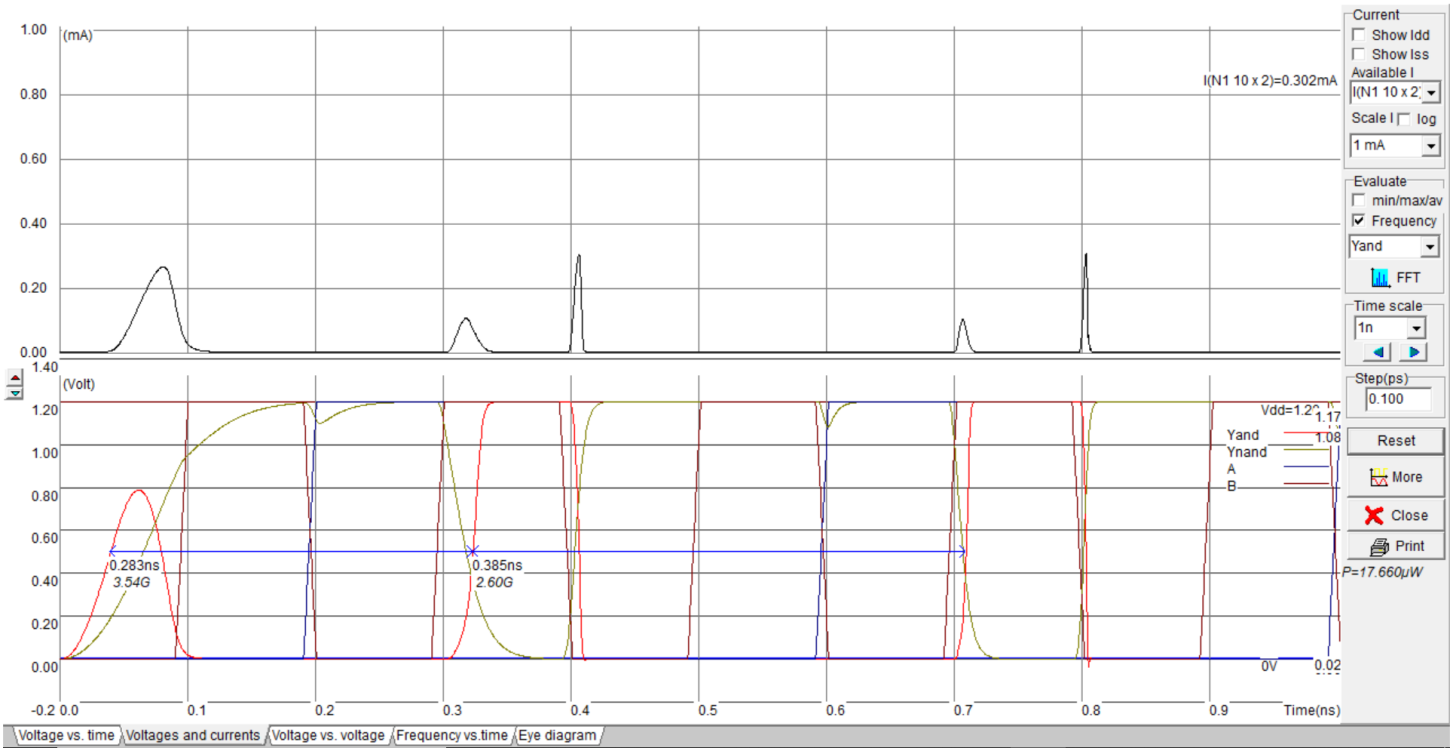
WAVEFORMS

1. V vs T Waveform



SR.NO.	PARAMETER	VALUE
1)	$P_{dynamic}$	17.996 µW
2)	f_{max}	2.5 GHz

2. V out, I out Waveform



SR.NO.	PARAMETER	VALUE
1)	$P_{dynamic}$	17.660 µW
2)	f_{max}	2.5 GHz

Conclusions:

Thus, we have:

1) Drawn the LAYOUT for CMOS NAND and AND Gate using 90 nm Foundry.
2) Simulated the LAYOUT to observe waveforms.
3) Verified its functionality as per TRUTH-TABLE.
4) Noted the values of $P_{dynamic}$ and f_{max}.