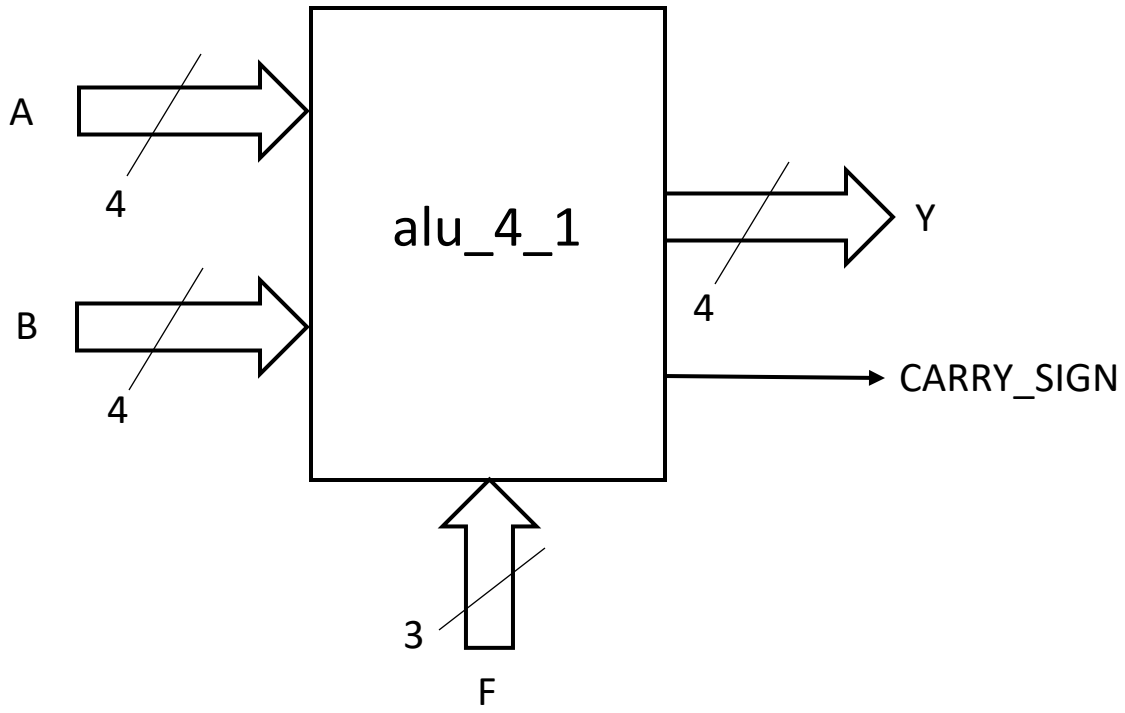
TITLE PAGE

Class	:	BE - 8
Roll. No	:	42428
Assignment No.	:	A. 1
Assignment Name	:	4-bit ALU
Date Of Performance	:	5-9-2020 to 19-9-2020

Block Diagram:



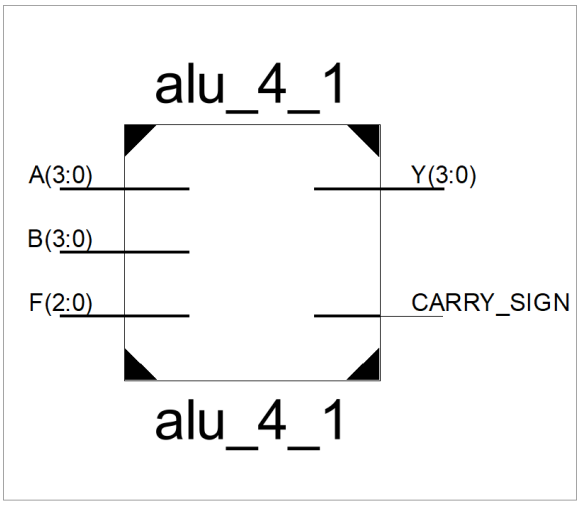
Truth-Table : A = 1010 B = 1100

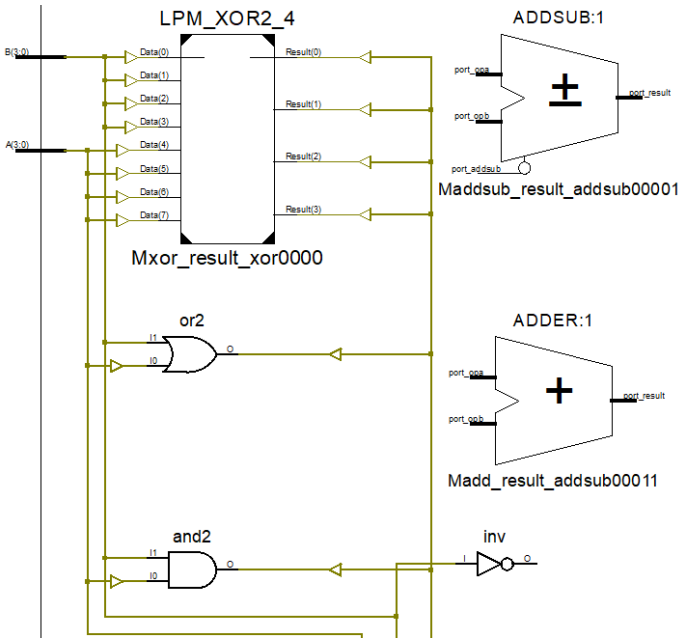
F	Y	Y_{exp}	CARRY_SIGN
000	A . B	1000	0
001	$\overline{A . B}$	0111	0
010	A + B	1110	0
011	$\overline{A + B}$	0001	0
100	A⊕B	0110	0
101	$\overline{A \oplus B}$	1001	0
110	A add B	0110	1
111	A - B	0010	1

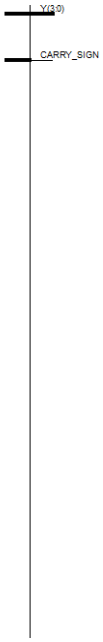
MAIN VHDL PROGRAM

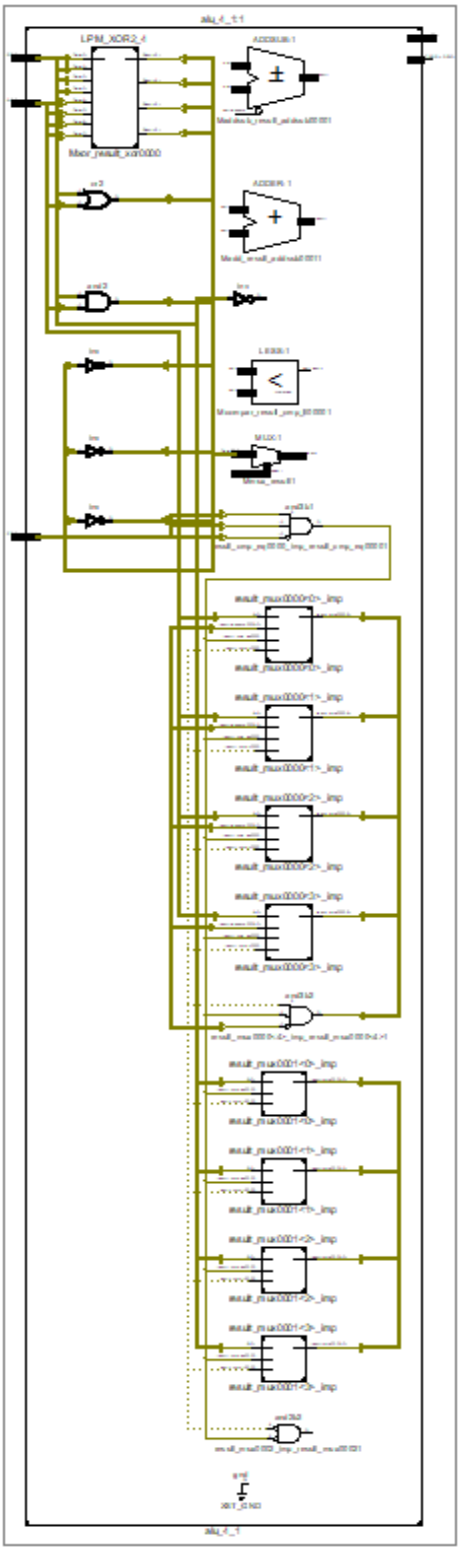
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity alu_4_1 is
   Port (
                A : in  STD_LOGIC_VECTOR (3 downto 0);
                B : in  STD_LOGIC_VECTOR (3 downto 0);
                F : in  STD_LOGIC_VECTOR (2 downto 0);
                Y : out  STD_LOGIC_VECTOR (3 downto 0);
                CARRY_SIGN : out  STD_LOGIC
        );
end alu_4_1;

architecture alu_4_1_arch of alu_4_1 is
        signal result: STD_LOGIC_VECTOR(4 DOWNTO 0):="00000";
begin
        process(A,B,F)
        begin
                case F is
                        when "000" =>
                                result<= '0' & (A AND B);
                        when "001" =>
                                result<= '0' & (A NAND B);
                        when "010" =>
                                result<= '0' & (A OR B);
                        when "011" =>
                                result<= '0' & (A NOR B);
                        when "100" =>
                                result<= '0' & (A XOR B);
                        when "101" =>
                                result<= '0' & (A XNOR B);
                        when "110" =>
                                result<= ('0' & A)+('0' & B);
                        when others =>
                                IF A < B THEN
                                        result<= (NOT(('0' & A) + ('0' &(NOT B)) + 1))+1;
                                ELSE
                                        result <= ('0' & A)-('0' & B);
                                END IF;
                end case;

        end process;

                Y <= result(3 downto 0);
                CARRY_SIGN <= result(4);
end alu_4_1_arch;
```

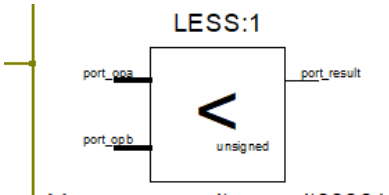
RTL SCHEMATIC

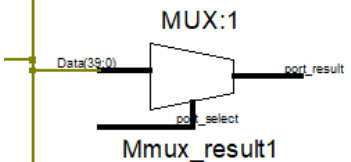


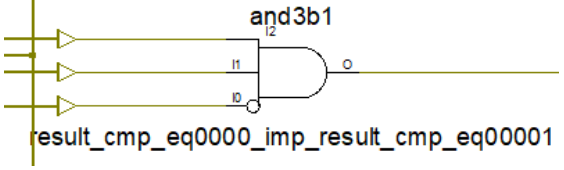


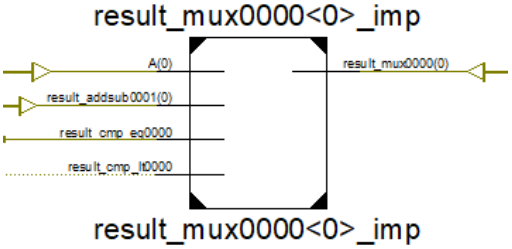




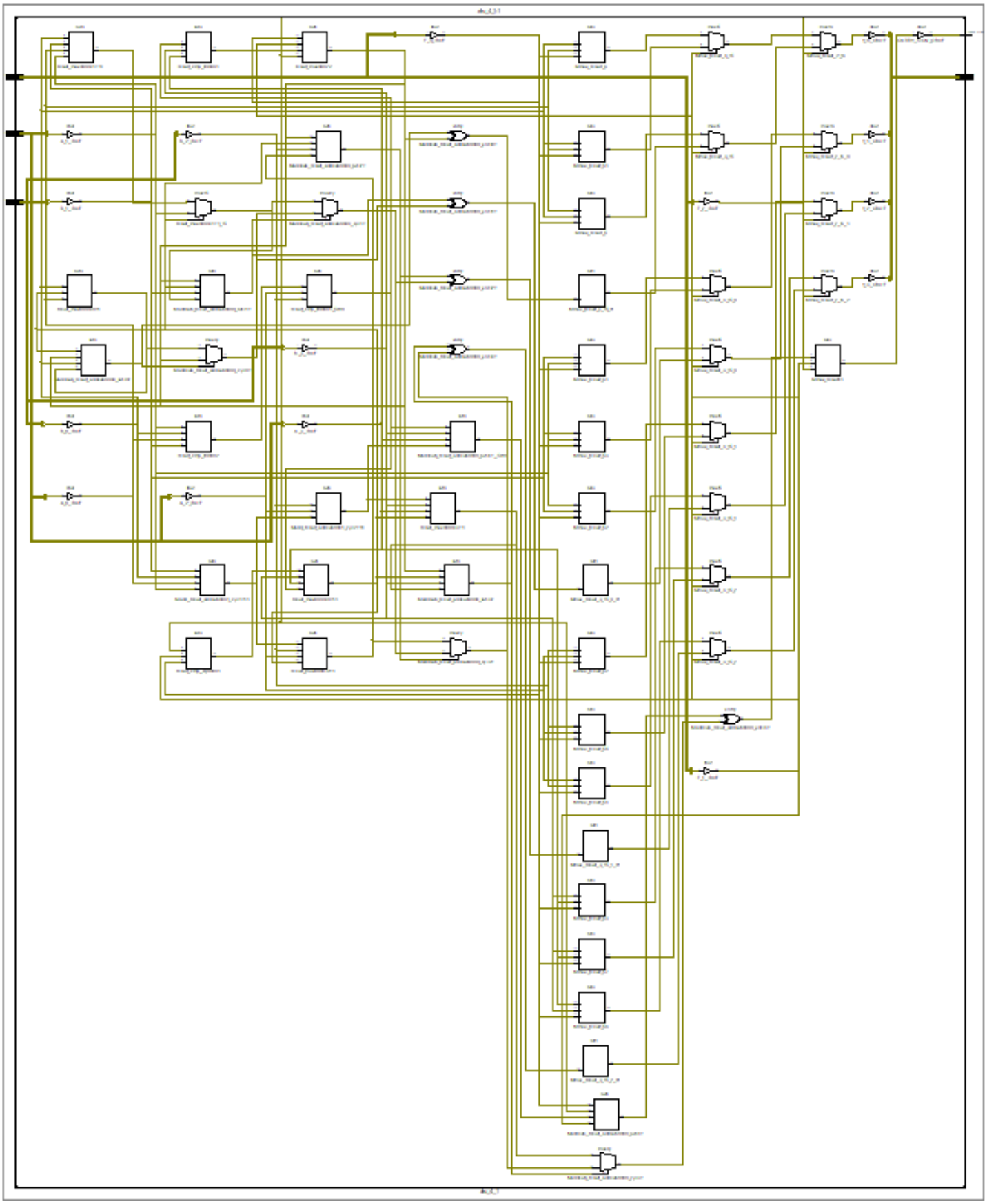


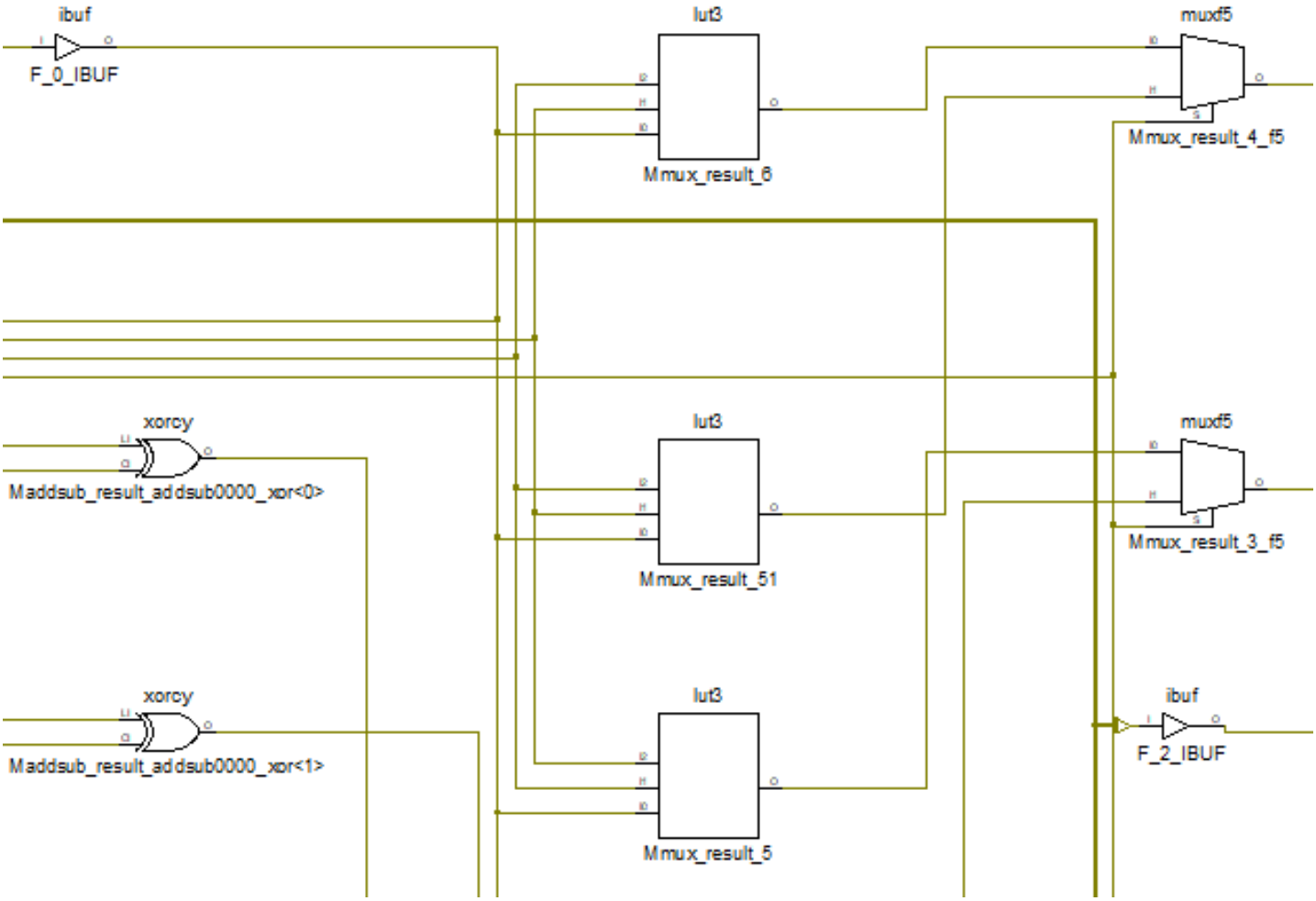






TECHNOLOGY SCHEMATIC




ibuf
F_0_IBUF
lut3
Mmux_result_6
muxf5
Mmux_result_4_f5
xorcy
Maddsub_result_addsub0000_xor<0>
lut3
Mmux_result_51
muxf5
Mmux_result_3_f5
xorcy
Maddsub_result_addsub0000_xor<1>
lut3
Mmux_result_5
ibuf
F_2_IBUF

SYNTHESIS REPORT

1) Device Utilisation Summary

```
=========================================================================
*                      Final Report                     *
=========================================================================
Final Results
RTL Top Level Output File Name     : alu_4_1.ngr
Top Level Output File Name         : alu_4_1
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 16

Cell Usage :
# BELS                             : 57
#      LUT1                        : 4
#      LUT3                        : 18
#      LUT4                        : 13
#      MUXCY                       : 4
#      MUXF5                       : 9
#      MUXF6                       : 4
#      XORCY                       : 5
# IO Buffers                       : 16
#      IBUF                        : 11
#      OBUF                        : 5
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                 19  out of   2448     0%
 Number of 4 input LUTs:           35  out of   4896     0%
 Number of IOs:                    16
 Number of bonded IOBs:            16  out of    158    10%
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
```

2) TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -5

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 13.714ns

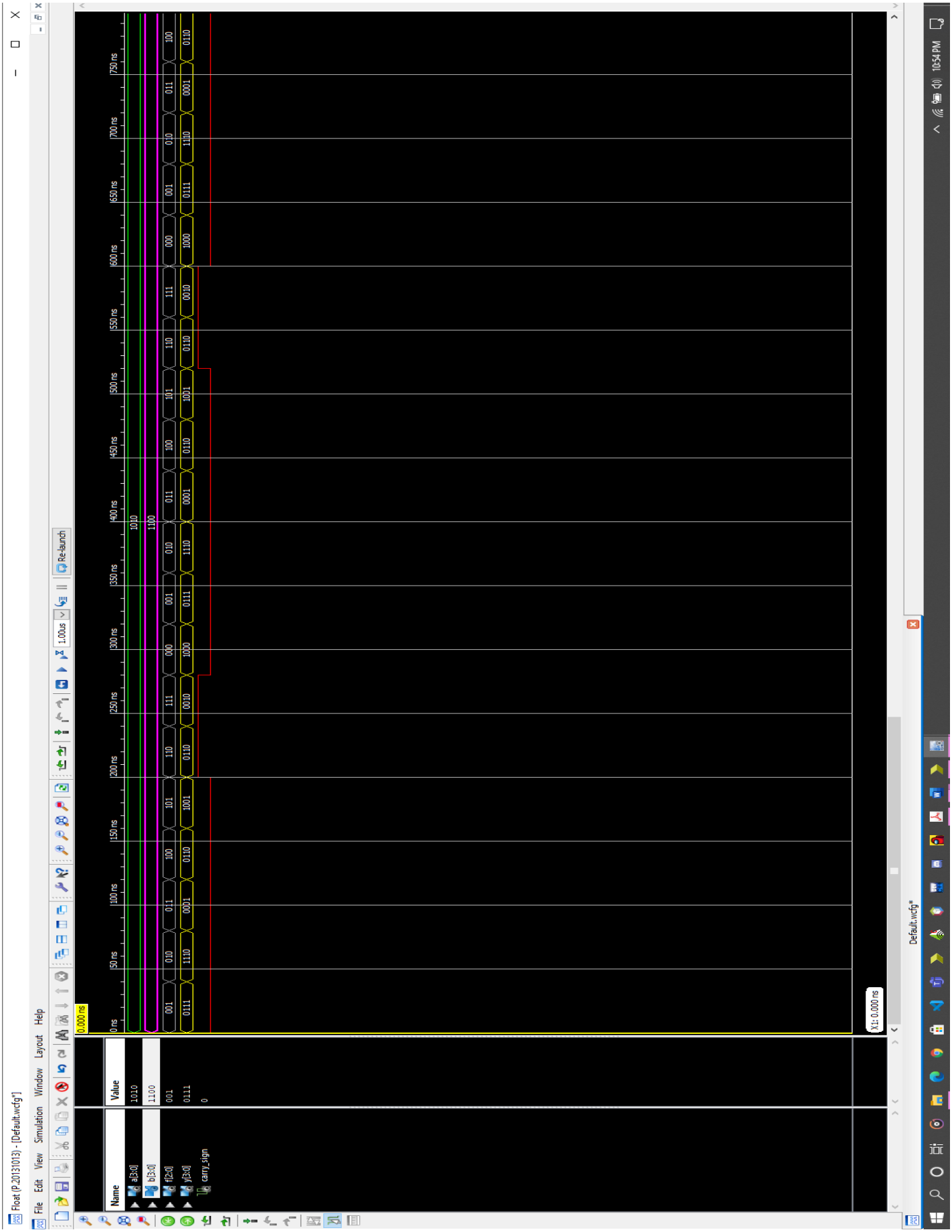
Timing Detail:

All values displayed in nanoseconds (ns)

TESTBENCH PROGRAM

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY alu_4_1_tb IS
END alu_4_1_tb;

ARCHITECTURE behavior OF alu_4_1_tb IS

   -- Component Declaration for the Unit Under Test (UUT)
   COMPONENT alu_4_1
   PORT(
        A : IN  std_logic_vector(3 downto 0);
        B : IN  std_logic_vector(3 downto 0);
        F : IN  std_logic_vector(2 downto 0);
        Y : OUT  std_logic_vector(3 downto 0);
        CARRY_SIGN : OUT  std_logic
       );
   END COMPONENT;

  --Inputs
  signal A : std_logic_vector(3 downto 0) := "1010";
  signal B : std_logic_vector(3 downto 0) := "1100";
  signal F : std_logic_vector(2 downto 0) := (others => '0');

          --Outputs
  signal Y : std_logic_vector(3 downto 0);
  signal CARRY_SIGN : std_logic;
  -- No clocks detected in port list. Replace <clock> below with
  -- appropriate port name

BEGIN

-- Instantiate the Unit Under Test (UUT)
  uut: alu_4_1 PORT MAP (
        A => A,
        B => B,
        F => F,
        Y => Y,
        CARRY_SIGN => CARRY_SIGN
       );

  -- Clock process definitions

  -- Stimulus process
  stim_proc: process
  begin
    F <= F+1;
          WAIT FOR 40 ns;
  end process;
END;
```

ISIM WAVEFORMS



PIN-LOCKING REPORT

PlanAhead Generated physical constraints

NET "A[3]" LOC = P205;

NET "A[2]" LOC = P206;

NET "A[1]" LOC = P203;

NET "A[0]" LOC = P200;

NET "B[3]" LOC = P192;

NET "B[2]" LOC = P193;

NET "B[1]" LOC = P189;

NET "B[0]" LOC = P190;

NET "F[2]" LOC = P179;

NET "F[1]" LOC = P180;

NET "F[0]" LOC = P177;

NET "Y[3]" LOC = P165;

NET "Y[2]" LOC = P167;

NET "Y[1]" LOC = P163;

NET "Y[0]" LOC = P164;

Conclusion:

Thus we have :

1) Modeled a 4-bit ALU using Behavioral Modeling Style.
2) Observed following Schematics: **RTL** & **Technology Schematics** generated **Post-Synthesis**.
3) Interpreted **Device Utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers & D FFs used out of the available device resources.
4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
5) Written a TESTBENCH to verify the functionality of 4-bit ALU & verified the functionality as per the TRUTH-TABLE by observing ISIM Waveforms.
6) Used PlanAhead Editor for pin-locking.
7) Prototyped the FPGA **XC3S250EPQ208-5** to realize 4-bit ALU & verified its operation by giving suitable input combinations.