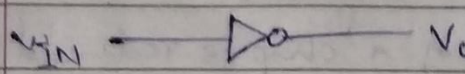
Class	:	BE - 8
Roll. No	:	42410
Assignment No.	:	B.1 a
Assignment Name	:	CMOS Inverter
Date of Performance	:	03-11-2020, 21-11-2020

Assignment 1:-

(1.a) CMOS INVERTER

SYMBOL



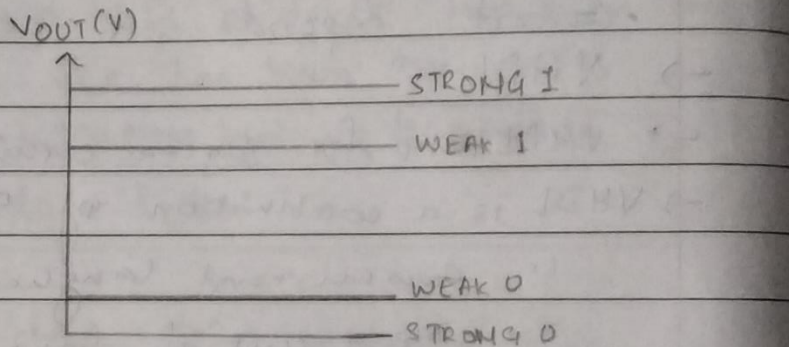
O/P	VALUE of V_{OUT} (V)
STRONG 1	$+V_{DD}$
WEAK-1	$< +V_{DD}$
STRONG 0	$-V_{SS}$ (0)
WEAK-0	> 0

TRUTH TABLE

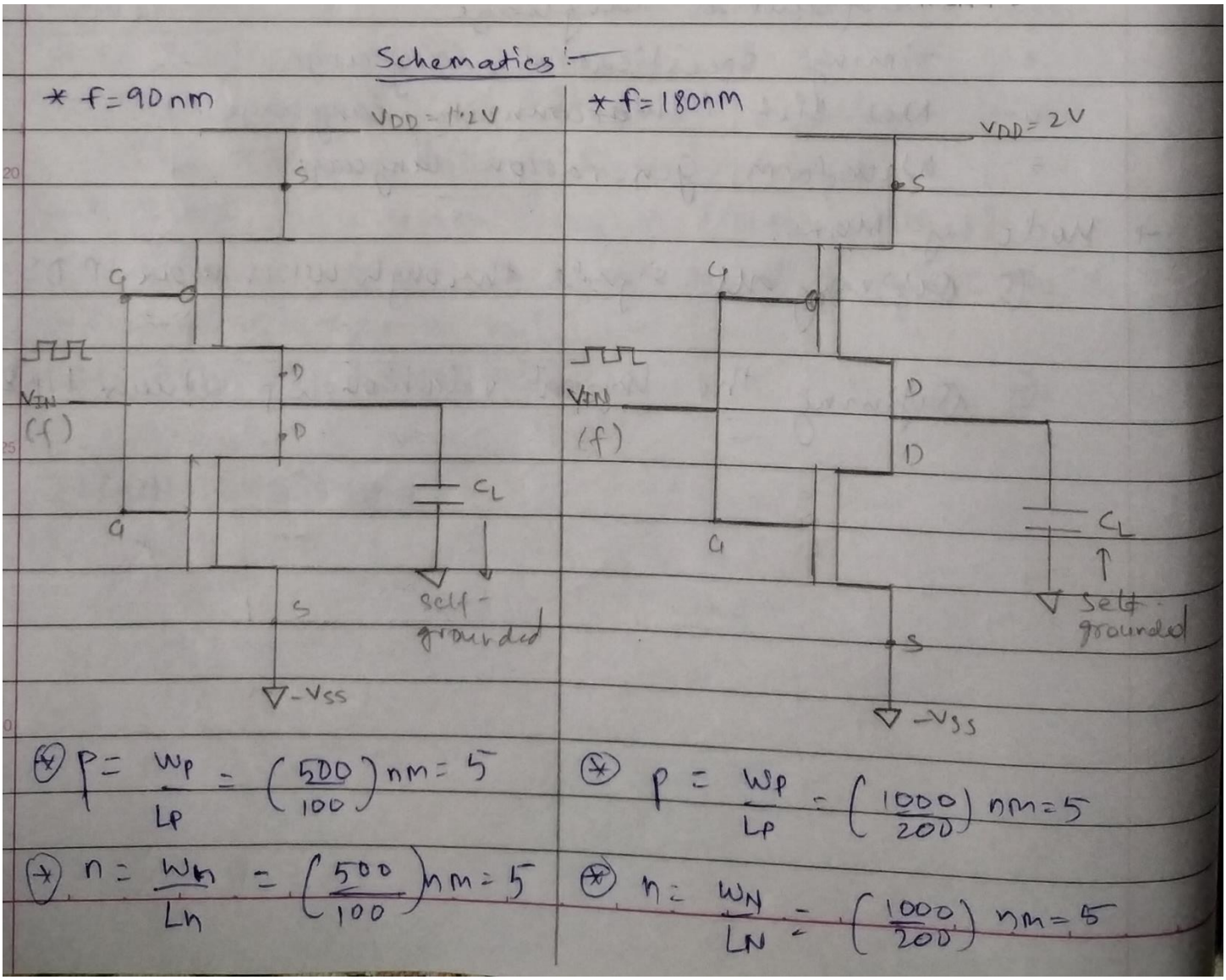
V_{IN}	$V_{OUT} = \overline{V_{IN}}$
0	STRONG-1
1	STRONG-0

* for 90 nm foundary
$V_{DD} = +1.2V$

* $P_{dyn} = C_L (V_{DD})^2 \cdot f$
  - $P_{dyn} \propto C_L$
    $\propto (V_{DD})^2$
    $\propto f$



Block Diagram



(*) $\frac{P}{P} = 1$

(*) Nominal Values :-

$C_L = 0.1\,pf$

$f = 2.5\,GHz$

$C_L' = 0.005\,pf$

$C_L'' = 0.02\,pf$

$f' = 1.25\,GHz$

$f'' = 5\,GHz$

(*) $\frac{P}{P} = 1$

Nominal Values : -

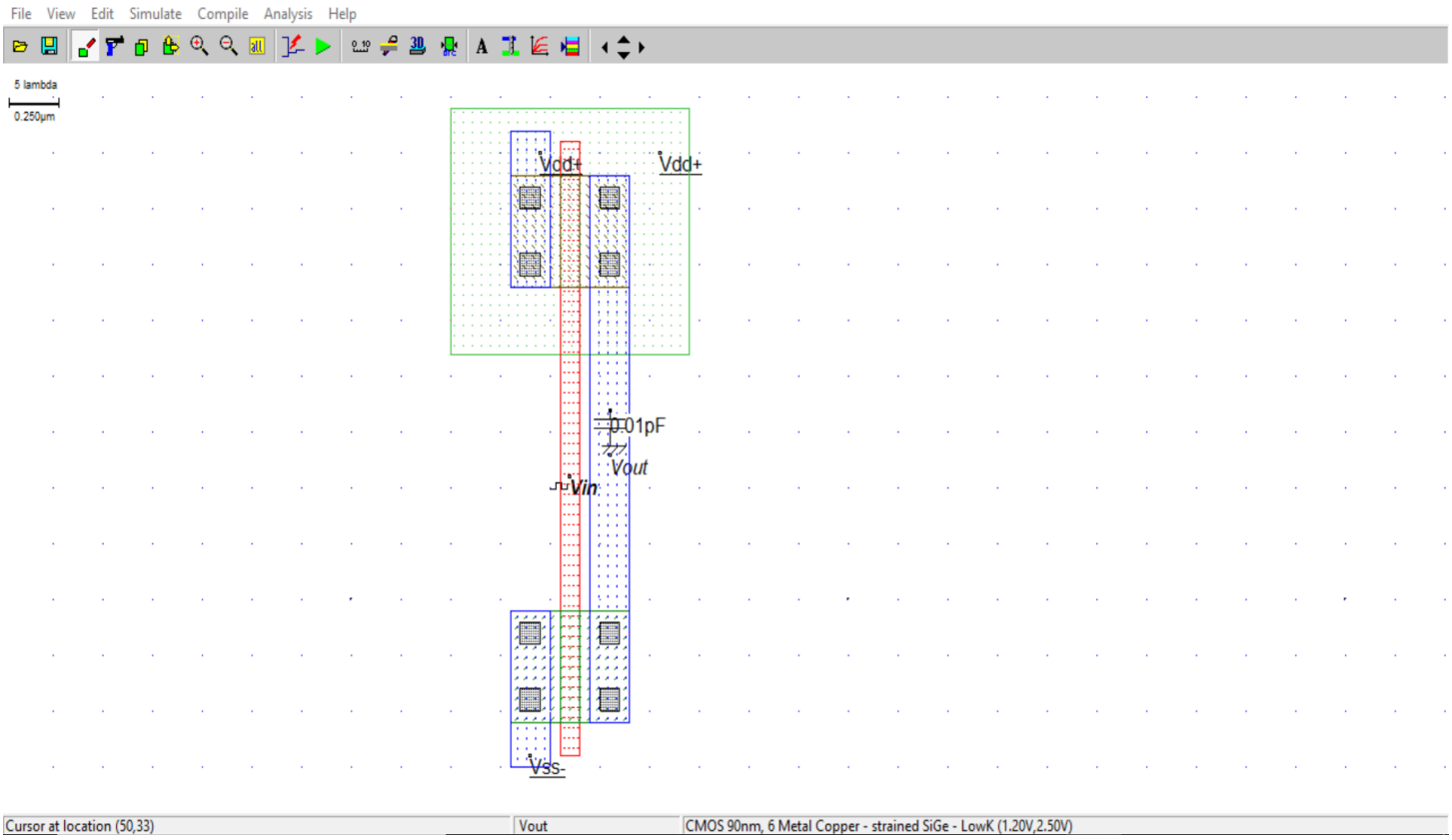
$C_L = 0.01\,pf$

$f = 2.5\,GHz$

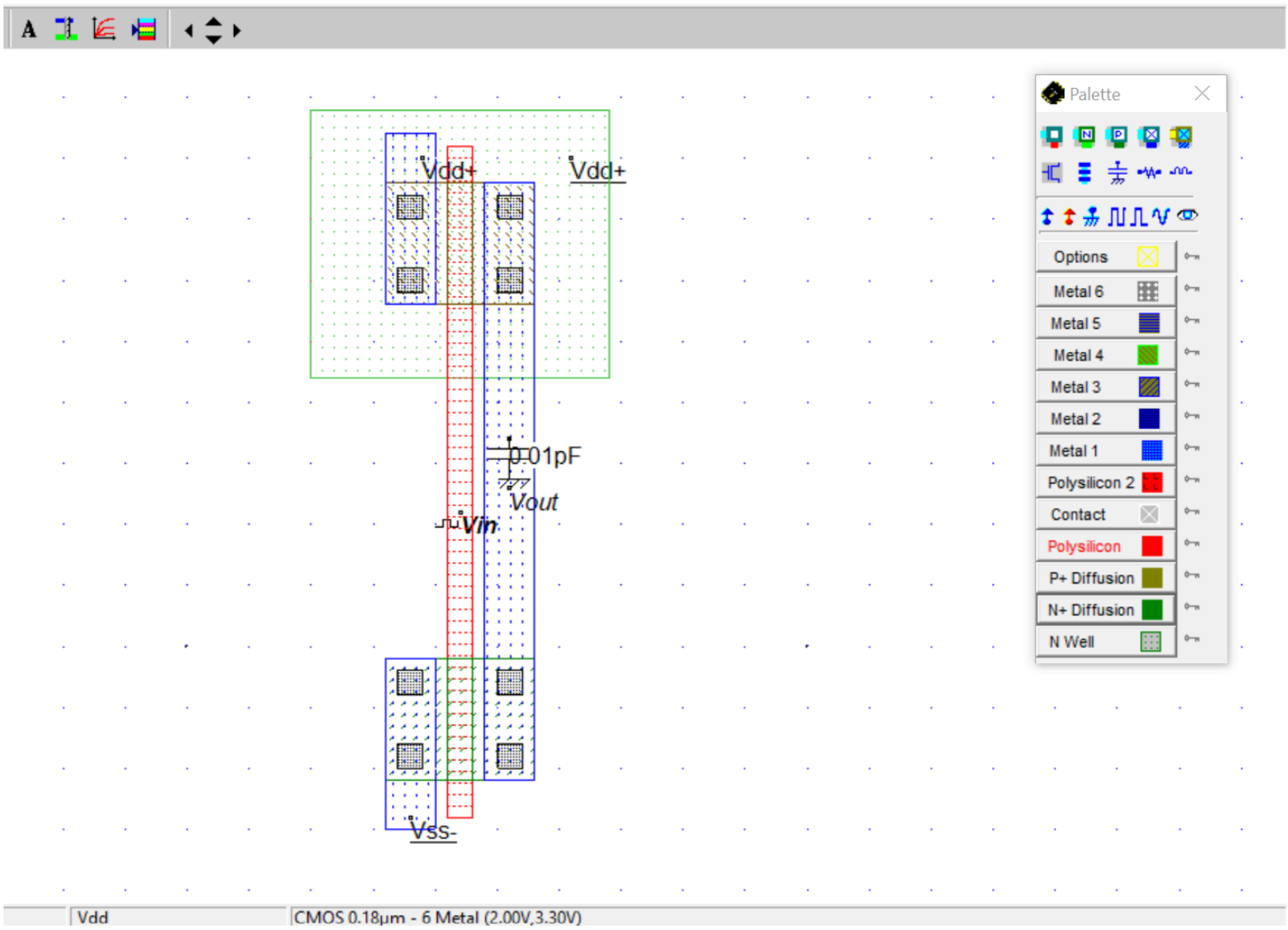
C_L if are not varied

LAYOUT

1) CMOS Inverter with 90nm Foundry

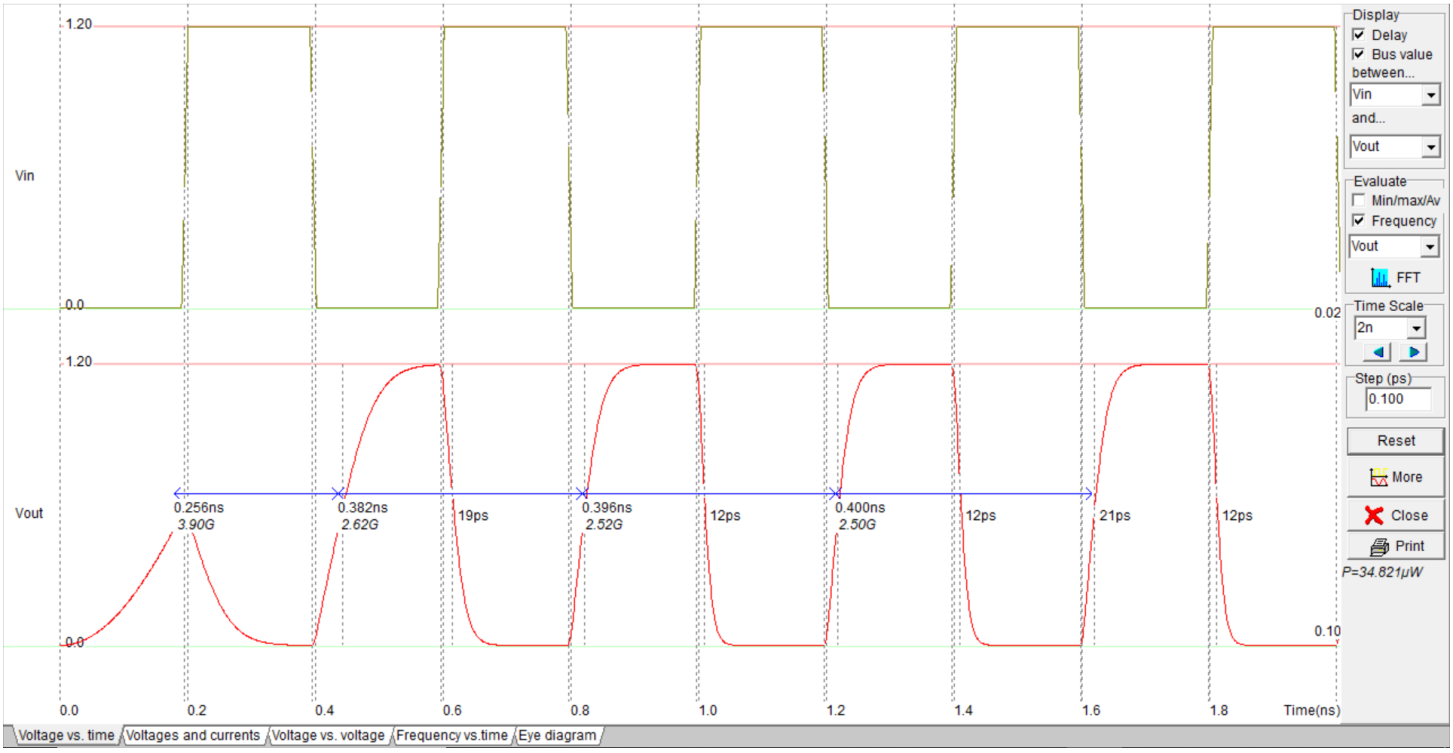


2) CMOS Inverter with 180 nm foundry


Vdd+
Vdd+
0.01pF
Vout
Vin
Vss-
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Vdd
CMOS 0.18µm - 6 Metal (2.00V,3.30V)

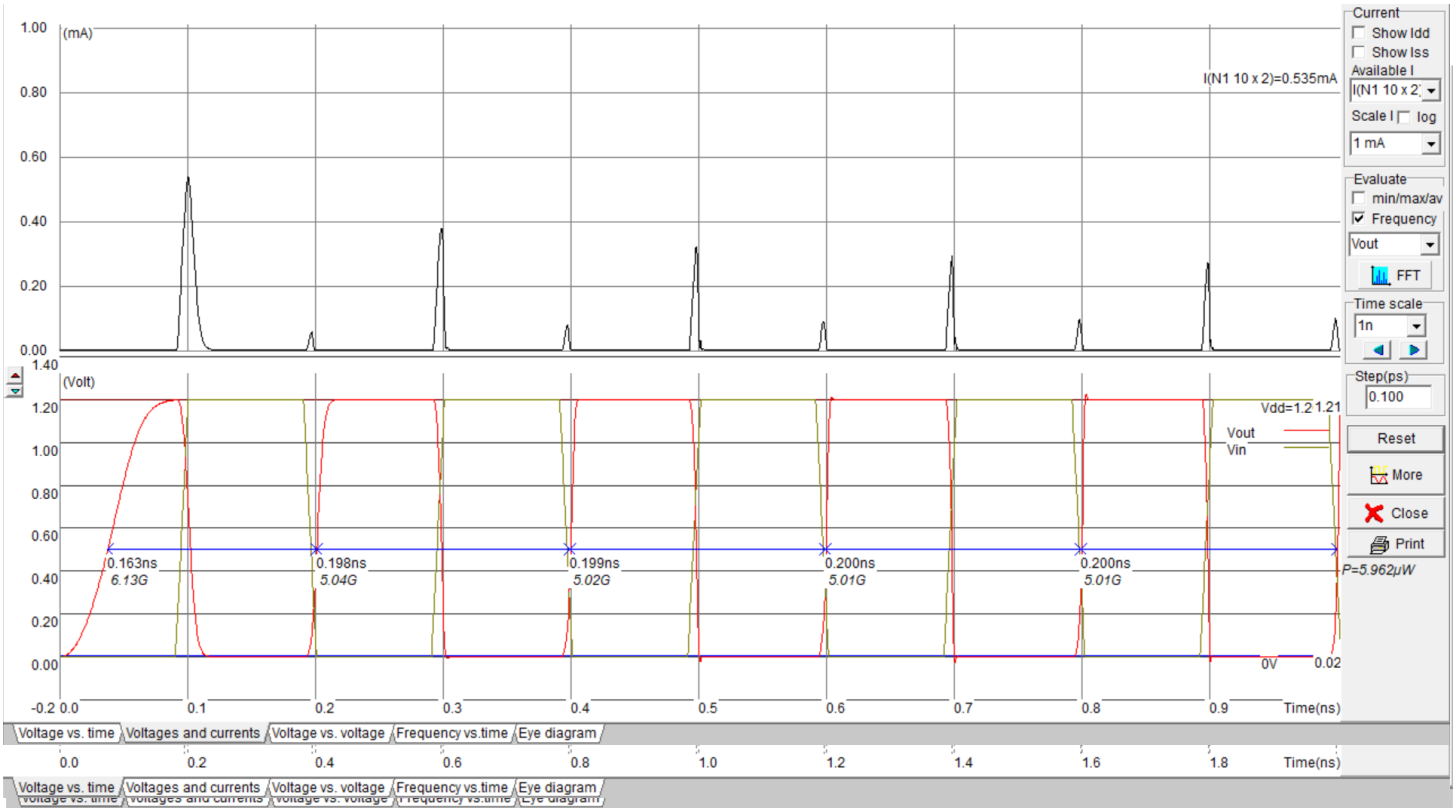
WAVEFORMS

1) Vin, Vout



SR.NO.		PARAMETER	VALUE	
1)		$P_{dynamic}$	34.621 µW	
2)		f_{max}	2.5 GHz	

2) Vout, Iout



SR.NO.		PARAMETER	VALUE	
1)		$P_{dynamic}$	5.962 µW	
2)		f_{max}	5 GHz	

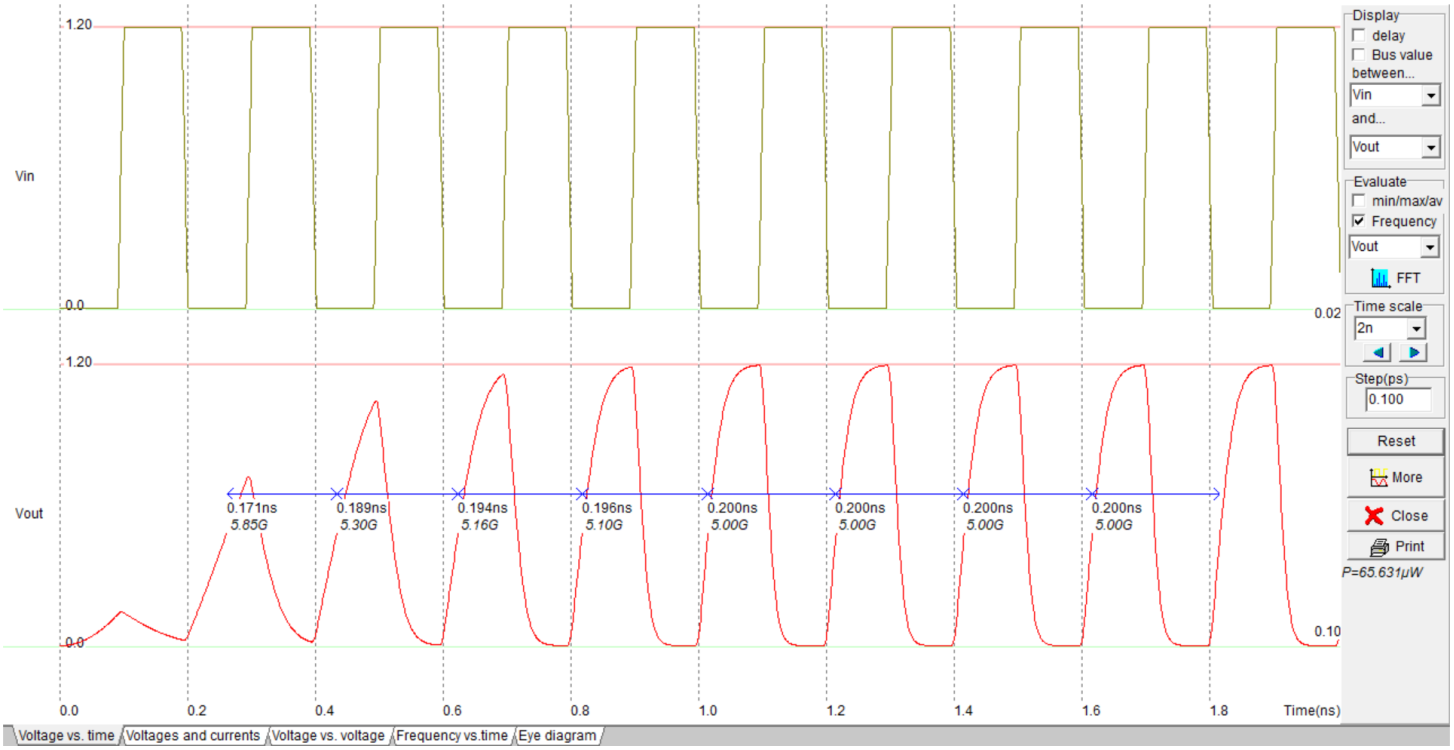
a) f = 2.5 GHz, C = 0.02 uF, Vdd = 1.2 V

SR.NO.		PARAMETER	VALUE	
1)		$P_{dynamic}$	62.402 µW	
2)		f_{max}	2.5 GHz	

b) f = 2.5 GHz, C = 0.005 uF, Vdd = 1.2 V

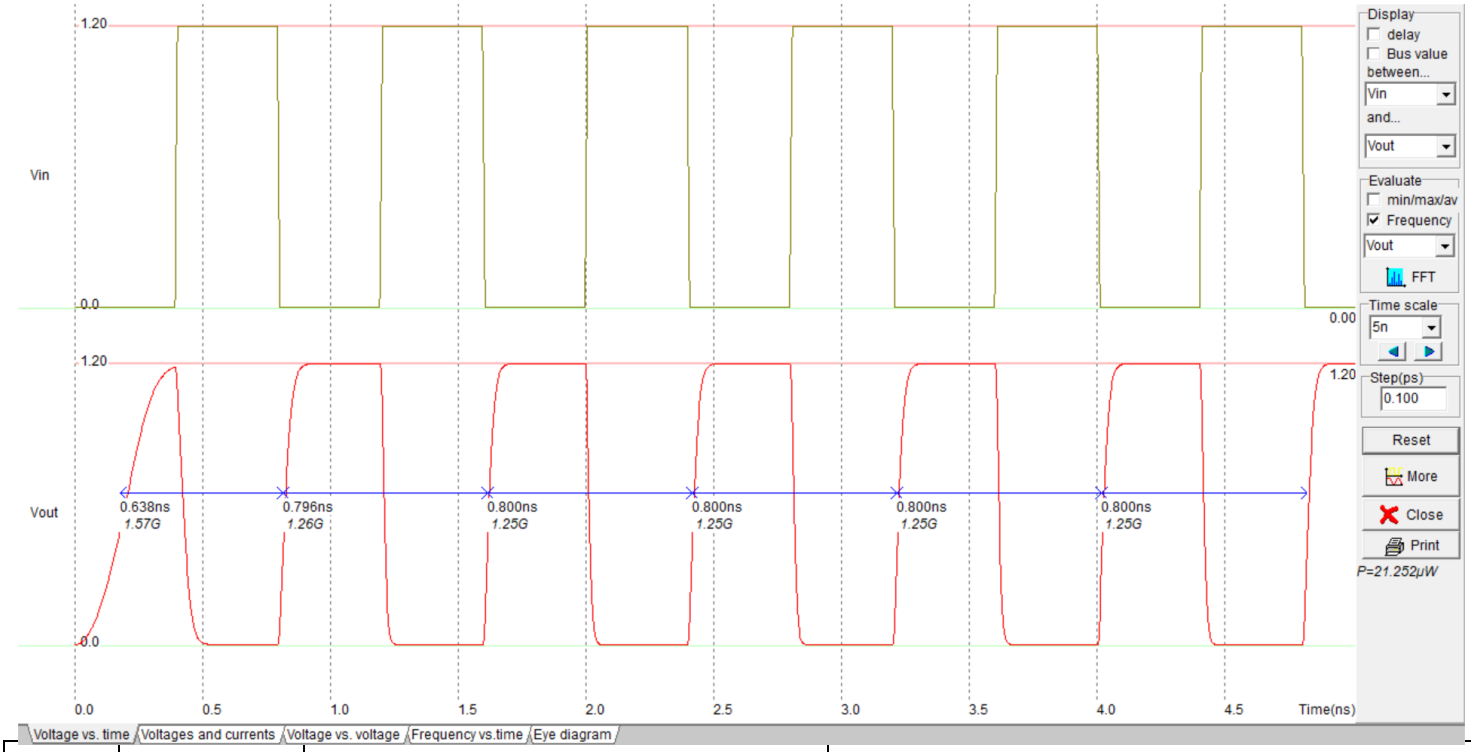
SR.NO.		PARAMETER	VALUE
1)		$P_{dynamic}$	20.062 µW
2)		f_{max}	2.5 GHz

c) f = 5 GHz, C = 0.01 u F, Vdd = 1.2 V



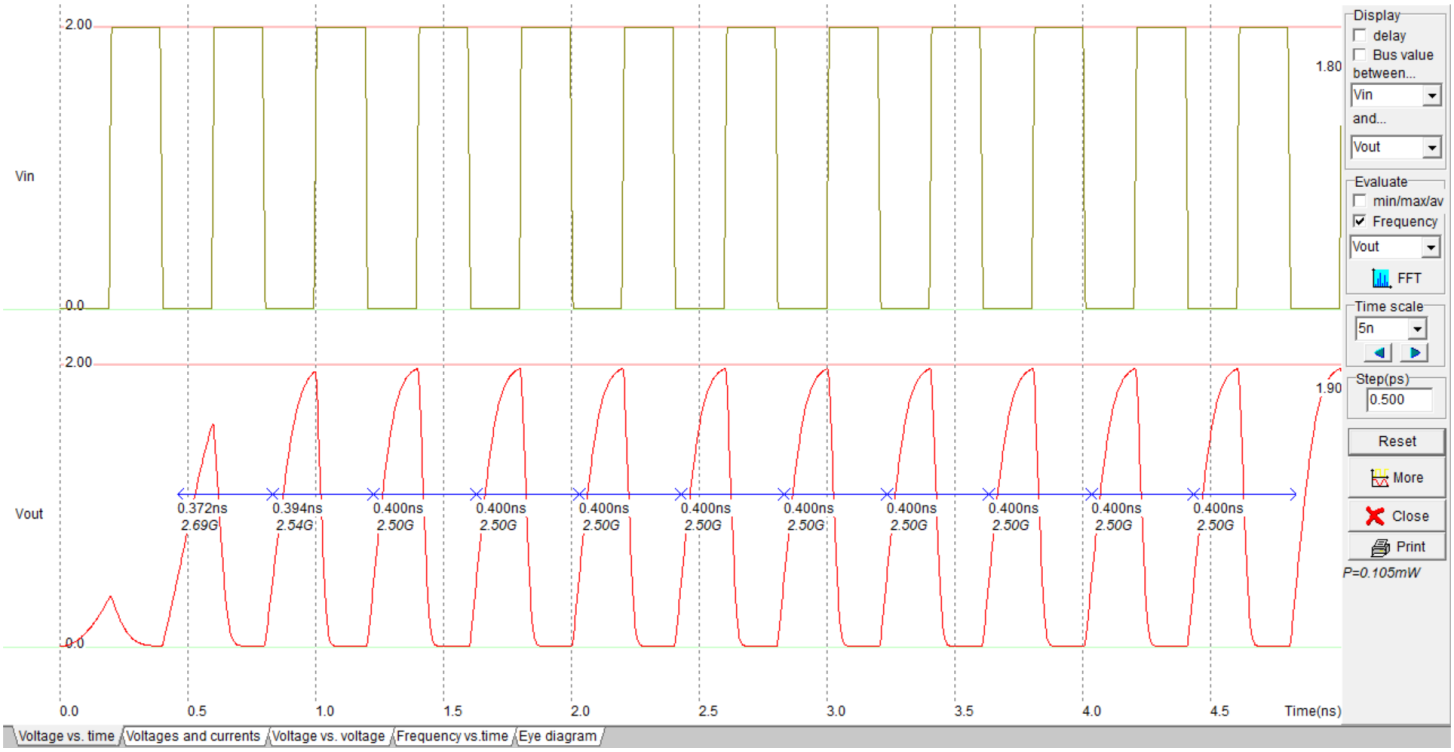
SR.NO.		PARAMETER	VALUE
1)		$P_{dynamic}$	65.631 µW
2)		f_{max}	5 GHz

d) f = 1.25 GHz, C = 0.01 uF, Vdd = 1.2 V



SR.NO.		PARAMETER	VALUE
1)		$P_{dynamic}$	21.252 µW
2)		f_{max}	1.25 GHz

e) f = 2.5 GHz, C = 0.01 uF, Vdd = 2V



SR.NO.		PARAMETER	VALUE
1)		$P_{dynamic}$	0.105 mW
2)		f_{max}	2.5 GHz

Conclusions:

Thus, we have:

1) Drawn the LAYOUT for CMOS Inverter using 90 nm & 180 nm Foundry.
2) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
3) Noted the values of $P_{dynamic}$ for floating Load.

4) Appreciated the validity of the mathematical model: $P_{dynamic} = C_L * (Vdd\ 2) * f_{clk}$ by Doubling & Halving the values of C_L & f_{clk}
5) Found a reduction in $P_{dynamic}$ by using a better Foundry i.e., 90 nm instead of 180 nm
6) Learnt that the presence of spikes in O / P waveform at Switching instants indicate the inability of the MOSFETs to switch at GHz frequencies.
7) Learnt that the using a better Foundry enables the MOSFETs the inability of the MOSFETs to switch at Higher GHz frequencies, as proved by the removal of Spikes at the O/P.