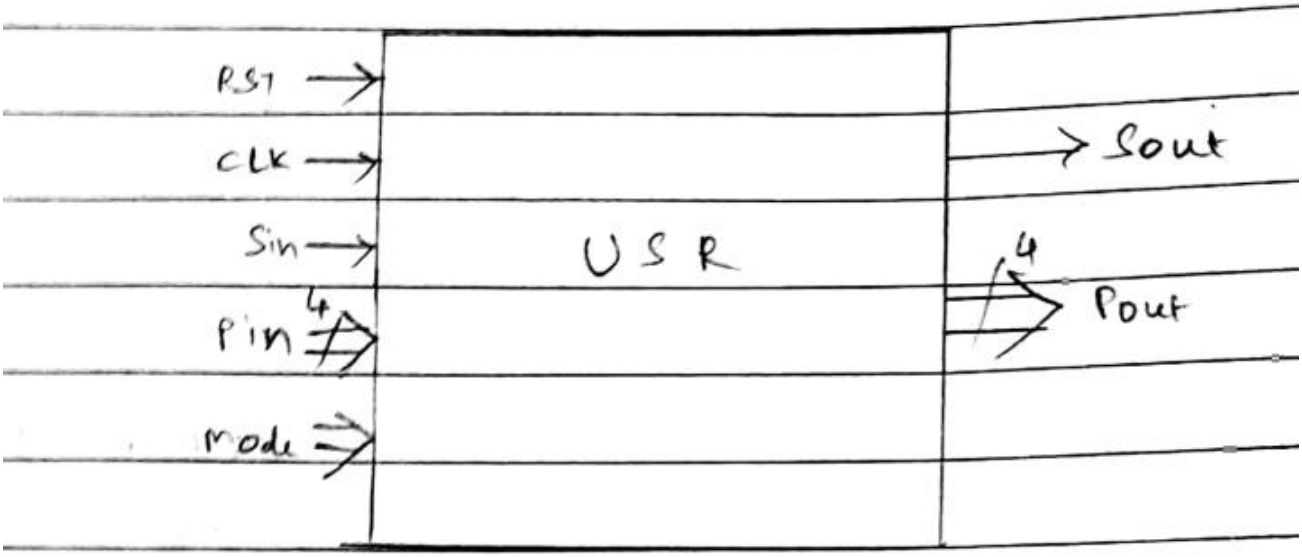
Class	:	BE - 8
Roll No	:	42410
Assignment No	:	2
Assignment Name	:	4-Bit USR
Date of Performance	:	19-9 to 3-10

BLOCK DIAGRAM



* Power hierarchy

Highest	RST
	Clk
lowest	Mode
(equal)	Sin, Pin

TRUTH TABLE:

RST	Clk	Mode	Outputs / Mode
1	x	x	Sout = 0 Pout : 0000
0	↓	00	SISO
0	↓	01	SIPO
0	↓	10	PISO
0	↓	11	PIPO

* Mode Latency (No. of cycles)

SISO = 4+4 = 8

SIPO = 4+1 = 5

PISO = 1+4 = 5

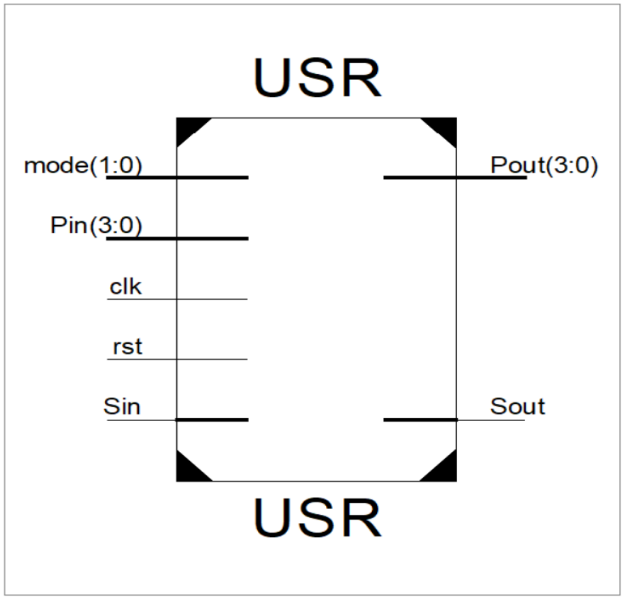
PIPO = 1+1 = 2

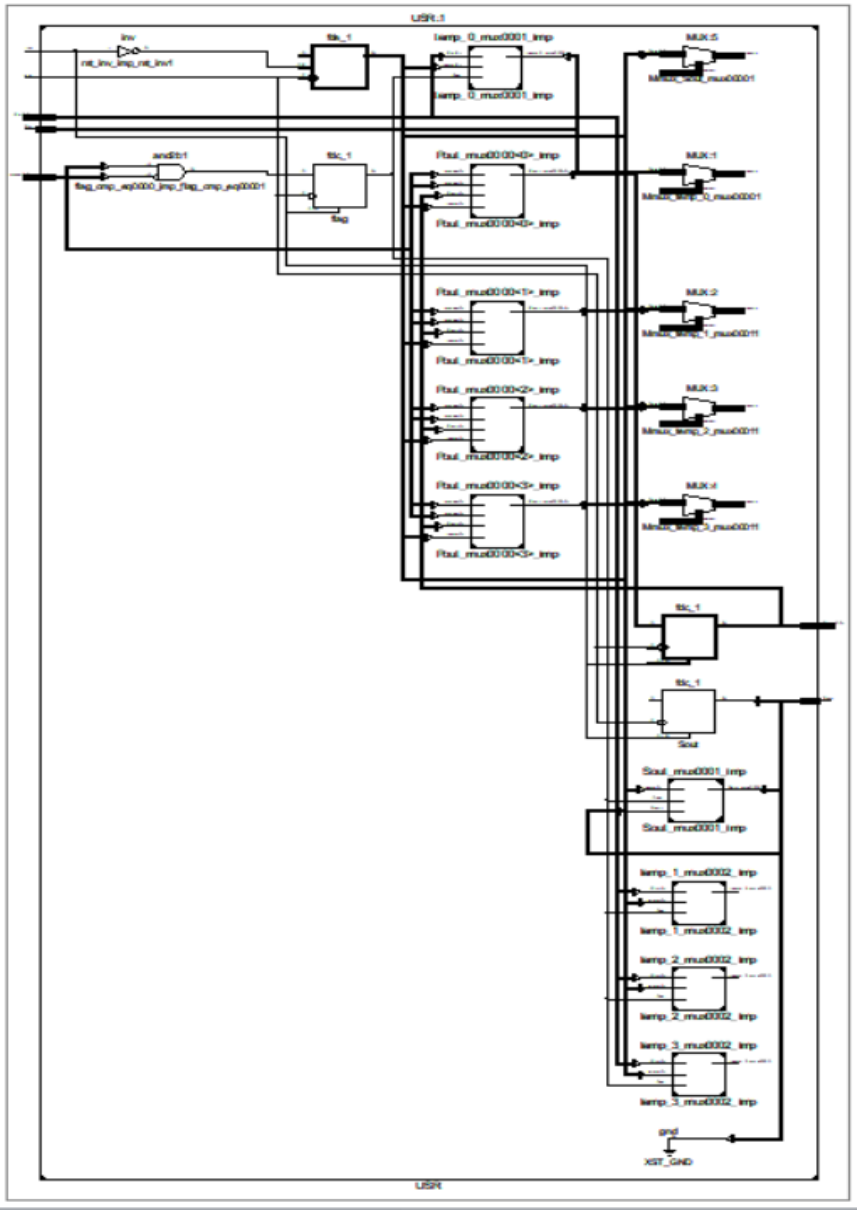
MAIN VHDL PROGRAM

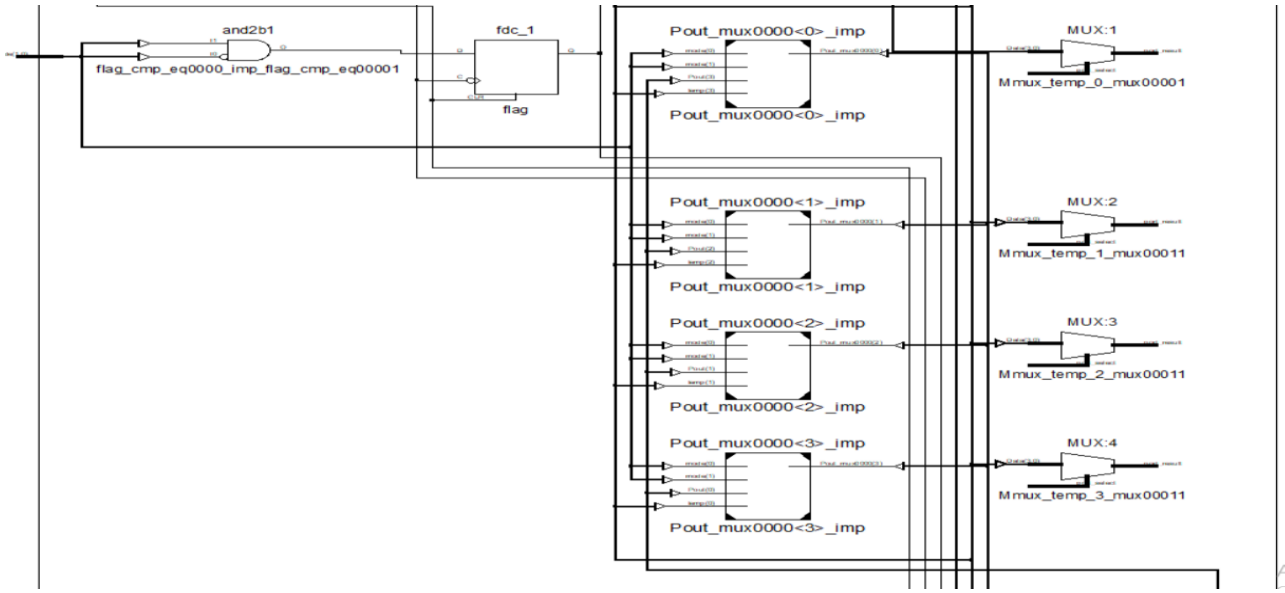
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity USR is
   Port ( rst : in  STD_LOGIC;
          clk : in  STD_LOGIC;
          mode : in  STD_LOGIC_VECTOR (1 downto 0);
          Sin : in  STD_LOGIC;
          Pin : in  STD_LOGIC_VECTOR (3 Downto 0);
          Sout : out  STD_LOGIC;
          Pout : out  STD_LOGIC_VECTOR (3 downto 0));
end USR;

architecture USR_arch of USR is

   SIGNAL temp : STD_LOGIC_VECTOR(3 DOWNTO 0):="0000" ;
       SIGNAL flag : STD_LOGIC:='0';

      begin
      PROCESS(rst, clk, mode, Sin, Pin)
      BEGIN
            IF rst='1' THEN
                  Sout <= '0';
                  Pout <= "0000";
                  flag <= '0';

            ELSIF falling_edge(clk)  THEN
                  CASE MODE IS
                        WHEN "00" =>   -- SISO
                              temp(3 DOWNTO 1) <= temp(2 DOWNTO 0);
                              temp(0) <= Sin;
                              Sout <= temp(3);
                              Pout <="0000";
                              flag <= '0';
                        WHEN "01" =>      --SIPO
                              temp(3 DOWNTO 1) <= temp(2 DOWNTO 0);
                              temp(0) <= Sin;
                              Pout<=temp;
                              Sout <= '0';
                              flag <= '0';
                        WHEN "10" =>                              --PISO
                              IF flag='0' THEN
                                 temp <= Pin;
                              ELSE
                                 temp(3 DOWNTO 1) <= temp(2 DOWNTO 0);
                                     Sout <= temp(3);
                               END IF;
                        flag <= '1';
```

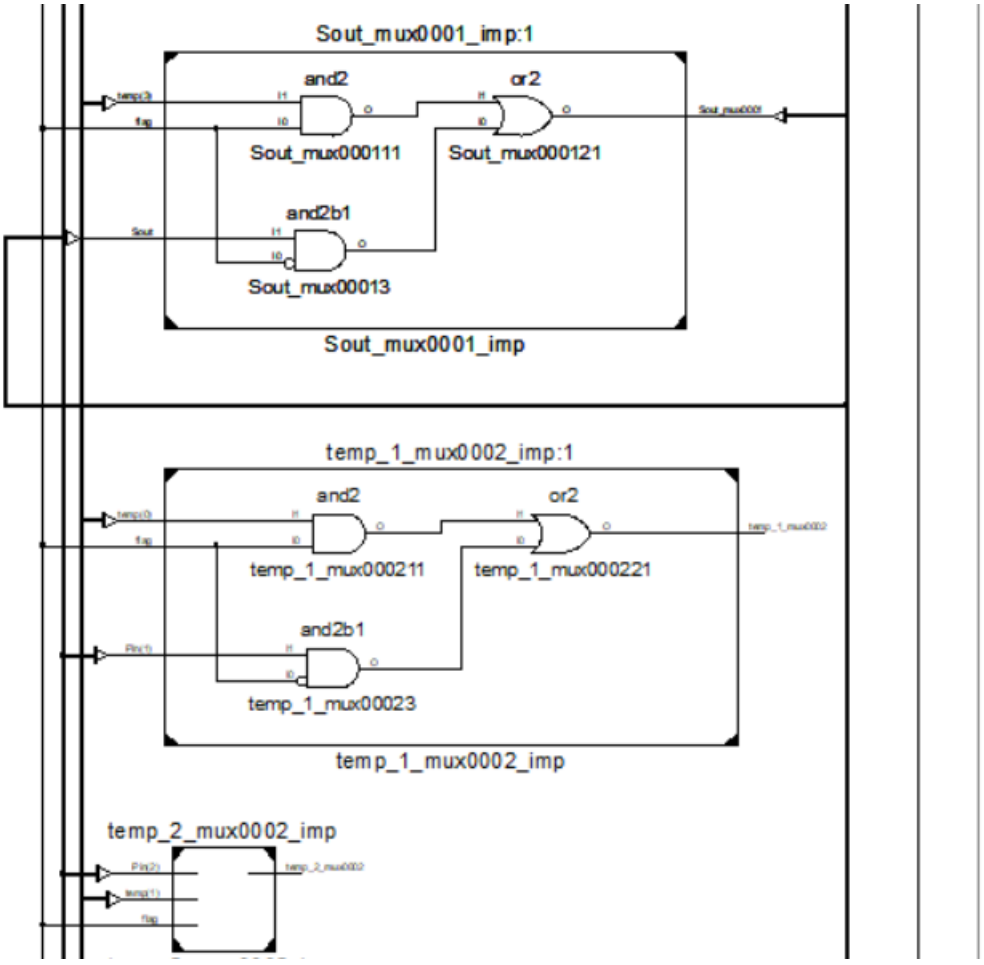
```
                    WHEN OTHERS =>   -- PIPO
                        temp <= Pin;
                        Pout <= temp;
                        flag <= '0';
                END CASE;
            END IF;
        END PROCESS;

end USR_arch;
```

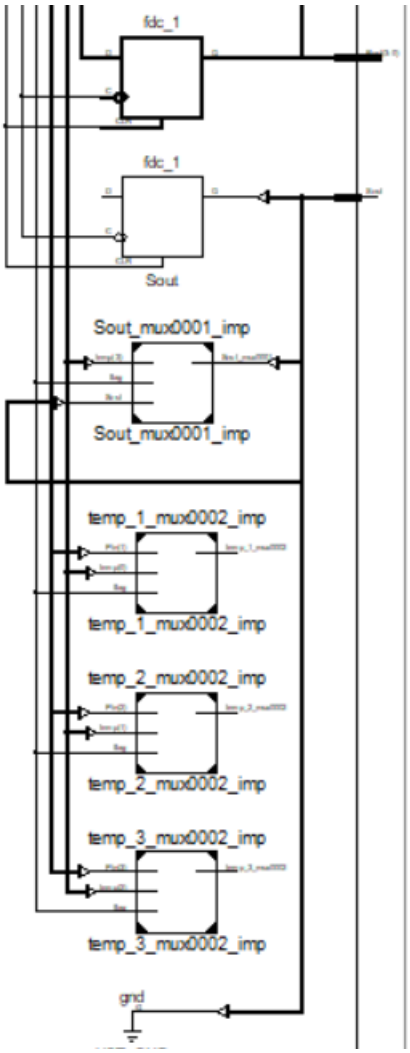
RTL SCHEMATIC

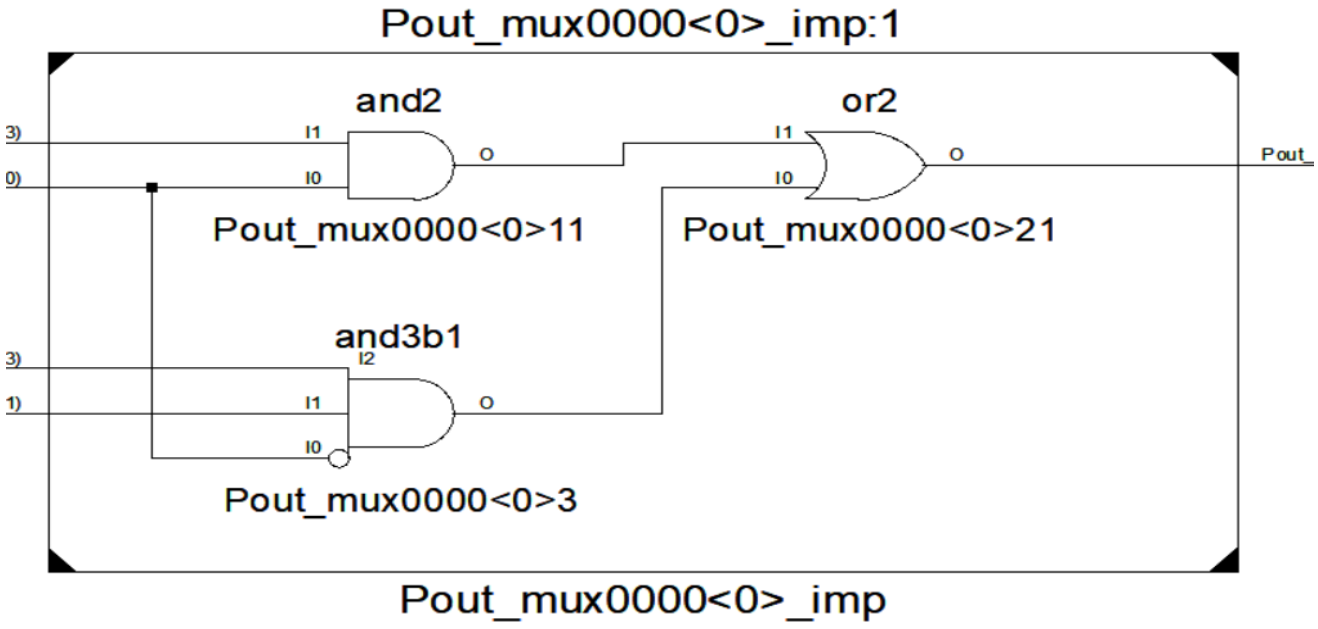




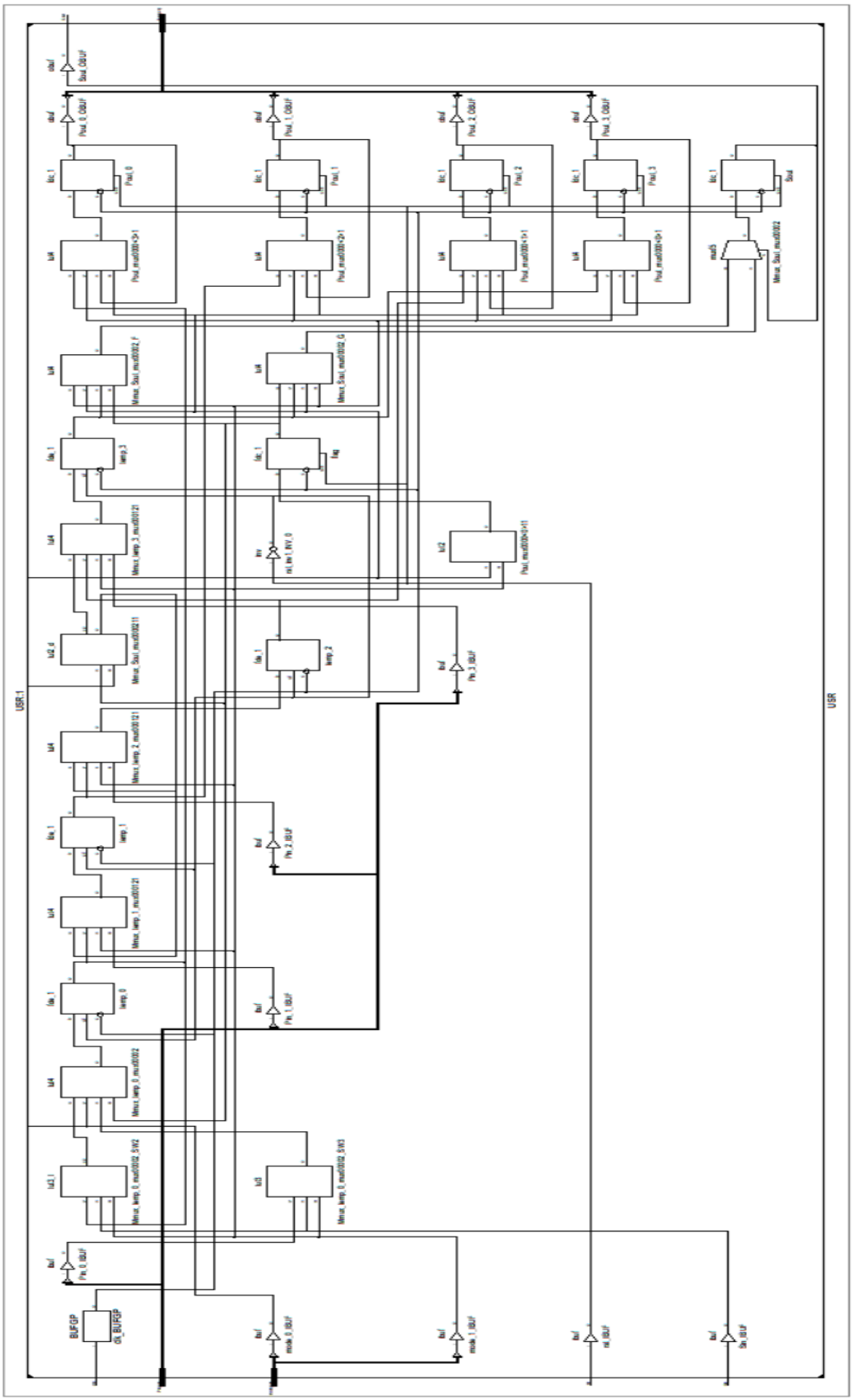

and2b1
flag_cmp_eq0000_imp_flag_cmp_eq00001
fdc_1
flag
Pout_mux0000<0>_imp
Pout_mux0000<0>_imp
Pout_mux0000<1>_imp
Pout_mux0000<1>_imp
Pout_mux0000<2>_imp
Pout_mux0000<2>_imp
Pout_mux0000<3>_imp
Pout_mux0000<3>_imp
MUX:1
Mmux_temp_0_mux00001
MUX:2
Mmux_temp_1_mux00011
MUX:3
Mmux_temp_2_mux00011
MUX:4
Mmux_temp_3_mux00011

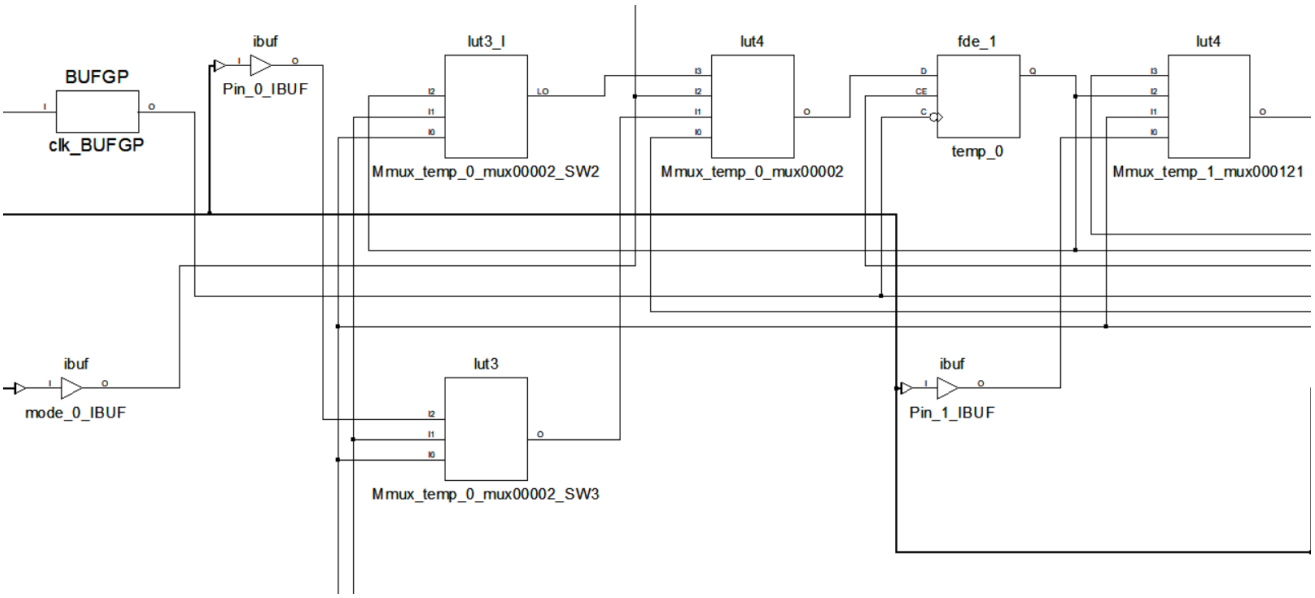

Sout_mux0001_imp:1
and2
or2
Sout_mux000111
Sout_mux000121
and2b1
Sout_mux00013
Sout_mux0001_imp
temp_1_mux0002_imp:1
and2
or2
temp_1_mux000211
temp_1_mux000221
and2b1
temp_1_mux00023
temp_1_mux0002_imp
temp_2_mux0002_imp

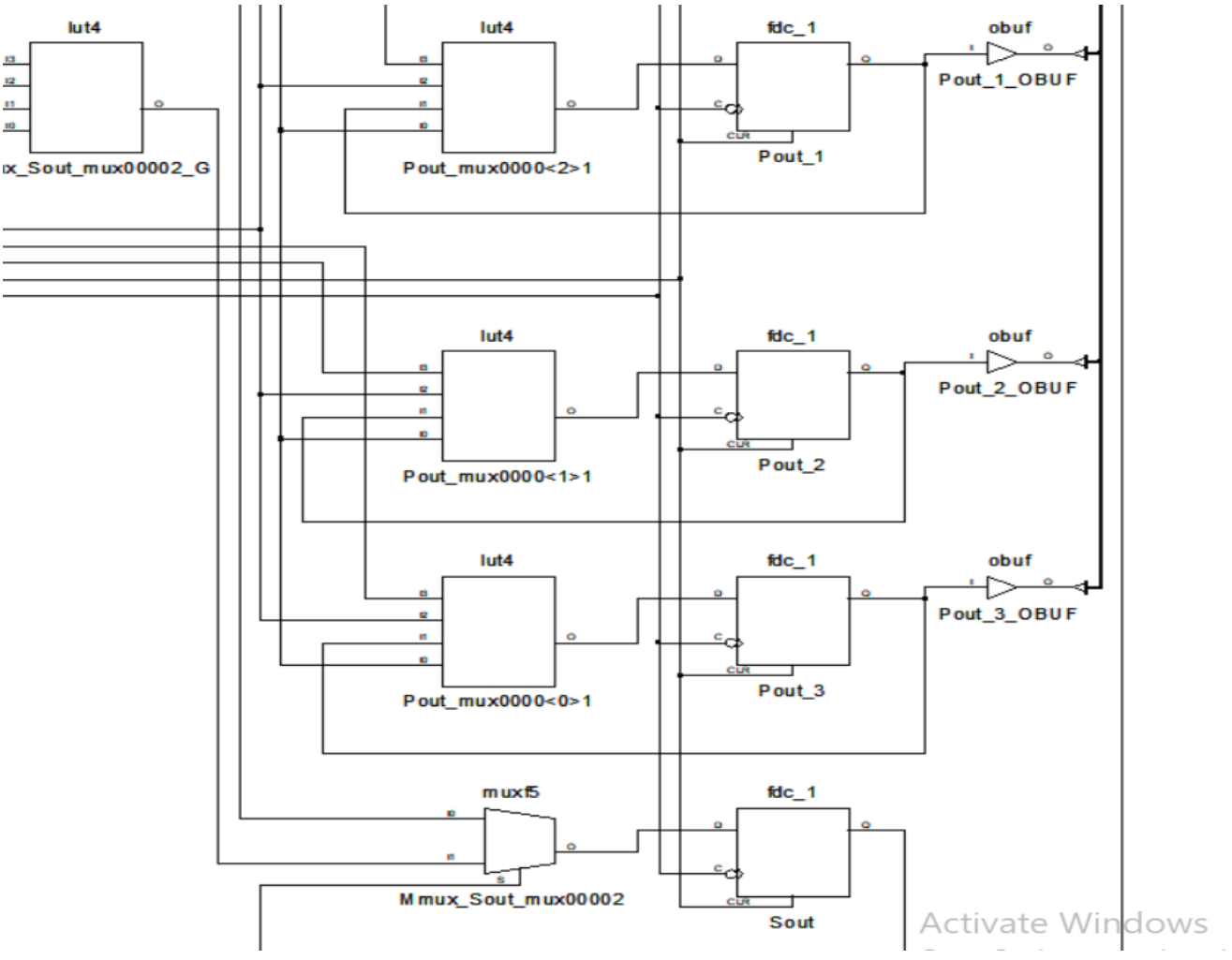

fdc_1
fdc_1
Sout
Sout_mux0001_imp
Sout_mux0001_imp
temp_1_mux0002_imp
temp_1_mux0002_imp
temp_2_mux0002_imp
temp_2_mux0002_imp
temp_3_mux0002_imp
temp_3_mux0002_imp
gnd


Pout_mux0000<0>_imp:1
and2
or2
3)
0)
I1
I0
O
I1
I0
O
Pout_
Pout_mux0000<0>11
Pout_mux0000<0>21
and3b1
3)
1)
I2
I1
I0
O
Pout_mux0000<0>3
Pout_mux0000<0>_imp

TECHNOLOGY SCHEMATIC







SYNTHESIS REPORT

A)Device Utilisation Summary

```
=========================================================================
*                      Final Report                      *
=========================================================================
Final Results
RTL Top Level Output File Name     : USR.ngr
Top Level Output File Name         : USR
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 14

Cell Usage :
# BELS                             : 16
#      INV                         : 1
#      LUT2                        : 1
#      LUT2_D                      : 1
#      LUT3                        : 1
#      LUT3_L                      : 1
#      LUT4                        : 10
#      MUXF5                       : 1
# FlipFlops/Latches                : 10
#      FDC_1                       : 6
#      FDE_1                       : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 13
#      IBUF                        : 8
#      OBUF                        : 5
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                  8  out of   2448     0%
 Number of Slice Flip Flops:        10  out of   4896     0%
 Number of 4 input LUTs:            15  out of   4896     0%
 Number of IOs:                     14
 Number of bonded IOBs:             14  out of    158     8%
 Number of GCLKs:                   1  out of     24     4%

---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
```

B) TIMMING REPORT

```
=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 10    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
rst                                | IBUF                   | 6     |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 2.957ns (Maximum Frequency: 338.192MHz)
   Minimum input arrival time before clock: 3.993ns
   Maximum output required time after clock: 4.063ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 10    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
```

Control Signal	Buffer(FF name)	Load
rst	IBUF	6

Timing Summary:

Speed Grade: -5

Minimum period: 2.957ns (Maximum Frequency: 338.192MHz)
Minimum input arrival time before clock: 3.993ns
Maximum output required time after clock: 4.063ns
Maximum combinational path delay: No path found

Timing Detail:

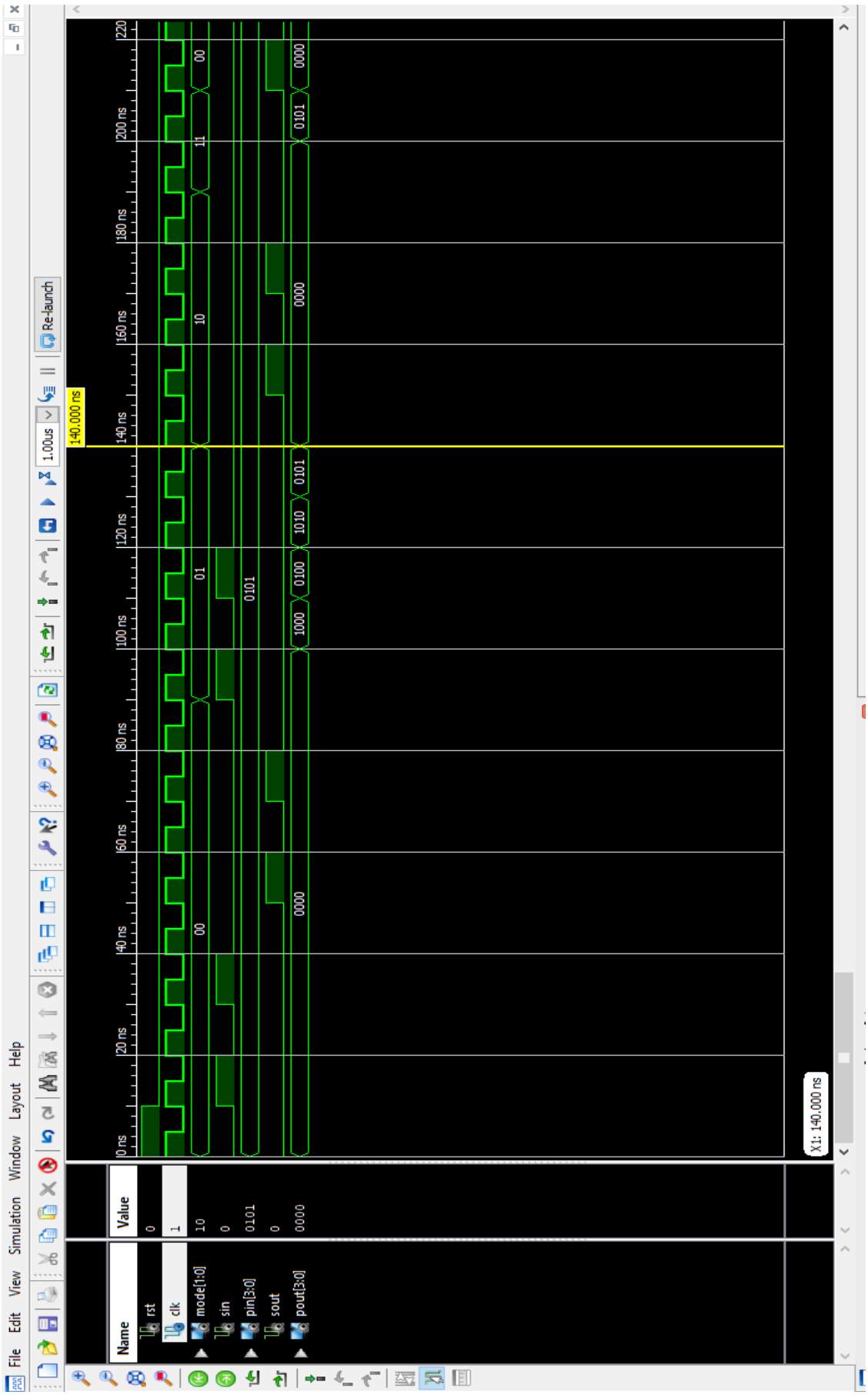
All values displayed in nanoseconds (ns)

TEST BENCH PROGRAM

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
USE ieee.numeric_std.ALL;

ENTITY USR_tb IS
END USR_tb;

ARCHITECTURE usr_arch OF USR_tb IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT USR
   PORT(
        rst : IN  std_logic;
        clk : IN  std_logic;
        mode : IN  std_logic_vector(1 downto 0);
        Sin : IN  std_logic;
        Pin : IN  std_logic_vector(3 downto 0);
        Sout : OUT  std_logic;
        Pout : OUT  std_logic_vector(3 downto 0)
       );
   END COMPONENT;

  --Inputs
  signal rst : std_logic := '0';
  signal clk : std_logic := '0';
  signal mode : std_logic_vector(1 downto 0) := (others => '0');
  signal Sin : std_logic := '0';
  signal Pin : std_logic_vector(3 downto 0) := "1001";
      --Outputs
  signal Sout : std_logic;
  signal Pout : std_logic_vector(3 downto 0);
  -- Clock period definitions
  constant clk_period : time := 10 ns;

BEGIN
      -- Instantiate the Unit Under Test (UUT)
  uut: USR PORT MAP (
         rst => rst,
         clk => clk,
         mode => mode,
         Sin => Sin,
         Pin => Pin,
         Sout => Sout,
         Pout => Pout
       );
  -- Clock process definitions
  clk_process :process
  begin
              clk <= '0';
```

```
		wait for clk_period/2;
		clk <= '1';
		wait for clk_period/2;
	end process;
	-- Stimulus process
	stim_proc_rst: process
	begin
		rst<='1';
		wait for 300 ns;
		rst<='0';
		wait for 10 ns;
	end process;

-- Stimulus process
	stim_proc_mode: process
	begin
	  mode <= "00";
	    wait for 80 ns;
	    mode <= "01";
	    wait for 50 ns;
	    mode <= "10";
	    wait for 50 ns;
	    mode <= "11";
	    wait for 20 ns;

	end process;

	stim_proc_Sin: process
	begin
	  wait for 10 ns;
		Sin <= '1';
		wait for 10 ns;
		Sin <= '0';
		wait for 10 ns;
		Sin <= '1';
		wait for 10 ns;
		Sin <= '0';
		wait for 10 ns;
		Sin <= '0';
		wait for 50 ns;
		Sin <= '1';
		wait for 10 ns;
		Sin <= '0';
		wait for 10 ns;
		Sin <= '1';
		wait for 10 ns;
		Sin <= '0';
		wait for 10 ns;
		Sin <= '0';
		wait;

	end process;
END;
```

ISIM WAVEFORMS



PIN-LOCKING REPORT

PlanAhead Generated physical constraints

NET "CLK" LOC = P132;

NET "RST" LOC = P204;

NET "mode[1]" LOC = P205;

NET "mode[0]" LOC = P206;

NET "Sin" LOC = P203;

NET "Pin[3]" LOC = P202;

NET "Pin[2]" LOC = P197;

NET "Pin[1]" LOC = P199;

NET "Pin[0]" LOC = P196;

NET "Sout" LOC = P193;

NET "Pout[3]" LOC = P186;

NET "Pout[2]" LOC = P187;

NET "Pout[1]" LOC = P185;

NET "Pout[0]" LOC = P181;

Conclusion:

Thus, we have:

1) Modeled a 4-bit USR using Behavioral Modeling Style.
2) Observed following Schematics: **RTL** & **Technology Schematics** generated **Post-Synthesis**.
3) Interpreted **Device utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers & D FFs used out of the available device resources.
4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
5) Written a TESTBENCH to verify the functionality of 4-bit USR & verified the functionality as per the TRUTH-TABLE, by observing ISIM Waveform.
6) Used Plan Ahead Editor for pin-locking.
7) Prototyped the FPGA **XC3S250EPQ208-5** to realize 4-bit USR & verified its operation by giving suitable input combinations