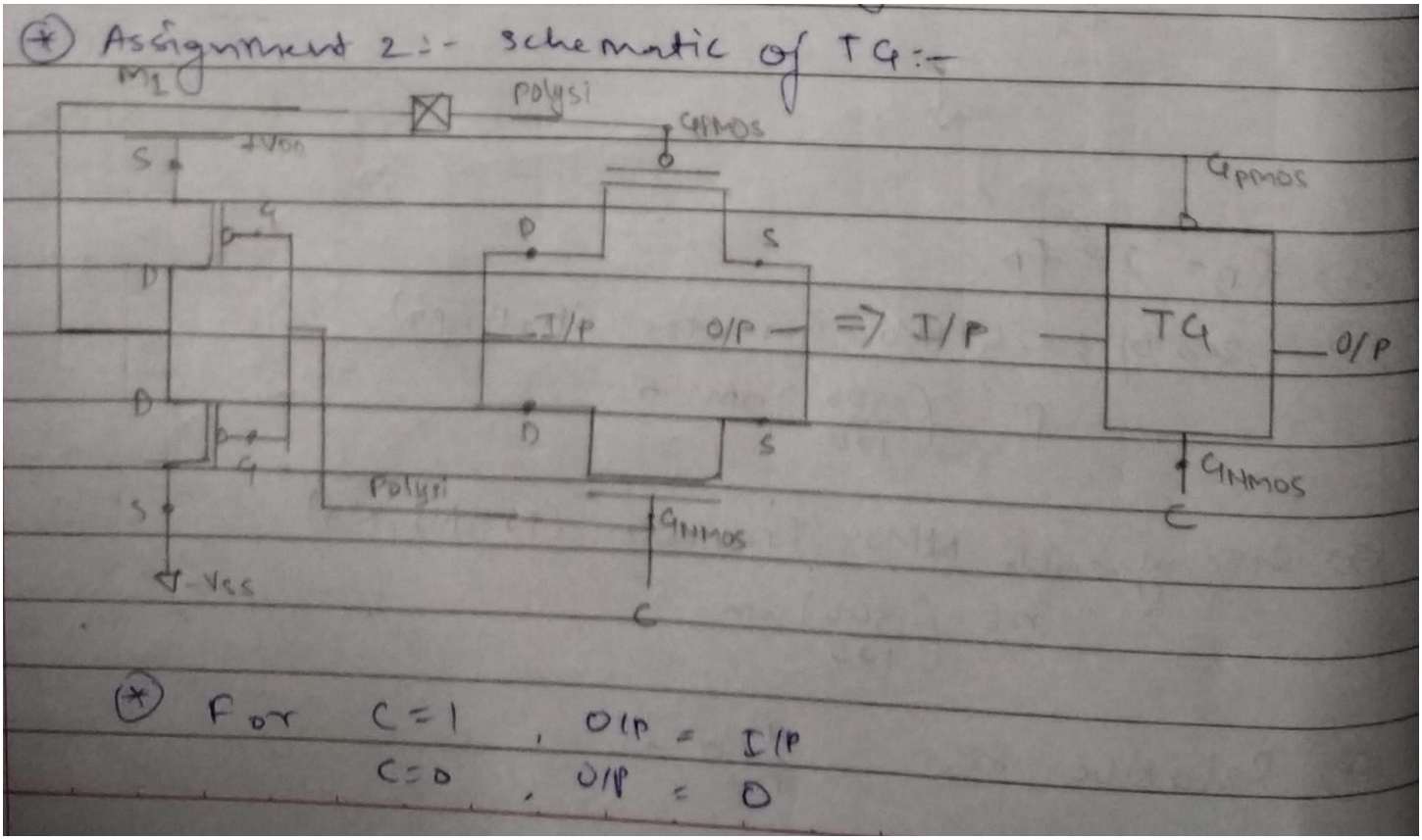
Class	:	BE - 8
Roll. No	:	42410
Assignment No.	:	2
Assignment Name	:	2:1 MUX USING TG LOGIC
Date of Performance	:	23-11-2020

(*) Assignment 2 :- Schematic of TG :-

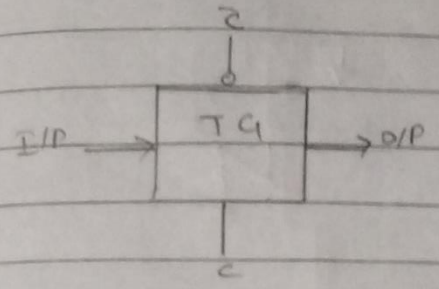


(*) For C = 1 , O/P = I/P

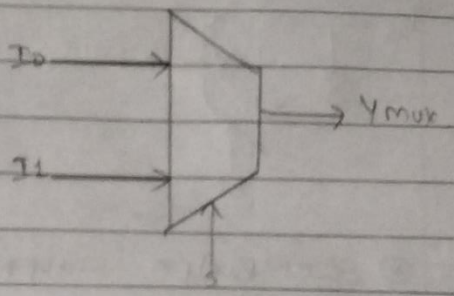
C = 0 , O/P = 0

⊛ Schematic of 2:1 MUX using TG:

symbol of TG :



symbol of 2:1 MUX

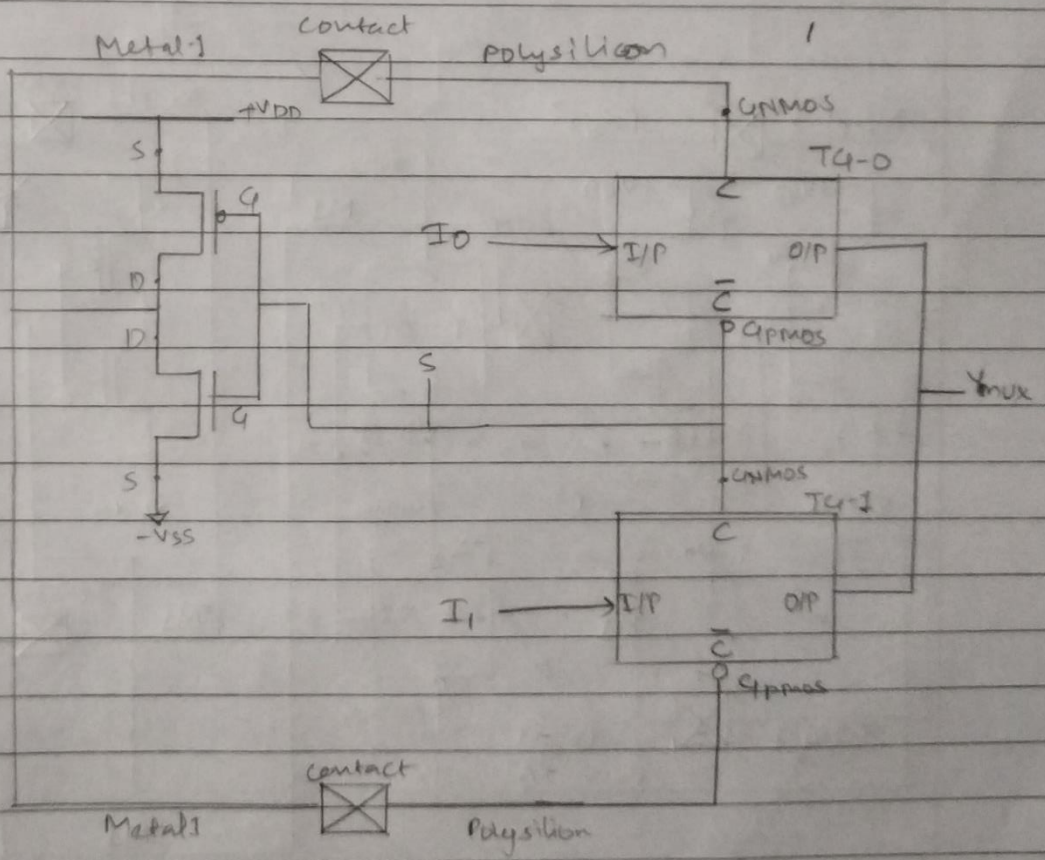


TRUTH TABLE

C	O/P
1	I/P
0	0

TRUTH TABLE

S	Ymux
0	I_0
1	I_1

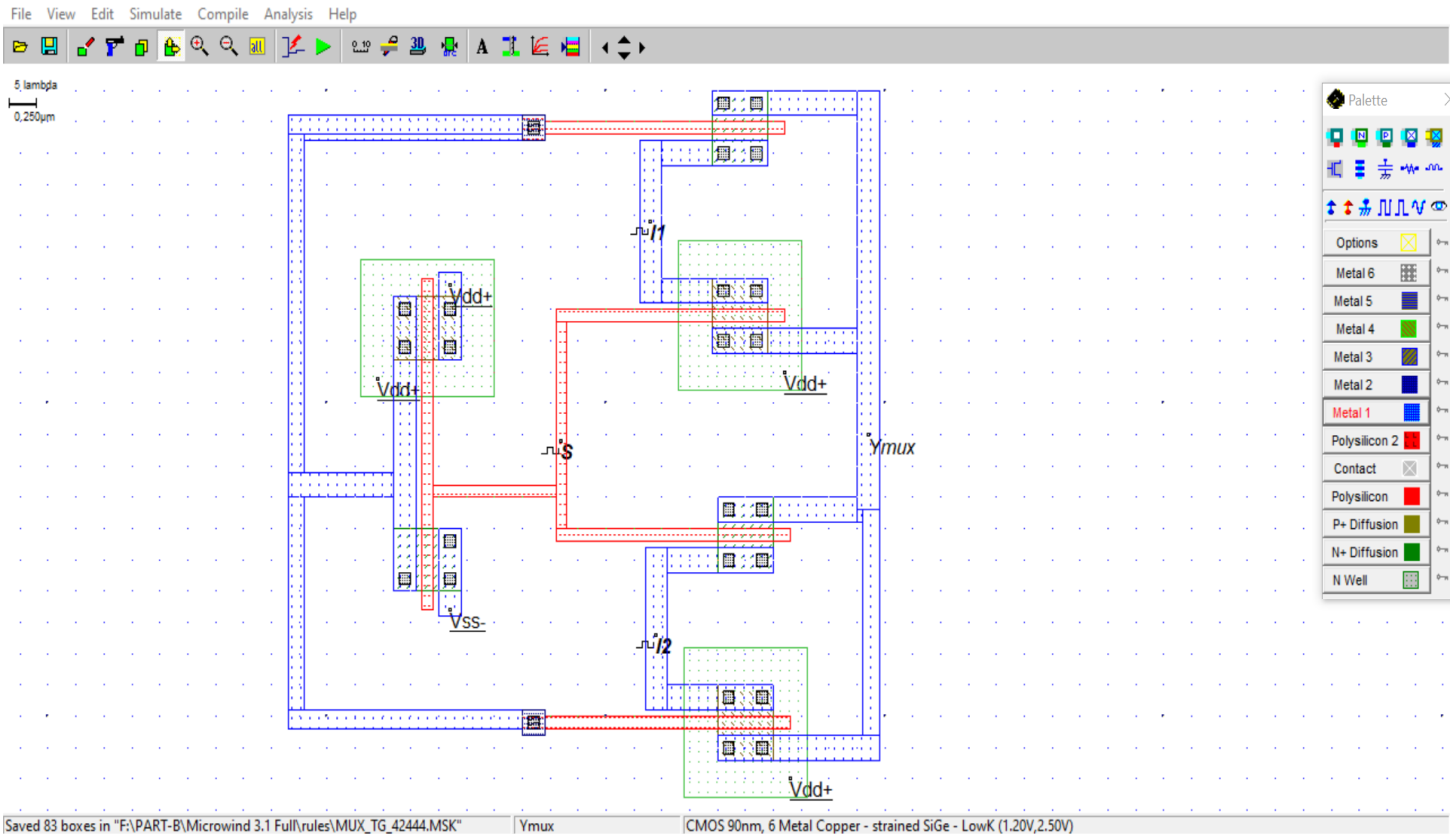


⊛ All PMOS & NMOS Devices have sizes:-

⊛ $P = n = \left(\frac{500}{100}\right) nm = 5$

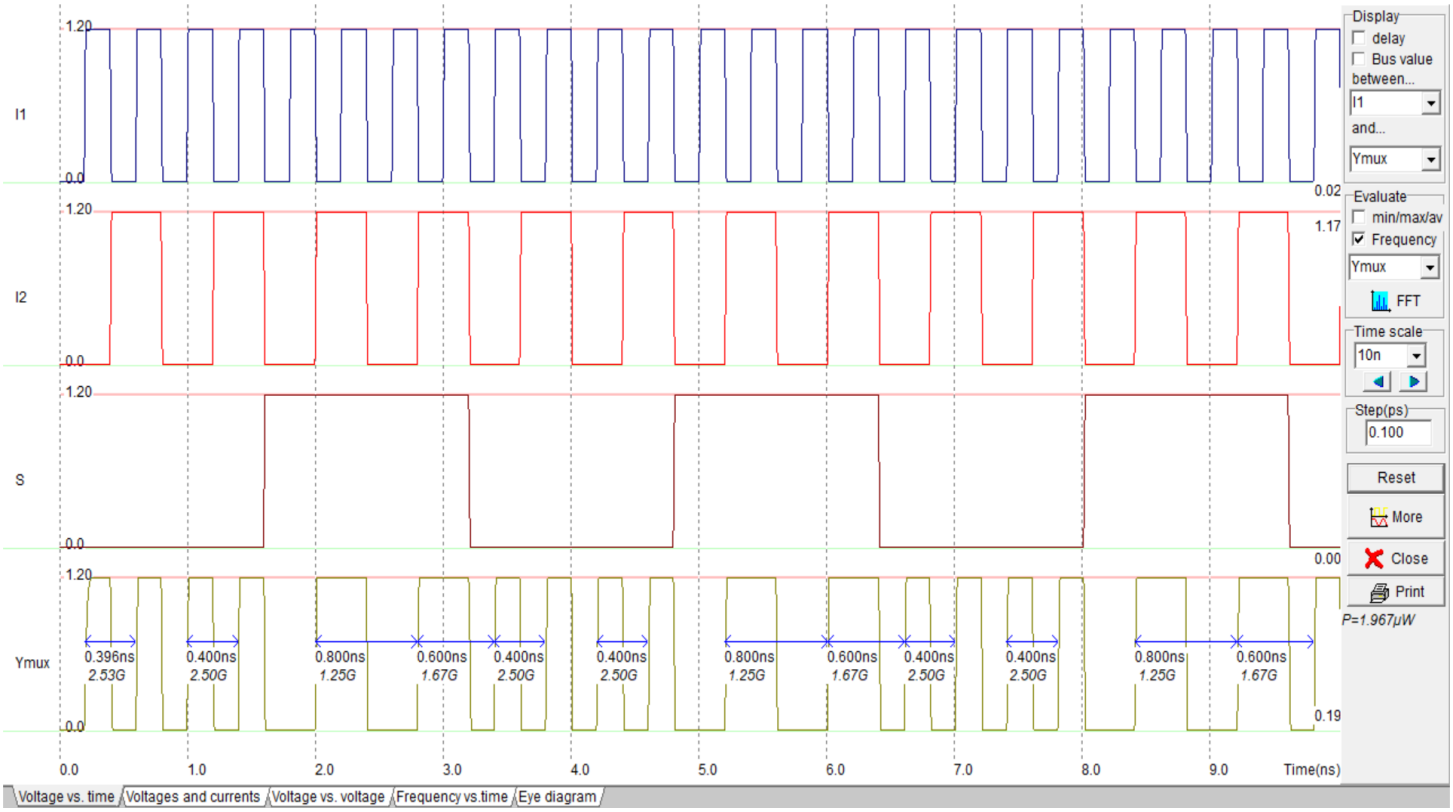
⊛ $\frac{P}{n} = 1$

Layout

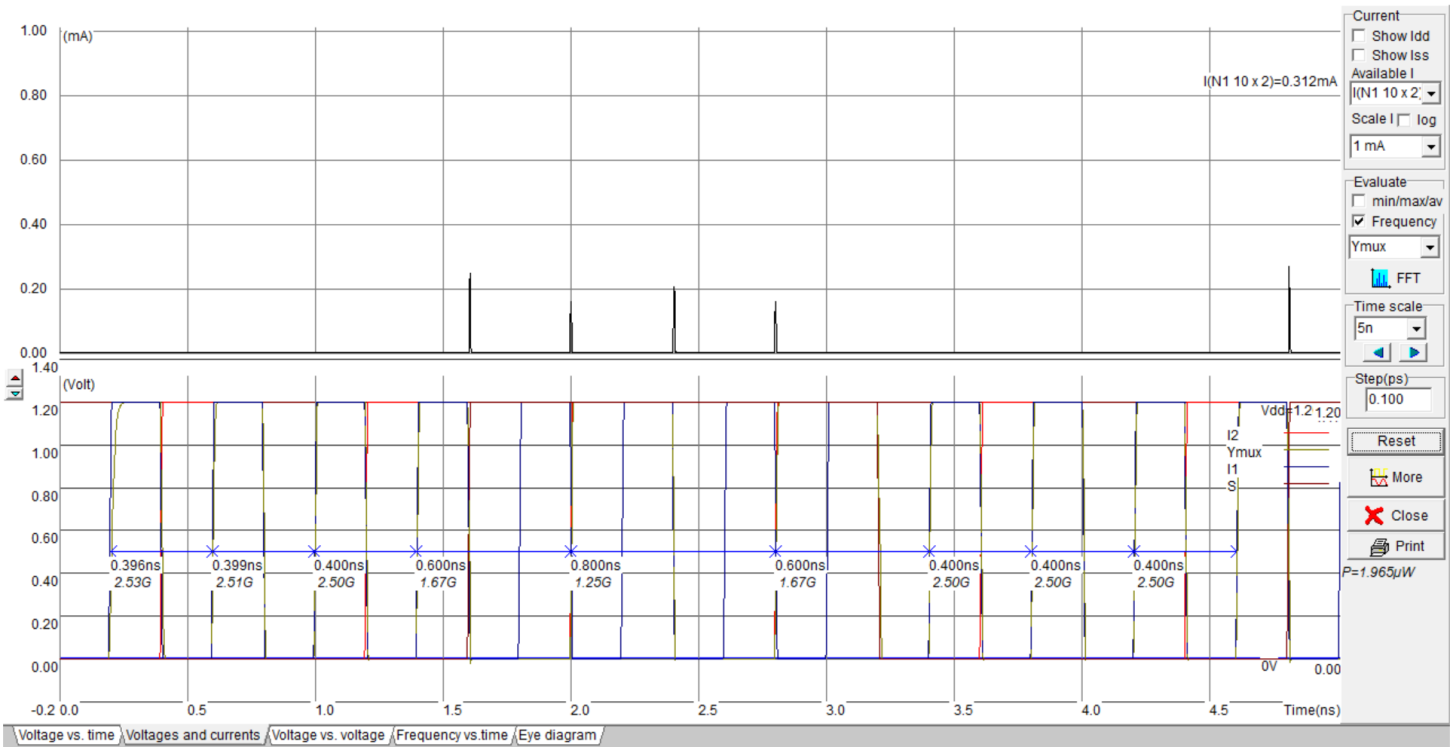

File View Edit Simulate Compile Analysis Help
5 lambda
0,250µm
I1
Vdd+
Vdd+
Vdd+
S
Ymux
Vss-
I2
Vdd+
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Saved 83 boxes in "F:\PART-B\Microwind 3.1 Full\rules\MUX_TG_42444.MSK"
Ymux
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

WAVEFORMS

1. V vs T Waveform



2. V out, I out Waveform



Conclusions:

Thus, we have:

1) Drawn the LAYOUT for Transmission Gate and 2:1 MUX using TG using 90 nm Foundry.
2) Simulated the LAYOUT to observe waveforms.
3) When the S is 0, the output is same as I0 and when S=1 output is same as I1.
4) Verified its functionality as per TRUTH-TABLE.
5) Noted the values of $P_{dynamic.}$