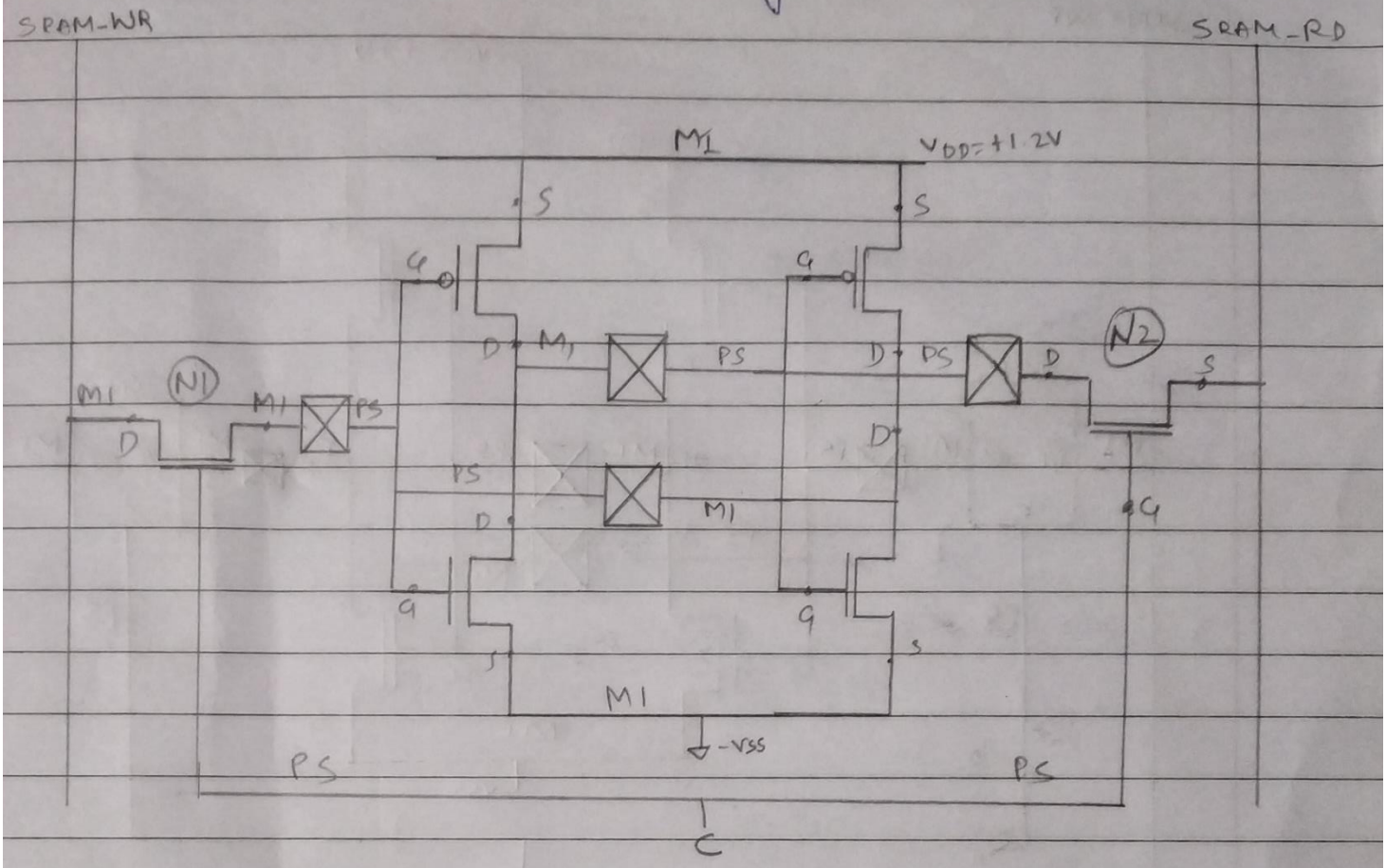
Class	:	BE - 8
Roll. No	:	42410
Assignment No.	:	B.3 (a,b)
Assignment Name	:	1 Bit SRAM Cell using NMOS and TG S/W
Date of Performance	:	30-11-2020

⊛ Assignment 3 : 1-bit SRAM cell

(3.a) :- 1-bit SRAM cell using NMOS switches!

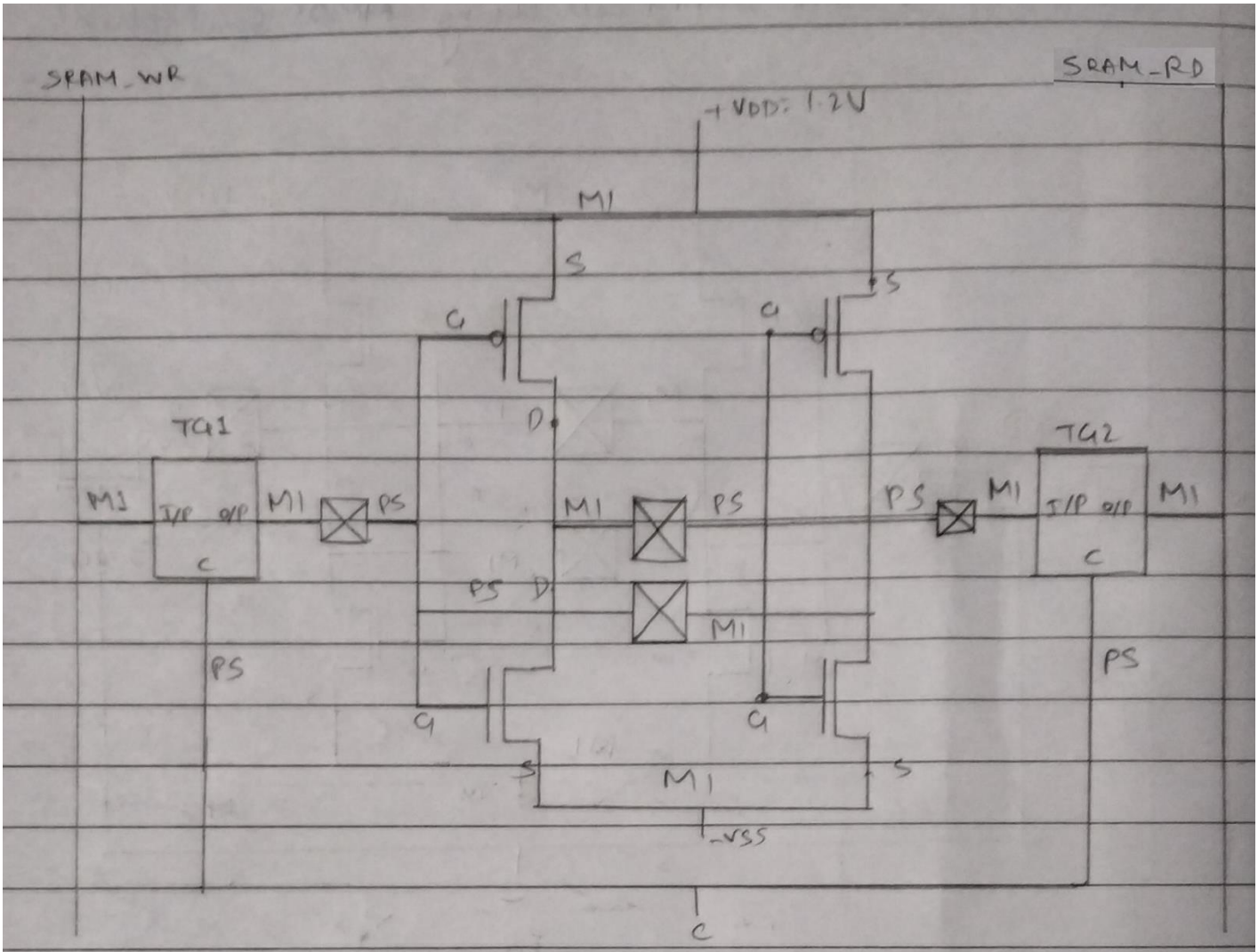


⊛ N_1, N_2 : NMOS s/w's

⊛ function Table:

C	SRAM_WR	SRAM_RD
1	0	WEAK 1
1	1	STRONG 0
0	X	D/Hold

(3.b) 1-bit SRAM cell using TG switches :-



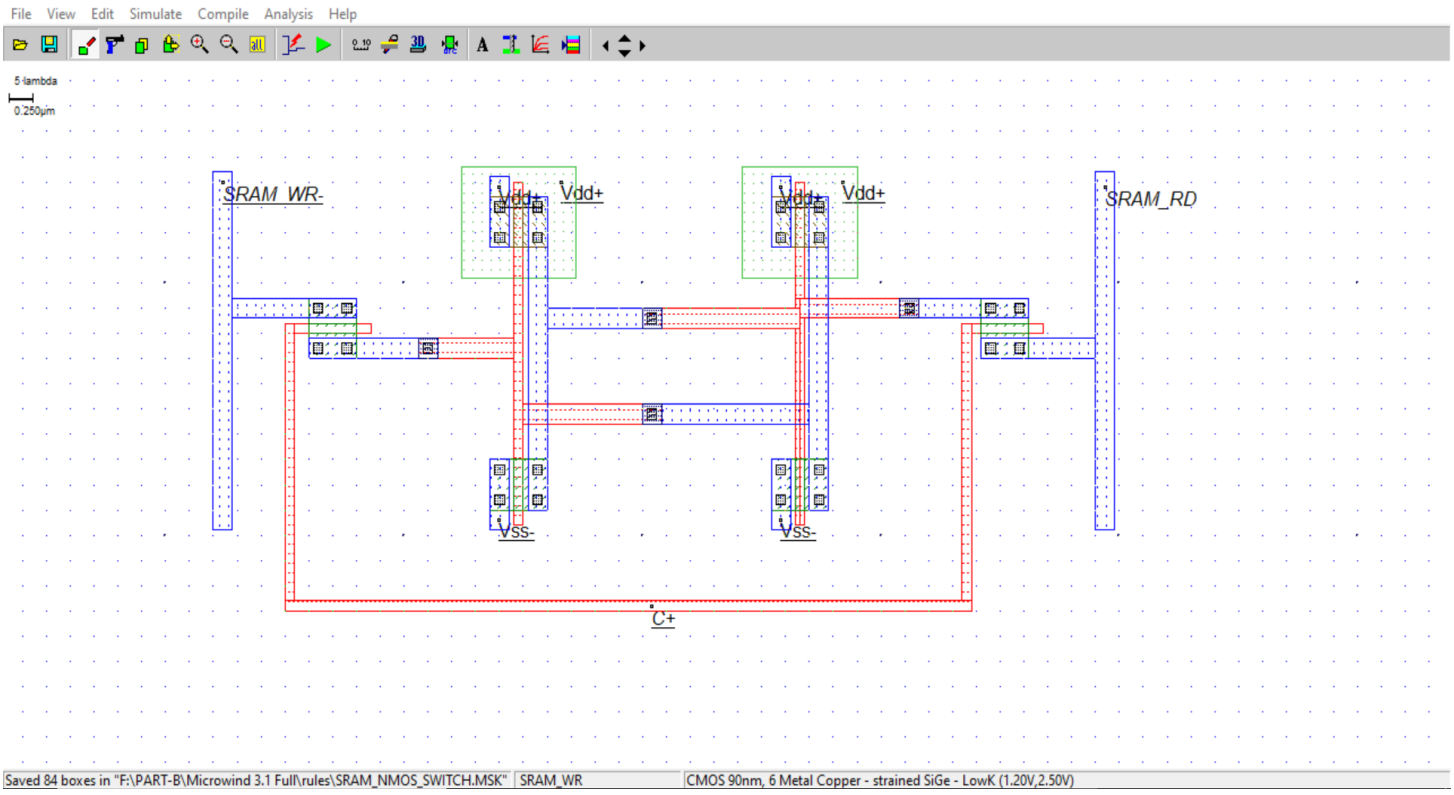
* TG1, TG2 : TG S/W's

* Function - Table

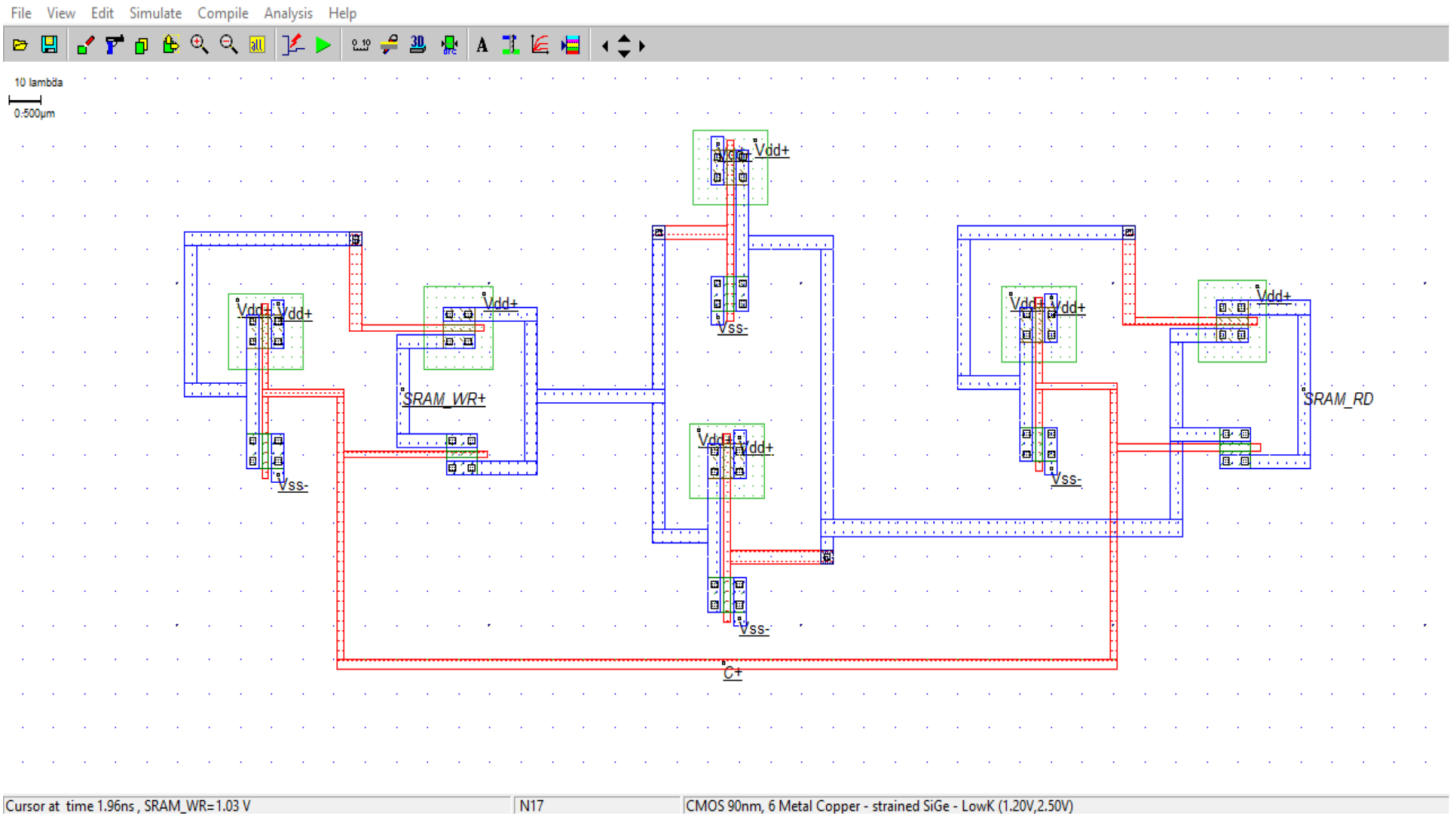
C	SRAM_WR	SRAM_RD
1	0	STRONG - 1
1	1	STRONG - 0
0	X	0 / HOLD

LAYOUT

1) 1-bit SRAM using NMOS Switches

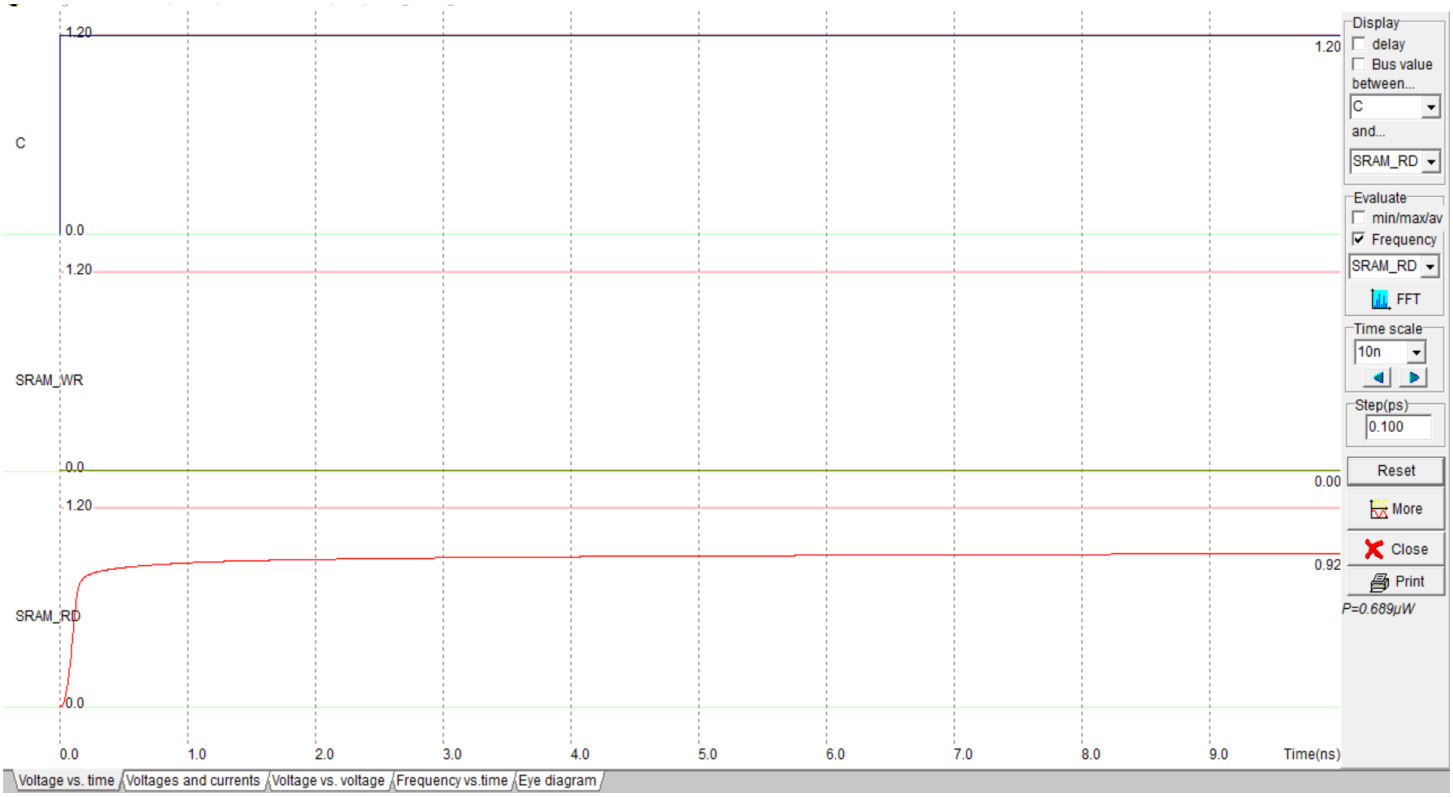


2) 1-bit SRAM cell using TG.

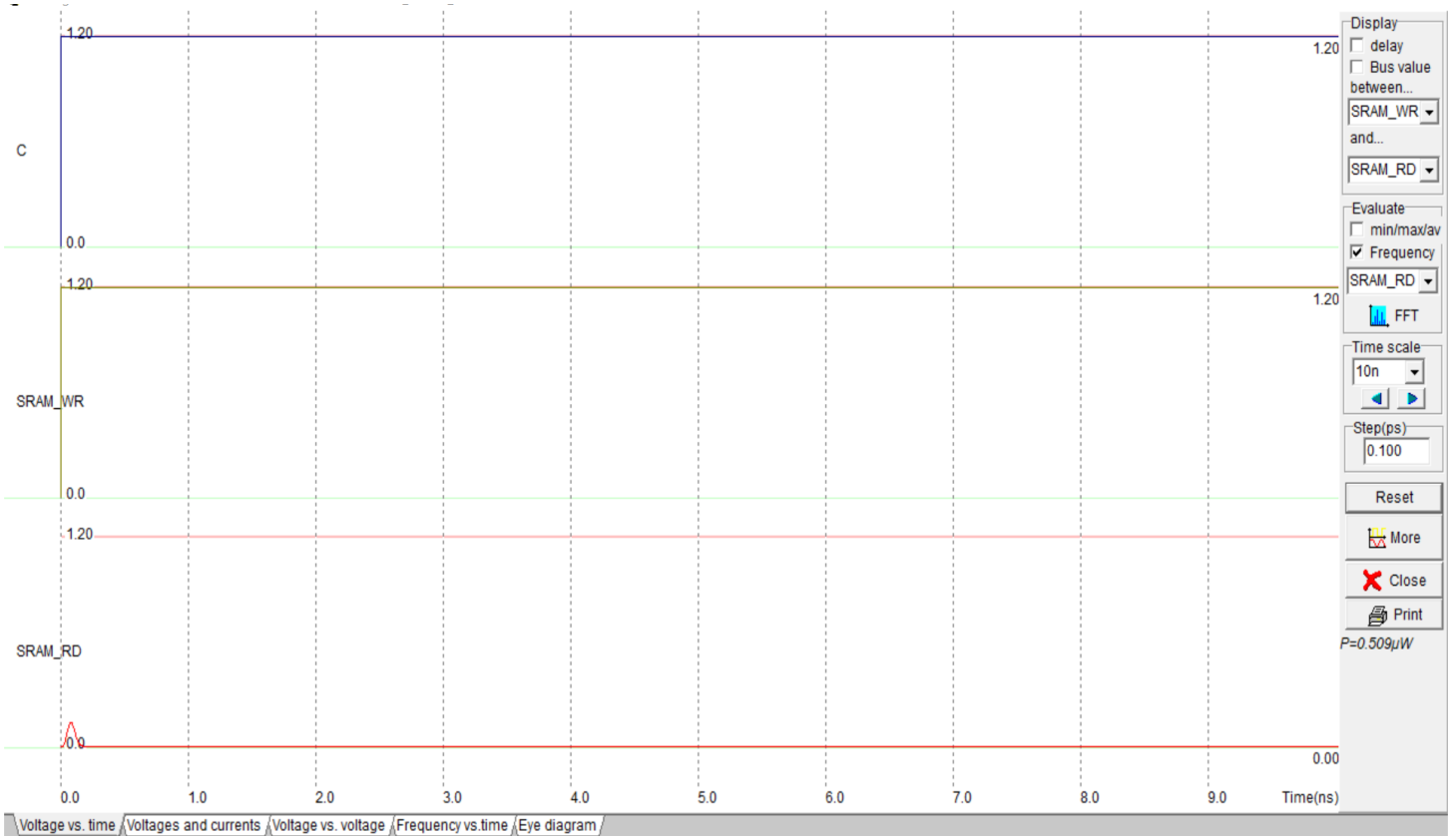


WAVEFORMS

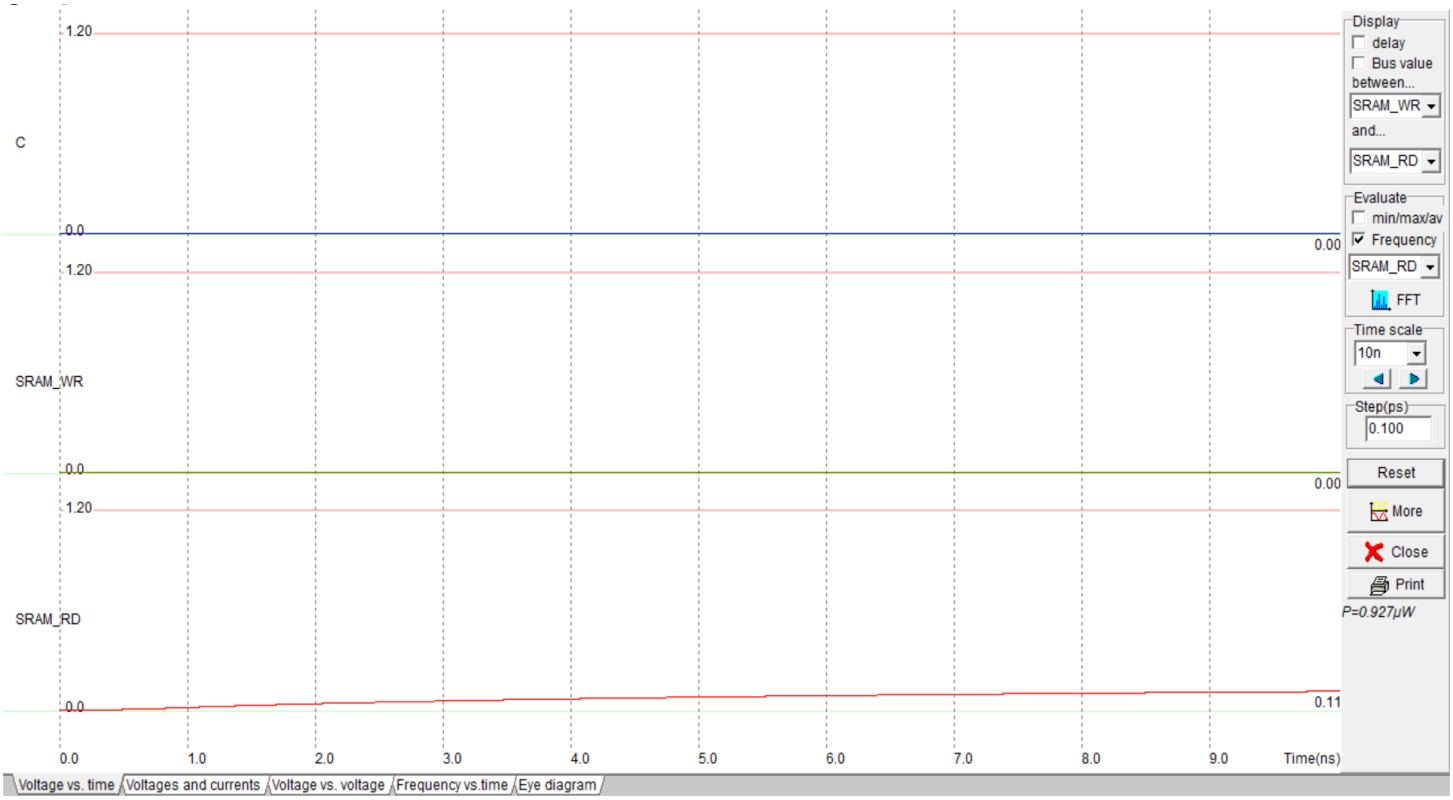
1. **C = 1, SRAM_WRITE = 0 using NMOS Switches.**



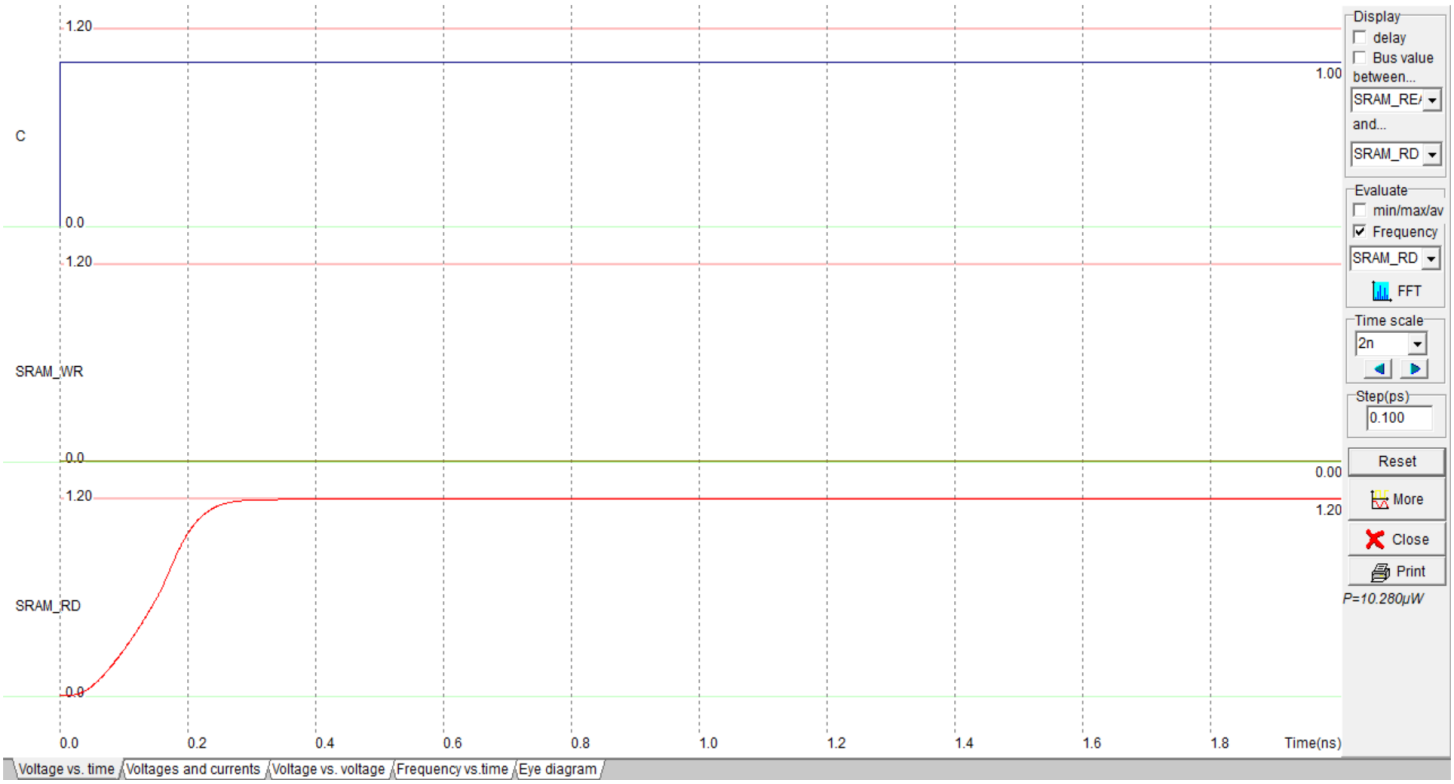
2. C =1, SRAM_WRITE=1 using NMOS Switches.



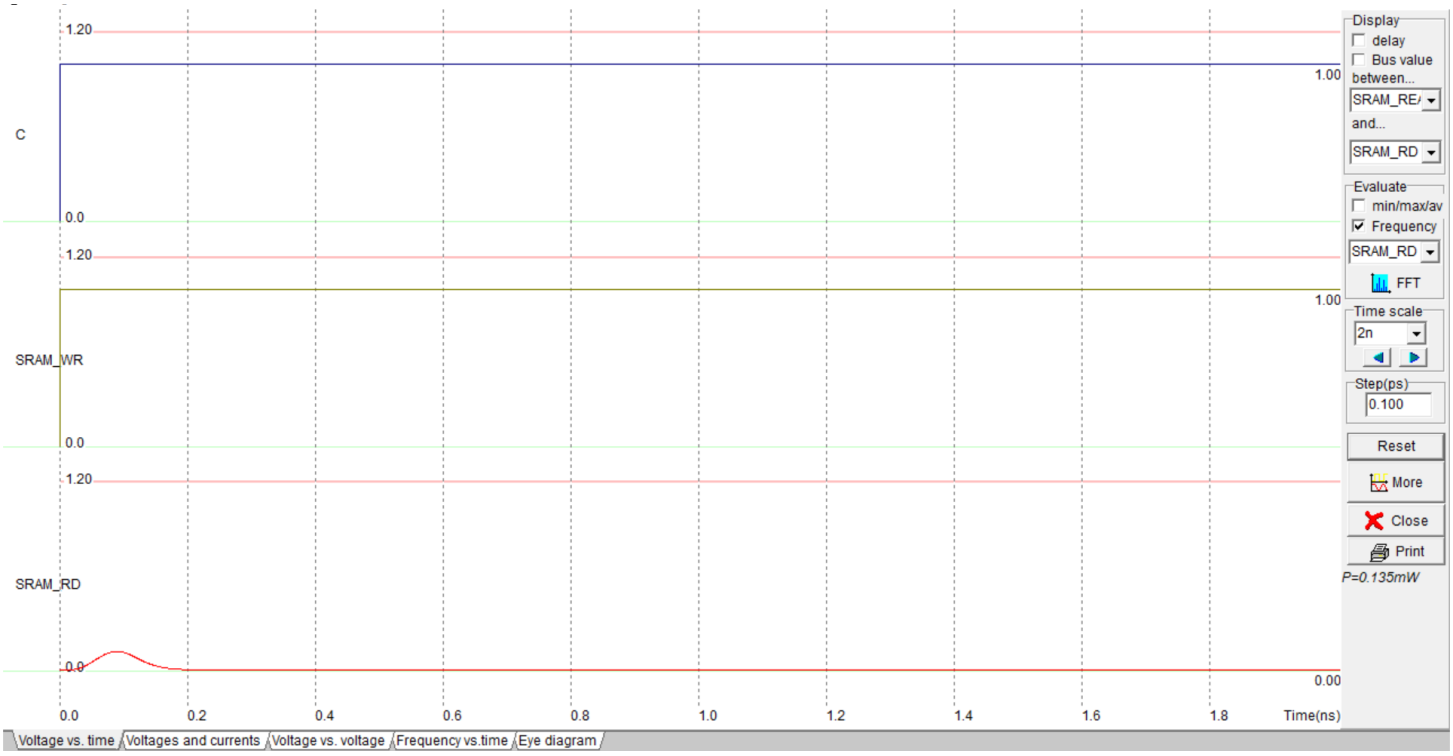
3. C = 0 using NMOS Switches.



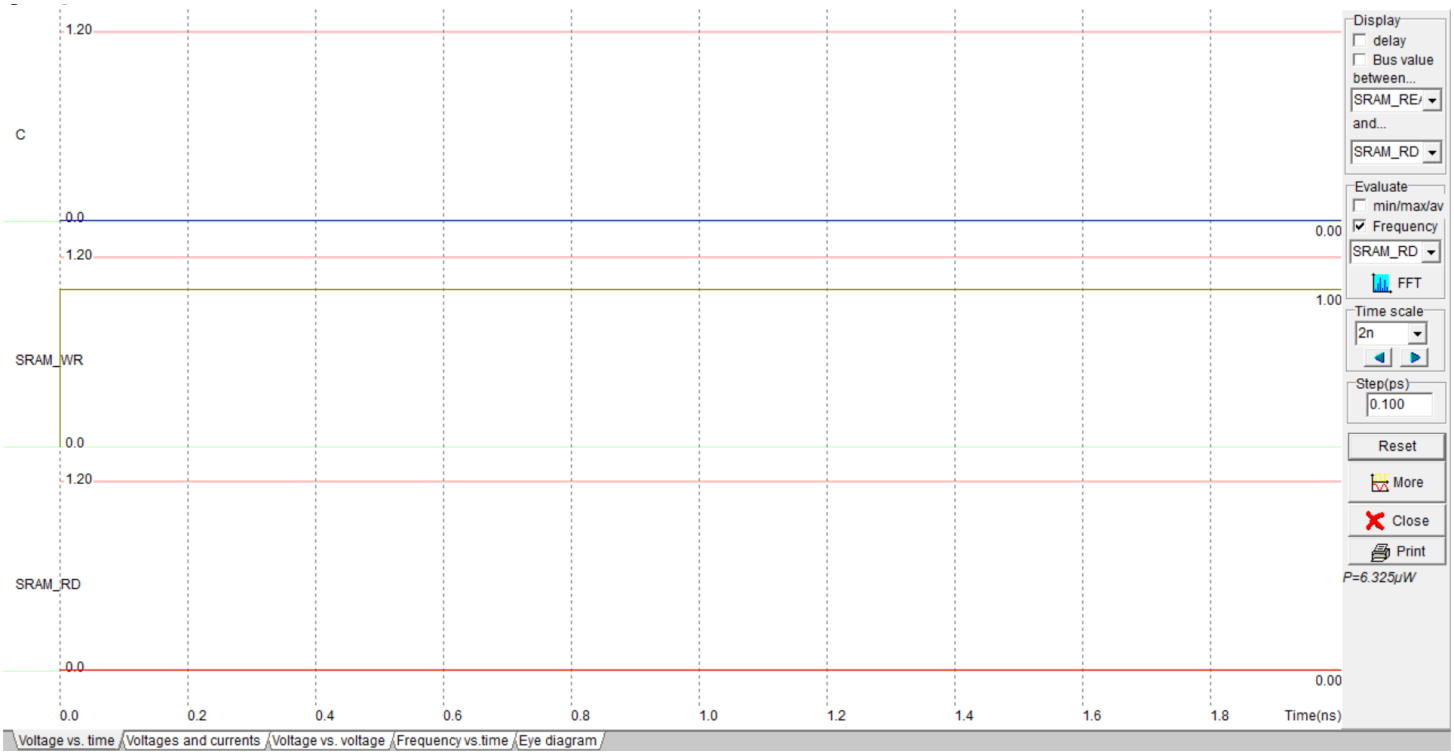
4. C =1, SRAM_WRITE=0 using TG Logic.



5. C =1, SRAM_WRITE=1 using TG Logic.



6. C =0 using TG Logic.



<u>Conclusions</u>:

Thus, we have:

1) Drawn the LAYOUT for 1-bit SRAM Cell using NMOS Switches and TG Switches using 90 nm Foundry.
2) Verified the waveforms of SRAM Cell.
3) Compared them with Truth table.
4) Verified the functionality of SRAM Cell.