

Respected Sir,

I think I'm a good fit for this internship opportunity because I have the right skills and experience. I have knowledge of **Verilog, System-Verilog, UVM and Linux Environment** which are important for this role. I am not from Tier 1 or Tier 2 college, still I deserve a chance to at least represent my skills. I have completed my Btech from KIET group of Institutions (2025 Passout). I have done **non-paid training from Cadence (Noida)**, now looking for internship/Entry Level Roles.

I have worked on two major projects **UVM/System Verilog** Based:

1. DDR Memory Controller – (<https://github.com/danishrana2604/DDR-MemoryController-UVM-Project> ). I wrote **coverage, monitor checks, data comparision, randomization** etc to verify the DUT. This helped me learn about memory systems and how to create a verification environment in advanced verification techniques using the Universal Verification Methodology (UVM).
2. APB (Bus Protocol) – (<https://github.com/danishrana2604/APB-RAM-System-VerilogProject> ). This project has enabled me to gain hands-on experience of design and verification in SystemVerilog.

Resume : ([https://github.com/danishrana2604/About-Me-DanishRana/blob/main/Danish%20Rana%20Resume%20\(1\).pdf](https://github.com/danishrana2604/About-Me-DanishRana/blob/main/Danish%20Rana%20Resume%20(1).pdf))

Please go through my detail resume. I am someone who values integrity and hard work, I appreciate organizations that prioritize these qualities. I am genuinely passionate about digital design verification and committed to continuous learning and growth.