

## DANISH RANA

danishrana.151@gmail.com | (+91) 9289786471 | [linkedin.com/in/danish-rana-1a467521a](https://www.linkedin.com/in/danish-rana-1a467521a)

### EXPERIENCE

- ❖ **Cadence Design Systems (India), Noida | Product Validation Trainee** (Apr'25 – Jul '25)
  - Working in AVS-Xcelium department, focusing on the creation of modular test banks using makefile targets and analyse testcases and submit comprehensive work on Perforce.
  - Gained hands-on experience with Linux Bash scripting, GVim and Perforce commands.
  - Utilized Cadence's Xcelium simulator for running simulations of digital designs.
- ❖ **VDT Pipeline Integrity Solutions, Noida | Electronics Embedded Intern** (Mar '25)
  - Worked with Microchip PolarFire SoC FPGA using Microchip Libero SoC Design Suite software to store data from sensors and store it in memory unit.

### SKILLS

Verilog	System Verilog	UVM (Universal Verification Methodology)
Bash Scripting	Makefile	Digital Electronics

### SOFTWARES

AMD Xilinx Vivado Design Suite	Cadence Simvision Simulator	Ardino IDE
Microchip Libero SoC Design Suite	Perforce Version Control	Linux

### ACADEMIC PROJECTS

- ❖ **Memory Controller** : UVM based testbench to drive commands like READ, Write, Activate and Precharge to simple DRAM DUT.
- ❖ **Traffic Light Controller** : System Verilog based project to design 4 way traffic lights.
- ❖ **Serial Communication Protocols [UART** (Universal Asynchronous Receiver/Transmitter), **SPI** (Serial Peripheral Interface) and **I2C** Protocol (Inter-Integrated Circuit)]
- ❖ **AMBA Protocols [APB** Protocol (Advanced Peripheral Bus), **AHB** Protocol (Advanced High-performance Bus)] and **AXI** Protocol (Advanced extensible Interface)]

#Note: All projects are done with design and testbench code in Systemverilog and UVM.

### COURSES & CERTIFICATIONS

- ❖ Udemy: Verification Series Part 1: System Verilog Fundamentals
- ❖ Udemy: Verification Series Part 2: System Verilog Projects
- ❖ Udemy: Verification Series Part 3: UVM Fundamentals
- ❖ Udemy: Verification Series Part 4: UVM Projects
- ❖ Udemy: Verilog for an FPGA Engineer with Xilinx Vivado Design Suite.

### EDUCATION

<b>B.Tech (ECE) (2021-25)</b>	KIET Group of Institutions Ghaziabad (AKTU)	7 CGPA
<b>12<sup>TH</sup> (PCM) (2020-21)</b>	K.D.B Public School, Ghaziabad (CBSE)	88.8%
<b>10<sup>TH</sup> (2018-19)</b>	K.D.B Public School, Ghaziabad (CBSE)	87.6%

### HOBBIES

- ❖ Learning through various courses on platforms such as Udemy, YouTube, and LinkedIn Learning.