Respected Sir,

I think I'm a good fit for this internship opportunity because I have the right skills and experience. I know how to use Verilog, System-Verilog and UVM which are important for this role. I am not from Tier 1 or Tier 2 college, still I deserve a chance to at least represent my skills. I have done non-paid training from Cadence (Noida), now looking for internship/Entry Level Roles.

I have worked on two big projects:

DDR Memory Controller – (https://github.com/danishrana2604/DDR-Memory-Controller-UVM-Project). This helped me learn about memory systems and how to test them.

APB (Bus Protocol) – (https://github.com/danishrana2604/APB-RAM-System-Verilog-Project). This taught me about communication between different parts of a computer

Resume : (https://github.com/danishrana2604/About-Me-Danish-Rana/blob/main/Danish%20Rana%20Resume%20(1).pdf) Please go through my detail resume.

I am who values integrity and hard work, I appreciate organizations that prioritize these qualities. I am genuinely passionate about digital design verification and committed to continuous learning and growth.