Memoria practica 3

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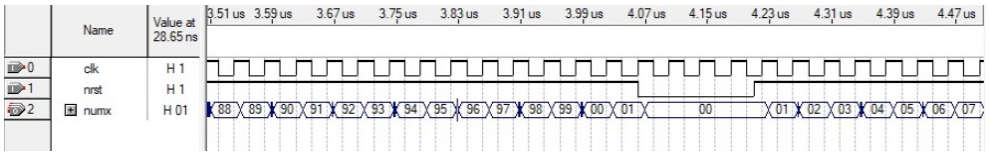
Índex

1 Part 1

1.1 Diseny Jerarquic

1.2 ComptadorBCD

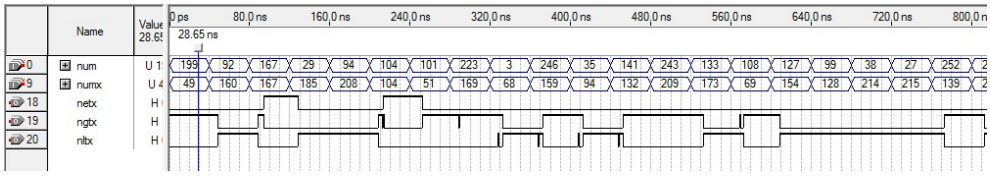
```
                library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_signed.all;

entity comptadorBCD is
        port (nrst, clk, ecnt : in std_logic;
                numx : out std_logic_vector(7 downto 0));
end comptadorBCD;

architecture compte of comptadorBCD is
        signal unitats, desenes : std_logic_vector (3 downto 0);

begin
        process(clk, nrst)
        begin
            if nrst = '0' then desenes <= "0000";
                        unitats <= "0000";
            elsif clk' event and clk='1' then
                if ecnt = '1' then
                if desenes = "1001" and unitats = "1001" then desenes <= "0000";
                        unitats <= "0000";
                elsif unitats = "1001" then desenes <= desenes +1;
                        unitats <= "0000";
                else unitats <= unitats+1;
                end if;
            end if;
        end if;
end process;
numx (7 downto 4) <= desenes;
numx (3 downto 0) <= unitats;

end compte;
```



Flow Status	Successful - Tue Dec 01 16:10:28 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	comptadorBCD
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	12 / 33,216 (< 1 %)
Total combinational functions	12 / 33,216 (< 1 %)
Dedicated logic registers	8 / 33,216 (< 1 %)
Total registers	8
Total pins	11 / 475 (2 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

1.3 ComparadorBCD

```
        library ieee;
use ieee.std_logic_1164.all;

entity comparadorBCD is
        port (numx,num : in std_logic_vector (7 downto 0);
                        ngtx,nltx,netx: out std_logic);
end comparadorBCD;

architecture comparador of comparadorBCD is
        begin
        ngtx <= '1' when num > numx else '0';
        netx <= '1' when num = numx else '0';
        nltx <= '1' when num < numx else '0';
end comparador;
```



Flow Status	Successful - Thu Dec 17 12:07:40 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	comparadorBCD
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	21 / 33,216 (< 1 %)
Total combinational functions	21 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	19 / 475 (4 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

1.4 Control

```
                library ieee;
use ieee.std_logic_1164.all;

entity control is
        port (nrst,clk,bcd,ast,coi,ngtx,netx,nltx : in std_logic;
                ecnt, eshft : out std_logic;
                led : out std_logic_vector(2 downto 0));
        end control;
```

```
architecture arcControl of control is
        type maquina is (inicial, intro_data, mostrar_resultat);
        signal estat: maquina;
begin
        process(clk, nrst) begin
        if nrst = '0' then estat <= inicial;
        elsif (clk'event and clk ='1') then
            case estat is
            when inicial => if ast = '1' then estat <= intro_data; end if;
            when intro_data => if coi = '1' and ast = '0' then estat <= mostrar_resultat;
                                                    elsif ast = '1' then estat <= inicial; end if;
            when mostrar_resultat => if ast = '1' then estat <= inicial;
                                     elsif netx = '1' then estat <= mostrar_resultat;
                                     elsif bcd = '1' then estat <= intro_data;
                                     end if;
            end case;
        end if;
end process;

ecnt <= '1' when estat = inicial else '0';
eshft <= '1' when (estat = intro_data or estat = mostrar_resultat) and bcd = '1' else '0';

led <= "111" when estat = inicial
    else "100" when estat = mostrar_resultat and nltx = '1'
        and netx= '0' and ngtx = '0'
    else "010" when estat = mostrar_resultat and netx = '1'
        and nltx = '0' and ngtx = '0'
    else "001" when estat = mostrar_resultat and ngtx = '1'
        and nltx = '0' and netx = '0'
    else "000";
end arcControl;
```

Aqui falte simulacio de Control

Flow Status	Successful - Thu Dec 17 12:13:17 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	control
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	11 / 33,216 (< 1 %)
Total combinational functions	11 / 33,216 (< 1 %)
Dedicated logic registers	3 / 33,216 (< 1 %)
Total registers	3
Total pins	13 / 475 (3 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

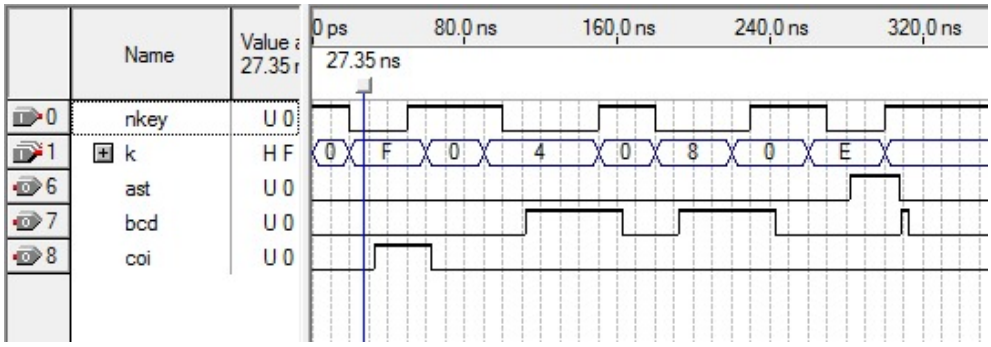
1.5 Registres

```
library ieee;
use ieee.std_logic_1164.all;

entity regs_v is
        port(clk, nrst, intro : in std_logic;
                keycode : in std_logic_vector(3 downto 0);
                opA, opB: out std_logic_vector(3 downto 0));
end regs_v;

architecture arq of regs_v is
signal a, b : std_logic_vector(3 downto 0);
begin
process (clk, nrst)
begin
        if(nrst = '0') then a <= "0000"; b <= "0000";
        elsif(nrst='1') and (clk'event and clk = '1') and (intro = '1') then
                        b <= a;
                        a <= keycode;
        end if;
end process;
opA <= a;
opB <= b;

end arq;
```

Flow Status	Successful - Thu Dec 17 18:29:47 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	regs_v
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	9 / 33,216 (< 1 %)
Total combinational functions	1 / 33,216 (< 1 %)
Dedicated logic registers	8 / 33,216 (< 1 %)
Total registers	8
Total pins	15 / 475 (3 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

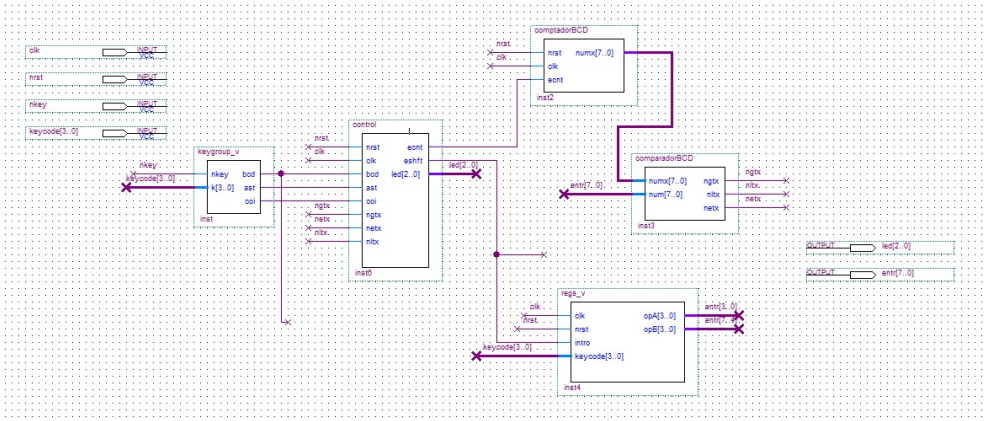
1.6 keygroup

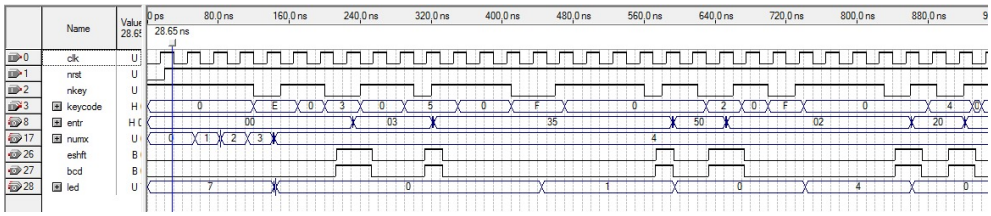
```
        library ieee;
use ieee.std_logic_1164.all;

entity keygroup_v is
        port(nkey : in std_logic;
                k : in std_logic_vector(3 downto 0);
                bcd, ast, coi : out std_logic);
end keygroup_v;

architecture arq of keygroup_v is
begin
process (nkey, k)
begin
        if (nkey = '0' and (k = "0000" or k = "0001" or k = "0010" or
                                                k = "0011" or k = "0100" or k = "0101" or
                                                k = "0110" or k = "0111" or k = "1000" or
                                                k = "1001")) then bcd <= '1'; ast <= '0'; coi <= '0';
        elsif(nkey = '0' and k = "1110")
                        then bcd <= '0'; ast <= '1'; coi <= '0';
        elsif(nkey = '0' and k = "1111")
                        then bcd <= '0'; ast <= '0'; coi <= '1';
        elsif(nkey = '1') then bcd <= '0'; ast <= '0'; coi <= '0';
        end if;
end process;
end arq;
```



Flow Status	Successful - Thu Dec 17 18:26:49 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	keygroup_v
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	10 / 33,216 (< 1 %)
Total combinational functions	10 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	8 / 475 (2 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

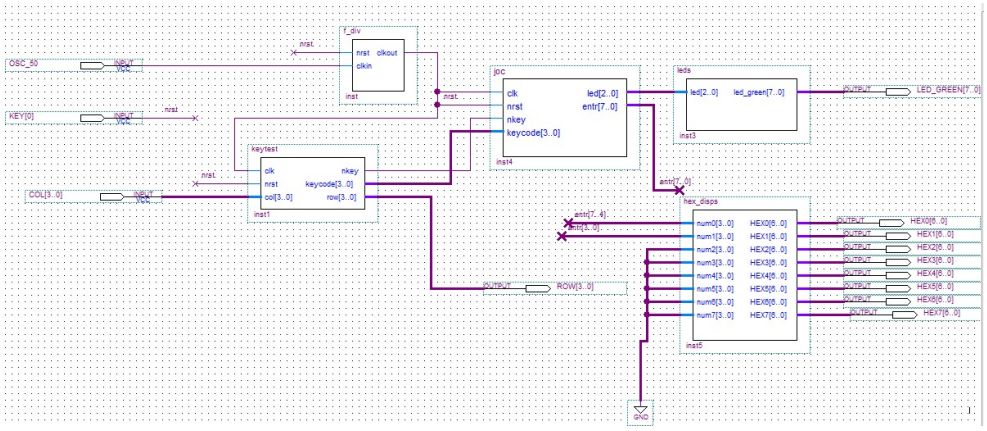
1.7 Joc


clk
nrst
nkey
keycode[3..0]
keygroup_v
inst
control
inst0
comptadorBCD
inst2
comparadorBCD
inst3
regs_v
inst4
led[2..0]
entr[7..0]
OUTPUT


Name
clk
nrst
nkey
keycode
entr
numx
eshft
bcd
led
28.65 ns

Flow Status	Successful - Thu Dec 17 18:36:42 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	joc
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	55 / 33,216 (< 1 %)
Total combinational functions	55 / 33,216 (< 1 %)
Dedicated logic registers	19 / 33,216 (< 1 %)
Total registers	19
Total pins	18 / 475 (4 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

1.8 Joc Placa



2 Part Extra

2.1 ComptadorBCD Extra

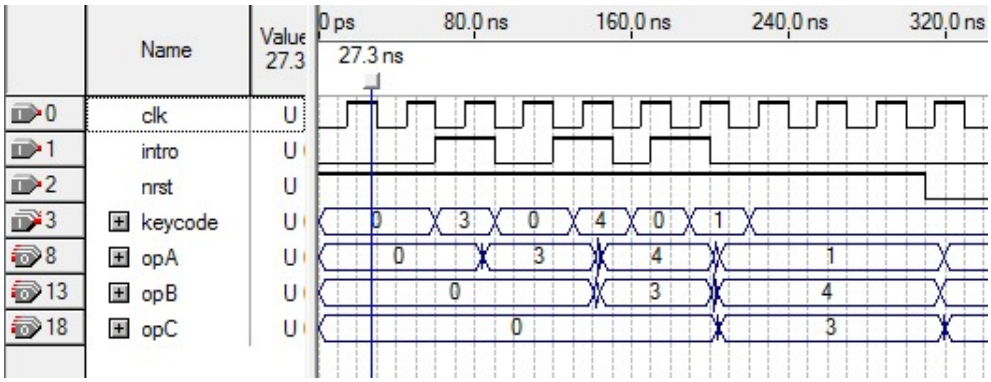
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_signed.all;

entity comptadorBCD_extra is
        port (nrst, clk, ecnt : in std_logic;
                numx : out std_logic_vector(11 downto 0));
end comptadorBCD_extra;

architecture compte of comptadorBCD_extra is
        signal unitats, desenes, centenes : std_logic_vector (3 downto 0);

begin
        process(clk, nrst)
        begin
            if nrst = '0' then desenes <= "0000";
                        unitats <= "0000"; centenes <= "0000";
            elsif clk' event and clk='1' then
                if ecnt = '1' then
                if desenes = "1001" and unitats = "1001" and centenes = "1001"
                        then desenes <= "0000"; unitats <= "0000"; centenes <= "0000";
                elsif desenes = "1001" and unitats = "1001" then centenes <= centenes + 1;
                        desenes <= "0000"; unitats <= "0000";
                elsif unitats = "1001" then desenes <= desenes + 1;
                        unitats <= "0000";
                else unitats <= unitats+1;
                end if;
            end if;
        end if;
end process;
numx (11 downto 8) <= centenes;
numx (7 downto 4) <= desenes;
numx (3 downto 0) <= unitats;

end compte;
```

Flow Status	Successful - Thu Dec 17 19:05:57 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	comptadorBCD_extra
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	20 / 33,216 (< 1 %)
Total combinational functions	20 / 33,216 (< 1 %)
Dedicated logic registers	12 / 33,216 (< 1 %)
Total registers	12
Total pins	15 / 475 (3 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2.2 Registres Extra

```
        library ieee;
use ieee.std_logic_1164.all;

entity regs_extra is
        port(clk, nrst, intro : in std_logic;
                keycode : in std_logic_vector(3 downto 0);
                opA, opB, opC: out std_logic_vector(3 downto 0));
end regs_extra;

architecture arq of regs_extra is
signal a, b, c : std_logic_vector(3 downto 0);
begin
process (clk, nrst)
begin
        if(nrst = '0') then a <= "0000"; b <= "0000"; c <= "0000";
        elsif(nrst='1') and (clk'event and clk = '1') and (intro = '1') then
                        c <= b;
                        b <= a;
                        a <= keycode;
        end if;
end process;
opA <= a;
opB <= b;
opC <= c;
```

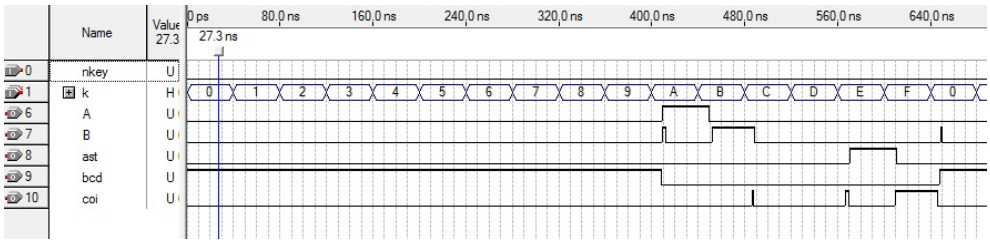
```
end arq;
```



Flow Status	Successful - Thu Dec 17 19:01:16 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	regs_extra
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	13 / 33,216 (< 1 %)
Total combinational functions	1 / 33,216 (< 1 %)
Dedicated logic registers	12 / 33,216 (< 1 %)
Total registers	12
Total pins	19 / 475 (4 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2.3 Keygroup Extra

```
library ieee;
use ieee.std_logic_1164.all;

entity keygroup_extra is
        port(nkey : in std_logic;
                k : in std_logic_vector(3 downto 0);
                bcd, ast, coi, A, B : out std_logic);
end keygroup_extra;

architecture arq of keygroup_extra is
begin
process (nkey, k)
begin
        if (nkey = '0' and (k = "0000" or k = "0001" or k = "0010" or
                                                k = "0011" or k = "0100" or k = "0101" or
                                                k = "0110" or k = "0111" or k = "1000" or
                                                k = "1001")) then bcd <= '1'; ast <= '0'; coi <= '0'; A <= '0'; B <
        elsif(nkey = '0' and k = "1010") then bcd <= '0'; ast <= '0'; coi <= '0'; A <= '1'; B <= '0';
        elsif(nkey = '0' and k = "1011") then bcd <= '0'; ast <= '0'; coi <= '0'; A <= '0'; B <= '1';
        elsif(nkey = '0' and k = "1110") then bcd <= '0'; ast <= '1'; coi <= '0'; A <= '0'; B <= '0';
        elsif(nkey = '0' and k = "1111") then bcd <= '0'; ast <= '0'; coi <= '1'; A <= '0'; B <= '0';
        elsif(nkey = '1') then bcd <= '0'; ast <= '0'; coi <= '0'; A <= '0'; B <= '0';
        else bcd <= '0'; ast <= '0'; coi <= '0'; A <= '0'; B <= '0';
        end if;
end process;
end arq;
```



Flow Status	Successful - Thu Dec 17 19:07:41 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	keygroup_extra
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	7 / 33,216 (< 1 %)
Total combinational functions	7 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	10 / 475 (2 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2.4 Control Extra

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity control_extra is
        port (nrst,clk,bcd,ast,coi,A,B,ngtx,netx,nltx : in std_logic;
                ecnt, eshft : out std_logic;
                led : out std_logic_vector(2 downto 0);
                tot : out std_logic_vector(3 downto 0));
        end control_extra;

architecture arcControl of control_extra is
        type maquina is (inicial, intro_data, mostrar_resultat, trampa_A, trampa_B);
        signal estat: maquina;
        signal t : std_logic_vector(3 downto 0);
begin
        process(clk, nrst) begin
        if nrst = '0' then estat <= inicial;
        elsif (clk'event and clk ='1') then
            case estat is
            when inicial => if ast = '1' then estat <= intro_data; end if;
            when intro_data => if coi = '1' and ast = '0' then estat <= mostrar_resultat;
                                                elsif ast = '1' then estat <= inicial;
                                                elsif A = '1' then estat <= trampa_A;
```

```
                                                elsif B = '1' then estat <= trampa_B; end if;
            when mostrar_resultat => if ast = '1' then estat <= inicial;
                                     elsif bcd = '1' then estat <= intro_data;
                                     elsif A = '1' then estat <= trampa_A;
                                     elsif B = '1' then estat <= trampa_B;
                                     end if;
                when trampa_A => if ast = '1' then estat <= inicial;
                                     elsif bcd = '1' then estat <= intro_data;
                                     elsif B = '1' then estat <= trampa_B;
                                     end if;
                when trampa_B => if ast = '1' then estat <= inicial;
                                     elsif bcd = '1' then estat <= intro_data;
                                     elsif A = '1' then estat <= trampa_A;
                                     end if;
                end case;
                if(netx = '1' and estat = intro_data) then t <= t + 1; estat <= inicial; end if;
        end if;
end process;
tot <= t;

ecnt <= '1' when estat = inicial else '0';
eshft <= '1' when (estat = intro_data or estat = mostrar_resultat) and bcd = '1' else '0';

led <= "111" when estat = inicial
    else "100" when estat = mostrar_resultat and nltx = '1'
        and netx= '0' and ngtx = '0'
    else "010" when estat = mostrar_resultat and netx = '1'
        and nltx = '0' and ngtx = '0'
    else "001" when estat = mostrar_resultat and ngtx = '1'
        and nltx = '0' and netx = '0'
    else "110" when estat = trampa_A
    else "011" when estat = trampa_B
    else "000";
end arcControl;
```

Flow Status	Successful - Thu Dec 17 19:09:23 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	control_extra
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	50 / 33,216 (< 1 %)
Total combinational functions	50 / 33,216 (< 1 %)
Dedicated logic registers	9 / 33,216 (< 1 %)
Total registers	9
Total pins	19 / 475 (4 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2.5 Trampes

```
library ieee;
use ieee.std_logic_1164.all;

entity trampes is
        port(tr : in std_logic_vector(2 downto 0);
                num: in std_logic_vector(11 downto 0);
                mostra: out std_logic_vector(3 downto 0));
end trampes;

architecture arq of trampes is
begin
process (tr)
begin
        if tr = "110" then mostra <= num(3 downto 0);
        elsif tr = "011" then mostra <= num(7 downto 4);
        else mostra <= "0000";
        end if;
end process;
end arq;
```

Flow Status	Successful - Thu Dec 17 19:18:19 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	trampes
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	6 / 33,216 (< 1 %)
Total combinational functions	6 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	19 / 475 (4 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2.6 Leds

```
        library ieee;
use ieee.std_logic_1164.all;

entity led_extra is
        port(led: in std_logic_vector(2 downto 0);
                num : in std_logic_vector(3 downto 0);
                led_green : out std_logic_vector(7 downto 0);
                led_level : out std_logic_vector(7 downto 0));
end led_extra;

architecture arq of led_extra is
begin
        led_green <= "11111111" when led = "111" else
                                "11110000" when led = "100" else
                                "00001111" when led = "001" else
                                "00111100" when led = "010" else
                                "00000000" when led = "000" else
                                "01010101" when led = "110" else
                                "10101010" when led = "011";
        led_level <= "00000000" when num = "0000" else
                                "10000000" when num = "0001" else
                                "11000000" when num = "0010" else
                                "11100000" when num = "0011" else
                                "11110000" when num = "0100" else
```

```
                                    "11111000" when num = "0101" else
                                    "11111100" when num = "0110" else
                                    "11111110" when num = "0111" else
                                    "11111111" when num = "1000";

end arq;
```

Flow Status	Successful - Thu Dec 17 19:19:14 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	led_extra
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	43 / 33,216 (< 1 %)
Total combinational functions	43 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	23 / 475 (5 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2.7 Temporitzador

```
        library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_signed.all;

entity temporitzador is
        port (nrst, clk, ecnt : in std_logic;
                numx : out std_logic_vector(7 downto 0));
end temporitzador;

architecture compte of temporitzador is
        signal unitats, desenes : std_logic_vector (3 downto 0);

begin
        process(clk, nrst)
        begin
```

```
            if nrst = '0' then desenes <= "1001";
                        unitats <= "1001";
            elsif clk' event and clk='1' then
                if ecnt = '1' then
                if desenes = "0000" and unitats = "0000" then desenes <= "0000";
                        unitats <= "0000";
                elsif unitats = "0000" then desenes <= desenes -1;
                        unitats <= "1001";
                else unitats <= unitats-1;
                end if;
            end if;
        end if;
end process;
numx (7 downto 4) <= desenes;
numx (3 downto 0) <= unitats;

end compte;
```

Flow Status	Successful - Thu Dec 17 19:20:20 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	temporitzador
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	13 / 33,216 (< 1 %)
Total combinational functions	13 / 33,216 (< 1 %)
Dedicated logic registers	8 / 33,216 (< 1 %)
Total registers	8
Total pins	11 / 475 (2 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

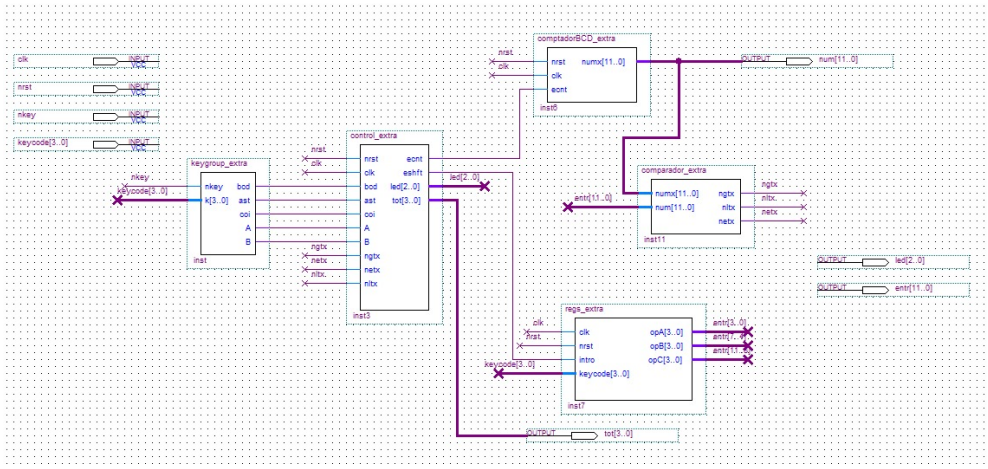
2.8 Slow Timer

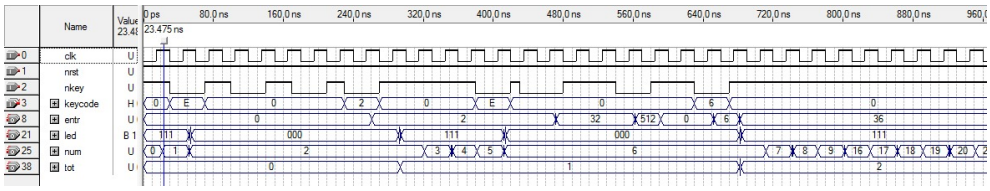
```
        -- Frequency divider by M
-- D = output duty cycle in %
-- version DD-1.0 - march 2011
```

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity slow_timer is
  port( nrst,clkin : in std_logic;
        clkout : out std_logic );
end slow_timer;

architecture dni of slow_timer is
constant M : integer :=750;
constant D : integer :=50;
constant n : integer :=D*M/100;
signal q : integer range 0 to M-1;
begin
  process(clkin,nrst) begin
     if nrst='0' then clkout <= '0'; q <= 0;
     elsif clkin'event and clkin='1' then
         if q < M-1 then q <= q+1;
            else q <= 0; end if;
         if q < n then clkout <= '1';
            else clkout <= '0'; end if;
     end if;
  end process;
end dni;
```

Flow Status	Successful - Thu Dec 17 19:31:34 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	slow_timer
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	16 / 33,216 (< 1 %)
Total combinational functions	16 / 33,216 (< 1 %)
Dedicated logic registers	11 / 33,216 (< 1 %)
Total registers	11
Total pins	3 / 475 (< 1 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2.9 Joc Extra


clk
nrst
nkey
keycode[3..0]
keygroup_extra
inst
control_extra
inst3
comptadorBCD_extra
inst6
comparador_extra
inst11
regs_extra
inst7
led[2..0]
entr[11..0]
num[11..0]
tot[3..0]


Name
clk
nrst
nkey
keycode
entr
led
num
tot

Flow Status	Successful - Thu Dec 17 19:22:34 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	practica3
Top-level Entity Name	joc_extra2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	291 / 33,216 (< 1 %)
Total combinational functions	291 / 33,216 (< 1 %)
Dedicated logic registers	86 / 33,216 (< 1 %)
Total registers	86
Total pins	82 / 475 (17 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2.10 Joc Extra Placa