

# **INTRODUCTION TO ELECTRONICS AND COMMUNICATION ENGINEERING (25ESC131)**

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# MODULE 1

## Introduction to materials used in electronics

### Materials used in electronics

1. Conductors
2. Insulators
3. Semiconductors

**Conductors-** A conductor is a material that easily conducts electrical current. Most metals are good conductors, which are characterized by atoms with only one valence electron very loosely bound to the atom. These loosely bound valence electrons become free electrons. Therefore, in a conductive material the free electrons are valence electrons.

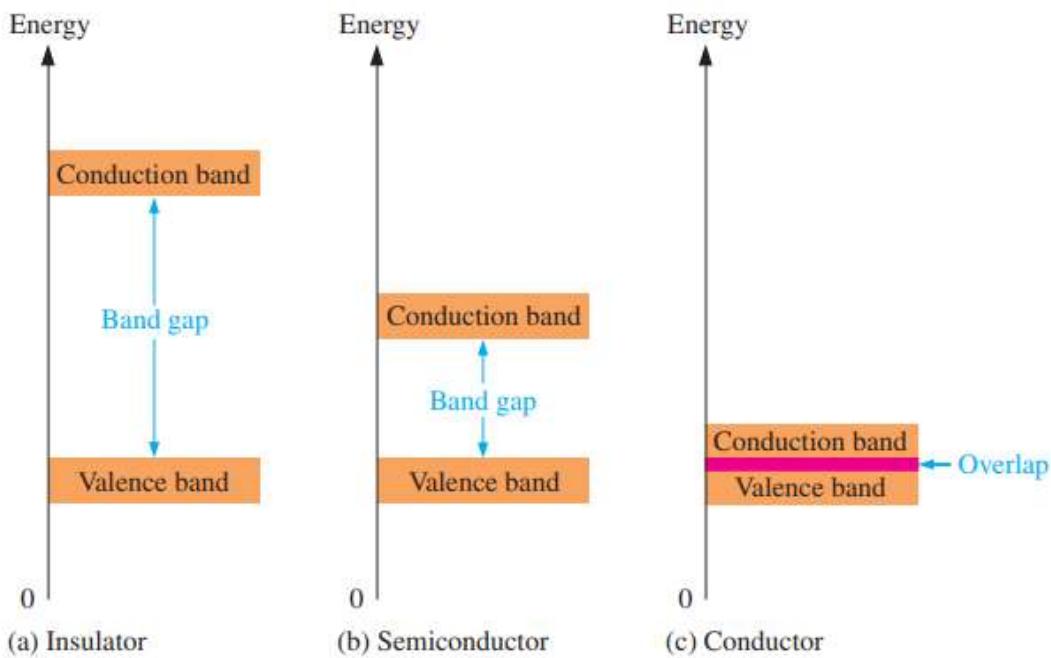
Examples of conductors are copper (Cu), silver (Ag), gold (Au), and aluminum (Al)

**Insulators-** An insulator is a material that does not conduct electrical current under normal conditions. □  
Most good insulators are compounds rather than single-element materials and have very high resistivity. □  
Valence electrons are tightly bound to the atoms; therefore, there are very few free electrons in an insulator.

Examples of insulators are rubber, plastics, glass, and quartz.

**Semiconductors-** A semiconductor is a material that is between conductors and insulators in its ability to conduct electrical current.

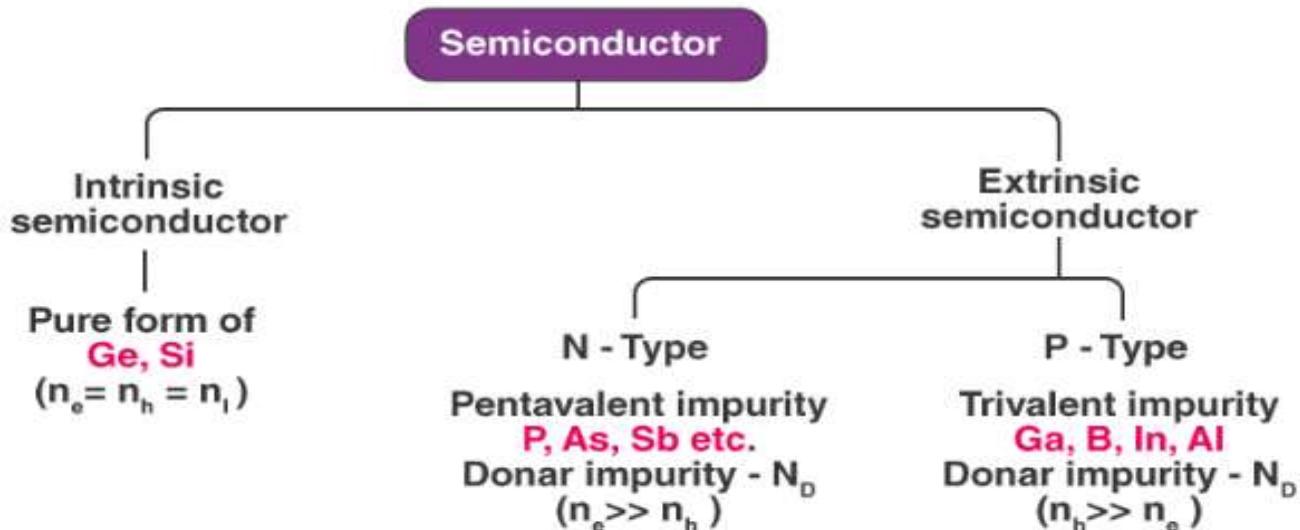
Examples of semiconductors are antimony (Sb), arsenic (As), boron (B), silicon (Si), and germanium (Ge).



## Types of Semiconductors

Semiconductors can be classified as follows:

- Intrinsic Semiconductor
- Extrinsic Semiconductor



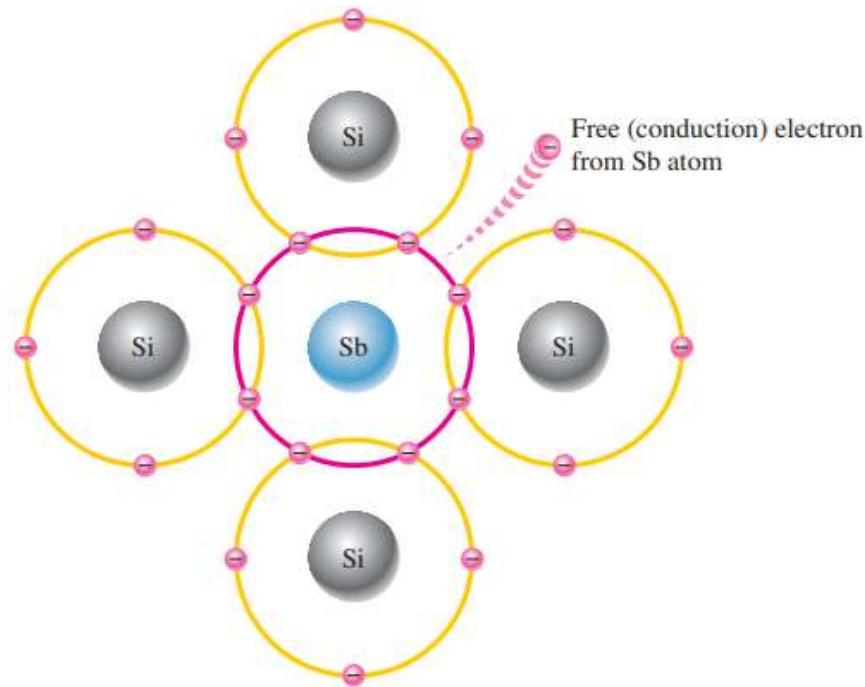
### Classification of Semiconductors

Since semiconductors are generally poor conductors, their conductivity can be drastically increased by the controlled addition of impurities to the intrinsic (pure) semiconductive material. This process, called **doping**, increases the number of current carriers (electrons or holes). The two categories of impurities are n-type and p-type.

## **N-Type Semiconductor**

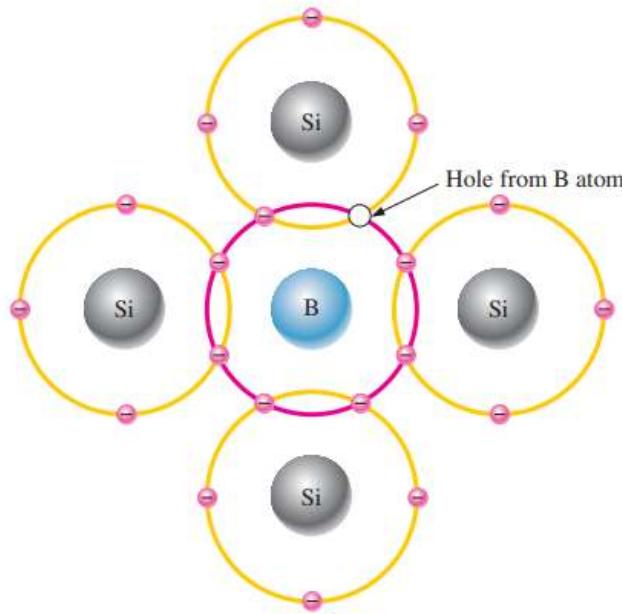
To increase the number of conduction-band electrons in intrinsic silicon, pentavalent impurity atoms are added. These are atoms with five valence electrons such as arsenic (As), phosphorus (P), bismuth (Bi), and antimony (Sb).

each pentavalent atom (antimony, in this case) forms covalent bonds with four adjacent silicon atoms. Four of the antimony atom's valence electrons are used to form the covalent bonds with silicon atoms, leaving one extra electron. This extra electron becomes a conduction electron because it is not involved in bonding. Because the pentavalent atom gives up an electron, it is often called a donor atom.



**The electrons are called the majority carriers and Holes are minority charge carriers**

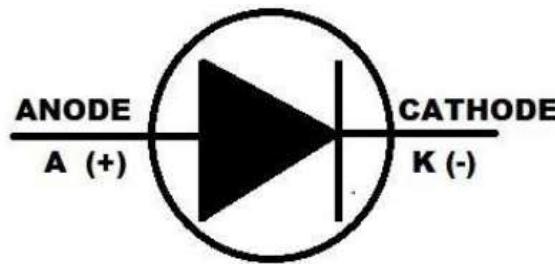
O-Type Semiconductor To increase the number of holes in intrinsic silicon, trivalent impurity atoms are added. These are atoms with three valence electrons such as boron (B), indium (In), and gallium (Ga). As illustrated in fig , each trivalent atom (boron, in this case) forms covalent bonds with four adjacent silicon atoms. All three of the boron atom's valence electrons are used in the covalent bonds; and, since four electrons are required, a hole results when each trivalent atom is added. Because the trivalent atom can take an electron, it is often referred to as an **acceptor atom**.



**The Holes are called the majority carriers and Electrons are minority charge carriers**

## P-N Junction diode – operation, characteristics

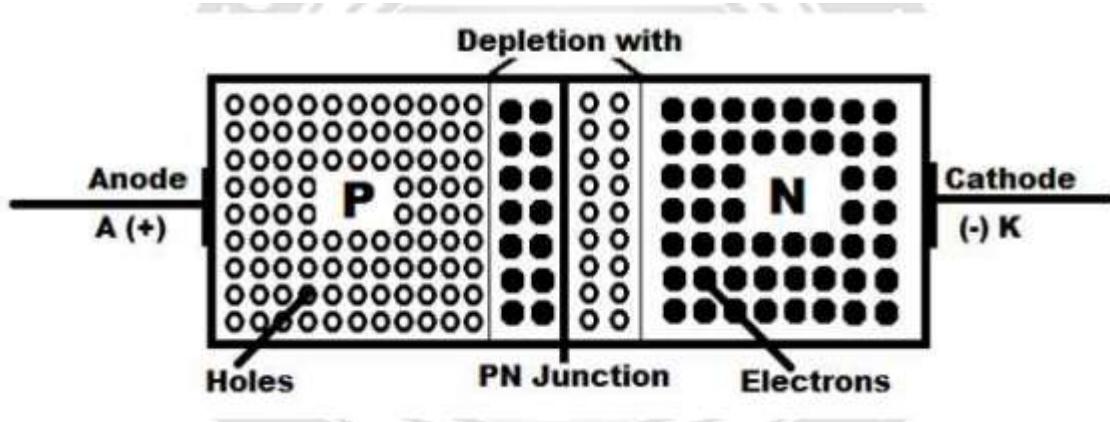
PN JUNCTION DIODE A diode is a device which only allows unidirectional flow of current if operated within a rated specified voltage level. A diode only blocks current in the reverse direction while the reverse voltage is within a limited range otherwise reverse barrier breaks and the voltage at which this breakdown occurs is called reverse breakdown voltage. The diode acts as a valve in the electronic and electrical circuit. A P-N junction is the simplest form of the diode which behaves as ideally short circuit when it is in forward biased and behaves as ideally open circuit when it is in the reverse biased. SYMBOL OF DIODE The name diode is derived from "di-ode" which means a device having two electrodes.



A simple PN junction diode by doping donor impurity in one portion and acceptor impurity in other portion of silicon or germanium crystal block. These make a p n junction at the middle part of the block beside which one portion is p-type (doped with trivalent or acceptor impurity), and another portion is n-type (doped with pentavalent or donor impurity). It can also be formed by joining a p-type (semiconductor doped with a

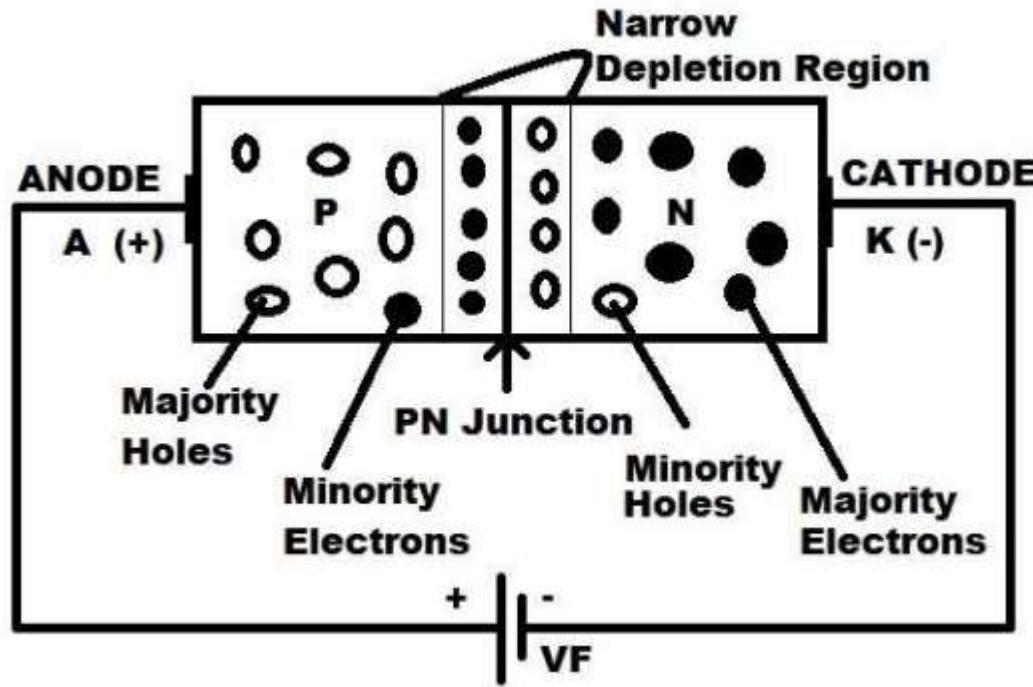
trivalent impurity) and n-type semiconductor (intrinsic semiconductor doped with a pentavalent impurity) together with a special fabrication technique such that a p-n junction is formed. It can also be formed by joining a p-type (semiconductor doped with a trivalent impurity) and n-type semiconductor (intrinsic semiconductor doped with a pentavalent impurity) together with a special fabrication technique such that a p-n junction is formed.

**CONSTRUCTION** The p-type forms anode and the n-type forms the cathode. These terminals are brought out to make the external connections. N-side will have a significant number of electrons, and very few holes (due to thermal excitation) whereas the p side will have a high concentration of holes and very few electrons. Due to this, a process called diffusion takes place. In this process free electrons from n side will diffuse (spread) into the p side and recombine with holes present there, leaving positive immobile (not moveable) ions in n side and creating negative immobile ions in p side of the diode. Hence, there will be uncovered positive donor ions in n-type side near the junction edge.

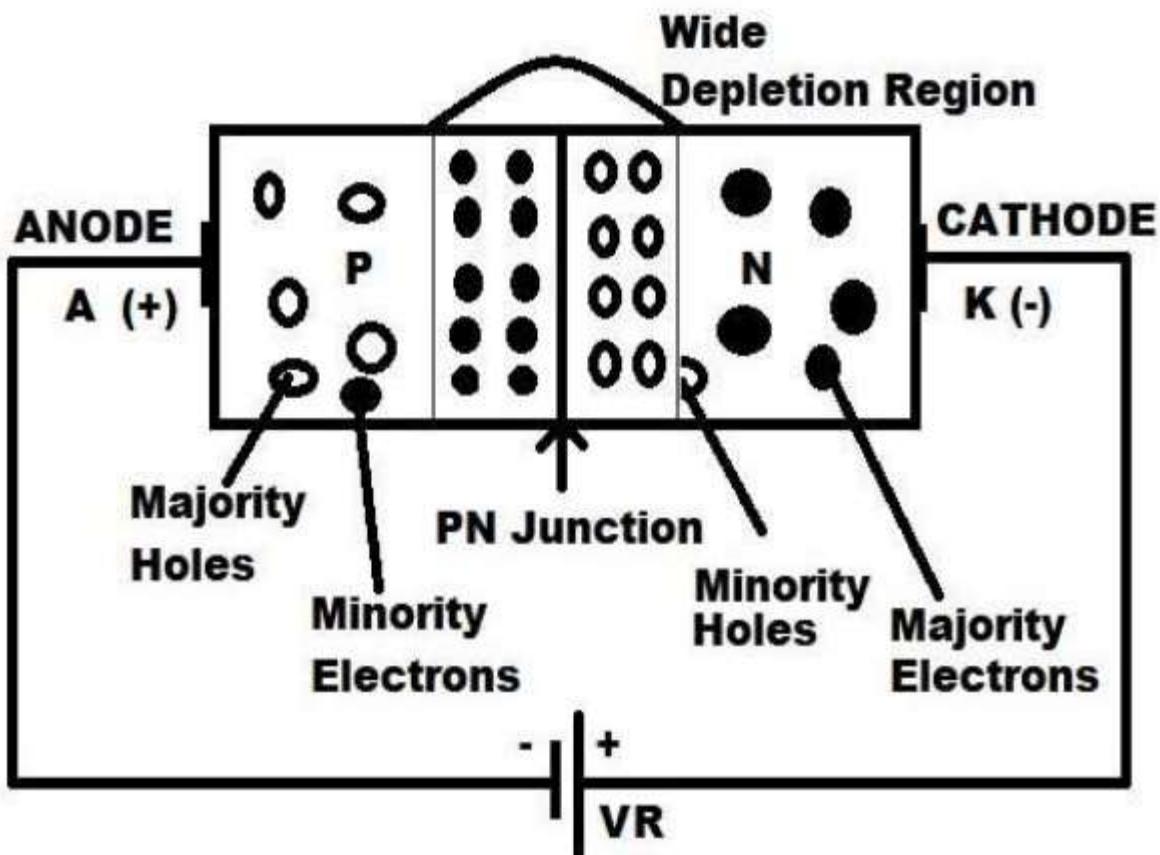


Similarly, there will be uncovered negative acceptor ions in p-type side near the junction edge. Due to this, numbers of positive ions and negative ions will accumulate on n-side and p-side respectively. This region so formed is called as depletion region due to the "depletion" of free carriers in the region. Due to the presence of these positive and negative ions a static electric field called as barrier potential is created across the pn junction of the diode. It is called as "barrier potential" because it acts as a barrier and opposes the further migration of holes and electrons across the junction. **FORWARD BIAS** In a PN junction diode when the forward voltage is applied i.e. positive terminal of a source is connected to the p-type side, and the negative terminal of the source is connected to the n-type side, the diode is said to be in forward biased condition.

There is a barrier potential across the junction. This barrier potential is directed in the opposite of the forward applied voltage. So a diode can only allow current to flow in the forward direction when forward applied voltage is more than barrier potential of the junction. This voltage is called forward biased voltage. For silicon diode, it is 0.7 volts. For germanium diode, it is 0.3 volts.



When forward applied voltage is more than this forward biased voltage, there will be forward current in the diode, and the diode will become short circuited. Hence, there will be no more voltage drop across the diode beyond this forward biased voltage, and forward current is only limited by the external resistance connected in series with the diode. Thus, if forward applied voltage increases from zero, the diode will start conducting only after this voltage reaches just above the barrier potential or forward biased voltage of the junction. The time taken by this input voltage to reach that value or in other words, the time taken by this input voltage to overcome the forward biased voltage is called recovery time. REVERSE BIAS The diode is reverse biased i.e. positive terminal of the source is connected to the n-type end, and the negative terminal of the source is connected to the p-type end of the diode, there will be no current through the diode except reverse saturation current. This is because at the reverse biased condition the depletion layer of the junction becomes wider with increasing reverse biased voltage. Although there is a tiny current flowing

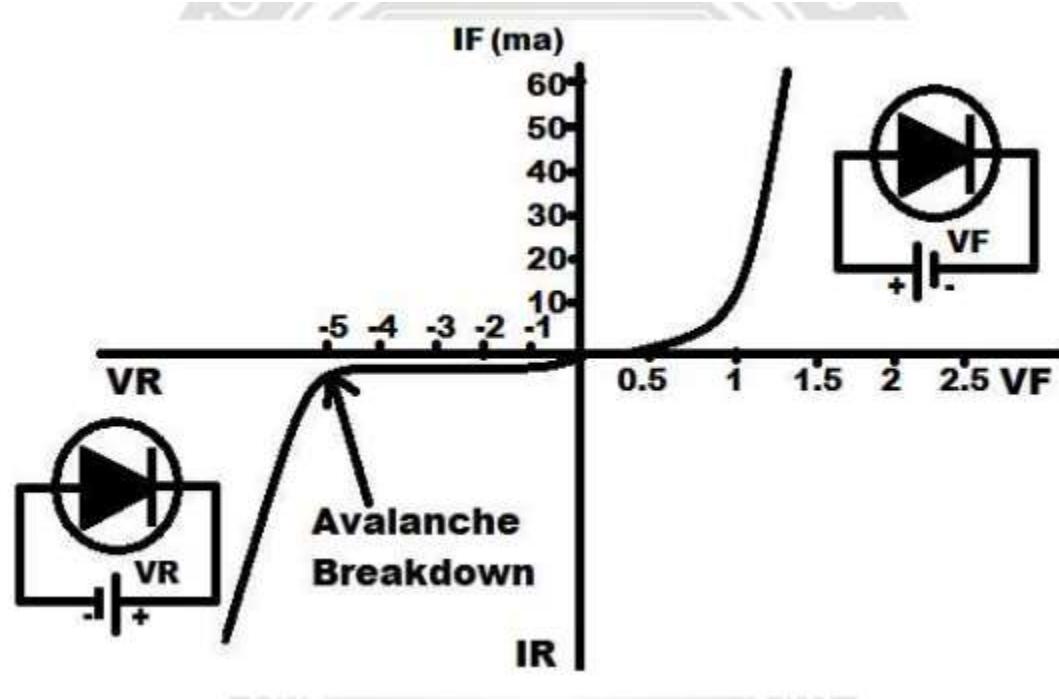


from n-type end to p-type end in the diode due to minority carriers. This tiny current is called reverse saturation current. Minority carriers are mainly thermally generated electrons and holes in p-type semiconductor and n-type semiconductor respectively.

Now if reverse applied voltage across the diode is continually increased, then after certain applied voltage the depletion layer will destroy which will cause a huge reverse current to flow through the diode. If this current is not externally limited and it reaches beyond the safe value, the diode may be permanently destroyed. This is because, as the magnitude of the reverse voltage increases, the kinetic energy of the minority charge carriers also increases. These fast moving electrons collide with the other atoms in the device to knock-off some more electrons from them. The electrons so released further release much more electrons from the atoms by breaking the covalent bonds. This process is termed as carrier multiplication and leads to a considerable increase in the flow of current through the p-n junction. The associated phenomenon is called Avalanche Breakdown.

## V-I Characteristics

**Forward Bias** When, P terminal is more positive as compared to N-terminal i.e. P-terminal connected to positive terminal of battery and N-terminal connected to negative terminal of battery, it is said to be forward biased. Positive terminal of the battery repels majority carriers, holes, in P-region and negative terminal repels electrons in the N-region and push them towards the junction. This result in increase in concentration of carriers near junction, recombination takes place and width of depletion region decreases. As forward bias voltage is raised depletion region continues to reduce in width, and more and more carriers recombine. This results in exponential rise of current.



**Reverse Bias** In reverse biasing P- terminal is connected to negative terminal of the battery and N- terminal to positive terminal of battery. Thus applied voltage makes N-side more positive than P-side. Negative terminal of the battery attracts majority carriers, holes, in P-region and positive terminal attracts electrons in the N-region and pull them away from the junction. This result in decrease in concentration of charge carriers near junction and width of depletion region increases. A small amount of current flow due to minority carriers, called as reverse bias current or leakage current. As reverse bias voltage is raised

depletion region continues to increase in width and no current flows. It can be concluded that diode acts only when forward biased. Operation of diode can be summarized in form of I-V diode characteristics graph. For reverse bias diode,

$$V < 0, I_D = I_S$$

Where, V = supply voltage ID = diode current IS = reverse saturation current

$$V > 0, I_D = I_S(e^{V/NV_r} - 1)$$

For forward bias, Where, VT = volt's equivalent of temperature = KT/Q = T/11600 Q = electronic charge K = Boltzmann's constant N = 1, for Ge = 2, for Si

## Applications

PN junction diodes have a wide range of applications, including rectifiers for AC to DC conversion, LEDs for lighting, photodiodes and solar cells for light detection and energy conversion, and use in voltage regulators, switches, oscillators, and various wave-shaping circuits like clippers and clamps.

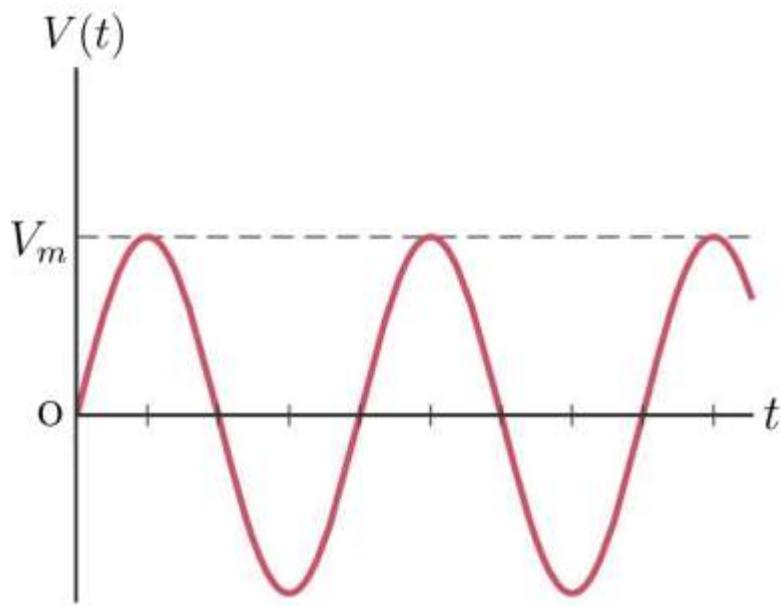
## Half-Wave rectifier

Alternating current (AC) Alternating current (AC) describes the flow of charge that changes direction periodically. As a result, the voltage level also reverses along with the current. AC is used to deliver power to houses, office buildings, etc.

The AC voltage of a periodic waveform may be written as

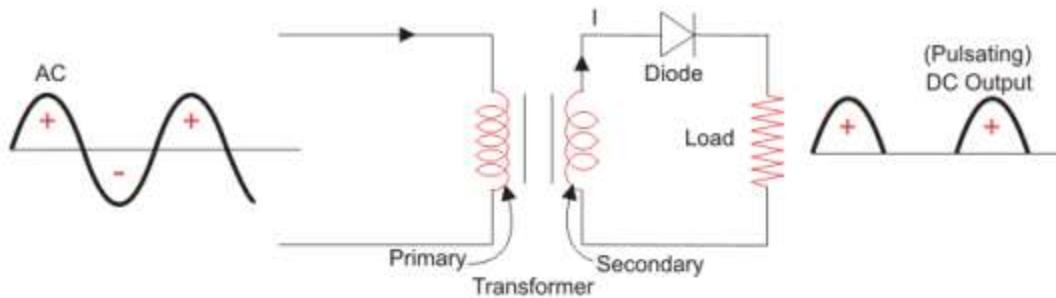
$$V(t) = V_m \sin(\omega t), (1)$$

where  $\omega = 2\pi/T$  is the angular frequency of the waveform or voltage and T is the time period of the voltage.



## Half wave rectifier

A half wave rectifier is a type of rectifier that only allows one half-cycle of an AC voltage waveform to pass, blocking the other half-cycle. Half-wave rectifiers are used to convert AC voltage to DC voltage, and only require a single diode to construct. A half wave rectifier is the simplest form of rectifier available. Figure 2 shows the input AC voltage waveform, the circuit diagram and the final output voltage waveform of a half wave rectifier. During the positive half cycle, the diode is forward biased making the current flow through the load resistor. While during the Negative half cycle the diode is reverse biased so it stops the current flow through the load resistor. Since current can not flow through the load during the negative half cycles, the output voltage is equal to zero.



**Figure 2:** Half wave rectifier circuit diagram and waveform [electrical4u.com].

Therefor, for an AC voltage given by (1) the output voltage of a half wave rectifier will be (for an ideal diode)

$$V_o(t) = \begin{cases} V_m \sin(\omega t), & 0 \leq t \leq T/2 \\ 0, & T/2 \leq t \leq T \end{cases}$$

### Average output voltage of a half wave rectifier

To calculate the average voltage,  $V_{dc}$ , of the pulsating DC output of a half wave rectifier we use the definition (2). Therefore, for the voltage (8) we have

$$\begin{aligned} V_{dc} &= \frac{1}{T} \int_0^T V_o(t) dt \\ &= \frac{1}{T} \int_0^{T/2} V_m \sin(\omega t) dt + \frac{1}{T} \int_{T/2}^T 0 dt \\ &= \frac{V_m}{T} \int_0^{T/2} \sin(\omega t) dt \\ &= \frac{V_m}{T} \left[ -\frac{\cos(\omega t)}{\omega} \right]_0^{T/2} \\ &= \frac{V_m}{\omega T} \{-\cos(\omega T/2) + \cos(0)\} \\ &= \frac{V_m}{\pi}. \end{aligned}$$

Here we have used the relation  $\omega = 2\pi/T$ .

## RMS value of the output voltage of a half wave rectifier

To calculate the RMS value of the output voltage,  $V_{\text{rms}}$ , of the pulsating DC output of a half wave rectifier we use the definition (5). Therefore, for the voltage (8) we have

$$\begin{aligned}
 V_{\text{rms}}^2 &= \frac{1}{T} \int_0^T V_o^2(t) dt \\
 &= \frac{V_m^2}{T} \int_0^{T/2} \sin^2(\omega t) dt + \frac{V_m^2}{T} \int_{T/2}^T 0 dt \\
 &= \frac{V_m^2}{2T} \int_0^{T/2} 2 \sin^2(\omega t) dt \\
 &= \frac{V_m^2}{2T} \int_0^{T/2} \{1 - \cos(2\omega t)\} dt \\
 &= \frac{V_m^2}{2T} \int_0^{T/2} dt - \frac{V_m^2}{T} \int_0^{T/2} \cos(2\omega t) dt \\
 &= \frac{V_m^2}{2T} \left[ T \right]_0^{T/2} - \frac{V_m^2}{2T} \left[ \frac{\sin(2\omega t)}{2\omega} \right]_0^{T/2} \\
 &= \frac{V_m^2}{4} - \frac{V_m^2}{\omega T} \left\{ \sin(2\omega T) - \sin(0) \right\} \\
 &= \frac{V_m^2}{4}.
 \end{aligned}$$

Hence for the half wave rectifier

$$V_{\text{rms}} = \frac{V_m}{2}.$$

Ripple factor of half wave rectifier Ripple is the unwanted AC component remaining when converting the AC voltage waveform into a DC waveform. Even though we try our best to remove all AC components, there is still some small amount left on the output side which pulsates the DC waveform. This undesirable AC component is called ripple. To quantify how well the half wave rectifier can convert the AC voltage into DC voltage, we use what is known as the ripple factor (represented by  $\gamma$ ). The ripple factor is the ratio between the RMS value of the AC voltage and the DC voltage of the rectifier.

$$\gamma = \frac{\text{RMS value of the AC component}}{\text{value of DC component}} = \frac{V_{\text{r(rms)}}}{V_{\text{dc}}}.$$

Note that the RMS value of the AC component of the signal is  $V_{\text{r(rms)}}$  and  $V_{\text{rms}}$  is the RMS value of the whole voltage signal.<sup>6</sup> To calculate  $V_{\text{r(rms)}}$ , the RMS value of the AC component present in the output of the half wave rectifier we write the output voltage as

$$V_o(t) = V_{ac} + V_{dc},$$

where  $V_{ac}$  is the AC component remaining when converting the AC voltage waveform into a DC waveform. The RMS value of the AC component present in the output of the half wave rectifier is given by

$$V_{r(rms)} = \left[ \frac{1}{T} \int_0^T V_{ac}^2 dt \right]^{1/2}.$$

Therefore,

$$\begin{aligned} V_{r(rms)}^2 &= \frac{1}{T} \int_0^T (V_o - V_{dc})^2 dt \\ &= \frac{1}{T} \int_0^T (V_o^2 - 2V_o V_{dc} + V_{dc}^2) dt \\ &= \frac{1}{T} \int_0^T V_o^2 dt - \frac{2V_{dc}}{T} \int_0^T V_o dt + V_{dc}^2 \\ &= V_{rms}^2 - 2V_{dc}^2 + V_{dc}^2 \\ &= V_{rms}^2 - V_{dc}^2. \end{aligned}$$

Hence the formula to calculate the ripple factor can be written as

$$\gamma = \frac{V_{r(rms)}}{V_{dc}} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

Using the values of  $V_{dc}$  and  $V_{rms}$  given in respectively for the half wave rectifier we find the the ripple factor as

$$\gamma = \sqrt{\left(\frac{V_m}{2} \times \frac{\pi}{V_m}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} \approx 1.21.$$

Note that to construct a good rectifier, one should keep the ripple factor as low as possible. This is why capacitors and inductors as filters are used to reduce the ripples in the circuit.

**Efficiency of half wave rectifier** The ratio of the DC power available at the load to the applied input AC power is known as the efficiency,  $\eta$ . Mathematically it can be given as:

$$\boxed{\eta = \frac{\text{DC power output}}{\text{AC power input}} = \frac{P_{dc}}{P_{ac}}}.$$

Let  $r_f$  and  $R_L$  be the forward resistance and load resistance of the diode. The voltage appearing across the secondary of the power transformer is given by The waveform diagram at the right side of the Figure shows

only a positive waveform at the output and a suppressed negative waveform. During the conduction period the instantaneous value of the current is given by the equation:

$$I(t) = \frac{V(t)}{R_L + r_f} = \frac{V_m}{R_L + r_f} \sin(\omega t) = I_m \sin(\omega t),$$

with  $I_m = V_m/(r_f + R_L)$  being the maximum current.

Now, the AC power input to the load is given as,

$$P_{ac} = I_{rms}^2 (R_L + r_f) = \frac{V_{rms}^2}{R_L + r_f}.$$

Since the output is obtained across  $R_L$ , the DC power output is given by

$$P_{dc} = I_{dc}^2 R_L = \frac{V_{dc}^2}{R_L}.$$

The half wave rectifier efficiency is then

$$\begin{aligned} \eta &= \frac{P_{dc}}{P_{ac}} \\ &= \frac{V_{dc}^2}{R_L} \times \frac{R_L + r_f}{V_{rms}^2} \\ &= \frac{V_{dc}^2}{V_{rms}^2} \times \frac{R_L + r_f}{R_L} \\ &= \left( \frac{V_{dc}}{V_{rms}} \right)^2 \times \left( 1 + \frac{r_f}{R_L} \right) \\ &= \left( \frac{V_m/\pi}{V_m/2} \right)^2 \times \left( 1 + \frac{r_f}{R_L} \right) \\ &\approx 0.4053 \left( 1 + \frac{r_f}{R_L} \right) \end{aligned}$$

In reality  $r_f$  is much smaller than  $R_L$ . If we neglect  $r_f$  compare to  $R_L$  then the efficiency of the rectifier is maximum. Therefore,

$$\boxed{\eta_{max} \approx 0.4053 = 40.53\%}.$$

This indicates that the half wave rectifier can convert maximum 40.53% of AC power into DC power, and the remaining power of 59.47% is lost in the rectifier circuit. In fact, 50% power in the negative half cycle is not converted and the remaining 9.47% is lost in the circuit.

**Peak Inverse Voltage (PIV)** of half wave rectifier Peak Inverse Voltage (PIV) is the maximum voltage that the diode can withstand during reverse bias condition. If a voltage is applied more than the PIV, the diode will be destroyed. The peak-inverse-voltage (PIV) rating of a diode is of the primary importance in the

design of rectification systems. During negative half cycles of the input voltage, the diode is reversed biased, no current flows through the load resistance  $RL$  and so causes no voltage drop across load resistance  $RL$  and consequently the whole of the input voltage appears across the diode. Thus the maximum voltage, that appears across the diode, is equal to the peak value of the secondary voltage i.e.  $V_m$ . Thus for a half-wave rectifier

$$PIV = V_m.$$

Peak factor of half wave rectifier It is defined as the ratio of the peak value of the output voltage to the RMS value of the output voltage.

$$\text{Peak factor} = \frac{V_m}{V_{\text{rms}}} = 2.$$

## **Applications of half wave rectifier**

Half wave rectifier is not so good as compared to Full-wave or Bridge rectifier, but sometimes we require this rectifier depending on the requirements. Some of the applications of half-wave rectifier are

- It is used for the detection of amplitude modulated radio signals.
- For the welding purpose, it supplies polarized voltage.
- It is used in many signal demodulation processes.

## **Advantages of half wave rectifier**

The main advantage of half-wave rectifiers is in their simplicity. As they do not require as many components, they are simpler and cheaper to setup and construct. As such, the main advantages of half-wave rectifiers are:

- Simple (lower number of components)
- Cheaper up front cost (as there is less equipment).

Although there is a higher cost over time due to increased power losses)

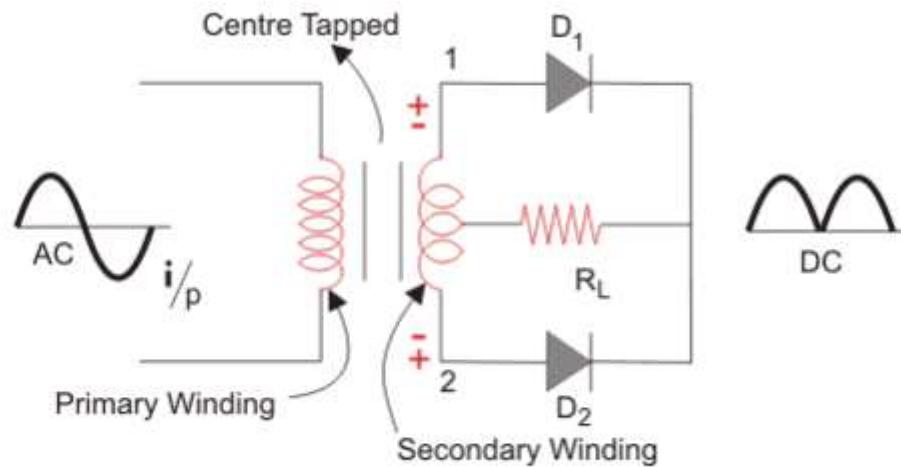
## **Disadvantages of half wave rectifier**

The disadvantages of half-wave rectifiers are:

- They only allow a half-cycle through per sinewave, and the other half-cycle is wasted. This leads to power loss.
- They produce a low output voltage.
- The output current we obtain is not purely DC, and it still contains a lot of ripple (i.e. it has a high ripple factor)

## **Full wave rectifier**

A full wave rectifier converts both halves of each cycle of an alternating wave (AC signal) into pulsating DC signal. Figure shows the input AC voltage waveform, the circuit diagram and the final output voltage waveform of a center tapped full wave rectifier.



Center tapped full wave rectifier circuit diagram and waveform

For an AC voltage given by (1) the waveform of the output voltage of a full wave rectifier can be written as (for an ideal diode)

$$V_o(t) = \begin{cases} V_m \sin(\omega t), & 0 \leq t \leq T/2 \\ V_m \sin(\omega t - \pi), & T/2 \leq t \leq T \end{cases}$$

### Average output voltage of a full wave rectifier

$$\begin{aligned} V_{dc} &= \frac{1}{T} \int_0^T V_o(t) dt \\ &= \frac{1}{T/2} \int_0^{T/2} V_m \sin(\omega t) dt \\ &= \frac{2V_m}{T} \int_0^{T/2} \sin(\omega t) dt \\ &= \frac{2V_m}{\pi}. \end{aligned}$$

### RMS value of the output voltage of a full wave rectifier

$$\begin{aligned} V_{rms} &= \left[ \frac{1}{T} \int_0^T V_o^2(t) dt \right]^{1/2} \\ &= \left[ \frac{V_m^2}{T/2} \int_0^{T/2} \sin^2(\omega t) dt \right]^{1/2} \\ &= \left[ \frac{V_m^2}{T} \int_0^{T/2} 2 \sin^2(\omega t) dt \right]^{1/2} \\ &= \frac{V_m}{\sqrt{2}}. \end{aligned}$$

### Ripple factor of full wave rectifier

$$\begin{aligned} \gamma &= \sqrt{\left( \frac{V_{rms}}{V_{dc}} \right)^2 - 1} \\ &= \sqrt{\left( \frac{\pi}{2\sqrt{2}} \right)^2 - 1} \\ &\approx 0.48 \end{aligned}$$

## Efficiency of full wave rectifier

$$\begin{aligned}\eta &= \frac{P_{dc}}{P_{dc}} \\ &= \left( \frac{V_{dc}}{V_{rms}} \right)^2 \times \left( 1 + \frac{r_f}{R_L} \right) \\ &\approx 0.8106 \left( 1 + \frac{r_f}{R_L} \right)\end{aligned}$$

In reality  $r_f$  is much smaller than  $R_L$ . If we neglect  $r_f$  compare to  $R_L$  then the efficiency of the rectifier is maximum. Therefore,

$$\boxed{\eta_{max} \approx 0.8106 = 81.06\%}$$

## Peak Inverse Voltage (PIV) of full wave rectifier

Peak inverse voltage(PIV) or peak reverse voltage(PRV) can be defined as the maximum value of the reverse voltage of a diode, which occurs at the peak of the input cycle when the diode is in reverse bias. PIV of center tapped full wave rectifier is  $2Vm$  and of a bridge rectifiers it is  $Vm$ .

Peak factor of full wave rectifier

$$\text{Peak factor} = \frac{V_m}{V_{rms}} = \sqrt{2}.$$

## Applications of full wave rectifier

Full wave rectifier is of two types; center tapped and bridge rectifier. Both these rectifiers are used for following purposes depends upon the requirement.

- It can be used to detect the amplitude of modulated radio signal.
- It can be used to supply polarized voltage in welding.
- The Bridge Rectifier circuits are widely used in power supply for various appliances, as they are capable of converting the High AC voltage into Low DC voltage.

## Advantages of full wave rectifier

- Full wave rectifiers have higher rectifying efficiency than half-wave rectifiers. This means that they convert AC to DC more efficiently.
- They have low power loss because no voltage signal is wasted in the rectification process.
- The output voltage of center tapped full wave rectifier has lower ripples than a half wave rectifiers.

## Disadvantages of full wave rectifier

- The center tapped rectifier is more expensive than half-wave rectifier and tends to occupy a lot of space.

## Bridge Rectifier

The basic bridge rectifier circuit is shown in Fig.

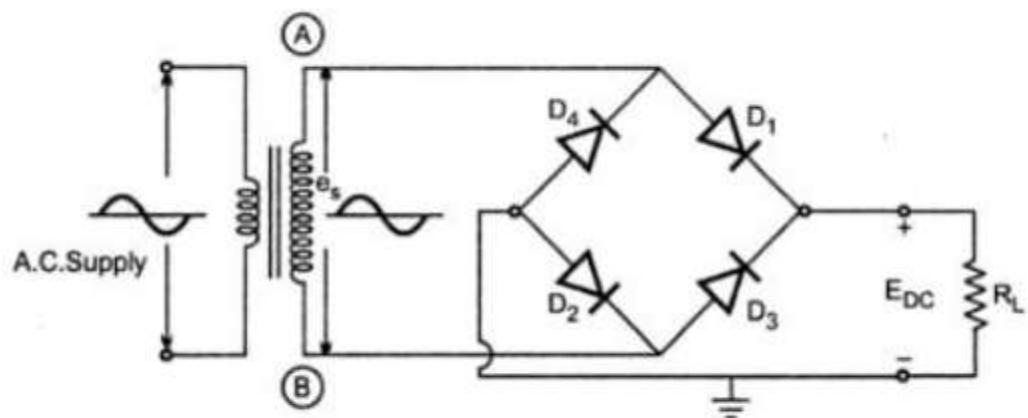


Fig. Bridge rectifier circuit

The bridge rectifier circuit is essentially a full wave rectifier circuit, using four diodes, forming the four arms of an electrical bridge. To one diagonal of the bridge, the a.c. voltage is applied through a transformer if necessary, and the rectified d.c. voltage is taken from the other diagonal of the bridge. The main advantage of this circuit is that it does not require a center tap on the secondary winding of the transformer. Hence wherever possible, a.c. voltage can be directly applied to the bridge.

### Operation of Bridge Rectifier

Consider the positive half of a.c. input voltage. The point A of secondary becomes positive. The diodes  $D_1$  and  $D_2$  will be forward biased, while  $D_3$  and  $D_4$  reverse biased. The two diodes  $D_1$  and  $D_2$  conduct in series with the load and the current flows as shown in Fig. 1.11

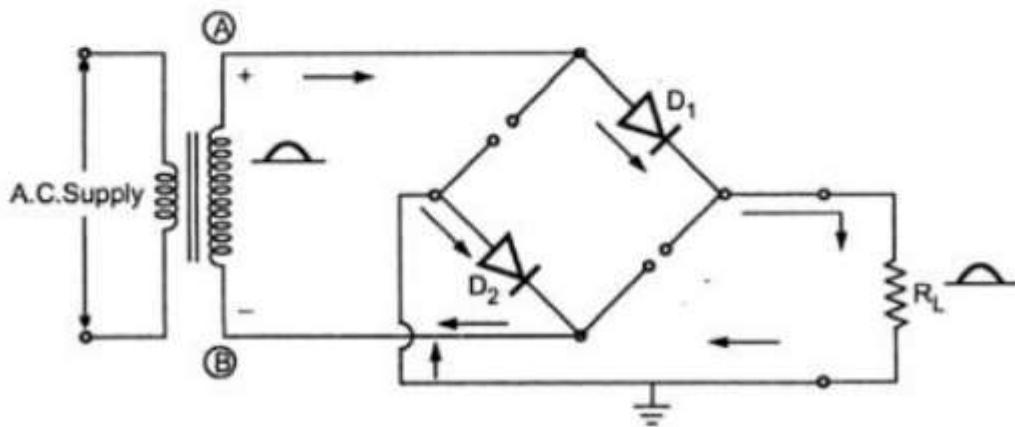


Fig. Current flow during positive half cycle

In the next half cycle, when the polarity of a.c. voltage reverses hence point B becomes positive, diodes  $D_3$  and  $D_4$  are forward biased, while  $D_1$  and  $D_2$  reverse biased. Now the diodes  $D_3$  and  $D_4$  conduct in series with the load and the current flows as shown in Fig.

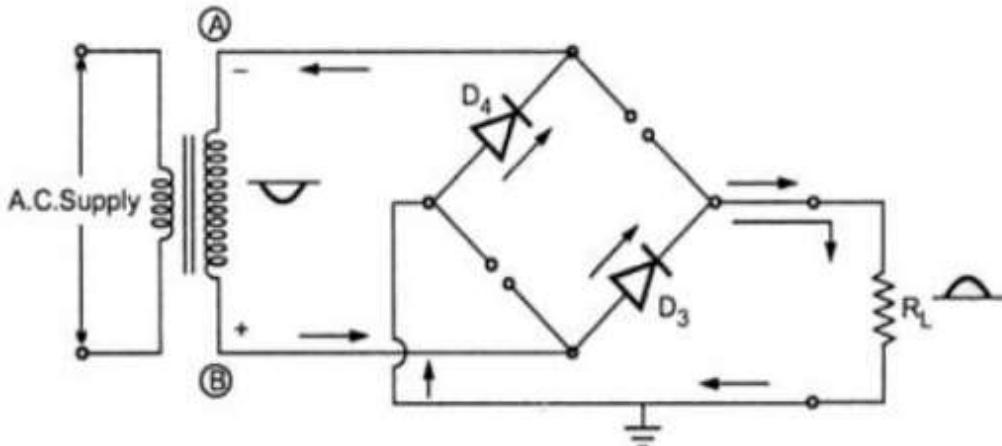


Fig. Current flow during negative half cycle

It is seen that in both cycles of a.c., the load current is flowing in the same direction hence, we get a full wave rectified output.

The waveforms of load current and voltage remain exactly same as shown before for full wave rectifier.

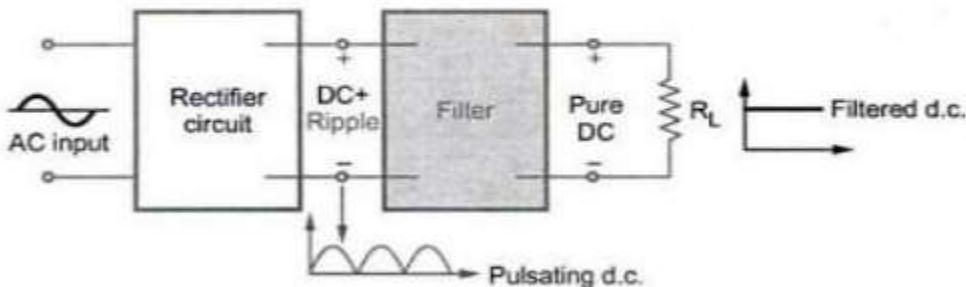
#### Advantages of Bridge Rectifier

- 1) The current in both the primary and secondary of the power transformer flows for the entire cycle and hence for a given power output, power transformer of a small size and less cost may be used.
- 2) No center tap is required in the transformer secondary. Hence, wherever possible, ac voltage can directly be applied to the bridge.
- 3) The current in the secondary of the transformer is in opposite direction in two half cycles. Hence net d.c. component flowing is zero which reduces the losses and danger of saturation.
- 4) Due to pure alternating current in secondary of transformer, the transformer gets utilised effectively and hence the circuit is suitable for applications where large powers are required.
- 5) As two diodes conduct in series in each half cycle, inverse voltage appearing across diodes get shared. Hence the circuit can be used for high voltage applications. Such a peak reverse voltage appearing across diode is called peak inverse voltage rating (PIV) of diode.

#### Disadvantages of Bridge Rectifier

The only disadvantage of bridge rectifier is the use of four diodes as compared to two diodes in normal full wave rectifier. This causes additional voltage drop as indicated by term  $2R_f$  present in expression of  $I_m$  instead of  $R_f$ . This reduces the output voltage.

It is seen that the output of a half-wave or full wave rectifier circuit is not pure d.c.; but it contains fluctuations or ripple, which are undesired. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load, as shown in the Fig. 1.13

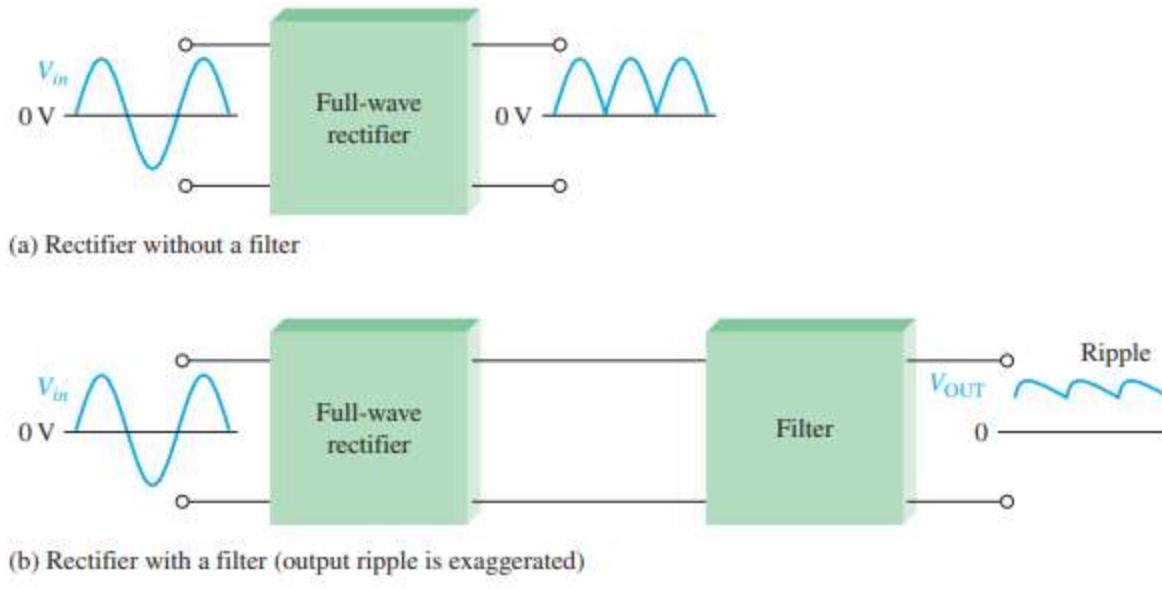


Power supply using rectifier and filter

## Power Supply Filters

A power supply filter ideally eliminates the fluctuations in the output voltage of a halfwave or full-wave rectifier and produces a constant-level dc voltage. Filtering is necessary because electronic circuits require a constant source of dc voltage and current to provide power and biasing for proper operation. Filters are implemented with capacitors, as you will see in this section. Voltage regulation in power supplies is usually done with integrated circuit voltage regulators. A voltage regulator prevents changes in the filtered dc voltage due to variations in input voltage or load.

In most power supply applications, the standard 60 Hz ac power line voltage must be converted to an approximately constant dc voltage. The 60 Hz pulsating dc output of a half-wave rectifier or the 120 Hz pulsating output of a full-wave rectifier must be filtered to reduce the large voltage variations. Figure illustrates the filtering concept showing a nearly smooth dc output voltage from the filter. The small amount of fluctuation in the filter output voltage is called *ripple*.



#### ▲ FIGURE

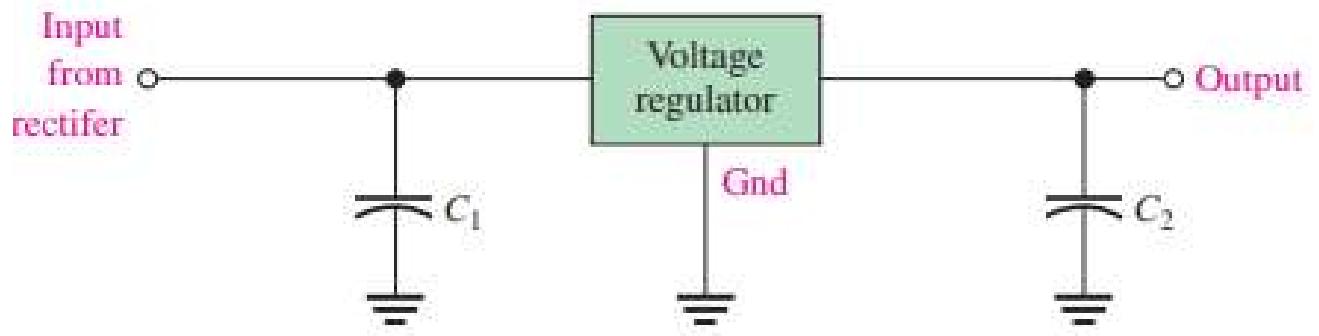
Power supply filtering.

## Voltage Regulators

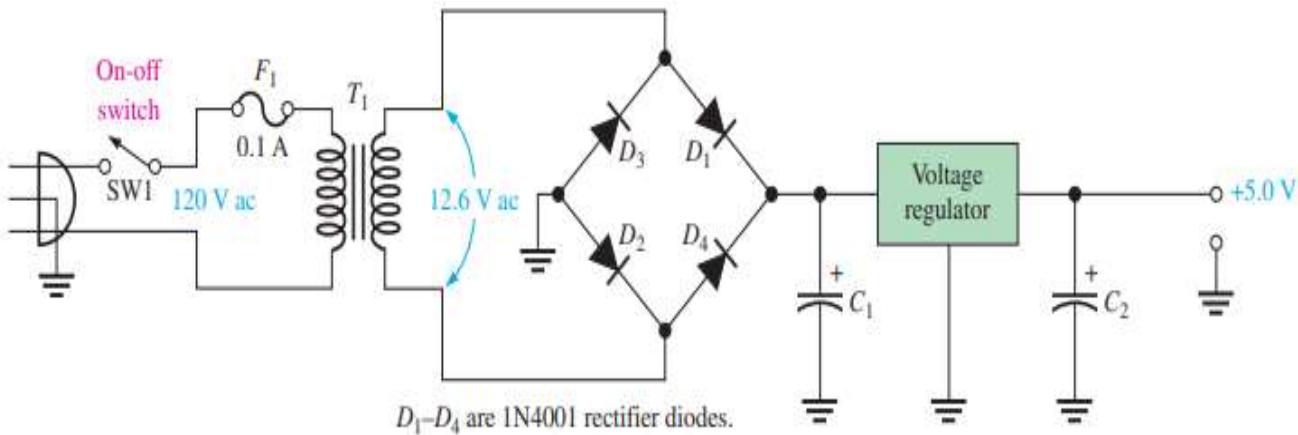
. A voltage regulator is connected to the output of a filtered rectifier and maintains a constant output voltage (or current) despite changes in the input, the load current, or the temperature. The capacitor-input filter reduces the input ripple to the regulator to an acceptable level. The combination of a large capacitor and a voltage regulator helps produce an excellent power supply.

Most regulators are integrated circuits and have three terminals—an input terminal, an output terminal, and a reference (or adjust) terminal. The input to the regulator is first filtered with a capacitor to reduce the ripple to <10%. The regulator reduces the ripple to a negligible amount. In addition, most regulators have an internal voltage reference, shortcircuit protection, and thermal shutdown circuitry. They are available in a variety of voltages, including positive and negative outputs, and can be designed for variable outputs with a minimum of external components. Typically, voltage regulators can furnish a constant output of one or more amps of current with high ripple rejection. Three-terminal regulators designed for fixed output voltages require only

external capacitors to complete the regulation portion of the power supply, as shown in Figure 2–50. Filtering is accomplished by a large-value capacitor between the input voltage and ground. An output capacitor (typically ) is connected from the output to ground to improve the transient response.  $0.1 \mu\text{F}$  to  $1.0 \mu\text{F}$



A basic fixed power supply with a +5 V voltage regulator is shown in Figure



A basic +5.0 V regulated power supply.

## Percent Regulation

The regulation expressed as a percentage is a figure of merit used to specify the performance of a voltage regulator. It can be in terms of input (line) regulation or load regulation.

**Line Regulation** The **line regulation** specifies how much change occurs in the output voltage for a given change in the input voltage. It is typically defined as a ratio of a change in output voltage for a corresponding change in the input voltage expressed as a percentage.

$$\text{Line regulation} = \left( \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \right) 100\%$$

**Load Regulation** The **load regulation** specifies how much change occurs in the output voltage over a certain range of load current values, usually from minimum current (no load, NL) to maximum current (full load, FL). It is normally expressed as a percentage and can be calculated with the following formula:

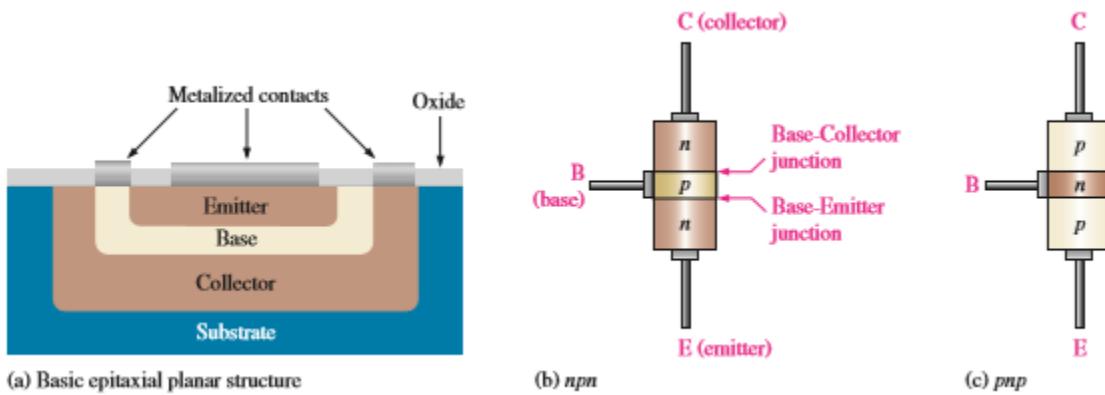
$$\text{Load regulation} = \left( \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \right) 100\%$$

where  $V_{\text{NL}}$  is the output voltage with no load and  $V_{\text{FL}}$  is the output voltage with full (maximum) load.

## MODULE-2: Bipolar Junction Transistor

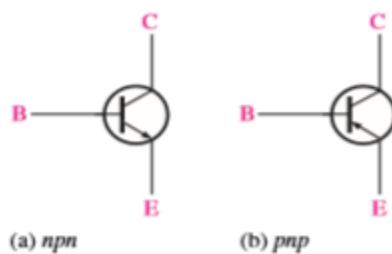
### BJT Structure:

The BJT is constructed with three doped semiconductor regions separated by two pn junctions, as shown in the epitaxial planar structure in Figure 2–1(a). The three regions are called emitter, base, and collector. Physical representations of the two types of BJTs are shown in Figure 2–1(b) and (c). One type consists of two n regions separated by a p region (npn), and the other type consists of two p regions separated by an n region (pnp). The term bipolar refers to the use of both holes and electrons as current carriers in the transistor structure.



**Figure 2 BJT construction. The substrate is a physical supporting material for the transistor.**

The pn junction joining the base region and the emitter region is called the base-emitter junction. The pn junction joining the base region and the collector region is called the base-collector junction, as indicated in Figure 2–1(b). A lead connects to each of the three regions, as shown. These leads are labeled E, B, and C for emitter, base, and collector, respectively. The base region is lightly doped and very thin compared to the heavily doped emitter and the moderately doped collector regions. Because of this difference in doping levels, the emitter and collector are not interchangeable. (The reason for this is discussed in the next section.) Figure 2–2 shows the schematic symbols for the npn and pnp bipolar junction transistors.



**Figure 2.2: Standard BJT (bipolar junction transistor) symbols.**

## Basic BJT operation:

In order for a BJT to operate properly as an amplifier, the two pn junctions must be correctly biased with external dc voltages. In this section, we mainly use the npn transistor for illustration. The operation of the pnp is the same as for the npn except that the roles of the electrons and holes, the bias voltage polarities, and the current directions are all reversed.

## Biasing

Figure 2–3 shows a bias arrangement for both npn and pnp BJTs for operation as an amplifier. Notice that in both cases the base-emitter (BE) junction is forward-biased and the base-collector (BC) junction is reverse-biased. This condition is called forward-reverse bias

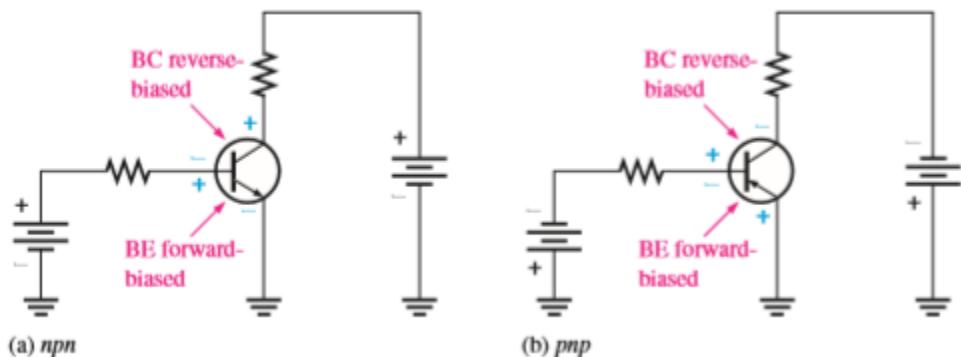
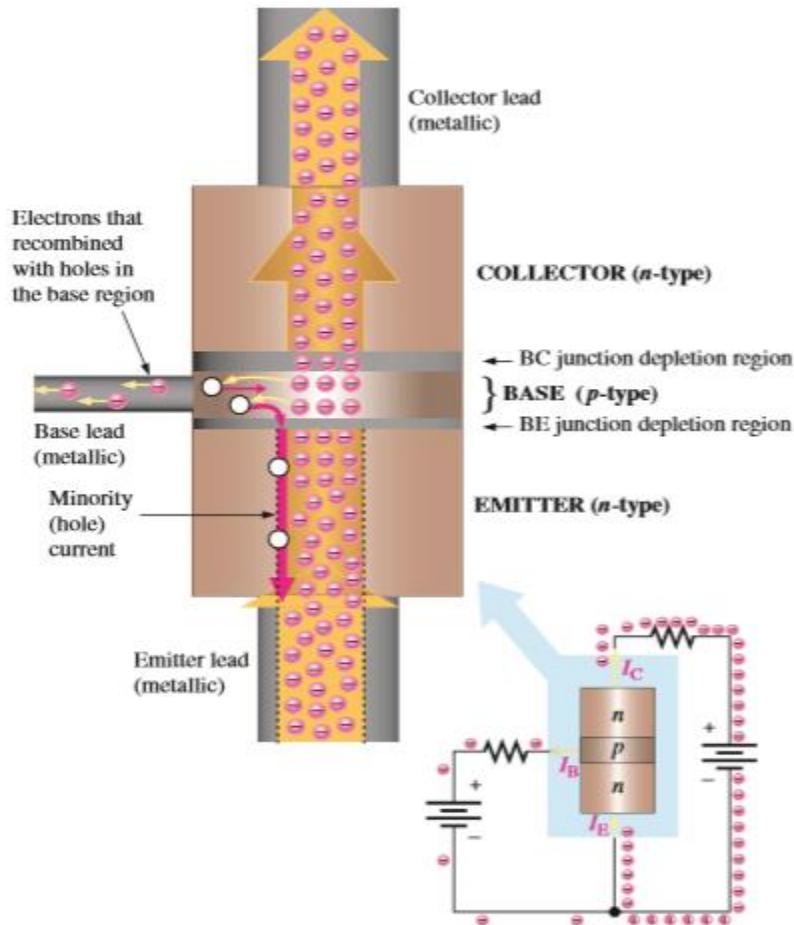


FIGURE 2–3: Forward-reverse bias of a BJT.

## Operation

To understand how a transistor operates, let's examine what happens inside the npn structure. The heavily doped n-type emitter region has a very high density of conduction-band (free) electrons, as indicated in Figure 2–4. These free electrons easily diffuse through the forward biased BE junction into the lightly doped and very thin p-type base region, as indicated by the wide arrow. The base has a low density of holes, which are the majority carriers, as represented by the white circles. A small percentage of the total number of free electrons injected into the base region recombine with holes and move as valence electrons through the base region and into the emitter region as hole current, indicated by the red arrows.



**FIGURE 2–4 BJT operation showing electron flow.**

When the electrons that have recombined with holes as valence electrons leave the crystalline structure of the base, they become free electrons in the metallic base lead and produce the external base current. Most of the free electrons that have entered the base do not recombine with holes because the base is very thin. As the free electrons move toward the reverse-biased BC junction, they are swept across into the collector region by the attraction of the positive collector supply voltage. The free electrons move through the collector region, into the external circuit, and then return into the emitter region along with the base current, as indicated. The emitter current is slightly greater than the collector current because of the small base current that splits off from the total current injected into the base region from the emitter.

**Transistor Currents** The directions of the currents in an npn transistor and its schematic symbol are as shown in Figure 2–5(a); those for a pnp transistor are shown in Figure 2–5(b). Notice that the arrow on the emitter inside the transistor symbols points in the direction of conventional current. These diagrams show that the emitter current ( $I_E$ ) is the sum of the collector current ( $I_C$ ) and the base current ( $I_B$ ), expressed as follows:

$$I_E = I_C + I_B$$

Equation 2–1

As mentioned before,  $I_B$  is very small compared to  $I_E$  or  $I_C$ . The capital-letter subscripts indicate dc values.

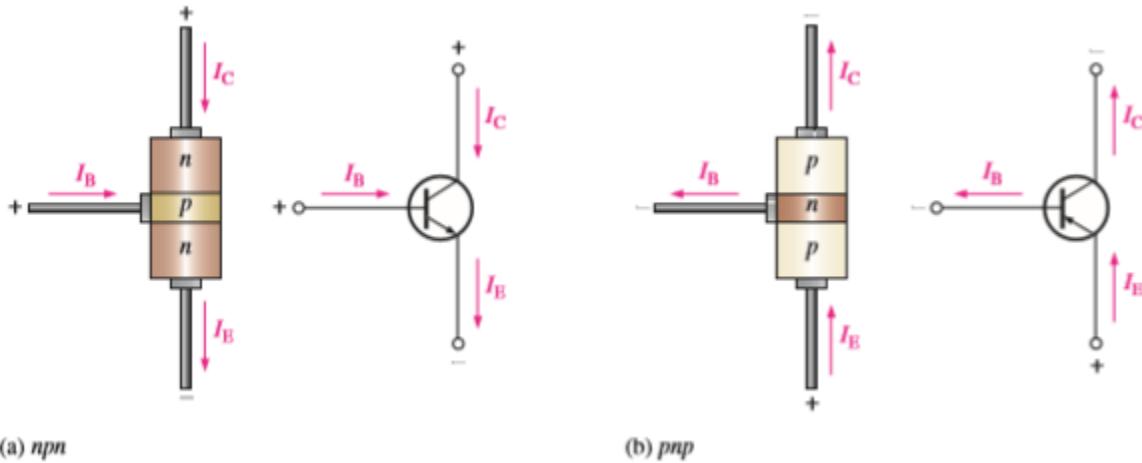


FIGURE 2–5 Transistor currents.

### BJT CHARACTERISTICS AND PARAMETERS:

When a transistor is connected to dc bias voltages, as shown in Figure 2–6 for both npn and pnp types,  $V_{BB}$  forward-biases the base-emitter junction, and  $V_{CC}$  reverse-biases the base-collector junction. Although in this chapter we are using separate battery symbols to represent the bias voltages, in practice the voltages are usually derived from a single dc power supply. For example,  $V_{CC}$  is normally taken directly from the power supply output and  $V_{BB}$  (which is smaller) can be produced with a voltage divider.

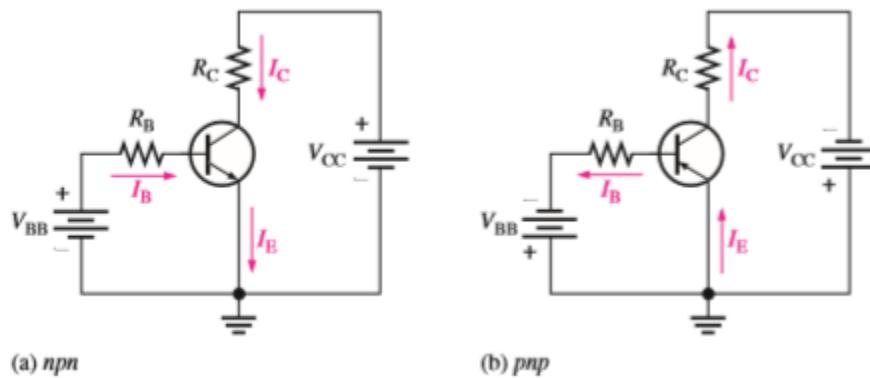


FIGURE 2–6 Transistor dc bias circuits.

**DC Beta ( $\beta_{dc}$ ) and DC Alpha ( $\alpha_{dc}$ )** The dc current gain of a transistor is the ratio of the dc collector current ( $I_C$ ) to the dc base current ( $I_B$ ) and is designated dc beta ( $\beta_{dc}$ ).

$$\beta_{DC} = \frac{I_C}{I_B}$$

Typical values of  $\beta_{DC}$  range from less than 20 to 200 or higher.  $\beta_{DC}$  is usually designated as an equivalent hybrid (h) parameter,  $h_{FE}$ , on transistor datasheets.

$$h_{FE} = \beta_{DC}$$

The ratio of the dc collector current ( $I_C$ ) to the dc emitter current ( $I_E$ ) is the dc alpha ( $\alpha_{DC}$ ). The alpha is a less-used parameter than beta in transistor circuits.

$$\alpha_{DC} = \frac{I_C}{I_E}$$

Typically, values of  $\alpha_{DC}$  range from 0.95 to 0.99 or greater, but  $\alpha_{DC}$  is always less than 1. The reason is that  $I_C$  is always slightly less than  $I_E$  by the amount of  $I_B$ . For example, if  $I_E = 100$  mA and  $I_B = 1$  mA, then  $I_C = 99$  mA and  $\alpha_{DC} = 0.99$ .

## Transistor DC Model

You can view the unsaturated BJT as a device with a current input and a dependent current source in the output circuit, as shown in Figure 2–7 for an npn. The input circuit is a forward-biased diode through which there is base current. The output circuit is a dependent current source (diamond-shaped element) with a value that is dependent on the base current,  $I_B$ , and equal to  $\beta_{DC}I_B$ . Recall that independent current source symbols have a circular shape.

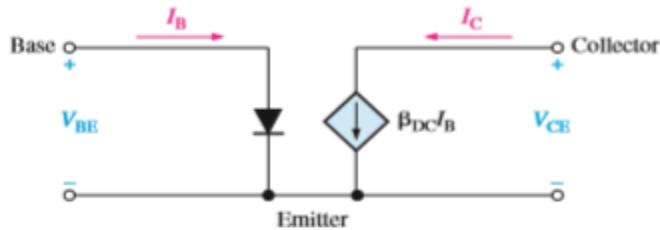


FIGURE 2–7 Ideal dc model of an npn transistor

## BJT Circuit Analysis

Consider the basic transistor bias circuit configuration in Figure 2–8. Three transistor dc currents and three dc voltages can be identified.

$I_B$ : dc base current

$I_E$ : dc emitter current

$I_C$ : dc collector current

$V_{BE}$ : dc voltage at base with respect to emitter

$V_{CB}$ : dc voltage at collector with respect to base

$V_{CE}$ : dc voltage at collector with respect to emitter

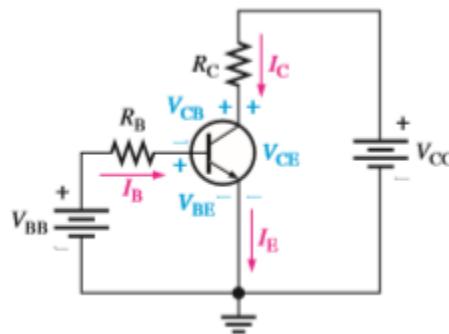


FIGURE 2–8 Transistor currents and voltages.

The base-bias voltage source,  $V_{BB}$ , forward-biases the base-emitter junction, and the collector-bias voltage source,  $V_{CC}$ , reverse-biases the base-collector junction. When the base-emitter junction is forward-biased, it is like a forward-biased diode and has a nominal forward voltage drop of

$$V_{BE} \cong 0.7 \text{ V} \quad \text{Equation 2-3}$$

Although in an actual transistor  $V_{BE}$  can be as high as 0.9 V and is dependent on current, we will use 0.7 V throughout this text in order to simplify the analysis of the basic concepts. Since the emitter is at ground (0 V), by Kirchhoff's voltage law, the voltage across  $R_B$  is

$$V_{R_B} = V_{BB} - V_{BE}$$

Also, by Ohm's law,

$$V_{R_B} = I_B R_B$$

Substituting for  $V_{RB}$  yields

$$I_B R_B = V_{BB} - V_{BE}$$

Solving for  $I_B$ ,

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} \quad \text{Equation 2-4}$$

The voltage at the collector with respect to the grounded emitter is

$$V_{CE} = V_{CC} - V_{R_C}$$

Since the drop across  $R_C$  is

$$V_{R_C} = I_C R_C$$

the voltage at the collector with respect to the emitter can be written as

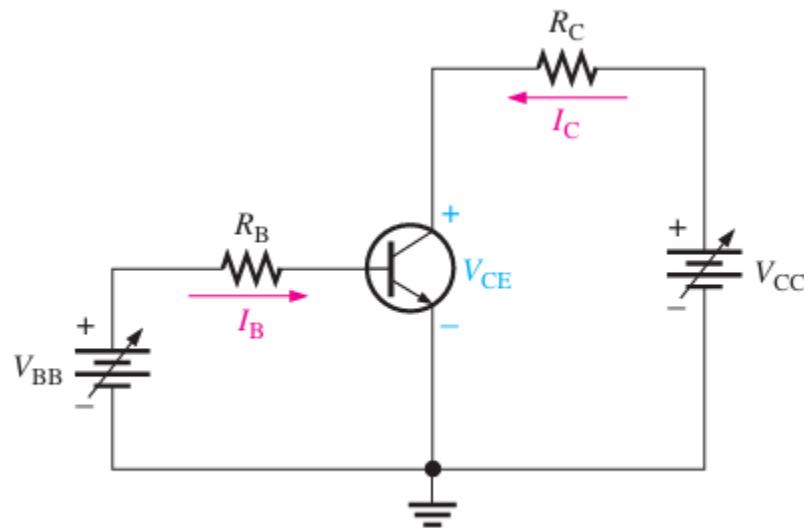
$$\text{where } I_C = \beta_{DC} I_B. \quad V_{CE} - V_{BE} \quad \text{Equation 2-5}$$

The voltage across the reverse-biased collector-base junction is

$$V_{CB} = V_{CE} - V_{BE} \quad \text{Equation 2-6}$$

## COLLECTOR CHARACTERISTIC CURVES

Using a circuit like that shown in Figure 2–10(a), a set of collector characteristic curves can be generated that show how the collector current,  $I_C$ , varies with the collector-to-emitter voltage,  $V_{CE}$ , for specified values of base current,  $I_B$ . Notice in the circuit diagram that both  $V_{BB}$  and  $V_{CC}$  are variable sources of voltage. Assume that  $V_{BB}$  is set to produce a certain value of  $I_B$  and  $V_{CC}$  is zero. For this condition, both the base-emitter junction and the base-collector junction are forward-biased because the base is at approximately 0.7 V while the emitter is at 0 V and the collector is near 0 V. The base current is primarily through the base-emitter junction because of the low



(a) Circuit

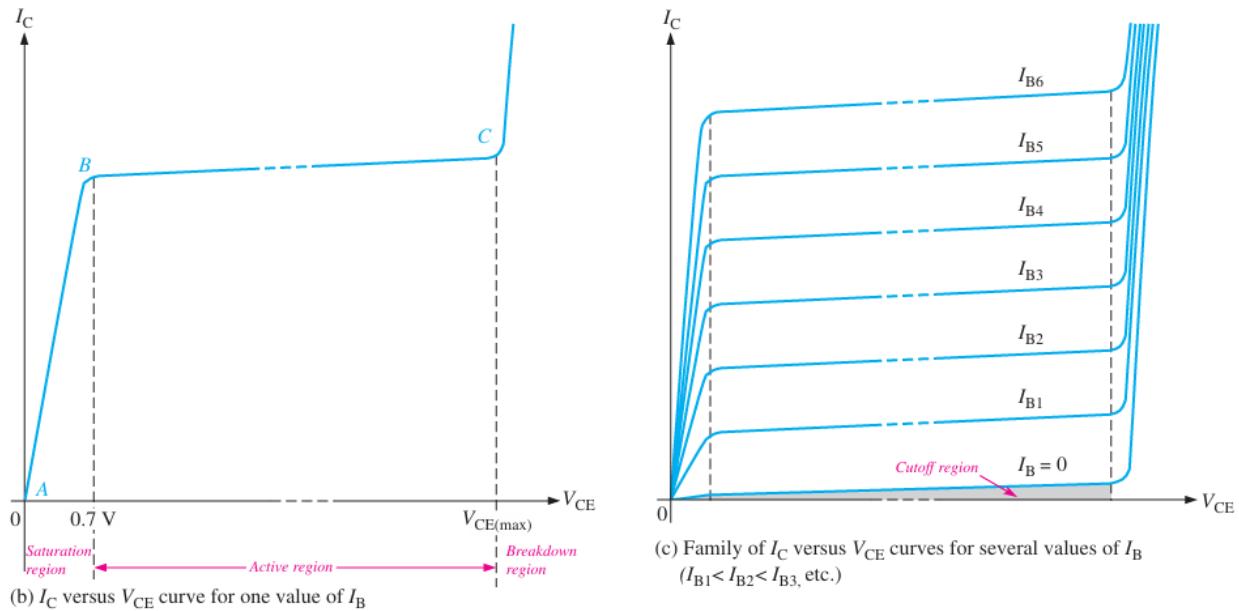


FIGURE 2–10 Collector characteristic curves

impedance path to ground and, therefore,  $I_C$  will be approximately zero and  $V_{CE}$  is near 0 V. When both junctions are forward-biased, the transistor is in the saturation region of its operation. Saturation is the state of a BJT in which the collector current has reached a maximum and is independent of the base current. As  $V_{CC}$  is increased,  $V_{CE}$  increases as the collector current increases. This is indicated by the portion of the characteristic curve between points A and B in Figure 2–10(b).  $I_C$  increases as  $V_{CC}$  is increased because  $V_{CE}$  remains less than 0.7 V due to the forward-biased base-collector junction. Ideally, when  $V_{CE}$  exceeds 0.7 V, the base-collector junction becomes reverse-biased and the transistor goes into the active, or linear, region of its operation. Once the base collector junction is reverse-biased,  $I_C$  levels off and remains essentially constant for a given value of  $I_B$  as  $V_{CE}$  continues to increase. Actually,  $I_C$  increases very slightly as  $V_{CE}$  increases due to widening of the base-collector depletion region. This results in fewer holes for recombination in the base region which effectively causes a slight increase in  $\beta_{DC}$ . This is shown by the portion of the characteristic curve between points B and C in Figure 2–10(b). For this portion of the characteristic curve, the value of  $I_C$  is determined only by the relationship expressed as  $I_C = \beta_{DC} I_B$ . When  $V_{CE}$  reaches a sufficiently high voltage, the reverse-biased base-collector junction goes into breakdown; and the collector current increases rapidly as indicated by the part of the curve to the right of point C in Figure 2–10(b). A transistor should never be operated in this breakdown region. A family of collector characteristic curves is produced when  $I_C$  versus  $V_{CE}$  is plotted for several values of  $I_B$ , as illustrated in Figure 2–10(c). When  $I_B=0$ , the transistor is in the cutoff region although there is a very small collector leakage current as indicated. Cutoff is the non-conducting state of a transistor. The amount of collector leakage current for  $I_B=0$  is exaggerated on the graph for illustration.

## CUTOFF

As previously mentioned, when  $I_B=0$ , the transistor is in the cutoff region of its operation. This is shown in Figure 2–13 with the base lead open, resulting in a base current of zero. Under this condition, there is a very small amount of collector leakage current,  $I_{CEO}$ , due mainly to thermally produced carriers. Because  $I_{CEO}$  is extremely small, it will usually be neglected in circuit analysis so that  $V_{CE}=V_{CC}$ . In cutoff, neither the base-emitter nor the base-collector junctions are forward-biased. The subscript CEO represents collector to-emitter with the base open.

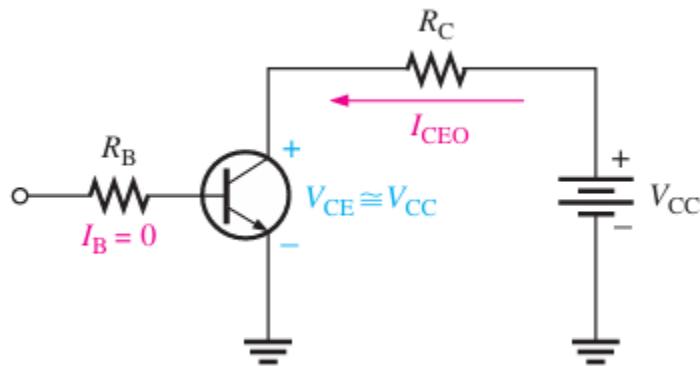
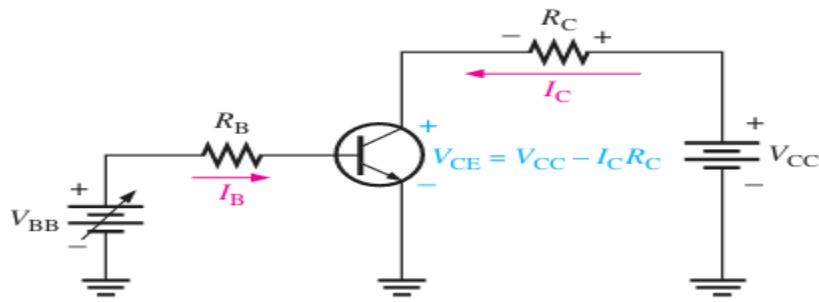


FIGURE 2–13 Cutoff: Collector leakage current ( $I_{CEO}$ ) is extremely small and is usually neglected. Base-emitter and base collector junctions are reverse-biased.

## SATURATION

when the base-emitter junction becomes forward-biased and the base current is increased, the collector current also increases ( $I_C=\beta_{DC}I_B$ ) and  $V_{CE}$  decreases as a result of more drop across the collector resistor ( $V_{CE}=V_{CC} - I_C R_C$ ). This is illustrated in Figure 2–14. When  $V_{CE}$  reaches its saturation value,  $V_{CE(sat)}$ , the base-collector junction becomes forward-biased and  $I_C$  can increase no further even with a continued increase in  $I_B$ . At the point of saturation, the relation  $I_C=\beta_{DC}I_B$  is no longer valid.  $V_{CE(sat)}$  for a transistor occurs somewhere below the knee of the collector curves, and it is usually only a few tenths of a volt

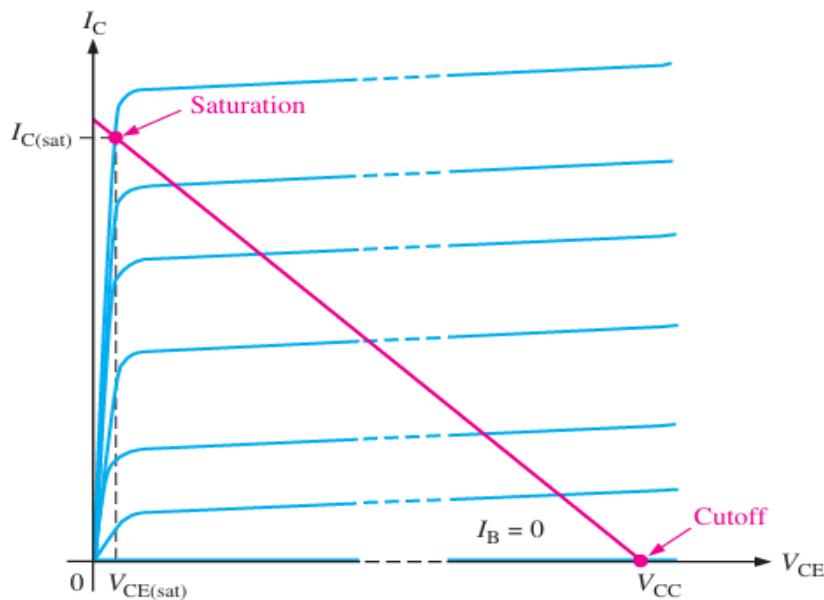


**FIGURE 2–14 Saturation:**

As  $I_B$  increases due to increasing  $V_{BB}$ ,  $I_C$  also increases and  $V_{CE}$  decreases due to the increased voltage drop across  $R_C$ . When the transistor reaches saturation,  $I_C$  can increase no further regardless of further increase in  $I_B$ . Base-emitter and base-collector junctions are forward-biased.

### DC LOAD LINE

Cutoff and saturation can be illustrated in relation to the collector characteristic curves by the use of a load line. A load line is a straight line that represents the voltage and current in the linear portion of the circuit that is connected to a device (a transistor in this case). Figure 2–15 shows a dc load line drawn on a family of curves connecting the cutoff point and the saturation point. The bottom of the load line is at ideal cutoff where  $I_C = 0$  and  $V_{CE} = V_{CC}$ . The top of the load line is at saturation where  $I_C = I_{C(sat)}$  and  $V_{CE} = V_{CE(sat)}$ . In between cutoff and saturation along the load line is the active region of the transistor's operation.



**FIGURE 2–15** DC load line on a family of collector characteristic curves illustrating the cutoff and saturation conditions.

### MAXIMUM TRANSISTOR RATINGS

A BJT, like any other electronic device, typically, maximum ratings are given for collector-to-base voltage, collector-to-emitter voltage, emitter-to-base voltage, collector current, and power

dissipation. The product of  $V_{CE}$  and  $I_C$  must not exceed the maximum power dissipation,  $P_{D(\max)}$ . (Data sheets may show this as simply  $P_D$  in a column labeled Maximum Ratings.) Both  $V_{CE}$  and  $I_C$  cannot be maximum at the same time. If  $V_{CE}$  is maximum,  $I_C$  can be calculated as

$$I_C = \frac{P_{D(\max)}}{V_{CE}}$$

If  $I_C$  is maximum,  $V_{CE}$  can be calculated by rearranging the previous equation as follows:

$$V_{CE} = \frac{P_{D(\max)}}{I_C}$$

### The BJT as an Amplifier

Amplification is the process of linearly increasing the amplitude of an electrical signal and is one of the major properties of a transistor.

### VOLTAGE AMPLIFICATION

The transistor amplifies current because the collector current is equal to the base current multiplied by the current gain,  $\beta$ . The base current in a transistor is very small compared to the collector and emitter currents. Because of this, the collector current is approximately equal to the emitter current. With this in mind, let's look at the circuit in Figure 2–21. An ac voltage,  $V_s$ , is superimposed on the dc bias voltage  $V_{BB}$  by capacitive coupling as shown. The dc bias voltage  $V_{CC}$  is connected to the collector through the collector resistor,  $R_C$ .

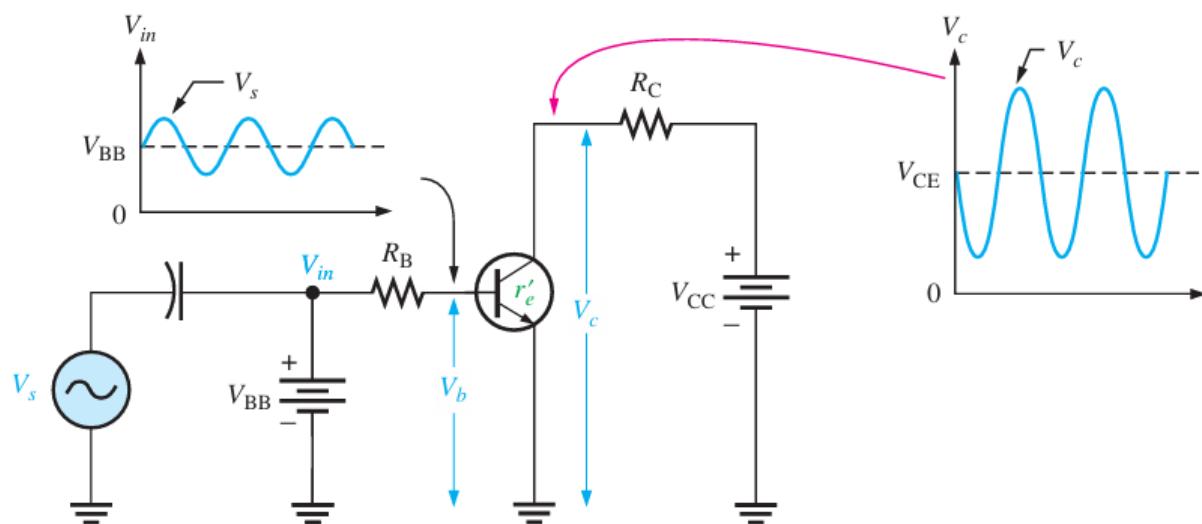


FIGURE 2–21 Basic transistor amplifier circuit

The ac input voltage produces an ac base current, which results in a much larger ac collector current. This ac collector current produces an ac voltage across  $R_C$ , thus producing an amplified, but inverted, reproduction of the ac input voltage in the active region of operation, as illustrated in Figure 2–21. The forward-biased base-emitter junction presents a very low resistance to the ac signal. This internal ac emitter resistance is designated  $r'_e$  in Figure 2–21 and appears in series with  $R_B$ . The ac base voltage is

$$V_b = I_e r'_e$$

The ac collector voltage,  $V_c$ , equals the ac voltage drop across  $R_C$

$$V_c = I_c R_C$$

Since  $I_c = I_e$ , the ac collector voltage is

$$V_c \cong I_e R_C$$

$V_b$  can be considered the transistor ac input voltage where  $V_b = V_s - I_b R_B$ .  $V_c$  can be considered the transistor ac output voltage. Since voltage gain is defined as the ratio of the output voltage to the input voltage, the ratio of  $V_c$  to  $V_b$  is the ac voltage gain,  $A_v$ , of the transistor

$$A_v = \frac{V_c}{V_b}$$

$$A_v = \frac{V_c}{V_b} \cong \frac{I_e R_C}{I_e r'_e}$$

$$A_v \cong \frac{R_C}{r'_e}$$

## THE BJT AS A SWITCH

Switching Operation Figure 2–23 illustrates the basic operation of a BJT as a switching device. In part (a), the transistor is in the cutoff region because the base-emitter junction is not forward-biased. In this condition, there is, ideally, an open between collector and emitter, as indicated by the switch equivalent. In part (b), the transistor is in the saturation region because the base emitter junction and the base-collector junction are forward-biased and the base current is made

large enough to cause the collector current to reach its saturation value. In this condition, there is, ideally, a short between collector and emitter, as indicated by the switch equivalent. Actually, a small voltage drop across the transistor of up to a few tenths of a volt normally occurs, which is the saturation voltage,  $V_{CE(sat)}$ <sup>2</sup>

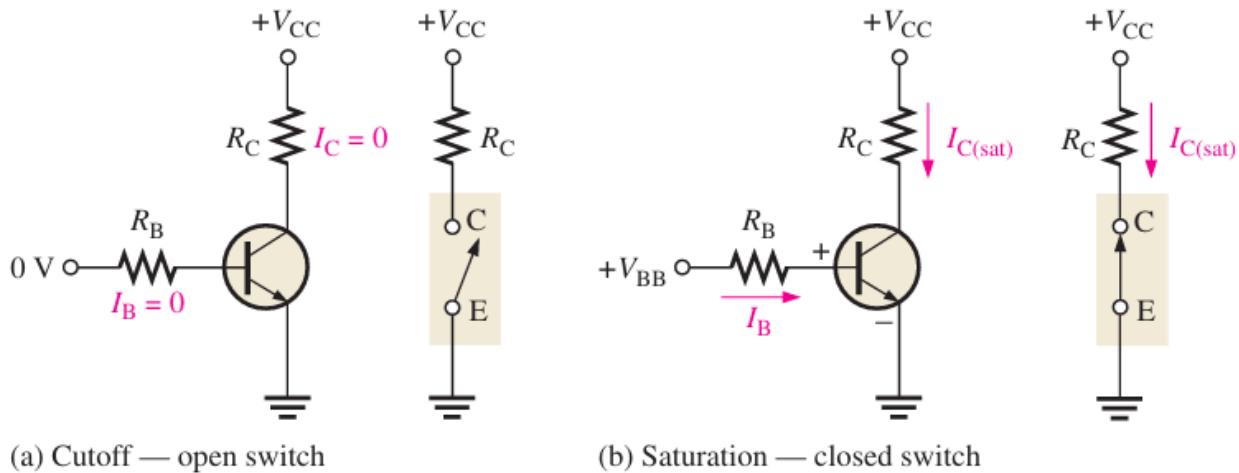


FIGURE 2–23 Switching action of an ideal transistor.

### Conditions in Cutoff

As mentioned before, a transistor is in the cutoff region when the base-emitter junction is not forward-biased. Neglecting leakage current, all of the currents are zero, and  $V_{CE}$  is equal to  $V_{CC}$ .

$$V_{CE(\text{cutoff})} = V_{CC}$$

### Conditions in Saturation

As you have learned, when the base-emitter junction is forward-biased and there is enough base current to produce a maximum collector current, the transistor is saturated. The formula for collector saturation current is

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C}$$

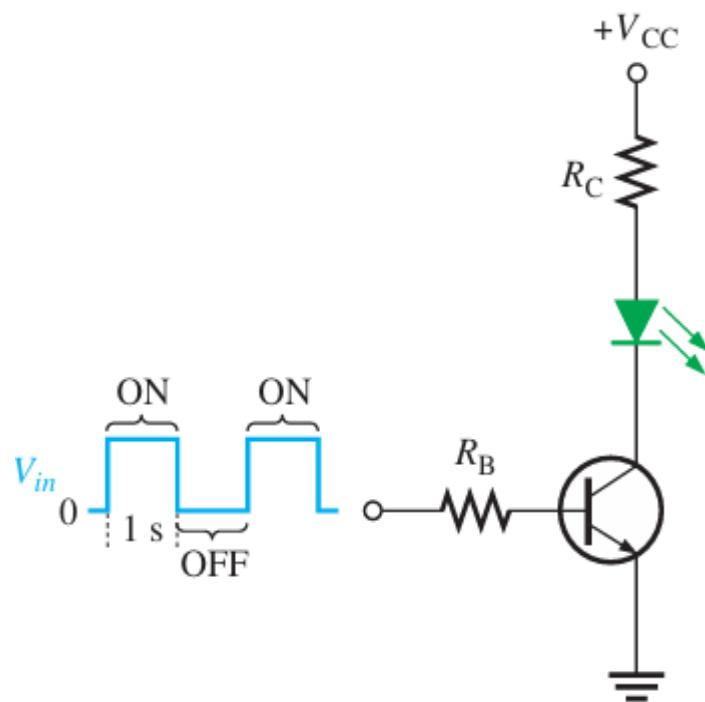
Since  $V_{CE(\text{sat})}$  is very small compared to  $V_{CC}$ , it can usually be neglected. The minimum value of base current needed to produce saturation is

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}}$$

Normally,  $I_B$  should be significantly greater than  $I_{B(\text{min})}$  to ensure that the transistor is saturated.

## A Simple Application of a Transistor Switch

The transistor in Figure 2–25 can be used as a switch to turn the LED on and off. For example, a square wave input voltage with a period of 2 s is applied to the input as indicated. When the square wave is at 0 V, the transistor is in cutoff; and since there is no collector current, the LED does not emit light. When the square wave goes to its high level and there is sufficient base current, the transistor saturates. This forward-biases the LED, and the resulting collector current through the LED causes it to emit light. Thus, the LED is on for 1 second and off for 1 second. The following example illustrates the switching operation for given circuit values.



**FIGURE 2–25** A transistor used to switch an LED on and off with proper  $R$  values selected based on transistor parameters.

### Need for Biasing

Transistor must be properly biased in order to operate as an amplifier. DC biasing is used to establish fixed dc values for the transistor currents and voltages called the dc operating point or quiescent point (Q-point).

### The DC Operating Point

A transistor must be properly biased with a dc voltage in order to operate as a linear amplifier. A dc operating point must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal.

## DC Bias

Bias establishes the dc operating point (Q-point) for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure below shows the effects of proper and improper dc biasing of an inverting amplifier. In part (a), the output signal is an amplified replica of the input signal except that it is inverted, which means that it is  $180^\circ$  out of phase with the input. The output signal swings equally above and below the dc bias level of the output,  $V_{DC(out)}$ . Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c). Part (b) illustrates limiting of the positive portion of the output voltage as a result of a Q-point (dc operating point) being too close to cutoff. Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation

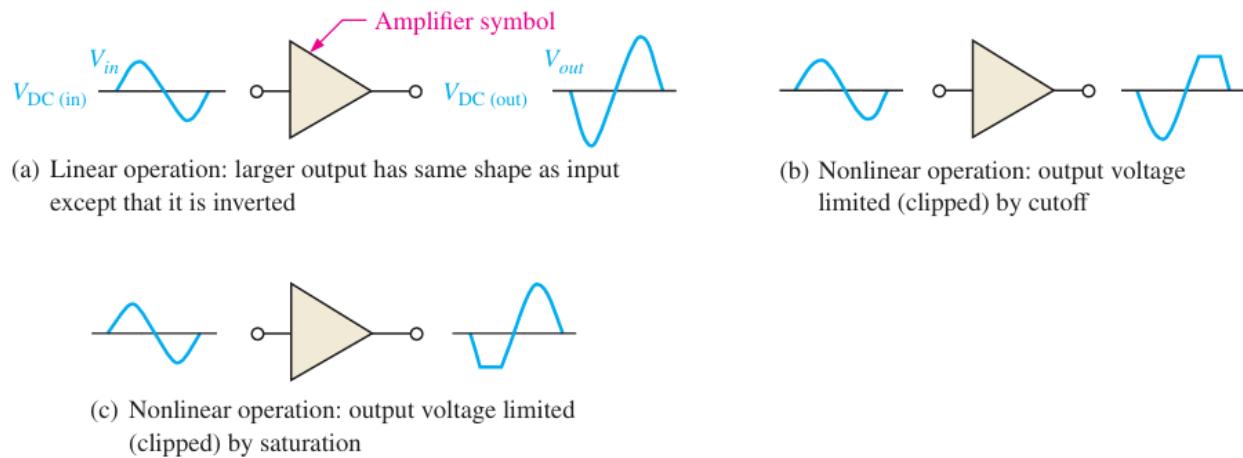
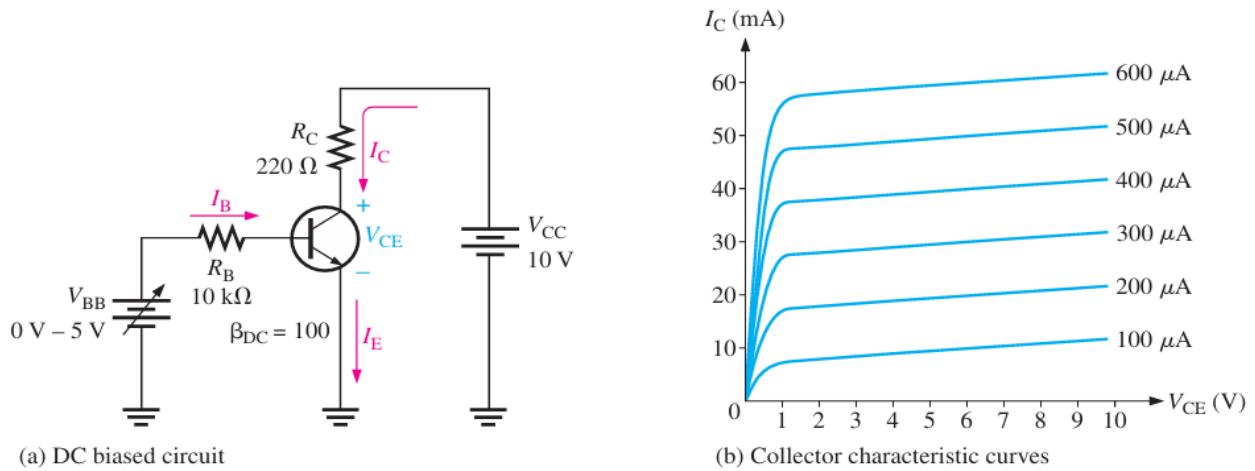


Figure: Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).

## Graphical Analysis

The transistor in Figure (a) is biased with  $V_{CC}$  and  $V_{BB}$  to obtain certain values of  $I_B$ ,  $I_C$ ,  $I_E$ , and  $V_{CE}$ . The collector characteristic curves for this particular transistor are shown in Figure (b); we will use these curves to graphically illustrate the effects of dc bias

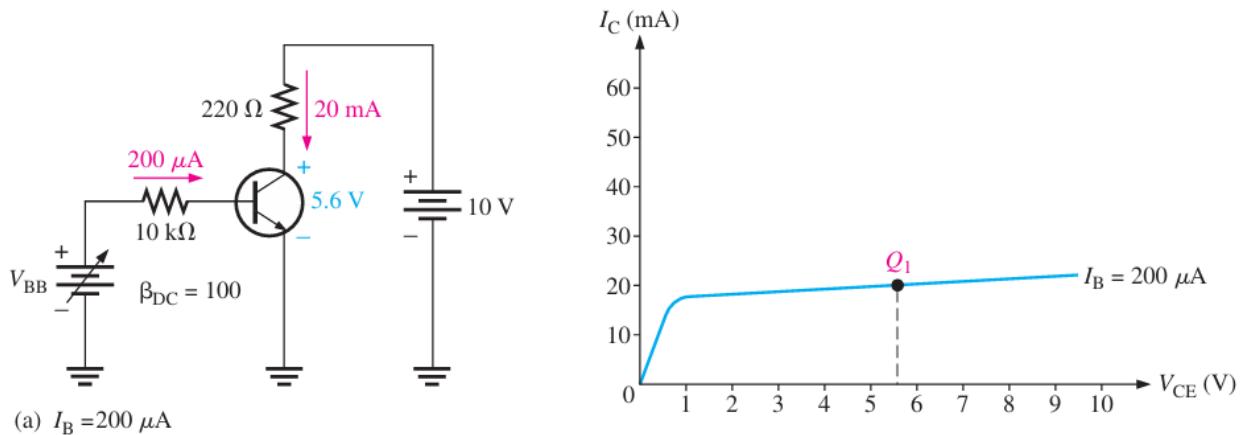


*FIGURE: A DC-biased transistor circuit with variable bias voltage ( $V_{BB}$ ) for generating the collector characteristic curves shown in part (b).*

$$V_{CE} = V_{CC} - I_C R_C = 10 \text{ V} - (20 \text{ mA})(220 \Omega) = 10 \text{ V} - 4.4 \text{ V} = 5.6 \text{ V}$$

In Figure (a) below, we assign three values to  $I_B$  and observe what happens to  $I_C$  and  $V_{CE}$ . First,  $V_{BB}$  is adjusted to produce an  $I_B$  of 200mA, as shown in Figure (a). Since  $I_C = \beta_{DC}I_B$ , the collector current is 20 mA, as indicated, and

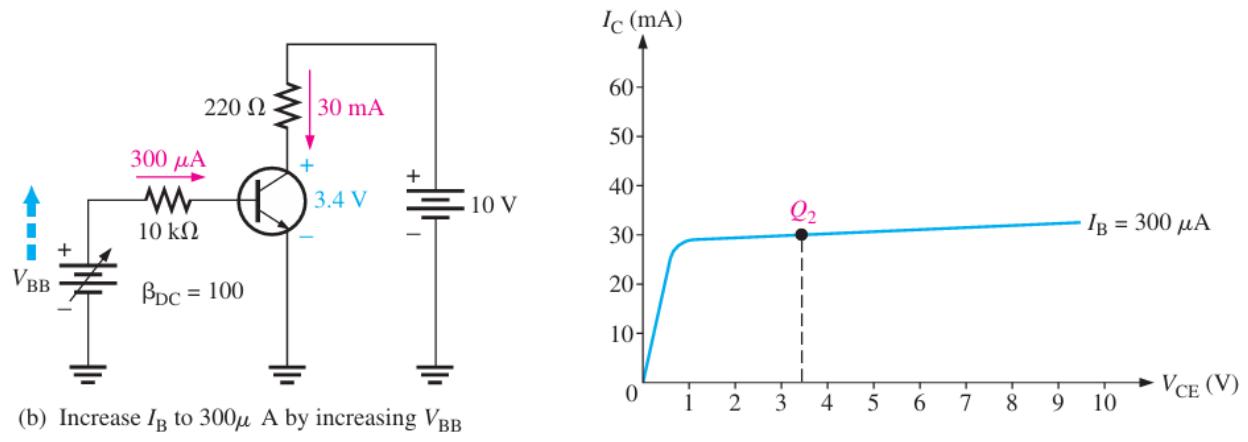
This Q-point is shown on the graph of Figure (a) as Q1.



Figure(a)

Next, as shown in Figure (b),  $V_{BB}$  is increased to produce an  $I_B$  of 300 mA and an  $I_C$  of 30 mA.

$$V_{CE} = 10 \text{ V} - (30 \text{ mA})(220 \Omega) = 10 \text{ V} - 6.6 \text{ V} = 3.4 \text{ V}$$



Figure(b)

The Q-point for this condition is indicated by  $Q_2$  on the graph. Finally, as in Figure (c),  $V_{BB}$  is increased to give an  $I_B$  of 400 mA and an  $I_C$  of 40 mA.

$$V_{CE} = 10\text{ V} - (40\text{ mA})(220\Omega) = 10\text{ V} - 8.8\text{ V} = 1.2\text{ V}$$

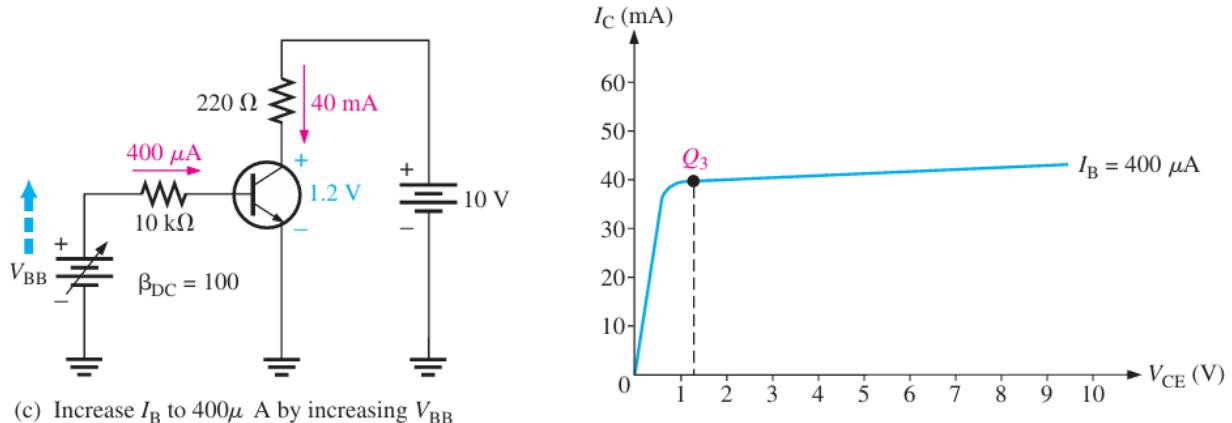


Figure (c)  $Q_3$  is the corresponding Q-point on the graph.

### Illustration of Q-point adjustment.

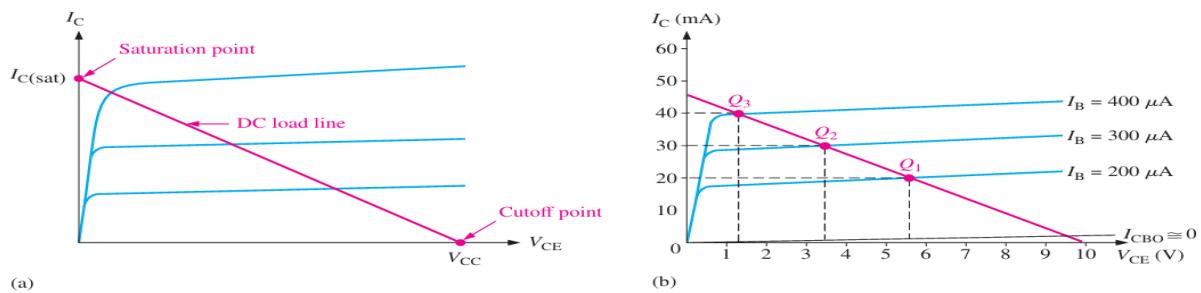


Figure: The dc load line.

## Linear Operation

The region along the load line including all points between saturation and cutoff is generally known as the linear region of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.

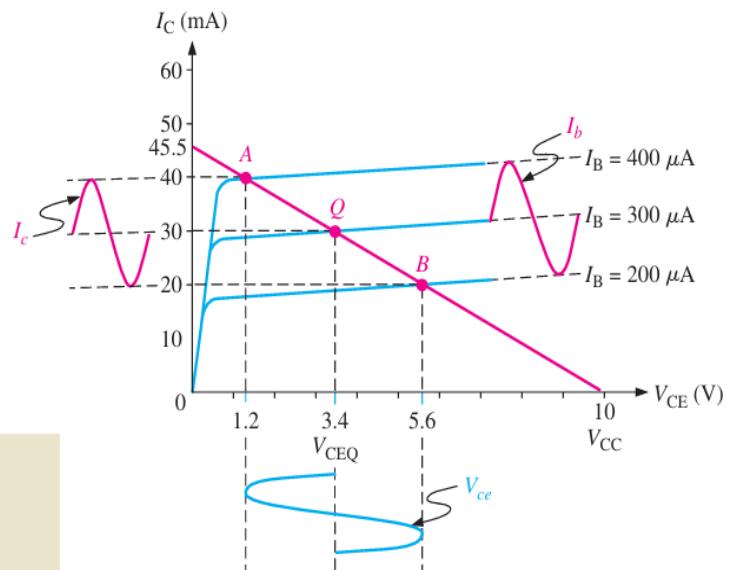
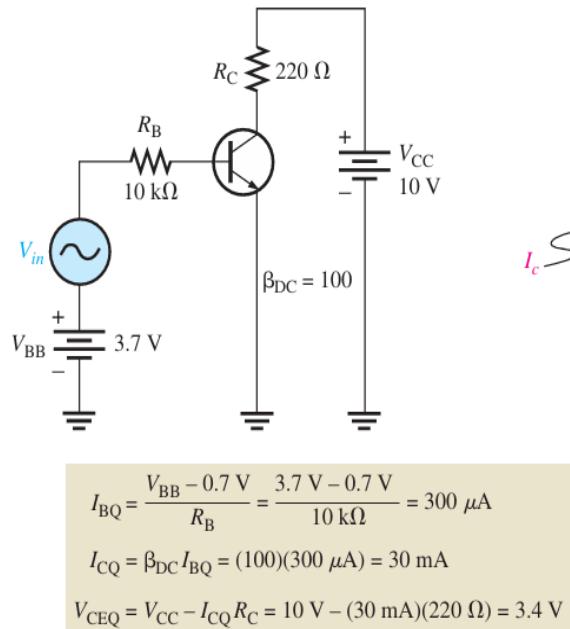


FIGURE : Variations in collector current and collector-to-emitter voltage as a result of a variation in base current

## The JFET:

The JFET (junction field-effect transistor) is a type of FET that operates with a reverse-biased pn junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, n channel or p channel.

### Basic Structure:

Figure (a) shows the basic structure of an n-channel JFET (junction field-effect transistor). Wire leads are connected to each end of the n-channel; the drain is at the upper end, and the source is

at the lower end. Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the gate lead. The gate lead is shown connected to only one of the p regions, which are internally connected together. A p-channel JFET is shown in Figure (b).

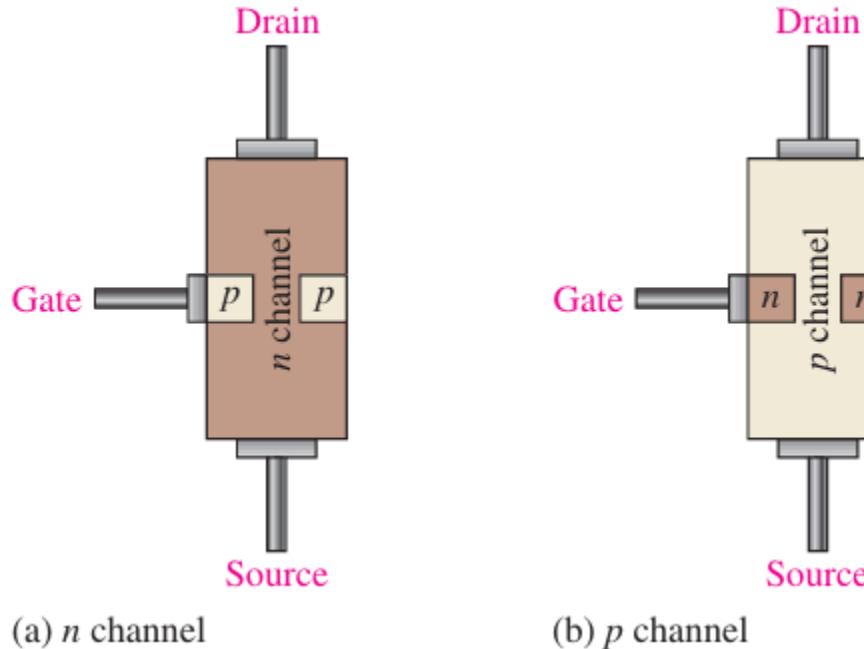


FIGURE: A

representation of the basic structure of the two types of JFET.

### Basic Operation

To illustrate the operation of a JFET, Figure shows dc bias voltages applied to an n-channel device.  $V_{DD}$  provides a drain-to-source voltage and supplies current from

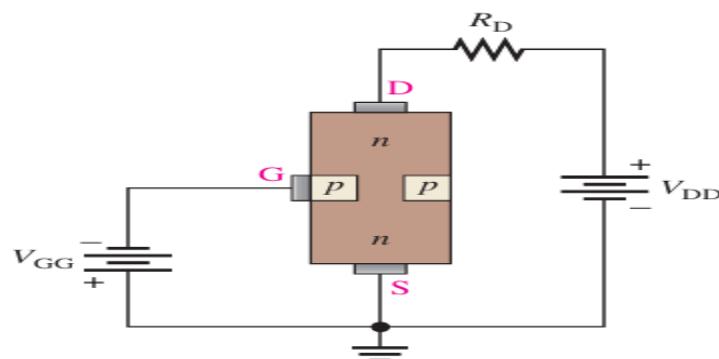
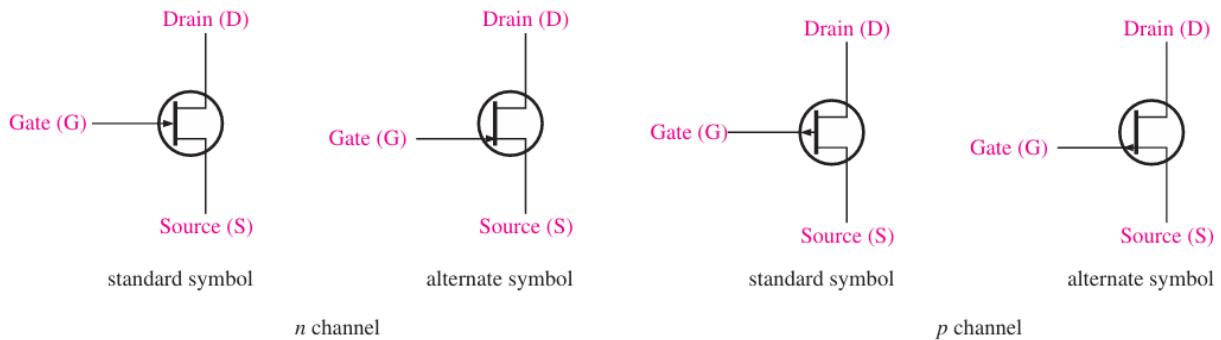


Figure: A biased n-channel JFET

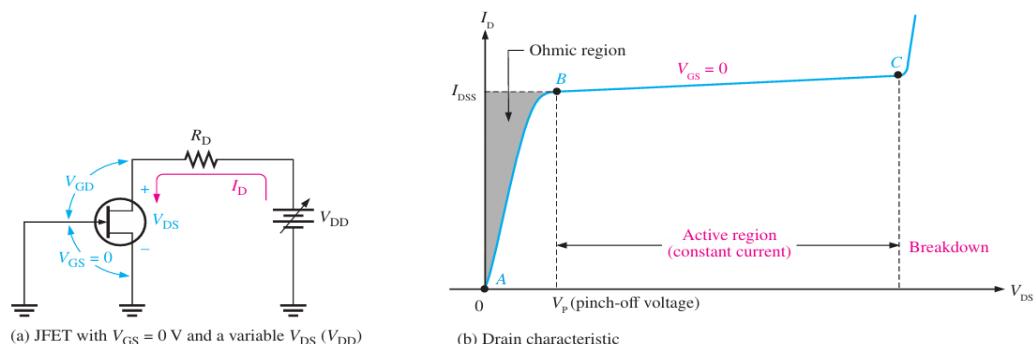
drain to source.  $V_{GG}$  sets the reverse-bias voltage between the gate and the source, as shown. The JFET is always operated with the gate-source pn junction reverse-biased. Reverse biasing of the gate-source junction produces a depletion region along the pn junction, which extends into the channel and thus increases its resistance by restricting the channel width. The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current,  $I_D$ . Above Figure illustrates this concept with an n-channel device. The white areas represent the depletion region created by the reverse bias. It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.



**Figure: JFET schematic symbols.**

## JFET Characteristics

**Drain Characteristic Curve** Consider the case when the gate-to-source voltage is zero ( $V_{GS} = 0$  V). This is produced by shorting the gate to the source, as in Figure (a) where both are grounded. As  $V_{DD}$  (and thus  $V_{DS}$ ) is increased from 0 V,  $I_D$  will increase proportionally, as shown in the graph of Figure (b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the ohmic region because  $V_{DS}$  and  $I_D$  are related by Ohm's law.

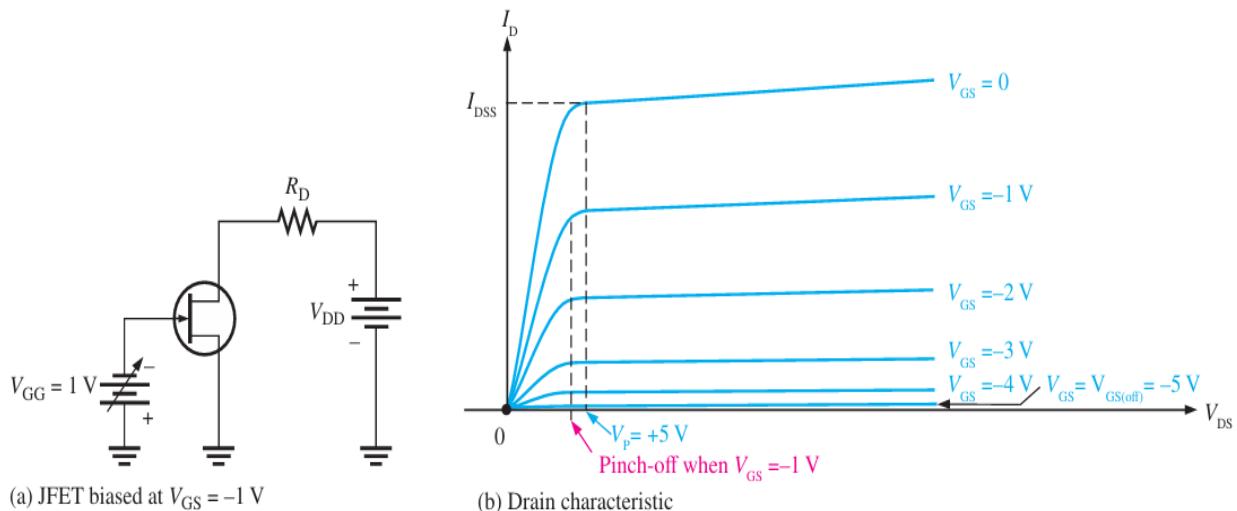


**FIGURE (b)** Drain characteristic curve of a JFET for  $V_{GS} = 0$  showing pinch-off voltage.

At point B in Figure (b), the curve levels off and enters the active region where  $I_D$  becomes essentially constant. As  $V_{DS}$  increases from point B to point C, the reverse-bias voltage from gate to drain ( $V_{GD}$ ) produces a depletion region large enough to offset the increase in  $V_{DS}$ , thus keeping  $I_D$  relatively constant. Pinch-Off Voltage For  $V_{GS} = 0$  V, the value of  $V_{DS}$  at which  $I_D$  becomes essentially constant (point B on the curve in Figure (b)) is the pinch-off voltage,  $V_P$ . For a given JFET,  $V_P$  has a fixed value. As you can see, a continued increase in  $V_{DS}$  above the pinch-off voltage produces an almost constant drain current until point C is reached. This value of drain current is  $I_{DSS}$  (Drain to Source current with gate Shorted) and is always specified on JFET datasheets.  $I_{DSS}$  is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition,  $V_{GS} = 0$  V. Breakdown As shown in the graph in Figure (b), breakdown occurs at point C when  $I_D$  begins to increase very rapidly with any further increase in  $V_{DS}$ . Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current)

### V<sub>GS</sub> Controls ID

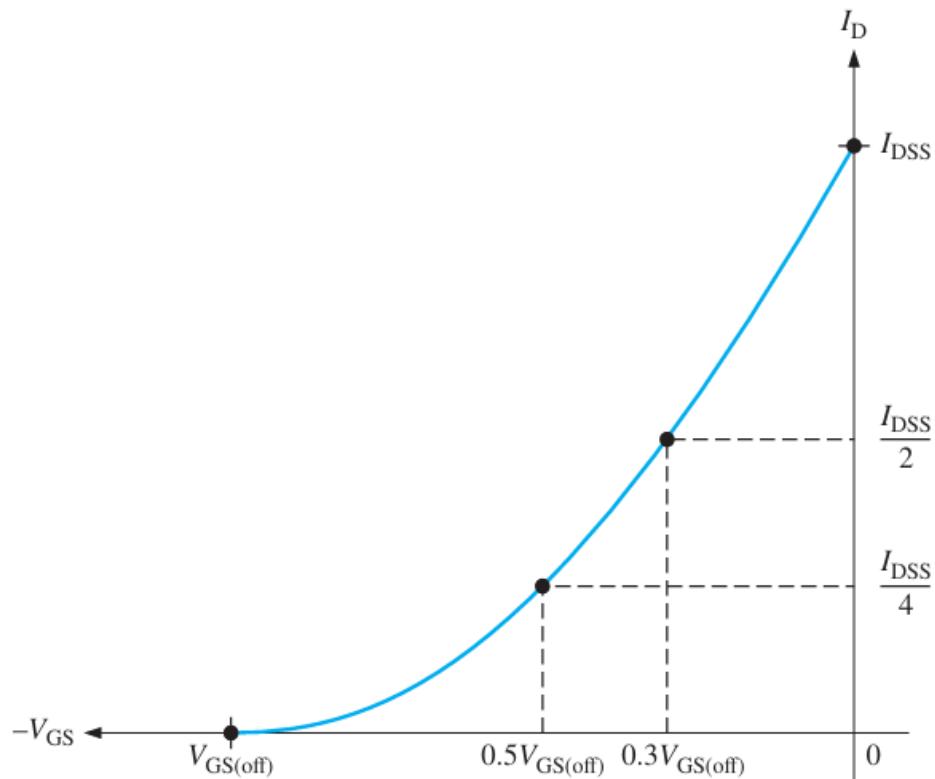
Let's connect a reverse-bias voltage,  $V_{GG}$ , from gate to source as shown in Figure (a). As  $V_{GS}$  is set to increasingly more negative values by adjusting  $V_{GG}$ , a family of drain characteristic curves is produced, as shown in Figure (b). Notice that  $I_D$  decreases as the magnitude of  $V_{GS}$  is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in  $V_{GS}$ , the JFET reaches pinch-off (where constant current begins) at values of  $V_{DS}$  less than  $V_P$ . The term pinch-off is not the same as pinch-off voltage,  $V_p$ . The JFET must be operated between  $V_{GS} = 0$  V and  $V_{GS(off)}$ . For this range of gate-to-source voltages,  $I_D$  will vary from a maximum of  $I_{DSS}$  to a minimum of almost zero.



**FIGURE:** Pinch-off occurs at a lower  $V_{DS}$  as  $V_{GS}$  is increased to more negative values.

### JFET Transfer Characteristics:

You have learned that a range of  $V_{GS}$  values from zero to  $V_{GS(off)}$  controls the amount of drain current. For an n-channel JFET,  $V_{GS(off)}$  is negative, and for a p-channel JFET,  $V_{GS(off)}$  is positive. Because  $V_{GS}$  does control  $I_D$ , the relationship between these two quantities is very important. Figure is a general transfer characteristic curve that illustrates graphically the relationship between  $V_{GS}$  and  $I_D$ .



**FIGURE: JFET Transfer Characteristic Curve (n-channel).**

Notice that the bottom end of the curve is at a point on the  $V_{GS}$  axis equal to  $V_{GS(off)}$ , and the top end of the curve is at a point on the  $I_D$  axis equal to  $I_{DSS}$ . This curve shows that

$$I_D = 0 \quad \text{when } V_{GS} = V_{GS(\text{off})}$$

$$I_D = \frac{I_{DSS}}{4} \quad \text{when } V_{GS} = 0.5V_{GS(\text{off})}$$

$$I_D = \frac{I_{DSS}}{2} \quad \text{when } V_{GS} = 0.3V_{GS(\text{off})}$$

$$I_D = I_{DSS} \quad \text{when } V_{GS} = 0$$

The transfer characteristic curve can also be developed from the drain characteristic curves by plotting values of  $I_D$  for the values of  $V_{GS}$  taken from the family of drain curves at pinch-off, as illustrated in Figure for a specific set of curves. Each point on the transfer characteristic curve corresponds to specific values of  $V_{GS}$  and  $I_D$  on the drain curves. For example, when  $V_{GS} = -2$  V,  $I_D = 4.32$  mA. Also, for this specific JFET,  $V_{GS(\text{off})} = -5$  V and  $I_{DSS} = 12$  mA.

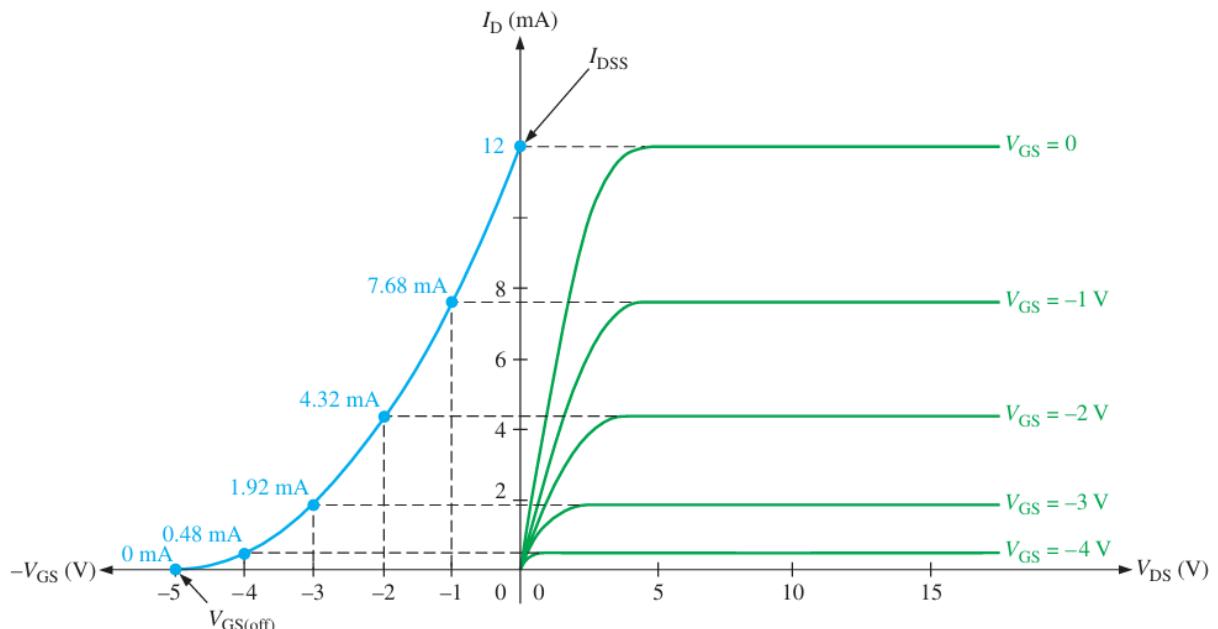


Figure: Example of the development of an n-channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green).

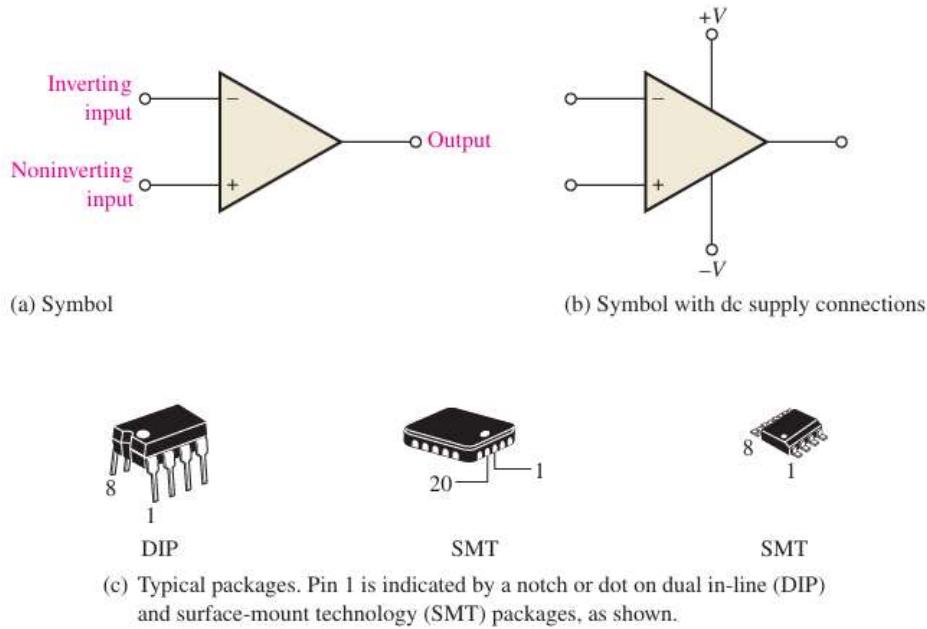
A JFET transfer characteristic curve is expressed approximately as

$$I_D \cong I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

### 3.1 Introduction to Operational Amplifiers

Early operational amplifiers (op-amps) were used primarily to perform mathematical operations such as addition, subtraction, integration, and differentiation—thus the term operational. These early devices were constructed with vacuum tubes and worked with high voltages. Today's op-amps are linear integrated circuits (ICs) that use relatively low dc supply voltages and are reliable and inexpensive.

The standard operational amplifier (op-amp) symbol is shown in Figure 3-1(a).



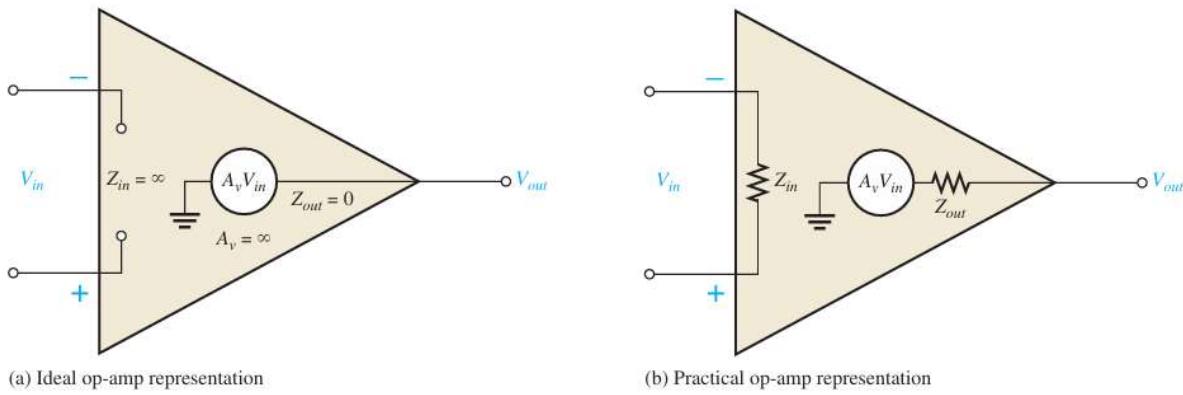
**Figure 3-1:Op-amp symbols and packages.**

It has two input terminals, the inverting (-) input and the noninverting (+) input, and one output terminal. Most op-amps operate with two dc supply voltages, one positive and the other negative, as shown in Figure 3-1(b), although some have a single dc supply. Usually these dc voltage terminals are left off the schematic symbol for simplicity but are understood to be there. Some typical op-amp IC packages are shown in Figure 3-1(c).

#### The Ideal Op-Amp

To illustrate what an op-amp is, let's consider its ideal characteristics. A practical op-amp, of course, falls short of these ideal standards, but it is much easier to understand and analyze the device from an ideal point of view.

First, the ideal op-amp has infinite voltage gain and infinite bandwidth. Also, it has an infinite input impedance (open) so that it does not load the driving source. Finally, it has a zero output impedance. Op-amp characteristics are illustrated in Figure 3-2(a). The input voltage,  $V_{in}$ , appears between the two input terminals, and the output voltage is  $A_v V_{in}$ , as indicated by the internal voltage source symbol.



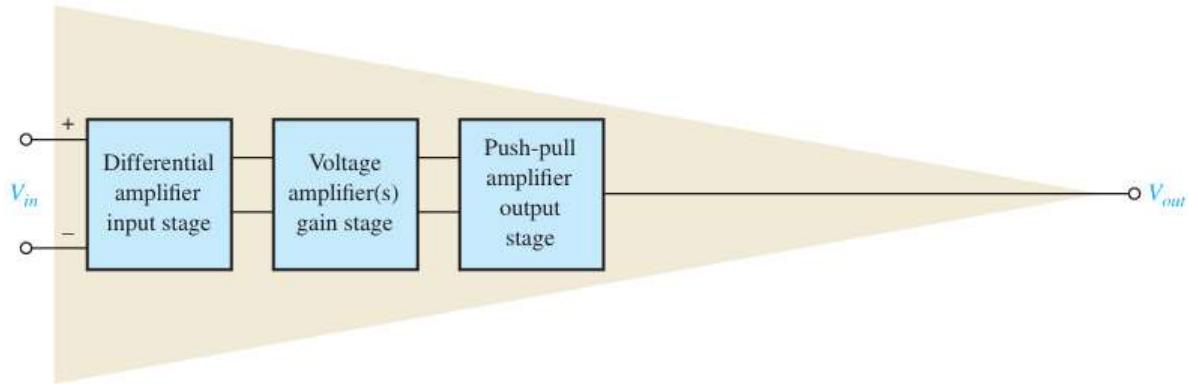
**Figure 3-2: Basic op-amp representations.**

Although integrated circuit (IC) op-amps approach parameter values that can be treated as ideal in many cases, the ideal device can never be made. Any device has limitations, and the IC op-amp is no exception. Op-amps have both voltage and current limitations. Peak to-peak output voltage, for example, is usually limited to slightly less than the two supply voltages. Output current is also limited by internal restrictions such as power dissipation and component ratings. Characteristics of a practical op-amp are very high voltage gain, very high input impedance, and very low output impedance. These are labelled in Figure 3-2(b). Another practical consideration is that there is always noise generated within the op-amp. Noise is an undesired signal that affects the quality of a desired signal. Today, circuit designers are using smaller voltages that require high accuracy, so low-noise components are in greater demand. All circuits generate noise; op-amps are no exception, but the amount can be minimized.

### Internal Block Diagram of an Op-Amp

A typical op-amp is made up of three types of amplifier circuits: a differential amplifier, a voltage amplifier, and a push-pull amplifier, as shown in Figure 3-3. The differential amplifier is the input stage for the op-amp. It provides amplification of the difference voltage between the two inputs. The second stage is usually a class A amplifier that provides additional gain. Some op-

amps may have more than one voltage amplifier stage. A push-pull class B amplifier is typically used for the output stage.



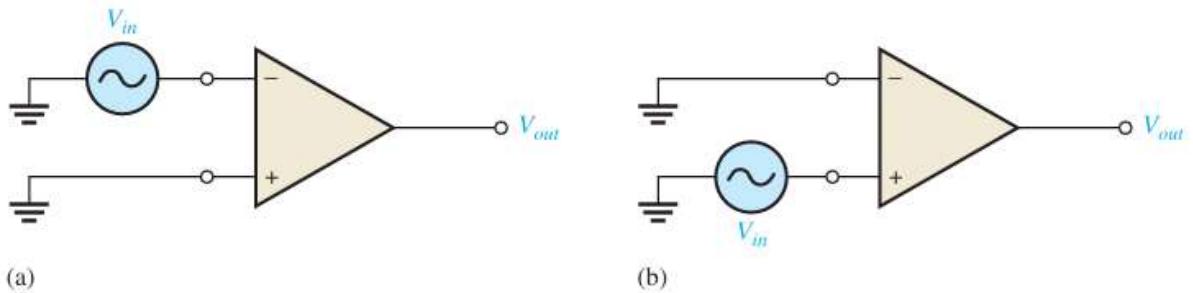
**Figure 3-3:Basic internal arrangement of an op-amp.**

The term differential comes from the amplifier's ability to amplify the difference of two input signals applied to its inputs. Only the difference in the two signals is amplified; if there is no difference, the output is zero. The differential amplifier exhibits two modes of operation based on the type of input signals. These modes are differential and common, which are described in the next section. Since the differential amplifier is the input stage of the op-amp, the op-amp exhibits the same modes.

### **Input Signal Modes**

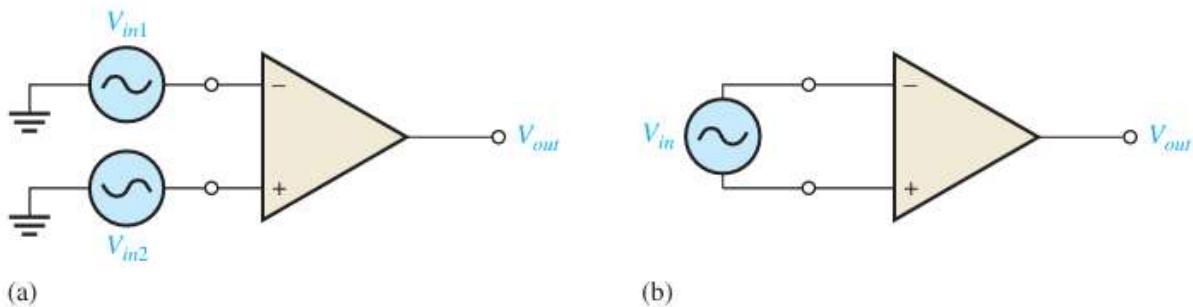
#### **Differential Mode**

In the differential mode, either one signal is applied to an input with the other input grounded or two opposite-polarity signals are applied to the inputs. When an op-amp is operated in the single-ended differential mode, one input is grounded and a signal voltage is applied to the other input, as shown in Figure 3-4. In the case where the signal voltage is applied to the inverting input as in part (a), an inverted, amplified signal voltage appears at the output. In the case where the signal is applied to the noninverting input with the inverting input grounded, as in Figure 3-4(b), a noninverted, amplified signal voltage appears at the output.



**Figure 3-4: Single-ended differential mode.**

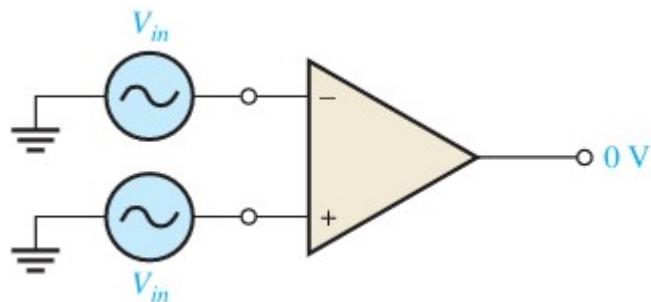
In the double-ended differential mode, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure 3-5(a). The amplified difference between the two inputs appears on the output. Equivalently, the double-ended differential mode can be represented by a single source connected between the two inputs, as shown in Figure 3-5(b).



**Figure 3-5: Double-ended differential mode.**

### Common Mode

In the common mode, two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure 3-6. When equal input signals are applied to both inputs, they tend to cancel, resulting in a zero output voltage.



**Figure 3-6: Common mode of operation**

This action is called common-mode rejection. Its importance lies in the situation where an unwanted signal appears commonly on both op-amp inputs. Common-mode rejection means that this unwanted signal will not appear on the output and distort the desired signal. Common-mode signals (noise) generally are the result of the pick-up of radiated energy on the input lines, from adjacent lines, the 60 Hz power line, or other sources.

## 3.2 Op-Amp Parameters

### Common-Mode Rejection Ratio

Desired signals can appear on only one input or with opposite polarities on both input lines. These desired signals are amplified and appear on the output as previously discussed. Unwanted signals (noise) appearing with the same polarity on both input lines are essentially cancelled by the op-amp and do not appear on the output. The measure of an amplifier's ability to reject common-mode signals is a parameter called the CMRR (common-mode rejection ratio). Ideally, an op-amp provides a very high gain for differential-mode signals and zero gain for common-mode signals. Practical op-amps, however, do exhibit a very small common-mode gain (usually much less than 1), while providing a high open-loop differential voltage gain (commonly from 100,000 to 1,000,000 or more for high-precision op-amps). The open loop voltage gain,  $A_{ol}$ , of an op-amp is the internal voltage gain of the device and represents the ratio of output voltage to input voltage when there are no external components. The higher the open-loop gain with respect to the common-mode gain, the better the performance of the op-amp in terms of rejection of common-mode signals. This suggests that a good measure of the op-amp's performance in rejecting unwanted common-mode signals is the ratio of the open-loop differential voltage gain,  $A_{ol}$ , to the common-mode gain,  $A_{cm}$ . This ratio is the common-mode rejection ratio, CMRR.

$$\text{CMRR} = \frac{A_{ol}}{A_{cm}}$$

The higher the CMRR, the better. A very high value of CMRR means that the open-loop gain,  $A_{ol}$ , is high and the common-mode gain,  $A_{cm}$ , is low.

The CMRR is often expressed in decibels (dB) as

$$\text{CMRR} = 20 \log\left(\frac{A_{ol}}{A_{cm}}\right)$$

The open-loop voltage gain is set entirely by the internal design. Open-loop voltage gain can range up to 1,000,000,000 or more (120 dB) and is not a well-controlled parameter. Generally,

a very high open-loop gain is better, but some very fast op-amps have values that are lower (a few thousand). Datasheets often refer to the open-loop voltage gain as the large-signal voltage gain. Even though open-loop gain is dimensionless, datasheets will often show it as V/mV or V/mV to express the very large values. Thus a gain of 200,000 can be expressed as 200 V/mV.

A CMRR of 100,000, for example, means that the desired input signal (differential) is amplified 100,000 times more than the unwanted noise (common-mode). If the amplitudes of the differential input signal and the common-mode noise are equal, the desired signal will appear on the output 100,000 times greater in amplitude than the noise. Thus, the noise or interference has been essentially eliminated.

CMRR is dependent on the frequency of the common-mode signal; as the frequency of the common-mode signal goes up, the CMRR is degraded. Manufacturers will publish a graph of the CMRR as a function of frequency. Figure 3-7 shows the response of CMRR as a function of the common-mode frequency for a high-quality op-amp. As you can see, the rejection is much better at very low frequencies.

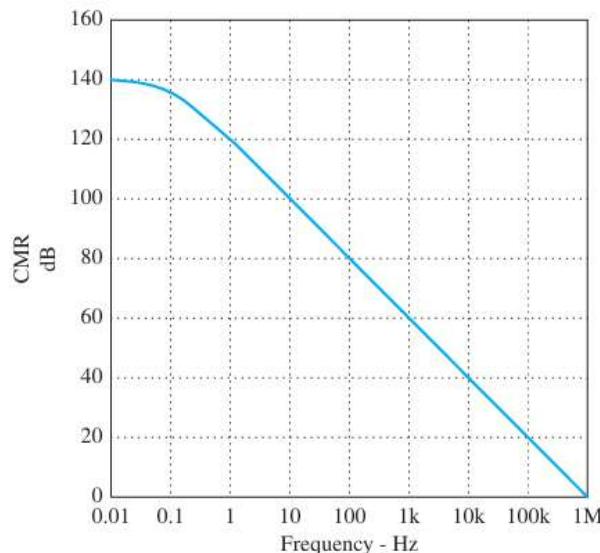


Figure 3-7: CMRR as a function of frequency.

### Maximum Output Voltage Swing ( $V_o(p-p)$ )

With no input signal, the output of an op amp is ideally 0 V. This is called the quiescent output voltage. When an input signal is applied, the ideal limits of the peak-to-peak output signal are  $\pm V_{CC}$ . In practice, however, this ideal can be approached but never reached.  $V_o(p-p)$  varies with the load connected to the op-amp and increases directly with load resistance. For example, the Fairchild KA741 datasheet shows a typical  $V_o(p-p)$  of  $\pm 13$  V for  $V_{CC} = \pm 15$  V when  $R_L = 2$  kV.  $V_o(p-p)$  increases to  $\pm 14$  V when  $R_L = 10$  kV.

Some op-amps do not use both positive and negative supply voltages. One example is when a single dc voltage source is used to power an op-amp that drives an analog-to-digital converter

(discussed in Chapter 14). In this case, the op-amp output is designed to operate between ground and a full-scale output that is near (or at) the positive supply voltage. Op-amps that operate on a single supply use the terminology VOH and VOL to specify the maximum and minimum output voltage. (Note that these are not the same as the digital definitions of VOL and VOH.)

## Input Offset Voltage

The ideal op-amp produces zero volts out for zero volts in. In a practical op-amp, however, a small dc voltage, VOUT(error), appears at the output when no differential input voltage is applied. Its primary cause is a slight mismatch of the base-emitter voltages of the differential amplifier input stage of an op-amp.

As specified on an op-amp datasheet, the input offset voltage, VOS, is the differential dc voltage required between the inputs to force the output to zero volts. Typical values of input offset voltage are in the range of 2 mV or less. In the ideal case, it is 0 V.

The input offset voltage drift is a parameter related to VOS that specifies how much change occurs in the input offset voltage for each degree change in temperature. Typical values range anywhere from about 5 mV per degree Celsius to about 50 mV per degree Celsius. Usually, an op-amp with a higher nominal value of input offset voltage exhibits a higher drift.

## Input Bias Current

You have seen that the input terminals of a bipolar differential amplifier are the transistor bases and, therefore, the input currents are the base currents.

The input bias current is the dc current required by the inputs of the amplifier to properly operate the first stage. By definition, the input bias current is the average of both input currents and is calculated as follows:

$$I_{BIAS} = \frac{I_1 + I_2}{2}$$

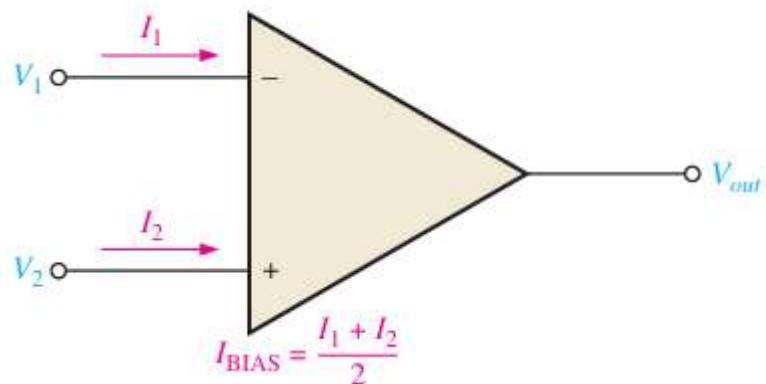


Figure 3-8: Input bias current is the average of the two op-amp input currents.

### Input Impedance

Two basic ways of specifying the input impedance of an op-amp are the differential and the common mode. The differential input impedance is the total resistance between the inverting and the noninverting inputs, as illustrated in Figure 3-9(a). Differential impedance is measured by determining the change in bias current for a given change in differential input voltage. The common-mode input impedance is the resistance between each input and ground and is measured by determining the change in bias current for a given change in common-mode input voltage. It is depicted in Figure 3-9(b).

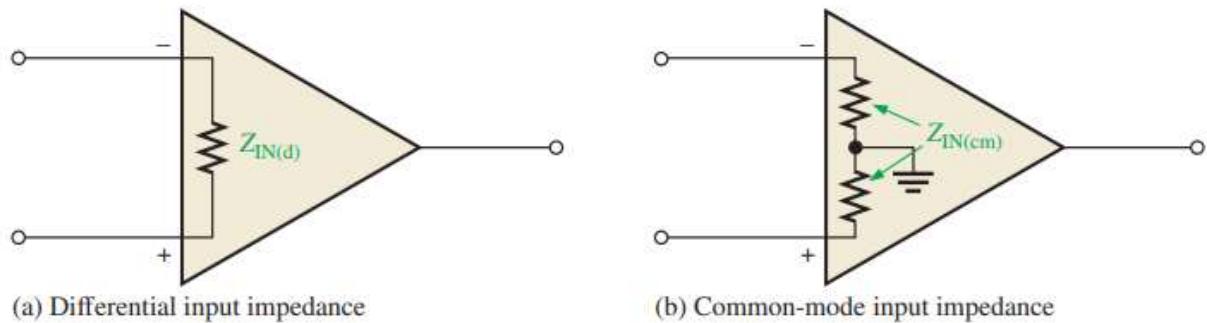


Figure 3-9: Op-amp input impedance.

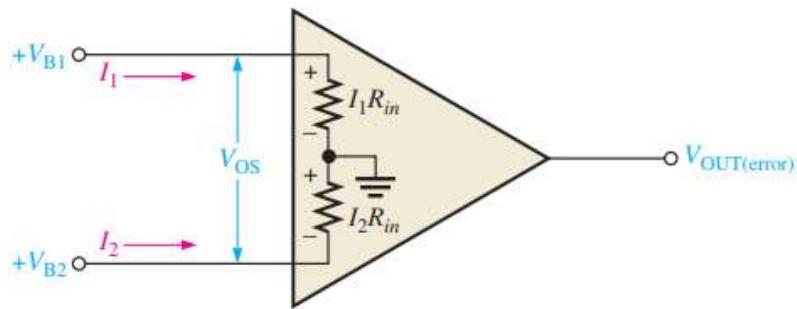
### Input Offset Current

Ideally, the two input bias currents are equal, and thus their difference is zero. In a practical op-amp, however, the bias currents are not exactly equal.

The input offset current, IOS, is the difference of the input bias currents, expressed as an absolute value.

$$I_{OS} = |I_1 - I_2|$$

Actual magnitudes of offset current are usually at least an order of magnitude (ten times) less than the bias current. In many applications, the offset current can be neglected. However, high-gain, high-input impedance amplifiers should have as little IOS as possible because the difference in currents through large input resistances develops a substantial offset voltage, as shown in Figure 3-10.



**Figure 3-10:Effect of input offset current.**

The offset voltage developed by the input offset current is

$$V_{OS} = I_1 R_{in} - I_2 R_{in} = (I_1 - I_2) R_{in}$$

$$V_{OS} = I_{OS} R_{in}$$

The error created by IOS is amplified by the gain  $A_v$  of the op-amp and appears in the output as

$$V_{OUT(error)} = A_v I_{OS} R_{in}$$

A change in offset current with temperature affects the error voltage. Values of temperature coefficient for the offset current in the range of 0.5 nA per degree Celsius are common.

## Output Impedance

The output impedance is the resistance viewed from the output terminal of the op-amp, as indicated in Figure 3-11.

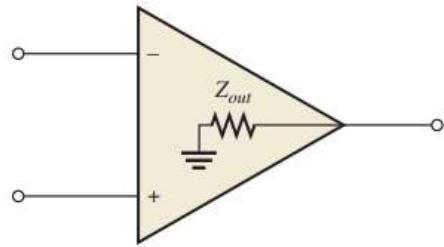


Figure 3-11:Op-amp output impedance.

## Slew Rate

The maximum rate of change of the output voltage in response to a step input voltage is the slew rate of an op-amp. The slew rate is dependent upon the high-frequency response of the amplifier stages within the op-amp. Slew rate is measured with an op-amp connected as shown in Figure 3-12(a).

This particular op-amp connection is a unity-gain, noninverting configuration that will be discussed in Section 12-4. It gives a worst-case (slowest) slew rate. Recall that the high frequency components of a voltage step are contained in the rising edge and that the upper critical frequency of an amplifier limits its response to a step input. For a step input, the slope on the output is inversely proportional to the upper critical frequency. Slope increases as upper critical frequency decreases

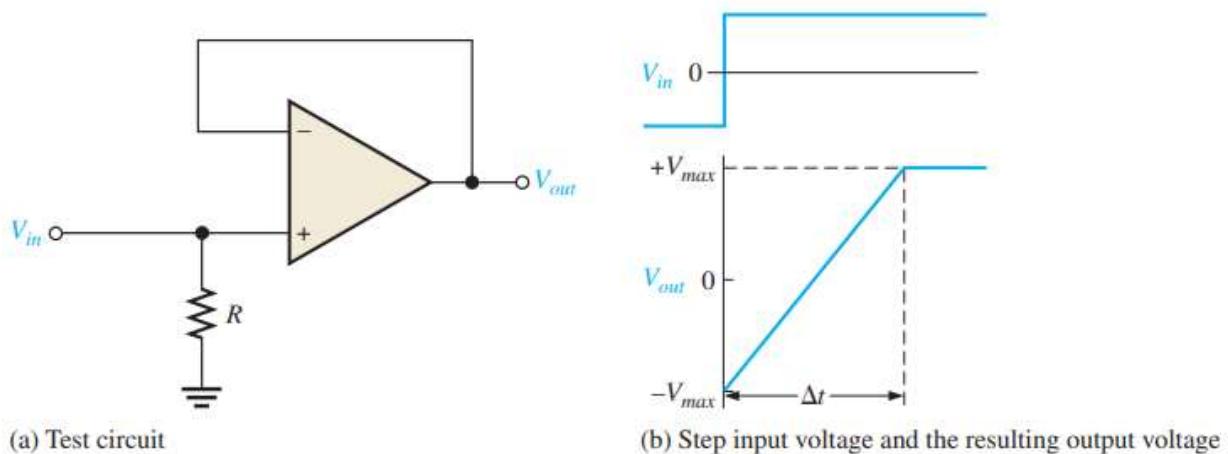


Figure 3-12:Slew-rate measurement.

A pulse is applied to the input and the resulting ideal output voltage is indicated in Figure 12-12(b). The width of the input pulse must be sufficient to allow the output to “slew” from its lower limit to its upper limit. A certain time interval,  $\Delta t$ , is required for the output voltage to go from its lower limit  $-V_{max}$  to its upper limit  $+V_{max}$ , once the input step is applied.

The slew rate is expressed as

$$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta t}$$

where  $\Delta V_{out} = +V_{max} - (-V_{max})$ . The unit of slew rate is volts per microsecond (V/ms).

## Frequency Response

The internal amplifier stages that make up an op-amp have voltage gains limited by junction capacitances, as discussed in Chapter 10. Although the differential amplifiers used in op-amps are somewhat different from the basic amplifiers discussed earlier, the same principles apply. An op-amp has no internal coupling capacitors, however; therefore, the low-frequency response extends down to dc (0 Hz).

## Noise Specification

Noise has become a more important issue in new circuit designs because of the requirement to run at lower voltages and with greater accuracy than in the past. As little as two or three microvolts can create errors in analog-to-digital conversion. Many sensors produce only tiny voltages that can be masked by noise. As a result, unwanted noise from op-amps and components can degrade the performance of circuits.

Noise is defined as an unwanted signal that affects the quality of a desired signal. While interference from an external source (such as a nearby power line) qualifies as noise, for the purpose of op-amp specifications, interference is not included. Only noise generated within the op-amp is considered in the noise specification. When the op-amp is added to a circuit, additional noise contributions are added from other circuit elements, such as the feedback resistors or any sensors. For example, all resistors generate thermal noise—even one sitting in the parts bin. The circuit designer must consider all sources within the circuit, but the concern here is the op-amp specification for noise, which only considers the op-amp.

There are two basic forms of noise. At low frequencies, noise is inversely proportional to the frequency; this is called 1/f noise or “pink noise.” Above a critical noise frequency, the noise becomes flat and is spread out equally across the frequency spectrum; this is called “white noise.” The power distribution of noise is measured in watts per hertz (W/ Hz). Power is proportional to the square of the voltage, so noise voltage (density) is found by taking the square root of the noise power density, resulting in units of volts per square root hertz (V/2Hz). For operational amplifiers, noise level is normally shown with units of nV/2Hz and is specified relative to the input at a specific frequency above the noise critical frequency. For example, a noise level graph for a low-noise op-amp is shown in Figure 3-13; the specification for this op-amp will indicate that the input

voltage noise density at 1 kHz is 1.1 nV/2Hz. At low frequencies, the noise level is higher than this due to the 1/f noise contribution as you can see from the graph.

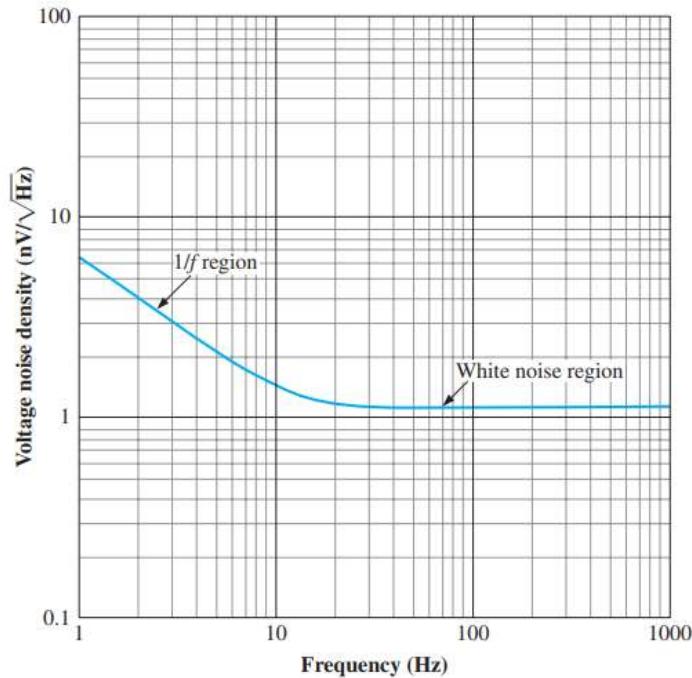


Figure 3-13:Noise as a function of frequency for a typical op-amp.

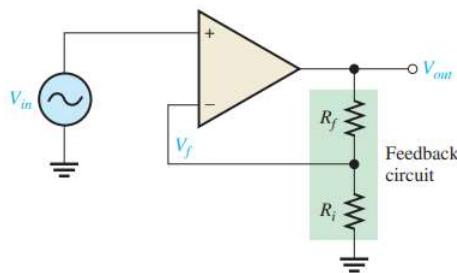
### 3.3 Op-Amps with Negative Feedback:

#### Closed-Loop Voltage Gain, $A_{cl}$

The closed-loop voltage gain is the voltage gain of an op-amp with external feedback. The amplifier configuration consists of the op-amp and an external negative feedback circuit that connects the output to the inverting input. The closed-loop voltage gain is determined by the external component values and can be precisely controlled by them.

#### Noninverting Amplifier

An op-amp connected in a closed-loop configuration as a noninverting amplifier with a controlled amount of voltage gain is shown in Figure 3-14. The input signal is applied to the noninverting (+) input. The output is applied back to the inverting (-) input through the feedback circuit (closed loop) formed by the input resistor  $R_i$  and the feedback resistor  $R_f$ . This creates negative feedback as follows. Resistors  $R_i$  and  $R_f$  form a voltage-divider circuit, which reduces  $V_{out}$  and connects the reduced voltage  $V_f$  to the inverting input.



**Figure 3-14:** Noninverting amplifier.

The feedback voltage is expressed as

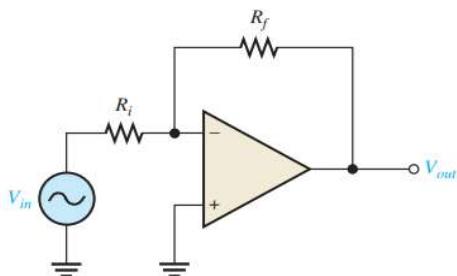
$$V_f = \left( \frac{R_f}{R_f + R_i} \right) V_{out}$$

The closed-loop gain of the noninverting (NI) amplifier is

$$A_{cl(NI)} = 1 + \frac{R_f}{R_i}$$

### Inverting Amplifier

An op-amp connected as an inverting amplifier with a controlled amount of voltage gain is shown in Figure 3-15. The input signal is applied through a series input resistor  $R_i$  to the inverting (-) input. Also, the output is fed back through  $R_f$  to the same input. The noninverting (+) input is grounded.



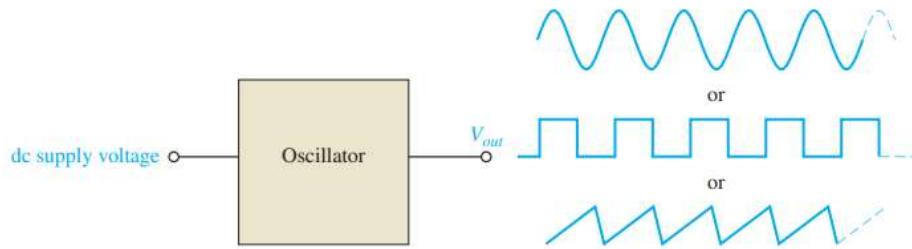
**Figure 3-15:** Inverting amplifier.

The closed-loop gain of the inverting amplifier is

$$A_{cl(I)} = -\frac{R_f}{R_i}$$

## Oscillators

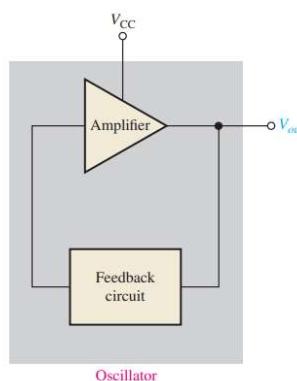
Essentially, an oscillator converts electrical energy from the dc power supply to periodic waveforms. A basic oscillator is shown in Figure 3-16.



**Figure 3-16:**The basic oscillator concept showing three common types of output waveforms: sine wave, square wave, and sawtooth.

### Feedback Oscillators

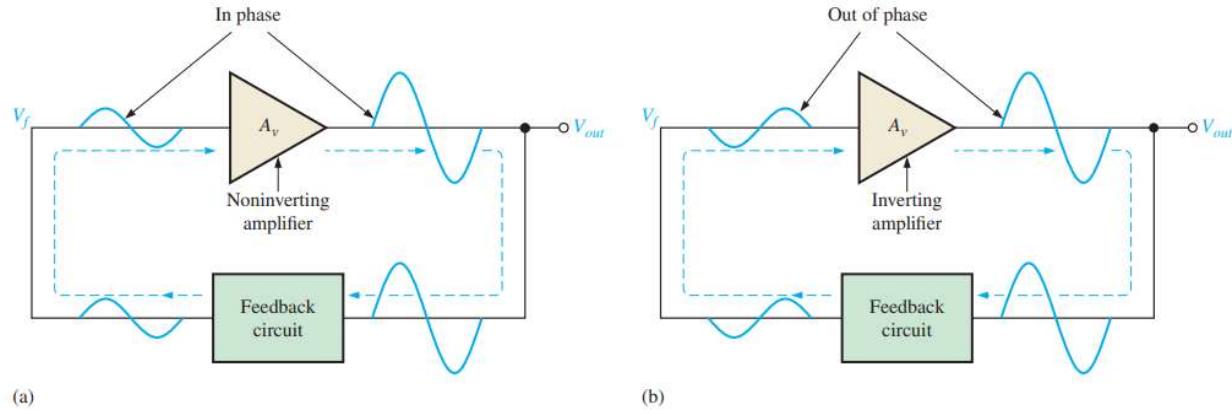
One type of oscillator is the feedback oscillator, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. For a sine wave output, the loop gain is maintained at 1.0 to maintain a low-distortion output. (If the gain is  $> 1$ , the output will be distorted and clipped.) A basic feedback oscillator that produces a sine wave is shown in block diagram form in Figure 3-17. The amplifier provides just enough gain to overcome attenuation in the feedback circuit but may introduce a phase shift in the process (depending on the type of amplifier). The feedback circuit samples the output and returns a fraction of it to the amplifier's input. The feedback circuit compensates for any phase shift introduced by the amplifier. The net result is that the input reinforces the signal to maintain oscillations.



**Figure 3-17:**Basic elements of a feedback oscillator.

## 3.4 Positive Feedback

Positive feedback is characterized by the condition wherein a portion of the output voltage of an amplifier is fed back to the input with no net phase shift around the loop, resulting in a reinforcement of the output signal. This basic idea is illustrated in Figure 3-18(a).



**Figure 3-18:Positive feedback produces oscillation.**

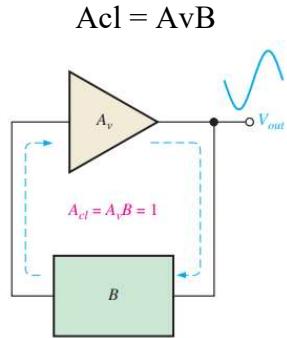
As you can see, the inphase feedback voltage, V<sub>f</sub>, is amplified to produce the output voltage, which in turn produces the feedback voltage. That is, a loop is created in which the signal sustains itself and a continuous sinusoidal output is produced. This phenomenon is called oscillation. In some types of amplifiers, the feedback circuit shifts the phase 180° and an inverting amplifier is required to provide another 180° phase shift so that there is no net phase shift. This is illustrated in Figure 3-18(b).

### 3.5 Conditions for Oscillation

Two conditions are required for a sustained state of oscillation:

1. The phase shift around the feedback loop must be effectively 0°. The feedback circuit accomplishes the necessary phase shift, as was illustrated in Figure 3-18. For a noninverting amplifier the input to the amplifier is returned in phase with the output. For an inverting amplifier, the input is returned 180° out of phase with the output.
2. The voltage gain, A<sub>cl</sub>, around the closed feedback loop (loop gain) must equal or greater than 1 (unity) as illustrated in Figure 3-19. For a sine wave oscillator, the loop gain must be exactly 1; otherwise the output is distorted with clipping.

The voltage gain around the closed feedback loop, A<sub>cl</sub>, is the product of the amplifier gain, A<sub>v</sub>, and the attenuation, B, of the feedback circuit.

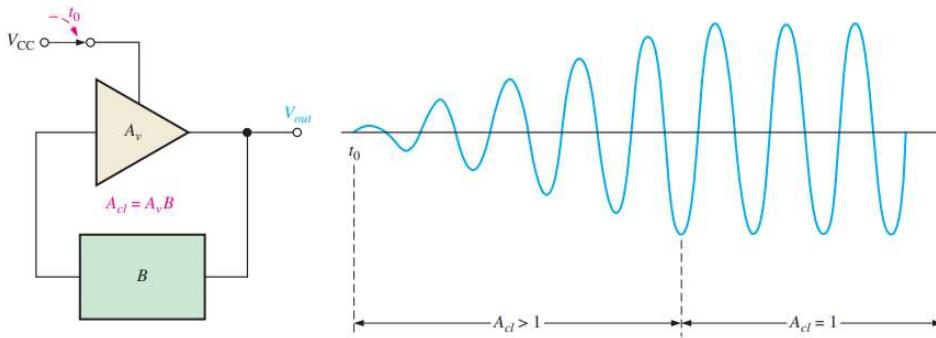


**Figure 3-19:**To maintain a sine wave, the loop gain (product of  $A_vB$ ) must be equal to 1.

If a sinusoidal wave is the desired output, a loop gain greater than 1 will rapidly cause the output to saturate at both peaks of the waveform, producing unacceptable distortion. To avoid this, some form of automatic gain control must be used to keep the loop gain at exactly 1 once oscillations have started. For example, if the attenuation of the feedback circuit is 0.01, the amplifier must have a gain of exactly 100 to overcome this attenuation and not create unacceptable distortion ( $0.01 * 100 = 1$ ). An amplifier gain of greater than 100 will cause the oscillator to limit both peaks of the waveform. An amplifier gain of less than 100 will cause oscillations to die out, hence the need for automatic gain control.

### Start-Up Conditions

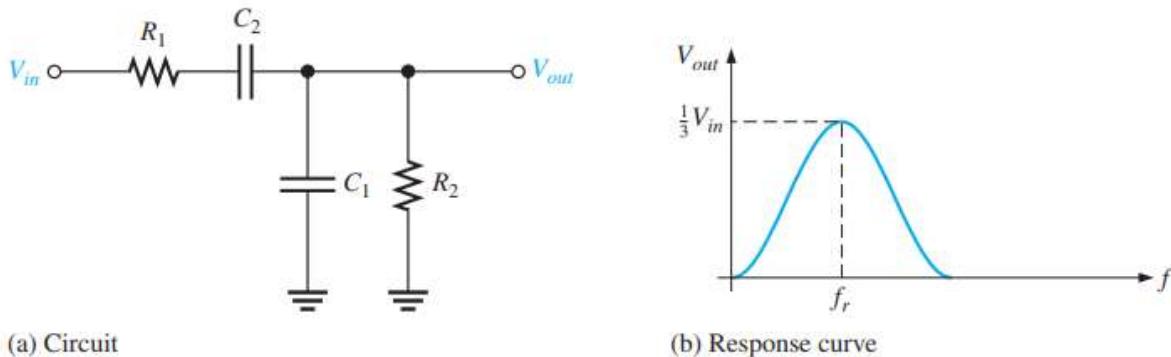
So far, you have seen what it takes for an oscillator to produce a continuous sinusoidal output. Now let's examine the requirements for the oscillation to start when the dc supply voltage is first turned on. As you know, the unity-gain condition must be met for an undistorted sine wave to be maintained. For oscillation to begin, the voltage gain around the positive feedback loop must be greater than 1 so that the amplitude of the output can build up to a desired level. The gain must then decrease to 1 to maintain the correct level of output without distortion. Ways that certain amplifiers achieve this reduction in gain after start-up are discussed in later sections of this chapter. The voltage gain conditions for both starting and sustaining oscillation are illustrated in Figure 3-20. A question that normally arises is this: If the oscillator is initially off and there is no output voltage, how does a feedback signal originate to start the positive feedback buildup process? Initially, a small positive feedback voltage develops from thermally produced broad-band noise in the resistors or other components or from power supply turn-on transients. The feedback circuit permits only a voltage with a frequency equal to the selected oscillation frequency to appear in phase on the amplifier's input. This initial feedback voltage is amplified and continually reinforced, resulting in a buildup of the output voltage as previously discussed.



**Figure 3-20:** When oscillation starts at  $t_0$ , the condition  $A_{cl} > 1$  causes the sinusoidal output voltage amplitude to build up to a desired level. Then  $A_{cl}$  decreases to 1 and maintains the desired amplitude.

### 3.6 The Wien-Bridge Oscillator

One type of sinusoidal feedback oscillator is the Wien-bridge oscillator. A fundamental part of the Wien-bridge oscillator is a lead-lag circuit like that shown in Figure 3-21(a). R1 and C1 together form the lag portion of the circuit; R2 and C2 form the lead portion. The operation of this lead-lag circuit is as follows. At lower frequencies, the lead circuit dominates due to the high reactance of C2. As the frequency increases, XC2 decreases, thus allowing the output voltage to increase. At some specified frequency, the response of the lag circuit takes over, and the decreasing value of XC1 causes the output voltage to decrease.



**Figure 3-21:** A lead-lag circuit and its response curve.

The response curve for the lead-lag circuit shown in Figure 16-6(b) indicates that the output voltage peaks at a frequency called the resonant frequency,  $f_r$ . At this point, the attenuation ( $V_{out}/V_{in}$ ) of the circuit is  $1/3$  if  $R1 = R2$  and  $XC1 = XC2$  as stated by the following equation

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$

The formula for the resonant frequency is,

$$f_r = \frac{1}{2\pi RC}$$

### The Basic Circuit

The lead-lag circuit is used in the positive feedback loop of an opamp, as shown in Figure 3-22(a). A voltage divider is used in the negative feedback loop.

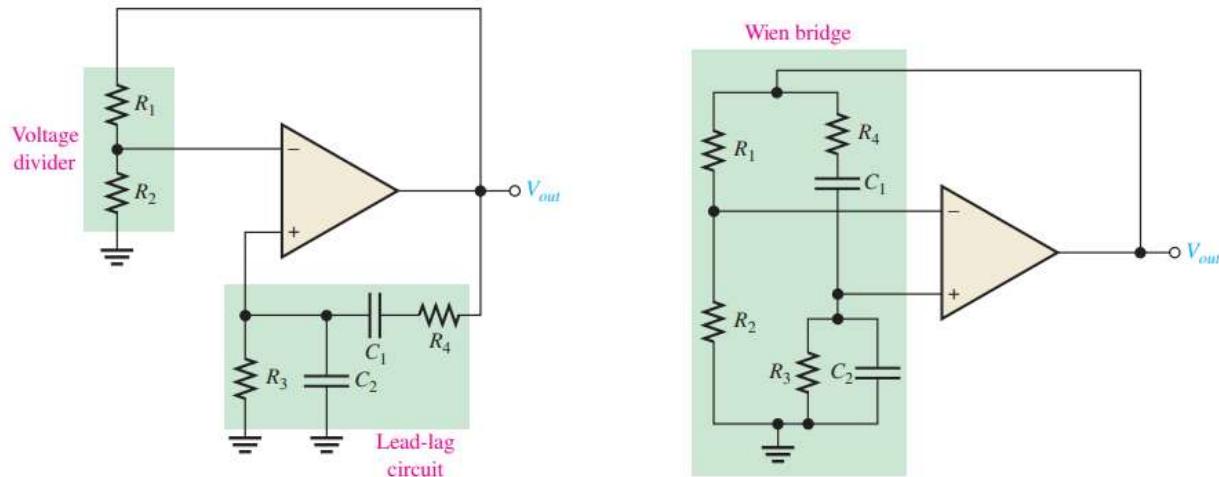


Figure 3-22: The Wien-bridge oscillator schematic drawn in two different but equivalent ways.

The Wien-bridge oscillator circuit can be viewed as a noninverting amplifier configuration with the input signal fed back from the output through the lead-lag circuit. Recall that the voltage divider determines the closed-loop gain of the amplifier.

$$A_{cl} = \frac{1}{B} = \frac{1}{R_2/(R_1 + R_2)} = \frac{R_1 + R_2}{R_2}$$

The circuit is redrawn in Figure 3-22(b) to show that the op-amp is connected across the bridge circuit. One leg of the bridge is the lead-lag circuit, and the other is the voltage divider.

The frequency of oscillations is,

$$f = \frac{1}{2\pi RC}$$

### 3.7 The R-C Phase-Shift Oscillator

Figure 3-23 shows a sinusoidal feedback oscillator called the phase-shift oscillator. Each of the three RC circuits in the feedback loop can provide a maximum phase shift approaching  $90^\circ$ . Oscillation occurs at the frequency where the total phase shift through the three RC circuits is

$180^\circ$ . The inversion of the op-amp itself provides the additional  $180^\circ$  to meet the requirement for oscillation of a  $360^\circ$  (or  $0^\circ$ ) phase shift around the feedback loop.

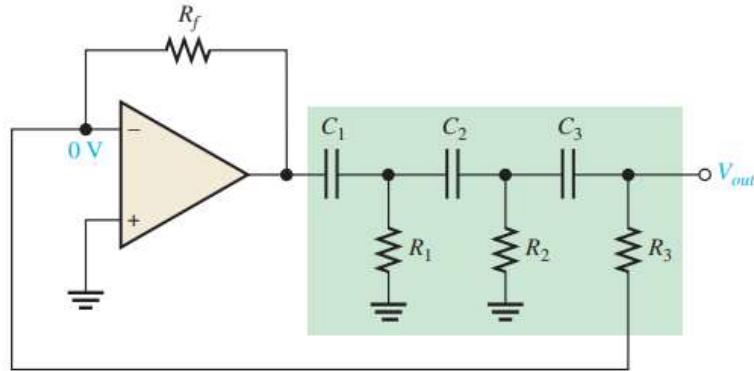


Figure 3-23:RC Phase-shift oscillator.

The attenuation, B, of the three-section RC feedback circuit is

$$B = \frac{1}{29}$$

where  $B = R_3/R_f$ . The derivation of this unusual result is given in “Derivations of Selected Equations” at [www.pearsonhighered.com/floyd](http://www.pearsonhighered.com/floyd). To meet the greater-than-unity loop gain requirement, the closed-loop voltage gain of the op-amp must be greater than 29 (set by  $R_f$  and  $R_3$ ). The frequency of oscillation ( $f_r$ ) is also derived on the website and is stated in the following equation, where  $R_1 = R_2 = R_3 = R$  and  $C_1 = C_2 = C_3 = C$ .

$$f_r = \frac{1}{2\pi\sqrt{6RC}}$$

## Module-4

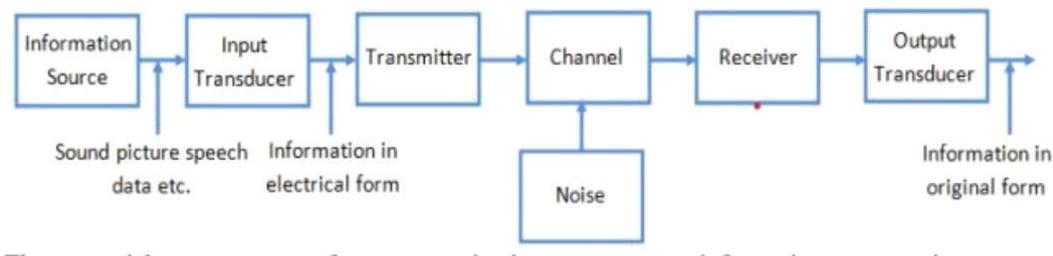
### Communication Systems

#### Communication Definition

- Communication is simply the basic process of exchanging information.
- The electronics equipment used for communication purposes, is called communication equipment.

Different communication equipment when assembled form a communication system.

**Block Diagram of Communication System**



- **Information Source** As we know, a communication system serves to communicate a message or information. This information originates in the information source. In general, there can be various messages in the form of words, group of words, code, symbols, sound signal etc. However, out of these messages, only the desired message is selected and communicated.
- **Input Transducer** A transducer is a device which converts one form of energy into another form. For example, in case of radio-broadcasting, a microphone converts the information or message which is in the form of sound waves into corresponding electrical signal.
- **Transmitter** The function of the transmitter is to process the electrical signal from different aspects
- **Channel and The Noise** There are two types of channels, Wire and wireless namely point- to-point channels and broadcast channels. Example of point-to-point

channels are wire lines, microwave links and optical fibres. Wirelines operate by guided electromagnetic waves and they are used for local telephone transmission. In case of microwave links, the transmitted signal is radiated as an electromagnetic wave in free space. Microwave links are used in long distance telephone transmission

- **Receiver:** The main function of the receiver is to reproduce the message signal in electrical form from the distorted received signal.
- **Destination:** Destination is the final stage which is used to convert an electrical message signal into its original form.

### **Modulation:**

Modulation is a process of superimposing low frequency information signal on a higher frequency signal.

Modulation is defined as changing the characteristics of the carrier signal in accordance with the baseband or message signal.

### **Need of Modulation**

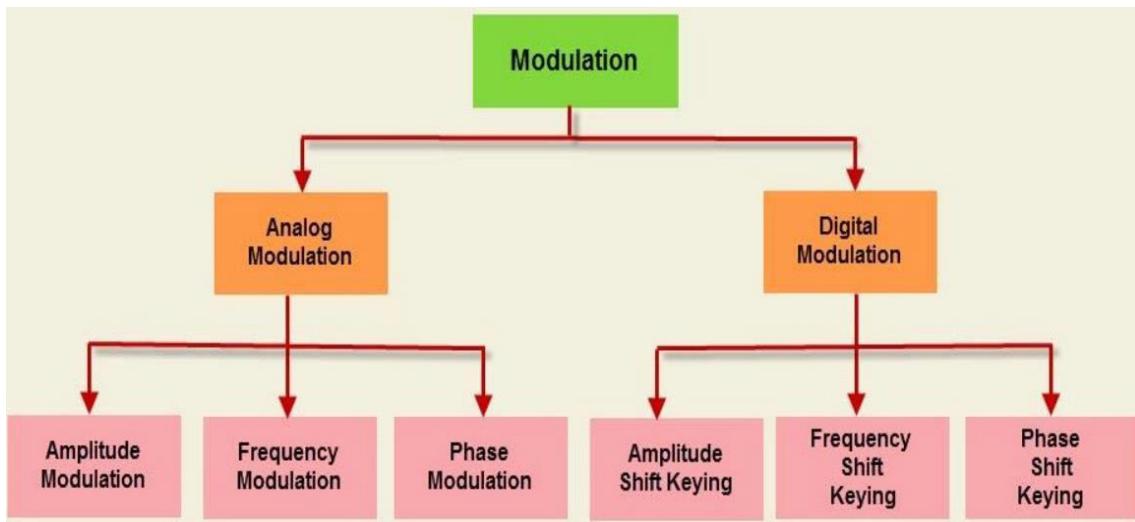
Baseband signal transmission cannot be used for radio communication. To transmit the baseband signal for radio communication, modulation must be used. Modulation is necessary because of the following advantages:

- Reduction in height of antenna.
- Avoids mixing of signals.
- Increase the range of communication.
- Multiplexing is possible.
- Improves quality of reception

### **Types of Communication**

- Analog Communication
- Digital Communication

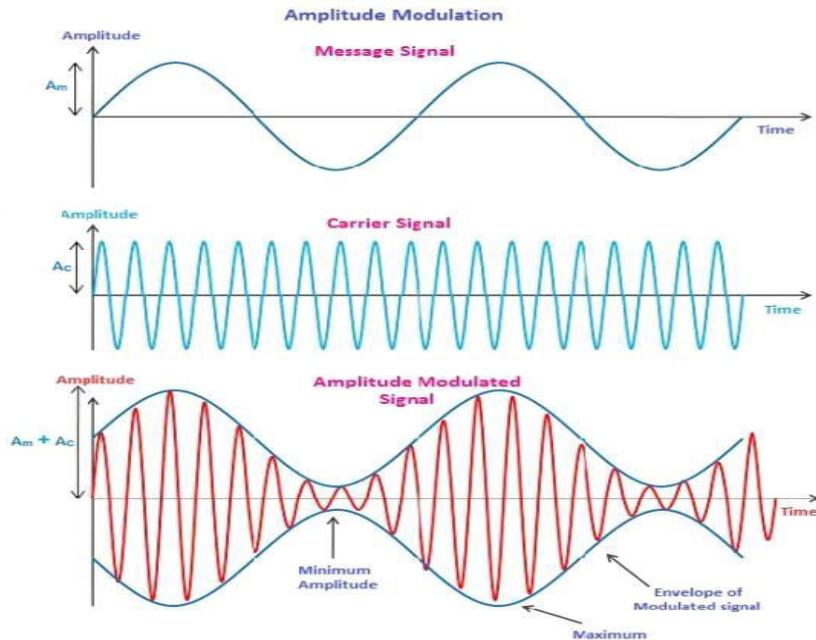
### **Modulation Techniques:**



## Analog Modulation Technique

### Amplitude Modulation:

In AM, the amplitude (signal strength) of the carrier wave is varied in proportion to the information signal (such as an audio signal) being sent, while the frequency of the carrier wave remains constant.



### Advantages of AM

- AM transmitters are not complex.
- AM receivers are simple and easy to detect.

- Less expensive.
- Covers large distance.

### **Disadvantages of AM**

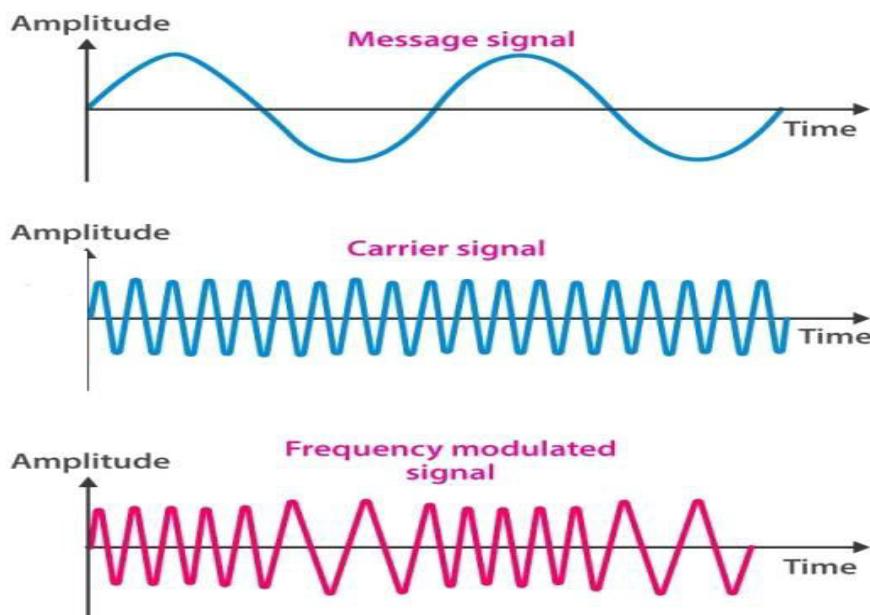
- Requires large bandwidth.
- Requires large power.
- Gets affected due to noise.

### **Applications of AM**

- Radio broadcasting.
- Picture transmission in TV

### **Frequency Modulation:**

In FM, the frequency of the carrier wave is varied in proportion to the information signal while the amplitude and phase remain constant.



### **Advantages of FM**

- Transmitted power remains constant.
- FM receivers are immune to noise.
- Good capture effect.

- No mixing of signals.

### **Disadvantages of FM**

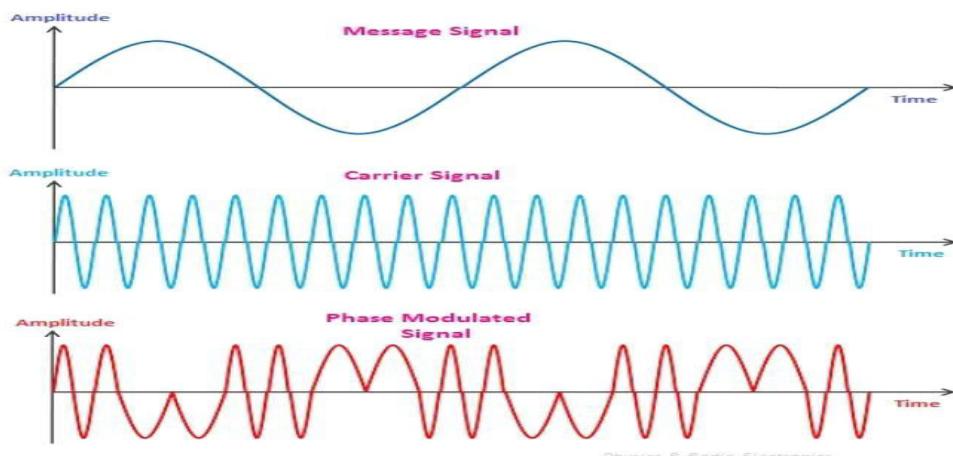
- It uses too much spectrum space.
- The bandwidth is wider.
- The modulation index can be kept low to minimize the bandwidth used.
- But reduction in M.I. reduces the noise immunity.
- Used only at very high frequencies.

### **Applications of FM**

- FM radio broadcasting.
- Sound transmission in TV.
- Police wireless.

### **Phase modulation:**

PM is a type of modulation where the phase of a carrier wave is varied in accordance with the information signal being transmitted. The amplitude and frequency of the carrier wave remain constant, but its phase shifts according to the changes in the modulating signal.



### **Advantage:**

- Phase modulation & demodulation is easy compared to Frequency modulation.
- Phase modulator is used in determining velocity of moving target by extracting Doppler information.

- Doppler information needs stable carrier which is possible in phase modulation but not in frequency modulation.

### **Disadvantage:**

- Phase ambiguity comes if we exceed its modulation index  $\pi$  radian(180 degree).
- we need frequency multiplier to increase phase modulation index.

## **Digital Modulation Technique**

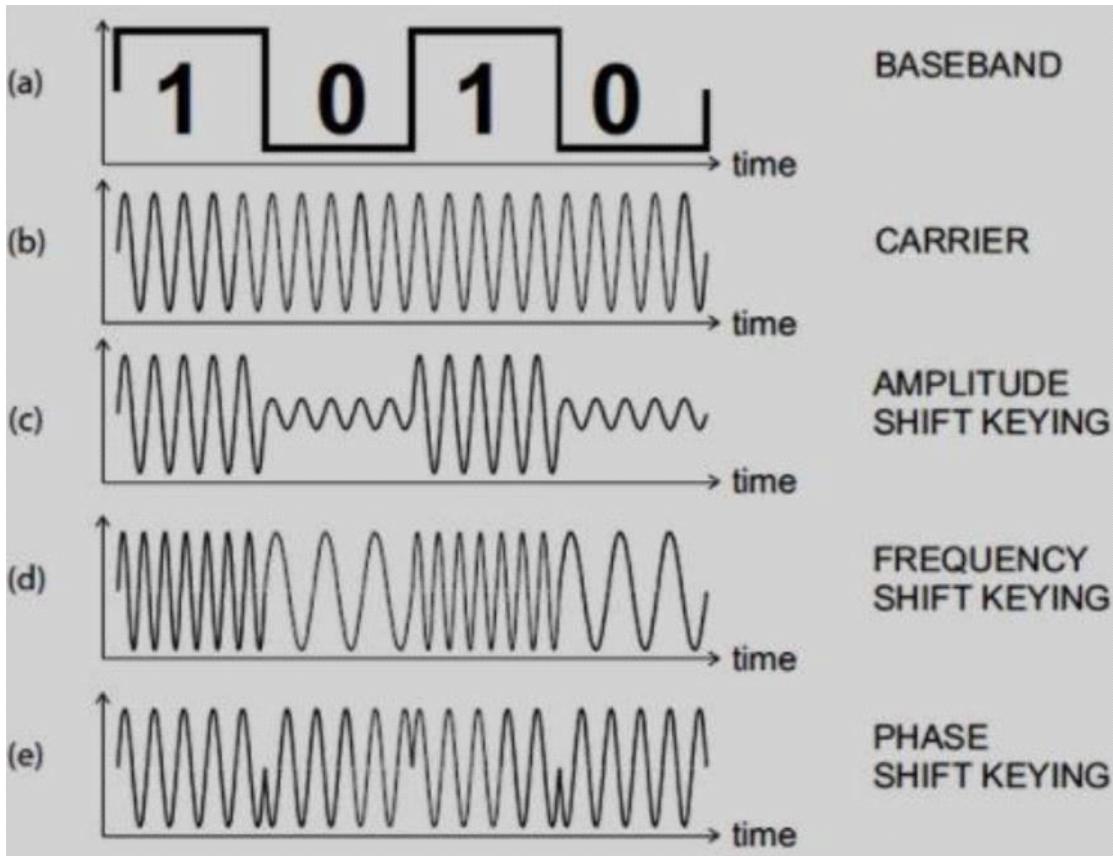
**Amplitude shift keying:** Is a digital modulation technique in which the amplitude of a carrier wave is varied to represent binary data (0s and 1s). In ASK, the carrier signal's amplitude takes on different values depending on whether the transmitted bit is a '1' or a '0'.

### **Frequency shift keying:**

Is a digital modulation technique where the frequency of the carrier signal is varied between predefined values to represent digital information. In FSK, different frequencies correspond to different binary states, typically '0' and '1'. The amplitude and phase of the signal remain constant while the frequency changes.

### **Phase shift Keying:**

Is a digital modulation technique where the phase of a carrier signal is changed to represent digital data. In PSK, different phase angles of the carrier wave correspond to distinct binary values (0s and 1s). This modulation is widely used in digital communication systems due to its efficiency in bandwidth usage and resistance to noise.



**Following are the benefits or advantages of ASK modulation.**

- It offers high bandwidth efficiency.
- It has simple receiver design.

**Following are the drawbacks or disadvantages of ASK modulation.**

- It offers lower power efficiency.
- ASK modulation is very susceptible to noise interference

**Following are the benefits or advantages of FSK:**

- It has lower probability of error ( $P_e$ ).
- It provides high SNR (Signal to Noise Ratio).

### **Disadvantages of FSK:**

It uses larger bandwidth compare to other modulation techniques such as ASK and PSK. Hence it is not bandwidth efficient.

### **Advantages and Disadvantages of PSK: Advantage**

- This type of PSK allows information to be carried with a radio communications signal more efficiently compare with FSK.
- It is less vulnerable to faults when we evaluate with ASK modulation & occupies similar bandwidth like ASK.

### **Disadvantage**

- The bandwidth efficiency of this PSK is less compared with ASK type of modulation
- It is a non-coherent reference signal

### **Comparison Between AM, FM, PM**

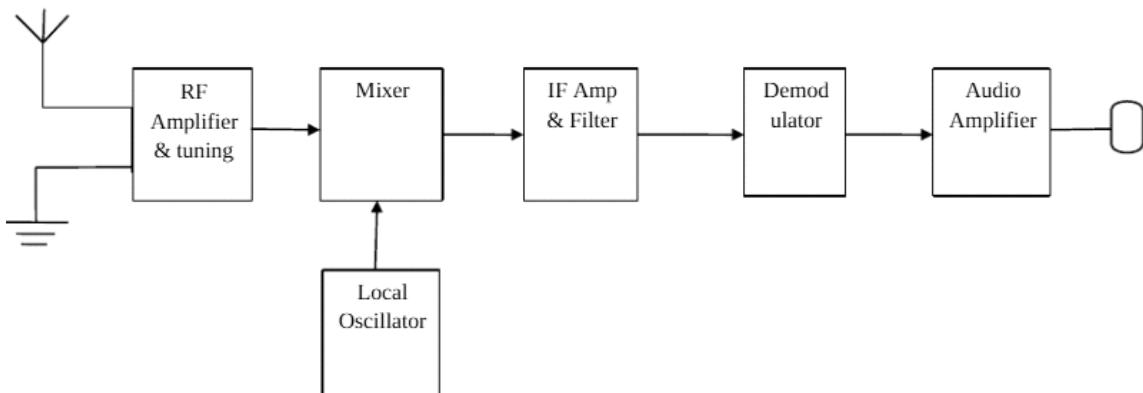
<b>Amplitude modulation</b>	<b>Frequency modulation</b>	<b>Phase modulation</b>
1. Amplitude of the carrier wave is varied in accordance with the message signal.	1. Frequency of the carrier wave is varied in accordance with the message signal.	1. Phase of the carrier wave is varied in accordance with the message signal.
2. Much affected by noise.	2. More immune to the noise.	2. Noise voltage is constant.
3. System fidelity is poor.	3. Improved system fidelity.	Improved system fidelity.
4. Linear modulation	4. Non Linear modulation	4. Non Linear modulation

### **Comparison of FM and PM**

Sr. No.	FM	PM
1	Frequency deviation is proportional to modulating voltage	Phase deviation is proportional to the modulating voltage
2	Noise immunity is better than AM and PM	Noise immunity is better than AM but worse than FM
3	SNR is better than PM	SNR is worse than FM
4	FM is widely used for radio broadcasting	PM is only used in some mobile systems
5	It is possible to receive FM on PM receive	It is possible to receive PM on FM receive
6	Modulation index is proportional to modulating voltage as well as the modulating frequency .	Modulation index is proportional to modulating voltage

## Superheterodyne Receiver

Block Diagram of Superheterodyne Receiver



### Definition

Superheterodyne is made with two different words.when a frequency is generated beyond the human hearing then it is called 'Super' sonic. 'Heterodyne' means mixing of two different frequencies so it is called superheterodyne or 'superhet'.

A Superheterodyne receiver is a type of radio receiver that uses frequency mixing to convert a received signal to a fixed intermediate frequency which can be more conveniently processed than the original carrier frequency.

## **Working**

1. In the superheterodyne receiver, the incoming signal through the antenna is filtered to reject the image frequency and then amplified by the RF amplifier.
2. RF amplifier can be tuned to select and amplify a particular carrier frequency within the AM broadcast range.
3. The carrier of the receiver signal is called radio frequency carrier. The amplified RF frequency is then mixed with the local oscillator frequency.
4. The frequency of local oscillator is not same as the frequency to which RF amplifier is tuned. Local oscillator is tuned to a frequency that may be either higher or lower than the incoming frequency by an amount equal to the if frequency.
5. IF amplifier operations are independent to the frequency at which receiver is tuned is tuned, maintaining the selectivity and sensitivity of the superheterodyne receiver considerably constant throughout the tuning range of the receiver.
6. The generated audio signal is then applied to the AF amplifier to increase the audio frequency level of signal and to provide enough gain to drive the speaker. A speaker is connected to the AF amplifier to play the audio information signal.

## **Advantages:**

- It is easy to filter IF signal compare to RF signal.
- It offers better sensitivity compare to homodyne receiver architecture

## **Disadvantages:**

- It requires additional LO and RF mixers to convert signal from RF to IF before conversion to baseband. This increases cost of overall receiver.
- Moreover filters are also LO leakage as well as undesired frequency components to prevent image frequencies. This also increases cost as well as complexity of the receiver.

## MODULE 3

Number Systems: Introduction, Number Systems (Decimal, Binary, Hexadecimal, Octal), Conversion from one number system to other, Complement of Binary Numbers (1's and 2's), Binary subtraction using 1's and 2's complement.

Digital Electronics: Logic gates, NAND and NOR as universal gates, Boolean Algebra Theorems, De Morgan's theorem, Algebraic Simplification.

### 1. Definition:-

Number System is the way to represent a number in different forms.

### 1.1 Types of Number System:-

#### 1.1.1 Binary Number System :-

It is the number system with base value 2 (ie) it has only two digits to represent the data. (Machine language)

Eg: Digits : 0 or 1

Data: 00, 01, 10, 11, 10010, 00011100 etc...

#### 1.1.2 Decimal Number System:-

It is the number system with base value 10 (ie) it has 10 digits to represent the data. (Human System)

Eg: Digits: 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9

Data: 36, 42, 729, 1256, 98.96 etc...

#### 1.1.3 Octal Number System:-

It is the number system with base value 8 (ie) it has 8 digits to represent the data.

Eg: Digits: 0, 1, 2, 3, 4, 5, 6 and 7

Data: 01, 17, 77, 67, 57 etc..

#### 1.1.4 Hexa decimal Number System:-

It is the number system with base value 16 (ie) it has 16 digits to represent the data.

Eg: Digits: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E  
etc F

Data: 01, 2A, 1E, 5F etc...

Bits & Bytes:-

Bit  $\Rightarrow$  Binary Information

1 Bit = 1 digit

1 Byte = 8 bits

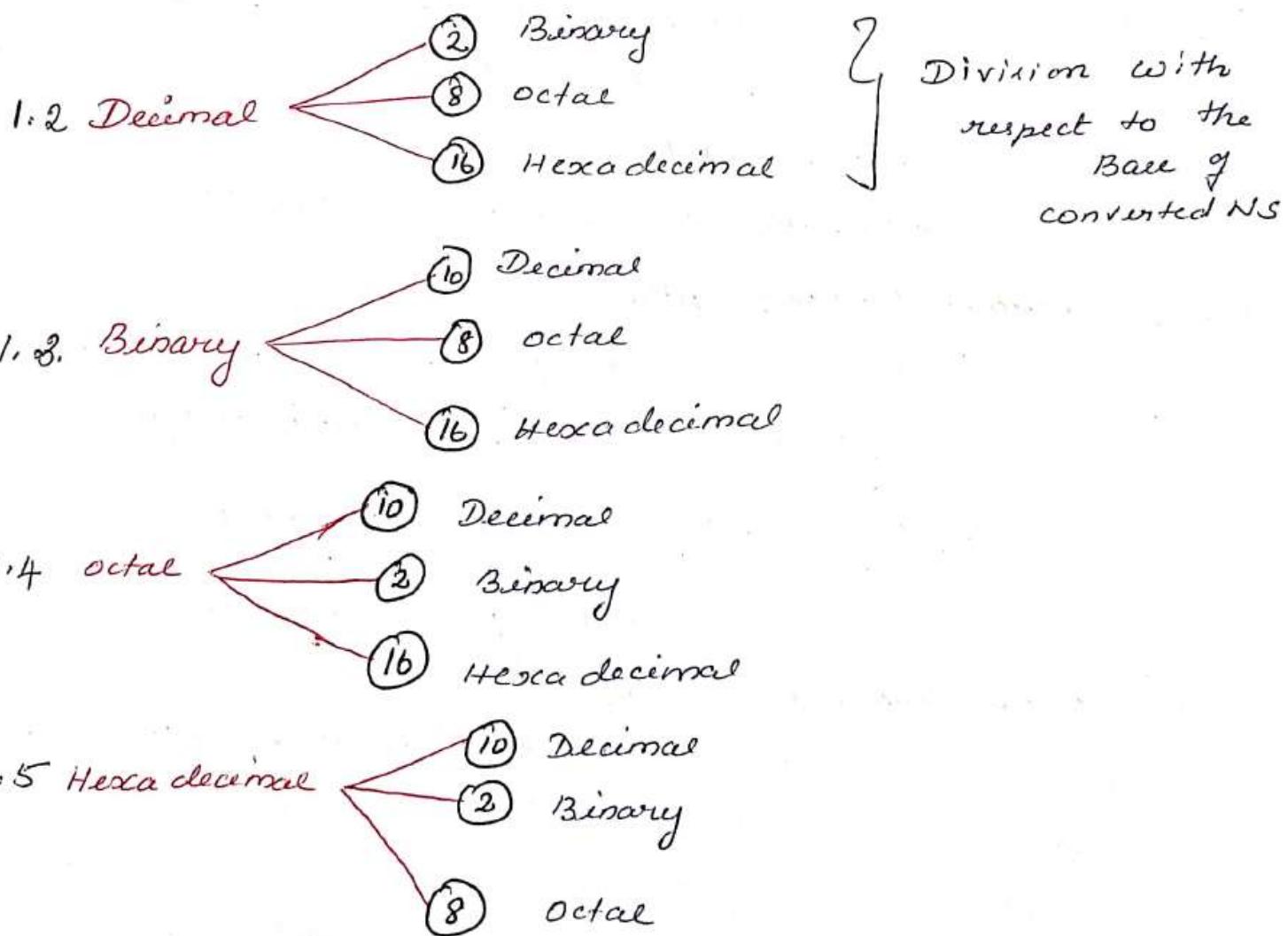
1 kilobyte =  $2^{10}$  = 1024 Bytes

1 megabyte =  $2^{10} \times 2^{10}$  =  $2^{20}$  = 1024 kilobytes

1 gigabyte =  $2^{30}$  = 1024 megabytes

1 terabyte =  $2^{40}$  = 1024 gigabytes

## 1.2 Conversion of Number system



### 1.2.1 Decimal to Binary conversion

1. whole number

2. Fractions

whole numbers

$$(186)_{10} = (10111010)_2$$

$$\begin{array}{r} 2 \mid 186 \\ 2 \mid 93 - 0 \\ 2 \mid 46 - 1 \\ 2 \mid 23 - 0 \\ 2 \mid 11 - 1 \\ 2 \mid 5 - 1 \\ 2 \mid 2 - 1 \\ \hline & 1 - 0 \end{array}$$

Fractions

$$(0.75)_{10} = .110$$

$$0.75 \times 2 = 1.50$$

$$0.50 \times 2 = 1.00$$

$$0.00 \times 2 = 0.00$$

if the Given decimal data is  $(186.75)_{10}$ , then the binary equivalent of the decimal data is  $(10111010.11)_2$

2. convert 65.45 into binary number

$$\begin{array}{r} 2 \mid 65 \\ 2 \mid 32 - 1 \\ 2 \mid 16 - 0 \\ 2 \mid 8 - 0 \\ 2 \mid 4 - 0 \\ 2 \mid 2 - 0 \\ \hline & 1 - 0 \end{array}$$

$$0.45 \times 2 = 0.9$$

$$0.9 \times 2 = 1.8$$

$$0.8 \times 2 = 1.6$$

$$0.6 \times 2 = 1.2$$

$$0.2 \times 2 = 0.4$$

$$0.4 \times 2 = 0.8$$

$$0.8 \times 2 = 1.6$$

$$(65)_{10} = (1000001)_2$$

$$0.45 = 0.111001$$

$$\therefore (65.45)_{10} = (1000001.0111001)_2$$

### 1.2.2 Decimal to octal conversion

1. whole Number

2. Fraction Number

$$(654)_{10} = \underline{\quad\quad\quad}_8$$

$$(890)_{10} = \underline{\quad\quad\quad}_8$$

$$\begin{array}{r} 8 \longdiv{654} \\ 8 \longdiv{81-6} \\ 8 \longdiv{10-1} \\ \hline 1-2 \end{array}$$

$$(654)_{10} = (1216)_8$$

$$\begin{array}{r} 8 \longdiv{890} \\ 8 \longdiv{111-2} \\ 8 \longdiv{13-7} \\ \hline 1-5 \end{array}$$

$$(890)_{10} = (1572)_8$$

$$(0.23)_{10} =$$

$$\begin{aligned} 0.23 \times 8 &= 1.84 \\ 0.84 \times 8 &= 6.72 \\ 0.72 \times 8 &= 5.76 \\ 0.76 \times 8 &= 6.08 \end{aligned}$$

$$\therefore (0.23)_{10} = (1656)_8$$

if  $(654.23)_{10}$  is a decimal number

then  $(1216.165)_8$  is octal equivalent.

### 1.2.3 Decimal to Hexadecimal :

1. whole Number

2. Fraction Number

Eg:  $\begin{array}{r} 16 \longdiv{246} \\ \hline 15 - 6 \end{array}$

$$(246)_{10} = (F6)_{16}$$

Eg:  $(342.56)_{10}$  to Hexadecimal

$$\begin{array}{r} 16 \longdiv{342} \\ 16 \longdiv{21-6} \\ \underline{1-57} \end{array}$$

$$(342)_{10} = (156)_{16}$$

$$\begin{aligned} 0.56 \times 16 &= 8.96 \\ 0.96 \times 16 &= 15.36 \\ 0.36 \times 16 &= 5.76 \end{aligned}$$

$$(0.56)_{10} = (0.8F5)_{16}$$

$$\therefore (342.56)_{10} = (156.8F5)_{16}$$

Binary to Decimal Conversion:

Eg: what is the decimal equivalent of binary number 11001.011

$$\begin{array}{r} 1 \ 1 \ 0 \ 0 1 . \ 0 \ 1 \ 1 \\ | \quad | \quad | \quad | \quad | \quad | \quad | \\ 1 \times 2^{-3} = 0.125 \\ 1 \times 2^{-2} = 0.25 \\ 0 \times 2^{-1} = 0 \\ 1 \times 2^0 = 1 \\ 0 \times 2^1 = 0 \\ 0 \times 2^2 = 0 \\ 1 \times 2^3 = 8 \\ 1 \times 2^4 = 16 \\ \hline 25.375 \end{array}$$

2. 110011.110

$$\begin{array}{r} 1 \ 1 \ 0 \ 0 1 1 . \ 1 \ 1 \ 0 \\ | \quad | \quad | \quad | \quad | \quad | \quad | \\ 0 \times 2^{-3} = 0 \\ 1 \times 2^{-2} = 0.25 \\ 1 \times 2^{-1} = 0.5 \\ 1 \times 2^0 = 1 \\ 1 \times 2^1 = 2 \\ 0 \times 2^2 = 0 \\ 0 \times 2^3 = 0 \\ 1 \times 2^4 = 16 \\ 1 \times 2^5 = 32 \\ \hline 51.75 \end{array}$$

### 1.3.2 Binary to octal:-

Binary Equivalent Table

Octal	Binary
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Table 1.1 - Octal to Binary Equivalent Table

Eg:-

1.  $(10101110101.110010)_2$  to octal number

$010|101|110|101.110|010$   
2 5 6 5 6 2

$$(10101110101.110010)_2 = (2565.62)_8$$

2.  $1101011110110.111001$

$11|010|111|110|110.111|001$   
3 2 7 6 6 . 7 1

$$(1101011110110.111001)_2 = (32766.71)$$

Crc

### Hexadecimal to Binary Conversion:

Hexadecimal	Binary
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A = 10	1010
B = 11	1011
C = 12	1100
D = 13	1101
E = 14	1110
F = 15	1111

Eg:-

Table 1.2 : Hexadecimal to binary Equivalent Table

1.  $(11000111001.110100)_2$  to Hexa decimal

0 1 1 0 | 0 0 1 1 | 1 0 0 1 . 1 1 0 1 | 0 0  
 6      3      9      .    D    0

$$(11000111001.110100)_2 = (639.D0)_H$$

2.  $(11011011110110.11001101)_2$  to Hexa decimal

0 1 1 1 | 0 1 1 0 | 1 1 1 | 0 1 1 0 . 1 1 0 0 | 1 1 0 1  
 7      6      F      6      .    C    D

$$(11011011110110.11001101)_2 = (E6F6.CD)_H$$

## Octal to Decimal Conversion

1. whole number
2. Fractional number

Eg.

$$\begin{array}{r}
 34.125 \\
 | \quad | \\
 5 \times 8^{-3} = 5 \times 0.001953125 = 0.009765625 \\
 2 \times 8^{-2} = 2 \times 0.015625 = 0.03125 \\
 1 \times 8^{-1} = 1 \times 0.125 = 0.125 \\
 4 \times 8^0 = 4 \times 1 = 4.0 \\
 3 \times 8^1 = 3 \times 8 = 24.0 \\
 \hline
 & & & & 28.166
 \end{array}$$

$$\therefore (34.125)_8 = (28.166)_{10}$$

Eg:  $(56.7)_8 = \underline{\hspace{2cm}}_{10}$

$$\begin{array}{r}
 5 \ 6 \ 7 \\
 | \quad | \\
 7 \times 8^0 = 7 \\
 6 \times 8^1 = 48 \\
 5 \times 8^2 = 320 \\
 \hline
 & & 375
 \end{array}$$

$$(56.7)_8 = (375)_{10}$$

Eg. Find the decimal value of octal 103.115

$$\begin{array}{r}
 1 \ 0 \ 3 . 1 \ 1 \ 5 \\
 | \quad | \\
 5 \times 8^{-2} = 0.018 \\
 4 \times 8^{-1} = 0.50 \\
 3 \times 8^0 = 3.00 \\
 0 \times 8^1 = 0.00 \\
 1 \times 8^2 = 64.00 \\
 \hline
 & & 64.518
 \end{array}$$

#### 1.4.2 Octal to Binary conversion:-

Refer Table 1.1 for this conversion

Eg  $(65.73)_2 = \underline{\hspace{2cm}}_2$

6 5. 7 3

110101 . 111011

$$\therefore (65.73)_2 = 110101.111011$$

#### 1.4.3 Octal to Hexa decimal conversion

Octal Number to hexa decimal conversion requires two stages of conversion.

1. Given octal number to Binary [1.4.2]

2. Binary Number to Hexa decimal [Table 1.2]

Eg:

1.  $(654)_8 = \underline{\hspace{2cm}}_{16}$

1. Octal to Binary

6 5 4  
110 101 100

2.  $(110101100)_2 = \underline{\hspace{2cm}}_{16}$

$$0001 | 1010 | 1100 = (1AC)_{16}$$

$$\therefore (654)_8 = (1AC)_{16}$$

### 1.5.1 Hexa decimal to Decimal conversion:-

Eg:  $(B6A)_H = \underline{\hspace{2cm}}_{10}$

$$\begin{array}{r}
 B \quad 6 \quad A \\
 | \quad | \quad | \\
 A : 10 \times 16^0 = 10 \\
 6 : 6 \times 16^1 = 96 \\
 B : 11 \times 16^2 = 2816 \\
 \hline
 2922
 \end{array}$$

$$\therefore (B6A)_H = (2922)_{10}$$

Eg:  $(3A1.4)_H = \underline{\hspace{2cm}}_{10}$

$$\begin{array}{r}
 3 \quad A \quad 1 \quad . \quad 4 \\
 | \quad | \quad | \quad | \quad | \\
 4 : 4 \times 16^{-1} = 0.25 \\
 1 : 1 \times 16^0 = 1.00 \\
 A : 10 \times 16^1 = 160.00 \\
 3 : 3 \times 16^2 = 768.00 \\
 \hline
 929.25
 \end{array}$$

### 1.5.2 Hexa decimal to Binary conversion:-

Consider Table 1.2 for converting hexa decimal Number to a Binary number.

Eg:  $B6A = (101101011010)_2$

1	0	1	1	0	1	0	1	0
B	6	A						

2.  $(3A1.4C)_{16} = \underline{\hspace{2cm}}_2$

3	A	1	.	4	C
0011	1010	0001	.	0100	1100

$$\therefore (3A1.4C)_H = (001110100001.01001100)_2$$

1.5.3 Hexadecimal to Octal conversion:-

Hexadecimal to octal conversion requires 2 steps of conversion.

1. Gives Hexadecimal Number to Binary [1.52]

2. obtained Binary Number to octal conversion  
[Table 1.1]

Eg:  $(ABCD.CA)_H = \underline{\hspace{2cm}}_8$

1. A    B    C    D    .    C    .    A  
 1010    1011    1100    1101    .    1100    1010

2.  $(00|010|10|11.11|00|101.110|010|00)_2$   
 1    2    5    7    1    5.6 2 4

$$\therefore (ABCD.CA)_H = (125715.624)_8$$

CRE

## Binary Addition:-

Addition of two Binary Bits should follow the Basic rules.

$$1. 0 + 0 = 0$$

$$2. 0 + 1 = 1$$

$$3. 1 + 0 = 1$$

$$4. 1 + 1 = 10 \quad [\text{sum} = 0; \text{carry} = 1]$$

Carry is also called as Overflow bit

Example: Convert decimal numbers 13 and 10 into binary, add them, and reconvert into decimal.

Decimal

$$\begin{array}{r} 13 \\ 10 \\ \hline 23 \end{array}$$

Binary

$$\begin{array}{r} 1101 \\ 1010 \\ \hline 10111 \end{array}$$

$$\begin{array}{r} 2 | 23 \\ 2 | 11 - 1 \\ 2 | 5 - 1 \\ 2 | 2 - 1 \\ \hline 1 - 0 \uparrow \end{array}$$

$$\therefore (10111)_2 = (23)_{10}$$

Example: convert  $(3.25)_{10}$  and  $(5.75)_{10}$  into binary, carry out the binary addition and reconvert the result into decimal

$$\begin{array}{r} 2 | 3 \\ \underline{1 - 1} \uparrow \\ 0.25 \times 2 = 0.5 \\ 0.5 \times 2 = 1.0 \downarrow \end{array}$$

$$(3.25)_{10} = (11.01)_2$$

$$(5.75)_{10}$$

$$0.75 \times 2 = 1.50 \downarrow$$
$$0.50 \times 2 = 1.00 \downarrow$$

$$\begin{array}{r} 2 \sqrt{5} \\ 2 \sqrt{2-1} \\ \underline{1-0} \uparrow \end{array}$$

$$(5.75)_{10} = (101.11)_2.$$

$$\begin{array}{r} 011.01 (+) \\ 101.11 \\ \hline 1001.00 \end{array}$$

$$\begin{array}{r} 1001 \\ | \quad | \quad | \quad | \\ 1 \times 2^0 = 1 \\ 0 \times 2^1 = 0 \\ 0 \times 2^2 = 0 \\ 1 \times 2^3 = 8 \\ \hline 9 \end{array}$$

Example:

Add the binary numbers 111.111 and 111

$$\begin{array}{r} 111.111 + \\ 111.000 \\ \hline 1110.111 \end{array}$$

Created in N

.x or

1's complement : 1's complement of a binary number  
 the inversion of individual bit . Inversion of each bit  
 '0' to '1' and '1' to '0'

Eg:	Binary Number	1's Complement
	10101	01010
	1101100	0010011

2's complement : 2's complement of a binary number  
 found by adding 1 to 1's complement

Find the 2's complement of  $(10110)_2$

$$\text{Step1: } 1\text{'s Compliment} = (01001)_2$$

$$\begin{array}{r} \text{Step2: add 1 to 1's Compliment} \\ \begin{array}{r} 01001 \\ + 1 \\ \hline \end{array} \end{array}$$

$$\overline{(01010)}_2$$

Cre

Subtraction using 1's complement [Subtraction in terms of addition]

case 1 Subtrahend (number to be subtracted) is smaller than the minuend (the other number)

Eg:  $1101 - 1000$

$$\begin{array}{r} - 1101 : \text{Minuend} \\ - 1000 : \text{Subtrahend} \\ \hline 0101 \end{array}$$

$$\begin{array}{r} 1101 \\ + \\ \text{'s comp: } 0111 \\ \hline \boxed{1} 0100 \\ \rightarrow 1 \\ \hline 0101 \end{array}$$

Eg:  $11101 - 11000$

$$\begin{array}{r} 11101 : \text{Minuend} \\ 11000 : \text{Subtrahend} \\ \hline 00101 \end{array}$$

$$\begin{array}{r} 11101 \\ + \\ \text{'s comp: } 00111 \\ \hline \boxed{1} 00100 \\ \rightarrow 1 \\ \hline 00101 \end{array}$$

Example: use the 1's complement to perform the following subtractions:-

1.  $1111 - 1011$

$$\begin{array}{r} 1111 \\ - 1011 \\ \hline 0100 \end{array} \quad \begin{array}{r} 1111 \\ 0100 (+) \\ \hline \boxed{1} 0011 \\ \rightarrow 1 \\ \hline 0100 \end{array} : \text{'s comp}$$

2.  $110011 - 100101$

$$\begin{array}{r} 110011 \\ 010101 (+) (\text{'s comp.}) \\ \hline \boxed{1} 001101 \\ \rightarrow 1 \\ \hline 001110 \end{array}$$

Case: 2 Subtrahend is larger than the minuend:

1. complement the subtrahend
2. proceed as in addition
3. complement the result and place a negative sign in front of the answer.

Eg:  $11000 - 11101$

~~01~~  $\begin{array}{r} 101101 \\ 11101 \\ \hline 11011 \end{array}$

1's  $\begin{array}{r} 00100 \\ \hline 00101 \end{array}$

9's  $\begin{array}{r} 00101 \\ \hline \end{array}$

$11000$

1's comp:  $00010$

$\begin{array}{r} 11010 \\ - 00101 \\ \hline \end{array}$

[complement result  
and place  
negative sign]

$\therefore \text{result} = -00101$

Example: use the 1's complement to perform the following subtractions:-

1.  $1111 - 1011$

$\begin{array}{r} 1111 \\ - 1011 \\ \hline 0100 \end{array}$

$\begin{array}{r} 1111 \\ 0100 \quad (+) \\ \hline 10011 \end{array}$  : 1's comp

2.  $110011 - 100101$

$\begin{array}{r} 110011 \\ 011010 \quad (+) \quad (1's \text{ comp.}) \\ \hline 1001101 \end{array}$

Subtraction using 2's complement:-

The 2's complement is found by adding 1 to the LSB (Least significant Bit) of the 1's complement.

use 2's complement of perform the subtraction

$$1101 - 1010$$

$$\begin{array}{r} 1101 \\ 0110 \quad (+) \\ \hline \boxed{0011} \end{array} \qquad \begin{array}{r} 1010 \\ 1\text{'s comp. } 0101 \\ 2\text{'s comp. } \overline{\underline{0110}} \end{array}$$

Rule for subtraction using 2's complement

1. Determine the 2's complement of subtrahend
2. Proceed as in addition
3. If there is a carry, disregard it
4. If there is no carry, answer is negative and is the 2's complement of the actual magnitude.

Example:-

Subtract  $(1101)_2$  from  $(11101)_2$  using 2's complement method.

$$\begin{array}{r} 11101 \\ 00101 \quad + \\ \hline \boxed{00010} \end{array} \qquad \begin{array}{r} 11011 \\ 1\text{'s comp. } 00100 \\ 2\text{'s comp. } \overline{\underline{00101}} \end{array}$$

Ans:  $(00010)_2$

Logic gates:-

- 1. OR
  - 2. AND
  - 3. NOT
  - 4. NOR
  - 5. NAND
  - 6. EX-OR
  - 7. EX-NOR
- Basic gates
- Universal gates : These gates can simulate all other gates function.
- Special gates

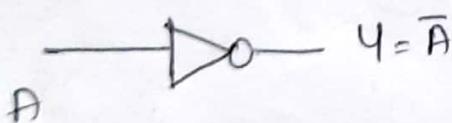
## Logic gates

- Logic gates are the building blocks of digital circuits
- A logic gate has one or more inputs & perform a particular logic function & produce a single output
- The operation of a logic gate can be well understood with the help of truth table
- Truth Table gives the output for all the possible combinations of the inputs.

### Types of gates

#### (i) NOT gate / INVERTER

The NOT gate accepts one input & the output is the opposite of the input



Boolean Expression:  $Y = \bar{A}$

Input A	Output Y = $\bar{A}$
0	1
1	0

- A low Voltage is converted to a high Voltage output & high Voltage is converted to a low Voltage input.
- ∴ In a Not gate, the output is the Complement of the input.

## AND gate

- AND gate performs logical multiplication ~~knowledge~~
- It can have two or more inputs & a single output.
- Operation of AND gate is such that, the output is high(1), only when all the inputs are high. low(0), when any of the inputs are low.

Symbol



Boolean Expression

$$Y = A \cdot B$$

Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

## OR gate

- OR gate performs logical addition.
- operation of OR gate is such that, the output is high(1), when one of inputs is high . low(0) , when all the inputs are low

Symbol

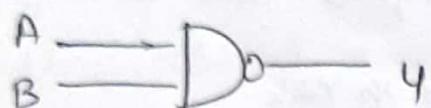


$$Y = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

## NAND gate

- NAND gate is the ~~an~~ AND gate with an inverted output.
- output of NAND gate is high, when any ~~or~~ all the inputs are low
- output is low when all the inputs are high.

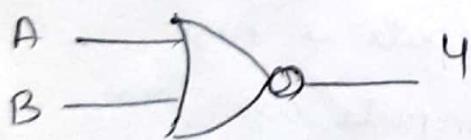


$$Y = \overline{AB}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

## NOR gate

- NOR gate is the OR gate with an inverted output
- output is high, when all the inputs are low
- output is low, when any of the inputs are high.

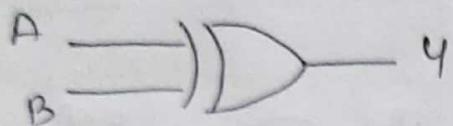


$$Y = \overline{A+B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

## XOR gate

- XOR gate stands for exclusive OR gate
- output will be high if the input values are different
- output will be low if input values are same

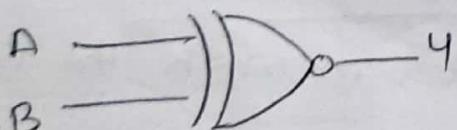


$$\begin{aligned} Y &= A \oplus B \\ &= \bar{A}B + A\bar{B} \end{aligned}$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

## XNOR gate

- It is the complement of XOR gate.
- output is high , when the inputs are ~~both~~ Equal
- output is low, when the inputs are not same

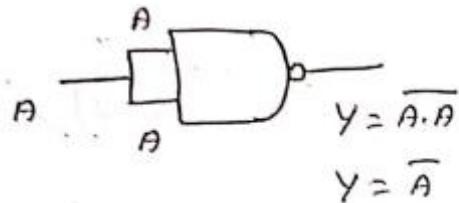


$$\begin{aligned} Y &= \overline{A \oplus B} \\ &= \bar{A}\bar{B} + AB \end{aligned}$$

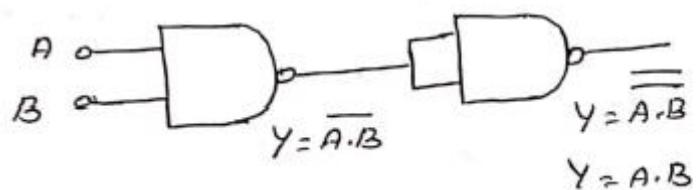
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

NAND as universal gate.

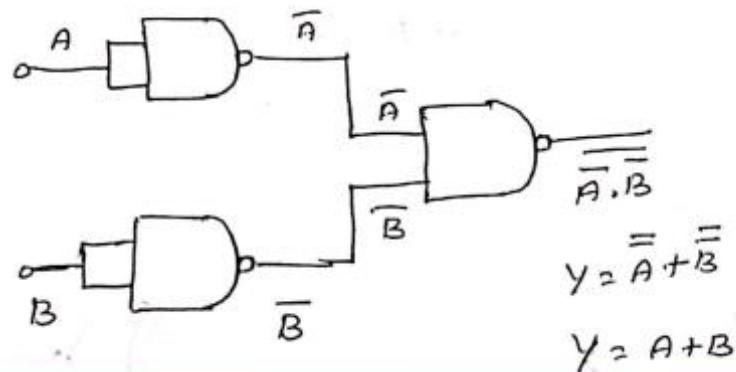
NOT gate using NAND



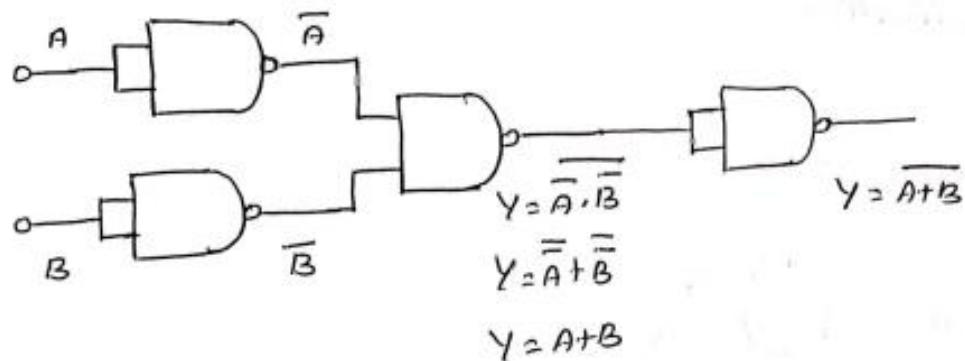
AND gate using NAND



OR gate using NAND



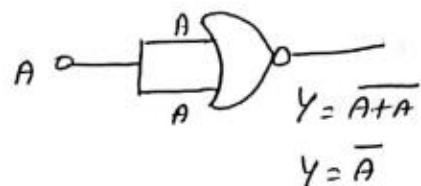
NOR gate using NAND gate



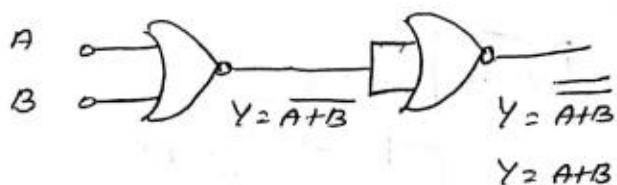
NOR Gate Implementation! -

Realization of other gates is possible using NOR gate

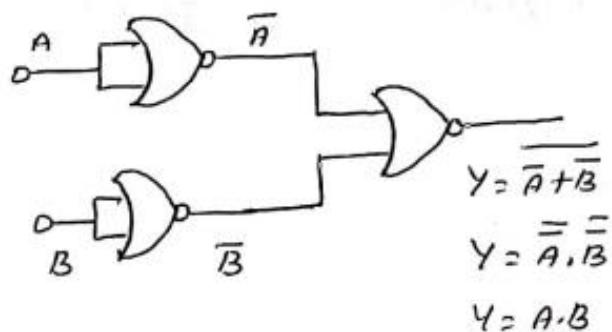
NOT gate using NOR



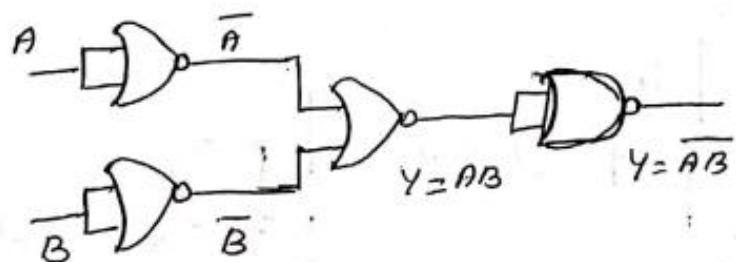
OR gate using NOR



AND gate using NOR



NAND gate using NOR



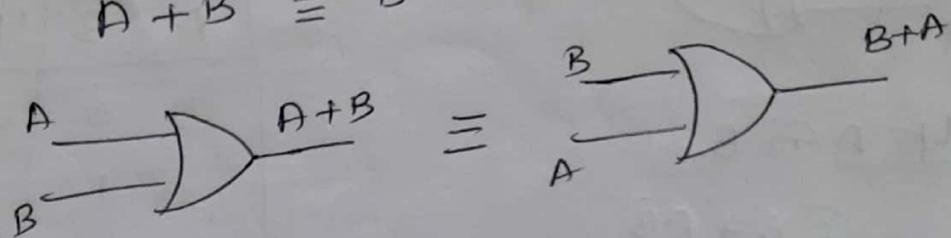
## Boolean Algebra

### Laws of Boolean Algebra

#### (i) Commutative Law of Addition

It states that the order in which the variables are ORed makes no difference in the output.

$$\text{ie } A + B \equiv B + A$$

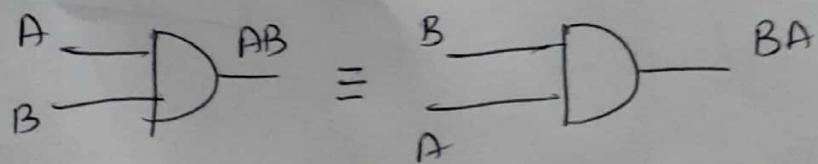


A	B	$A + B$	$B + A$
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

#### (ii) Commutative law of multiplication

It states that the order in which the variables are ANDed makes no difference in the output

$$AB \equiv BA$$



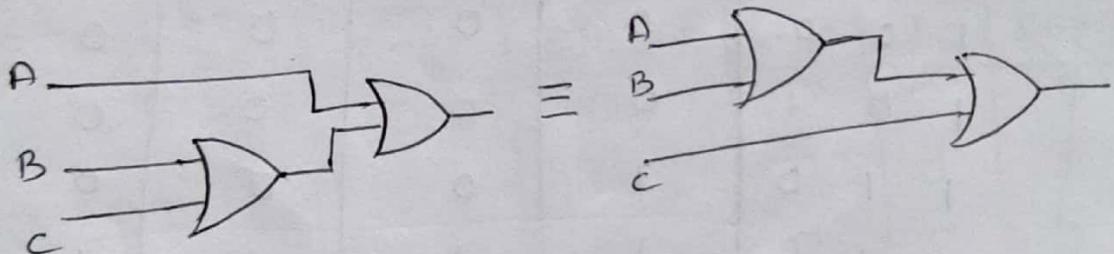
A	B	AB	BA
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

Associative Law

Associative Law for addition

This law states that ORing of several variables, the result is same, regardless of grouping of variables.

$$A + (B + C) \equiv (A + B) + C$$

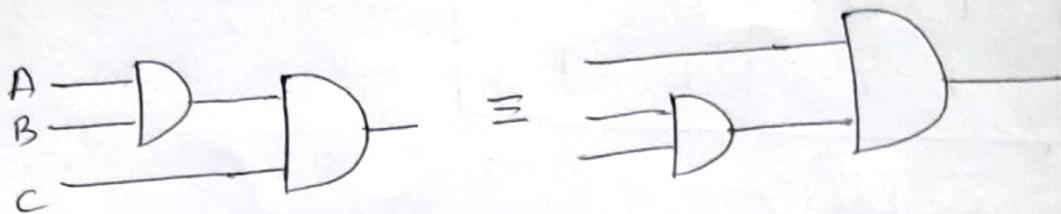


A	B	C	$B+C$	$A+(B+C)$	$A+B$	$(A+B)+C$
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

## Associative law for multiplication

This states that ANDing of several variables, the result is same regardless of grouping of variables.

$$(AB)C \equiv A(BC)$$



A	B	C	AB	(AB)C	BC	A(BC)
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

## Distributive Law

Distributive Law States that ORing several Variables & ANDing the result with a single Variable is Equivalent to ANDing Single Variable with Each of the Several Variables & then ORing the product

$$A(B+C) = AB + AC$$

$$A+BC = (A+B)(A+C)$$

A	B	C	$B+C$	$A(B+C)$	$AB$	$AC$	$AB+AC$
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

## Identities of Boolean Algebra

### • Identities of Boolean Addition / Multiplication

$$A + 0 = A$$

$$A + 1 = 1$$

$$A + A = A$$

$$A + \bar{A} = 1$$

$$\bar{\bar{A}} = A$$

$$A \cdot 0 = 0$$

$$A \cdot 1 = A$$

$$A \cdot A = A$$

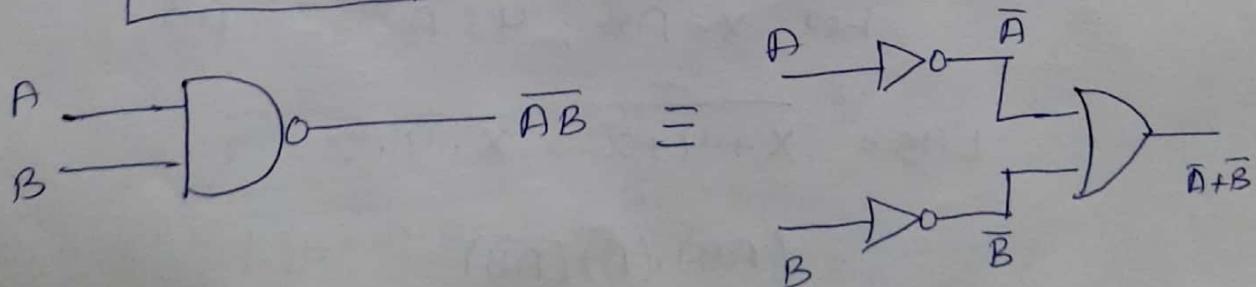
$$A \cdot \bar{A} = 0$$

### • DeMorgan's Law

$$\textcircled{1} \quad \overline{AB} = \bar{A} + \bar{B}$$

The complement of a product is equal to sum of the complements

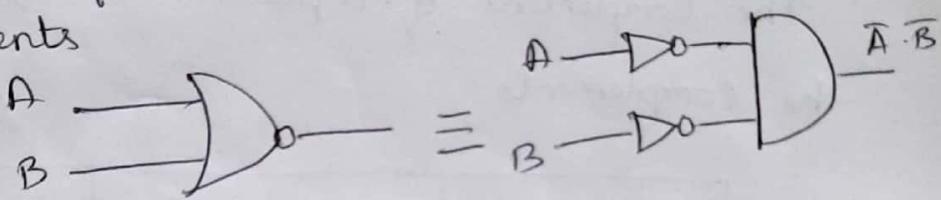
A	B	AB	$\overline{AB}$	$\bar{A}$	$\bar{B}$	$\bar{A} + \bar{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0



$$\textcircled{2} \quad \overline{A+B} = \overline{A} \cdot \overline{B}$$

A	B	$A+B$	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

- Complement of sum is equal to product of complements



### Algebraic Simplification

$$\textcircled{1} \quad \text{prove that } \overline{\overline{AB} + \overline{A} + AB} = 0$$

Proof: LHS =  $\overline{\overline{AB} + \overline{A} + AB}$

Let  $X = \overline{AB}$ ,  $Y = \overline{A}$ ,  $Z = AB$

$$\therefore \text{LHS} = \overline{X+Y+Z} = \overline{X} \cdot \overline{Y} \cdot \overline{Z}$$

$$= (AB) \cdot (A) (\overline{AB})$$

$$= AB (\overline{A} + \overline{B})$$

$$= A \cdot \overline{A} B + A B \overline{B}$$

$$= 0$$

$$\textcircled{2} \quad \text{Simplify } AB + \overline{AC} + A\overline{B}C(AB + C)$$

$$\text{Soln: } AB + \overline{AC} + A\overline{B}C(AB + C)$$

$$= AB + \overline{AC} + A\overline{B}C \cdot A \cdot B + A\overline{B}C \cdot C$$

$$= AB + \overline{AC} + A \cdot C(0) + A\overline{B}C$$

$$= AB + A\overline{B}C + \overline{AC}$$

$$= A[B + \overline{B}C] + \overline{AC}$$

$$= A[(B + \overline{B})(B + C)] + \overline{A} + \overline{C}$$

$$= A(B + C) + \overline{A} + \overline{C}$$

$$= \underbrace{AB}_{\text{1}} + \underbrace{AC}_{\text{1}} + \underbrace{\overline{A}}_{\text{1}} + \underbrace{\overline{C}}_{\text{1}}$$

$$= (A + \overline{A})(\overline{A} + B) + (\overline{C} + A)(\overline{C} + C)$$

$$= \overline{A} + B + A + \overline{C}$$

$$= \overline{B} + \overline{C}$$

$$\begin{aligned}\textcircled{3} \quad Y &= \overline{\overline{AB} + ABC + A(B + A\overline{B})} \\ &= \overline{A(\overline{B} + BC) + AB + A\overline{B}} = \\ &= \overline{A(\overline{B} + B)(\overline{B} + C)} + A(B + \overline{B}) \\ &= \overline{A(\overline{B} + C)} + A = \overline{\overline{A} + (\overline{B} + C) + A} \\ &= \overline{1 + \overline{B} + C} = \overline{1} = 0\end{aligned}$$

$$\begin{aligned}
 ④ & \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y + xy \\
 &= \bar{y} [\bar{x}\bar{z} + \bar{x}z + \bar{x} + x] \\
 &= \bar{y} [1 + \bar{x}\bar{z}] = \bar{y}
 \end{aligned}$$

$$\begin{aligned}
 ⑤ & ABC + A\bar{B}C + \bar{A}BC \\
 AB(C+\bar{C}) + \bar{A}BC &= AB + \bar{A}BC \\
 = B(A+\bar{A}C) &= B(A+\bar{A})(A+C) \\
 = B(A+C) &= AB + BC
 \end{aligned}$$

$$\begin{aligned}
 ⑥ & \overline{xy+x\bar{y}z} + x(\bar{y}+x\bar{y}) \\
 \overline{\overline{xy} + \overline{x\bar{y}z}} + \overline{x\bar{y}} &= \\
 \overline{\overline{xy} + \overline{x\bar{y}z}} &= \overline{1 + \overline{x\bar{y}}} = \overline{1} = 0
 \end{aligned}$$

$$\begin{aligned}
 ⑦ & y = (A+\bar{B}+\bar{C})(A+\bar{B}+C) \\
 &= A + A\bar{B} + AC + A\bar{B} + \bar{B} + \bar{B}C + A\bar{C} \\
 &\quad + \bar{B}\bar{C} + 0 \\
 &= A(1 + \bar{B} + C + \bar{B} + \bar{C}) + \bar{B}(1 + C + \bar{C}) \\
 &= A + \bar{B}
 \end{aligned}$$

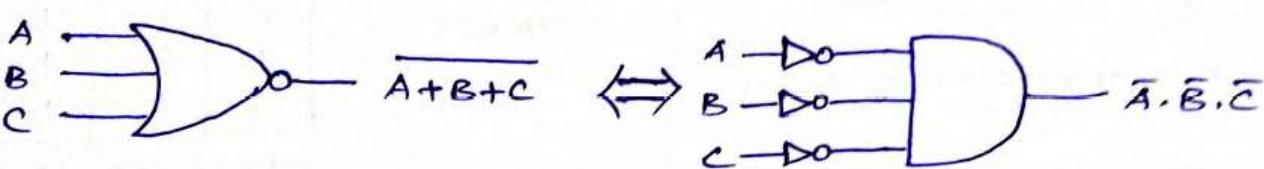
$$\begin{aligned}
 ⑧ & y = C(B+C)(A+B+C) \\
 &= (BC+C)(A+B+C) \\
 &= C(B+1)(A+B+C) = AC + BC + C \\
 &= C(A+B+1) = C
 \end{aligned}$$

## De Morgan's Theorem :-

First Law Statement :

✓ It is states that "The Compliment of Sum of the variables A, B & C is equal to the product of their Individual Complements.

$$\overline{A+B+C} = \bar{A} \cdot \bar{B} \cdot \bar{C}$$



Logic diagram

Logic diagram

A	B	C	$\overline{A+B+C}$	$\bar{A} \cdot \bar{B} \cdot \bar{C}$
0	0	0	1	1
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

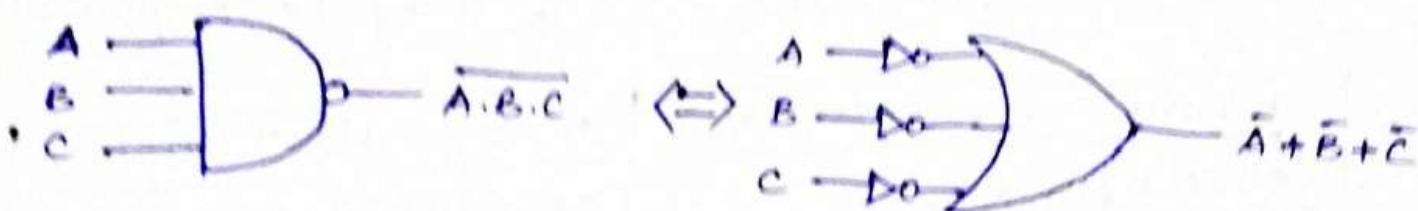
Truth Table

EQUAL

## Second Law Statement :-

✓ It is stated that "The complement of product of the variables A, B & C is equal to the sum of their individual Complements."

$$\overline{A \cdot B \cdot C} = \bar{A} + \bar{B} + \bar{C}$$



Logic diagram

A	B	C	$\overline{A \cdot B \cdot C}$	$\bar{A} + \bar{B} + \bar{C}$
0	0	0	1	1
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Truth Table

EQUAL

**Ex. 4.11 :**  $\bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + ABD$

$$\begin{aligned}
 &= \bar{A}BD (\bar{C} + C) + ABD \\
 &= \bar{A}BD + ABD \\
 &= BD (\bar{A} + A) \\
 &= BD
 \end{aligned}$$

Distributive law

Rule 6 :  $[A + \bar{A} = 1]$

Distributive law

Rule 6 :  $[A + \bar{A} = 1]$

**Ex. 4.12 :**

$$A + \bar{A}B + A\bar{B} = A + B$$

$$\begin{aligned}
 L.H.S &= A + \bar{A}B + A\bar{B} \\
 &= A + B + A\bar{B} \\
 &= A + A + B \\
 &= A + B
 \end{aligned}$$

Rule 11 :  $[A + \bar{A}B = A + B]$

Rule 11 :  $[A + A\bar{B} = A + B]$

Rule 5 :  $[A + A = A]$

**Ex. 4.13 :**

$$\begin{aligned}
 &\overline{AB + \bar{A} + AB} \\
 &= \overline{\bar{A} + \bar{B} + \bar{A} + AB} \\
 &= \overline{\bar{A} + \bar{B} + \bar{A} + B} \\
 &= \overline{\bar{A} + 1} \\
 &= \bar{1} \\
 &= 0
 \end{aligned}$$

Theorem 1 :  $\overline{AB} = \bar{A} + \bar{B}$

Rule 11 :  $[A + \bar{A}B = A + B]$

Rule 5 :  $[A + A = A]$  and

Rule 6 :  $[A + \bar{A} = 1]$

Rule 2 :  $[A + 1 = 1]$

**Ex. 4.14 :**  $AB + \bar{A}\bar{C} + A\bar{B}C (AB + C)$

$$\begin{aligned}
 &= AB + \bar{A}\bar{C} + A\bar{B}BC + A\bar{B}CC \quad \text{Distributive law} \\
 &= AB + \bar{A}\bar{C} + A\bar{B}CC \quad \text{Rule 8 : } [A \cdot \bar{A} = 0] \\
 &= AB + \bar{A}\bar{C} + A\bar{B}C \quad \text{Rule 7 : } [A \cdot A = A] \\
 &= AB + \bar{A} + \bar{C} + A\bar{B}C \quad \text{Theorem 1 : } [\bar{AB} = \bar{A} + \bar{B}] \\
 &= \bar{A} + B + \bar{C} + A\bar{B}C \quad \text{Rule 11 : } [A + \bar{A}B = A + B] \\
 &= \bar{A} + A\bar{B}C + B + \bar{C} \quad \text{Commutative law} \\
 &= \bar{A} + \bar{B}C + B + \bar{C} \quad \text{Rule 11 : } [A + \bar{A}B = A + B] \\
 &= \bar{A} + B + \bar{C} + \bar{B}C \quad \text{Here } B = \bar{B}C \\
 &= \bar{A} + B + \bar{C} + \bar{B} \quad \text{Commutative law} \\
 &= \bar{A} + \bar{C} + 1 \quad \text{Rule 11 : } [A + \bar{A}B = A + B] \\
 &= 1 \quad \text{Rule 6 : } [A + \bar{A} = 1] \\
 & \quad \text{Rule 2 : } [A + 1 = 1]
 \end{aligned}$$

**Ex. 5.5 :** Simplify the expression  $Z = A B + A \bar{B} \cdot (\bar{\bar{A}}\bar{\bar{C}})$

**Sol. :**

**Step 1 :** Apply the DeMorgan's theorem and multiply out all terms to get expression in sum of products form

$$\begin{aligned}Z &= A B + A \bar{B} \cdot (\bar{\bar{A}}\bar{\bar{C}}) \\&= A B + A \bar{B} \cdot (\bar{\bar{A}} + \bar{\bar{C}}) \\&= A B + A \bar{B} \cdot (A + C) \\&= A B + A \bar{B} A + A \bar{B} C\end{aligned}$$

De Morgan's theorem 1

Rule :  $[\bar{\bar{A}} = A]$

Distributive law

**Step 2 :** Search for common terms for factorization and apply boolean rules

$$\begin{aligned}Z &= A B + A \bar{B} A + A \bar{B} C \\&= A B + A \bar{B} + A \bar{B} C \\&= A B + A \bar{B} (1 + C) \\&= A B + A \bar{B} \\&= A ( B + \bar{B} ) \\&= A\end{aligned}$$

Rule 7 :  $[AA = A]$

Rule 2 :  $[1 + C = 1]$

Rule 6 :  $[A + \bar{A} = 1]$