AMD K6-III Architecture 32 KByte Level-One Instruction Cache Predecode 64-Entry ITLB Logic 20 KByte Predecode Cache 16 Byte Fetch Level-One Cache **Branch Logic** Controller Multiple Instruction Decoders x86 to RISC86 (8192-Entry BHT) (16-Entry BTC) (16-Entry RAS) Four RISC86 Decode 100 MHz Super Socket 7 Out-of-Order Bus **Execution Engine** Interface Scheduler Instruction Buffer **Control Unit** (24 RISC86) Six RISC86 **Operation Issue** Branch Store Register X Functional Units Register Y Functional Units Floating Load 256 KByte Resolution Integer/Multimedia/3DNow! Integer/Multimedia/3DNow! **Point Unit** Unit Unit Unit Level-Two Cache Store Queue 32 KByte Level-One Dual-Port Data Cache 128-Entry DTLB