Cyrix 6x86 architecture

Bus Control Unit

Cache
- 256 Byte Instruction Line Cache
- 16 KByte Unified Cache

Integer Unit
- IF / ID1
- X Pipe: ID2, AC1, AC2, EX, WB
- Y Pipe: ID2, AC1, AC2, EX, WB

Memory Management Unit

FPU
- Floating Point Queue
- Floating Point Processor

Instruction Address

Instruction Data — 128 bit

32 bit

Address — 32 bit

Data

X Data — 32 bit

X Data — 32 bit

Sequence Control Lines

FPU Opcode

X Linear Address — 32 bit

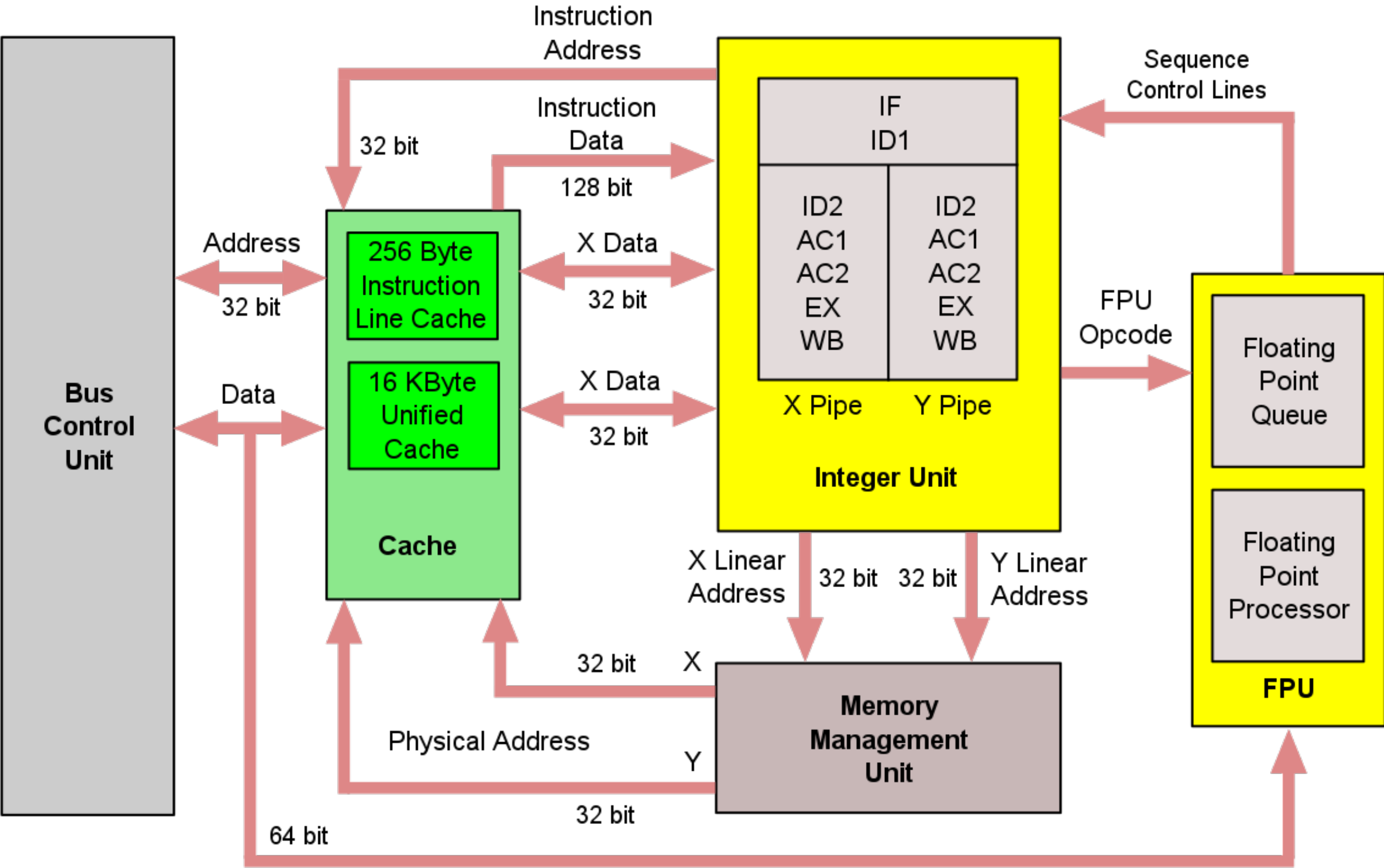Y Linear Address — 32 bit

32 bit   X

Physical Address

Y

32 bit

64 bit

IF: Prefetch Stage
AC: Address Calculation Stages
EX: Execution Stages
ID: Decode Stages
WB: Write Back Stages