	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSL (immediate)	0	0	0	0	0	imm5					Rm			Rd		
LSR (immediate)	0	0	0	0	1	imm5					Rm			Rd		
ASR (immediate)	0	0	0	1	0	imm5					Rm			Rd		
ADD (register1)	0	0	0	1	1	0	0	Rm			Rn			Rd		
SUB (register)	0	0	0	1	1	0	1	Rm			Rn			Rd		
ADD (3-bit immediate)	0	0	0	1	1	1	0	imm3			Rn			Rd		
SUB (3-bit immediate)	0	0	0	1	1	1	1	imm3			Rn			Rd		
MOV (immediate)	0	0	1	0	0	Rd			imm8							
CMP (immediate)	0	0	1	0	1	Rn			imm8							
ADD (8-bit immediate)	0	0	1	1	0	Rdn			imm8							
SUB (8-bit immediate)	0	0	1	1	1	Rdn			imm8							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AND (register)	0	1	0	0	0	0	0	0	0	0	Rm			Rdn		
EOR (register)	0	1	0	0	0	0	0	0	0	1	Rm			Rdn		
LSL (register)	0	1	0	0	0	0	0	0	1	0	Rm			Rdn		
LSR (register)	0	1	0	0	0	0	0	0	1	1	Rm			Rdn		
ASR (register)	0	1	0	0	0	0	0	1	0	0	Rm			Rdn		
ADC (register)	0	1	0	0	0	0	0	1	0	1	Rm			Rdn		
SBC (register)	0	1	0	0	0	0	0	1	1	0	Rm			Rdn		
ROR (register)	0	1	0	0	0	0	0	1	1	1	Rm			Rdn		
TST (register)	0	1	0	0	0	0	1	0	0	0	Rm			Rn		
RSB (immediate)	0	1	0	0	0	0	1	0	0	1	Rn			Rd		
CMP (register1)	0	1	0	0	0	0	1	0	1	0	Rm			Rn		
CMN (register)	0	1	0	0	0	0	1	0	1	1	Rm			Rn		
ORR (register)	0	1	0	0	0	0	1	1	0	0	Rm			Rdn		
MUL	0	1	0	0	0	0	1	1	0	1	Rn			Rdm		
BIC (register)	0	1	0	0	0	0	1	1	1	0	Rm			Rdn		
MVN (register)	0	1	0	0	0	0	1	1	1	1	Rm			Rd		

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD (register2)	0	1	0	0	0	1	0	0	DN		Rm			Rdn		
CMP (register2)	0	1	0	0	0	1	0	1	N		Rm			Rn		
MOV (register1)	0	1	0	0	0	1	1	0	D		Rm			Rd		
BX	0	1	0	0	0	1	1	1	0		Rm			0	0	0
BLX	0	1	0	0	0	1	1	1	1		Rm			0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LDR (PC-relative)	0	1	0	0	1	Rt			imm8							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STR (register)	0	1	0	1	0	0	0	Rm			Rn			Rt		
STRH (register)	0	1	0	1	0	0	1	Rm			Rn			Rt		
STRB (register)	0	1	0	1	0	1	0	Rm			Rn			Rt		
LDRSB (register)	0	1	0	1	0	1	1	Rm			Rn			Rt		
LDR (register)	0	1	0	1	1	0	0	Rm			Rn			Rt		

LDRH (register)	0	1	0	1	1	0	1	Rm			Rn			Rt		
LDRB (register)	0	1	0	1	1	1	0	Rm			Rn			Rt		
LDRSH (register)	0	1	0	1	1	1	1	Rm			Rn			Rt		
STR (5-bit immediate)	0	1	1	0	0	imm5					Rn			Rt		
LDR (5-bit immediate)	0	1	1	0	1	imm5					Rn			Rt		
STRB (immediate)	0	1	1	1	0	imm5					Rn			Rt		
LDRB (immediate)	0	1	1	1	1	imm5					Rn			Rt		
STRH (immediate)	1	0	0	0	0	imm5					Rn			Rt		
LDRH (immediate)	1	0	0	0	1	imm5					Rn			Rt		
STR (8-bit immediate)	1	0	0	1	0	Rt			imm8							
LDR (8-bit immediate)	1	0	0	1	1	Rt			imm8							

ADR	1	0	1	0	0	Rd			imm8							
ADD (SP immediate1)	1	0	1	0	1	Rd			imm8							

ADD (SP immediate2)	1	0	1	1	0	0	0	0	0	imm7						
SUB (SP immediate)	1	0	1	1	0	0	0	0	1	imm7						
SXTH	1	0	1	1	0	0	1	0	0	0	Rm			Rd		
SXTB	1	0	1	1	0	0	1	0	0	1	Rm			Rd		
UXTH	1	0	1	1	0	0	1	0	1	0	Rm			Rd		
UXTB	1	0	1	1	0	0	1	0	1	1	Rm			Rd		
PUSH	1	0	1	1	0	1	0	M	Register_list							
CPS	1	0	1	1	0	1	1	0	0	1	1	im	0	0	1	0
REV	1	0	1	1	1	0	1	0	0	0	Rm			Rd		
REV16	1	0	1	1	1	0	1	0	0	1	Rm			Rd		
REVSH	1	0	1	1	1	0	1	0	1	1	Rm			Rd		
POP	1	0	1	1	1	1	0	P	Register_list							
BKPT	1	0	1	1	1	1	1	0	imm8							
NOP	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
YIELD	1	0	1	1	1	1	1	1	0	0	0	1	0	0	0	0
WFE	1	0	1	1	1	1	1	1	0	0	1	0	0	0	0	0
WFI	1	0	1	1	1	1	1	1	0	0	1	1	0	0	0	0
SEV	1	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0

STM	1	1	0	0	0	Rn	Register_list
LDM	1	1	0	0	1	Rn	Register_list

B (conditional)	1	1	0	1	cond				imm8
SVC	1	1	0	1	1	1	1	1	imm8

B (unconditional)	1	1	1	0	0	imm11

MSR

1	1	1	1	0	0	1	1	1	0	0	0	Rn
1	0	0	0	1	0	0	0	SYSm				

MRS

1	1	1	1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	0	Rd				SYSm							

BL

1	1	1	1	0	S	imm10									
1	1	J1	1	J2	imm11										

DSB

1	1	1	1	0	0	1	1	1	0	1	1	1	1	1	1
1	0	0	0	1	1	1	1	0	1	0	0	option			

DMB

1	1	1	1	0	0	1	1	1	0	1	1	1	1	1	1
1	0	0	0	1	1	1	1	0	1	0	1	option			

ISB

1	1	1	1	0	0	1	1	1	0	1	1	1	1	1	1
1	0	0	0	1	1	1	1	0	1	1	0	option			