EE511 Computer Architecture

Instructions: Verilog Simulation

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- **Icarus Verilog Overview**

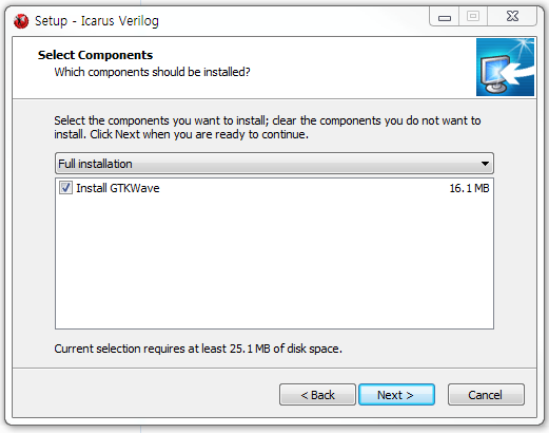
  Icarus Verilog is the most famous free Verilog compilation and simulation software. As the installation package includes a waveform display tool called **gtkwave**, you can compile your Verilog source file as well as check the waveform of the signals that go into and come out from the designed module.

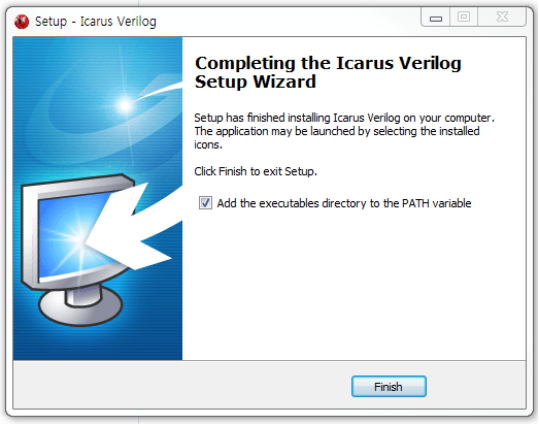
- **Icarus Verilog Installation**

  Windows environment(recommend)

  → Download iverilog-0.9.7_setup.exe (latest stable release) [10.5MB] from http://bleyer.org/icarus/.

  Check the license agreement and click next. Make sure that you choose "Full installation" which enables the installation of gtkwave. Updating PATH variable automatically as shown below will shorten the following processes (sometimes this does not work and the way of manual update is described below).





  Other environment

  → Follow Installation From Premade Packages section https://iverilog.fandom.com/wiki/Installation_Guide.

- **Design Flow**

① **Verilog description**

You can use any text editor such as Notepad and **gVim** to write a Verilog file. Just make sure that the filename extension is ".v".

② **Verilog compilation**

Execute the Windows prompt by using "**cmd**" command.

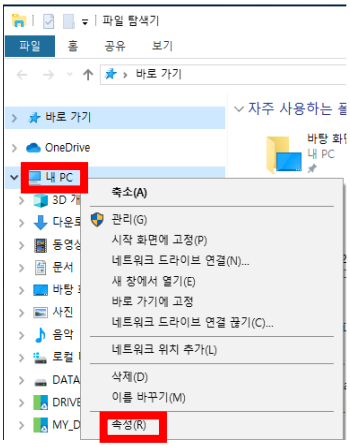
Some commands in cmd:

- cd aabb = go into the directory 'aabb'.
- cd .. = go back to the parental directory.
- dir = show files and folders in the current directory.

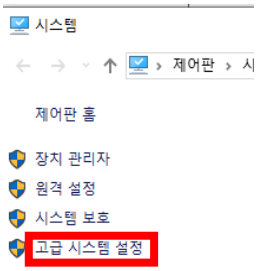
If you updated the PATH variable during the previous installation process, "iverilog" command works fine everywhere. A warning and usage hints shown below result from executing "iverilog".

```
Microsoft Windows [Version 10.0.17763.678]
(c) 2018 Microsoft Corporation. All rights reserved.

C:₩Users₩JIN>iverilog
iverilog: no source files.

Usage: iverilog [-ESvV] [-B base] [-c cmdfile|-f cmdfile]
                [-g1995|-g2001|-g2005] [-g<feature>]
                [-D macro[=defn]] [-I includedir] [-M depfile] [-m module]
                [-N file] [-o filename] [-p flag=value]
                [-s topmodule] [-t target] [-T min|typ|max]
                [-W class] [-y dir] [-Y suf] source_file(s)

See the man page for details.
```

Otherwise, you can manually update the PATH variable as shown below.

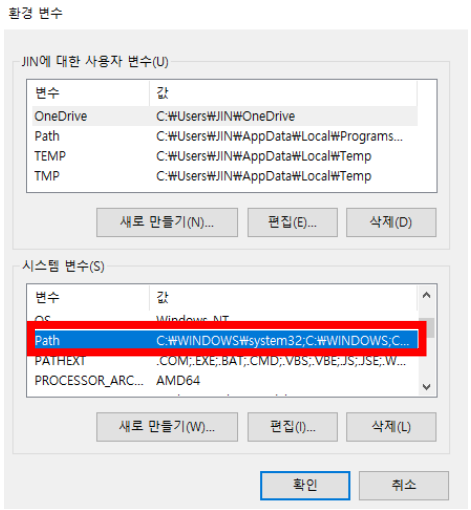


Right click my PC and go to properties.

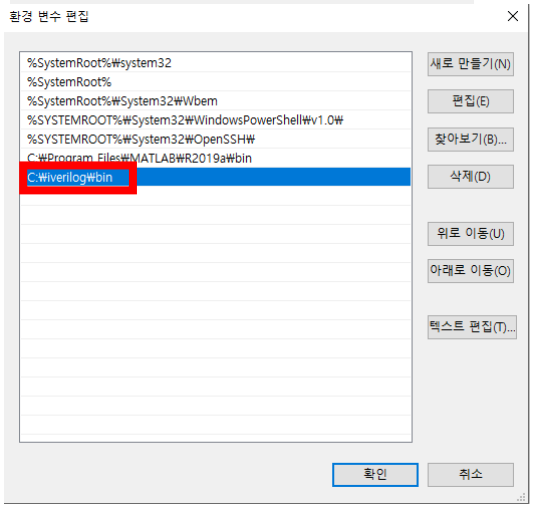


Click advanced system configuration

Click Environment Variables.



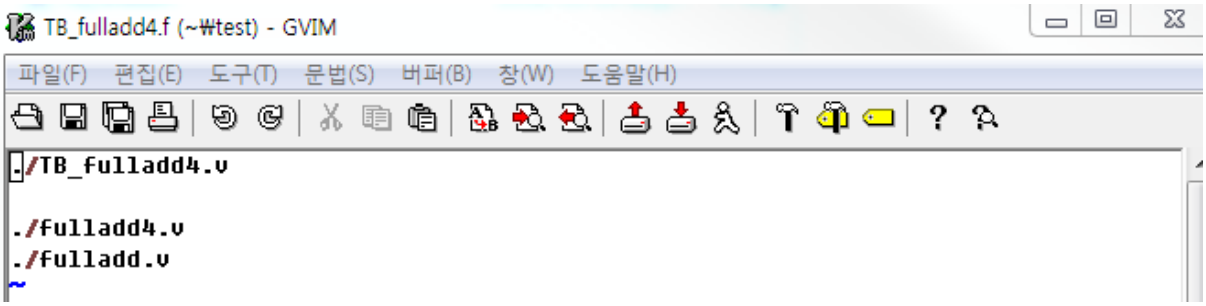
Double click Path



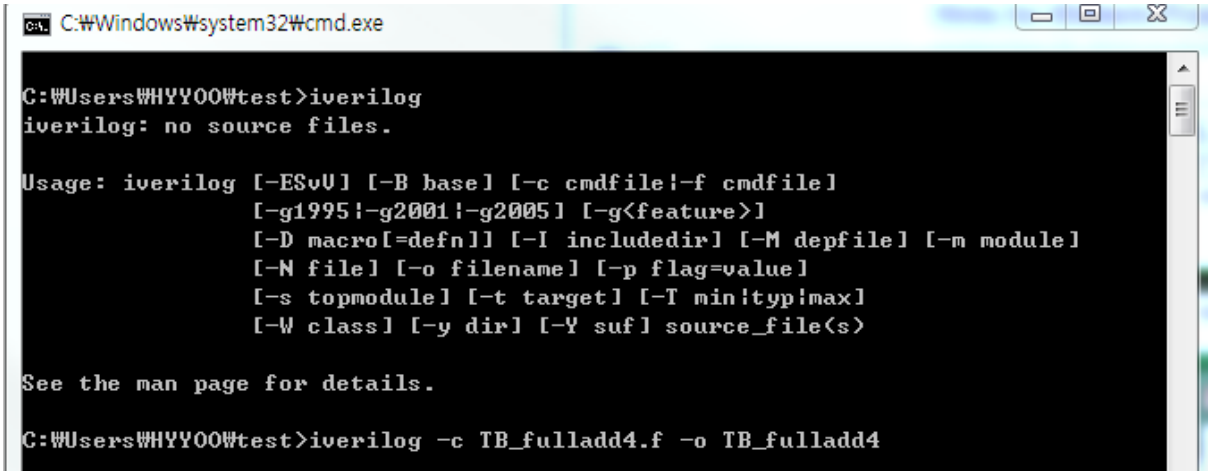
Append the path where iverilog binary files (₩bin) are installed as shown below. DO NOT ERASE the existing paths! Just append.

③ Go to the directory where the Verilog files reside. To simplify the compile command, a list of the Verilog files can be written in one ".f" file. Note that –c is a compile option for the ".f" file while -o specifies the output file name.

(example) TB_fulladd4.f file contains a list of all Verilog files.



Execute "iverilog –c TB_fulladd4.f –o TB_fulladd4" to compile the Verilog files listed in TB_fulladd4.f. The name of the output file is TB_fulladd4.



④ Verilog simulation

Add "$dumpfile("dump file name");" and "$dumpvars;" in a test-bench module (ex. TB_fulladd4.v) to record all variations of internal signals during the simulation. (It is already added in testbenches)

```
initial
        $dumpfile("myfile.dmp");
initial
        $dumpvars;
```

Execute "**vvp**" to simulate the previous compilation result (ex. TB_fulladd4). The simulation results are dumped into a dump file (ex. myfile.dmp) which will be opened by **gtkwave**.

```
C:\Users\HYYOO\test>vvp TB_fulladd4
VCD info: dumpfile myfile.dmp opened for output.

C:\Users\HYYOO\test>dir
 C 드라이브의 볼륨: BOOTCAMP
 볼륨 일련 번호: BA32-F8A3

 C:\Users\HYYOO\test 디렉터리

2012-11-19  오전 11:20    <DIR>          .
2012-11-19  오전 11:20    <DIR>          ..
2012-11-19  오전 11:18               208 fulladd.v
2012-11-19  오전 11:18               310 fulladd4.v
2012-11-19  오전 11:20             1,701 myfile.dmp
2012-11-19  오전 11:19             5,780 TB_fulladd4
2012-11-19  오전 11:14                42 TB_fulladd4.f
2012-11-19  오전 11:17               352 TB_fulladd4.v
               6개 파일               8,393 바이트
               2개 디렉터리  193,756,651,520 바이트 남음
```

⑤ Verification

Execute "**gtkwave**" to run the waveform viewer.

```
C:\Users\HYYOO\test>dir
 C 드라이브의 볼륨: BOOTCAMP
 볼륨 일련 번호: BA32-F8A3

 C:\Users\HYYOO\test 디렉터리

2012-11-19  오전 11:20    <DIR>          .
2012-11-19  오전 11:20    <DIR>          ..
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2012-11-19  오전 11:17               352 TB_fulladd4.v
               6개 파일               8,393 바이트
               2개 디렉터리  193,756,651,520 바이트 남음

C:\Users\HYYOO\test>gtkwave
```
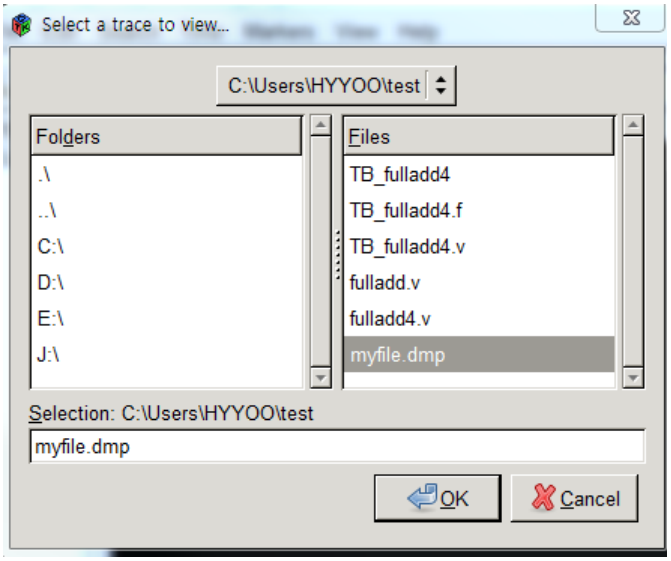
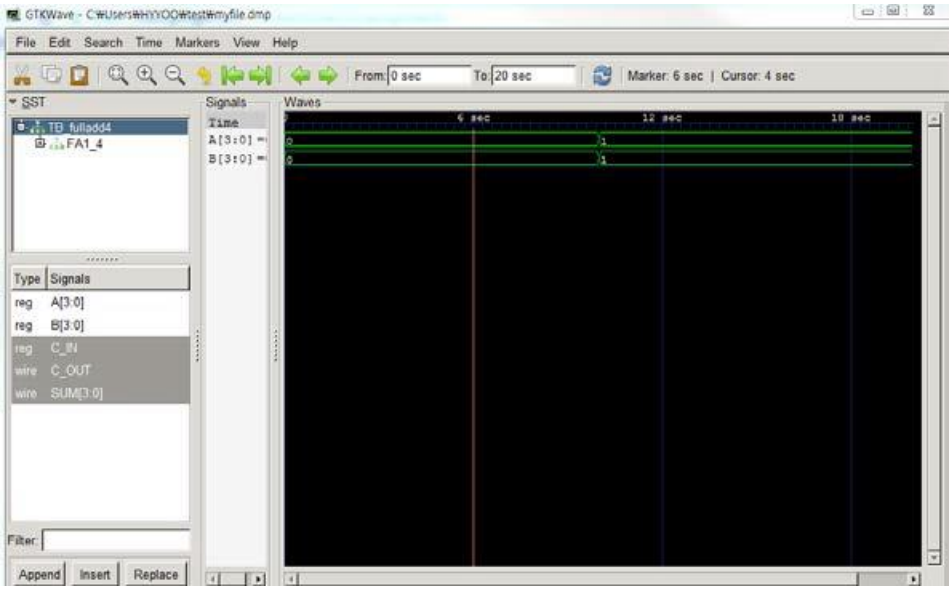

Click "File – Open New Tab" to open the dump file.



Drag the signals to the black background.



Check the operations and modify the Verilog design iteratively. Good luck!