**Experiment 5 – Logic Operations**

**CSCI 220 – Section 1**

**Lab Date: 2/24/2016**

Report By:

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On my honor I have neither received nor given aid on this report.

Signed: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Part I  
Objective of the Experiment**

In this experiment we created a programmable circuit which can apply four different operations to two of the four inputs.

**Part II  
Equipment/components necessary for the Experiment**

1 7404 NOT chip

1 7432 2-input OR chip

1 7408 2-input AND chip

1 7410 3-input NAND chip

1 7420 4-input NAND chip

**Part III  
Description of the followed procedure**

**(Truth table, Circuit design, etc.)**

In this lab we were told to construct a circuit with 4 inputs and one output. Two of the inputs control the operation performed on the second two inputs. The inputs in the lab manual C1, C2, X1, and X3 will be called A, B, C, and D respectively from now on. The truth table was derived by sectioning off the truth table with every four rows being one operation on the 4 combinations of C and D.

Truth Table:



With the truth table I constructed a Kmap. I have attached the kmap and the simplifcation of the equation to this lab report. The sum of products equation aquired by the kmap:

F(A,B,C,D) = A'C'D + A'CD' + B'CD + ACD + ABC'D'

This circuit would require 19 gates using only 2-input ORs and ANDs. Using NAND gates is the best way to limit the number of necessary gates. Because we have 3-input and 4-input NAND gates we can double invert 4 of the sums:

F(A,B,C,D) = ((A'C'D)' (A'CD')' (B'CD)' (ABC'D')')' + ACD

Now we can build this circuit using 12 gates:

4 NOTs

1 2-input OR

2 2-input ANDs

3 3-input NANDs

2 4-input NANDs

Gate diagram for function F(A,B,C,D) = ((A'C'D)' (A'CD')' (B'CD)' (ABC'D')')' + ACD:



**Part IV  
Conclusion**

Using NAND gates allowed us to eliminate several gates from the circuit. The circuit we built worked fine and when tested against the truth table all cases were correct.