Synchronous DRAM Controller
- For the OPB Bus

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CORE Facts

Provided with Core	
Documentation	User guide, design guide
Design File Formats	EDIF netlist; VHDL Source RTL (available at extra cost)
Constraints Files	SDRAM.ucf
Verification	VHDL test bench
Instantiation templates	VHDL
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
Modelsim v6.0	
Support	
Support provided by [RealFast AB]	

Features

- Available under terms of the SignOnce IP License.
- Low gate count, high speed, high performance solution.
- SDRAM Parametrizable refresh capability.
- Supports Virtex ™, Virtex ™ –E , Spartan ™ and Spartan ™ -II FPGA:s.
- Supports burst size of 1 to 8.
- Works with typical 64M-, 128M- and 256Mbit SDRAMs in x4, x8 or x16 organizations.
- Supports switching between single- and burst mode accesses during normal operation.

Applications

- Embedded systems in industrial applications.
- Networking equipment.
- Communication equipment.
- Video systems.
- PC peripherals.
- Digital signal processing.

General Description

The SDRAM Controller is the part of a system that controls the memory. It generates the necessary signals to control the reading and writing of information from and to the memory. DRAM (Dynamic Random Access Memory) constitutes the basic building block for most memory systems. The SDRAM controller automatically handles SDRAM timing such as row and column latency, precharge timing, and row access length.

Functional Description

Due to its generic implementation the design can easily be customized for specific applications, but the default configuration of the SDRAM controller is as follows:

- OPB bus interface
- 4 banks, 16-bit wide SDRAM data array
- 24-bit address width (16M)
- 4 times refresh cycle split-up
- CAS latency of 3 clock cycles
- Burst mode = 8
- Autoprecharge used for all accesses

Family	Example Device	Fmax (MHz)	Slices	IOB	GCLK	Design Tools
Spartan-IIE	XC2S50e-6	106	137	119	1	ISE 6.2i
Virtex-II	XC2V250-6	170	138	119	1	ISE 6.2i
Virtex-II Pro	XC2VP2-6	200	136	119	1	ISE 6.2i

Table 1: Example Implementation Statistics

All functional blocks are described in Figure 1.

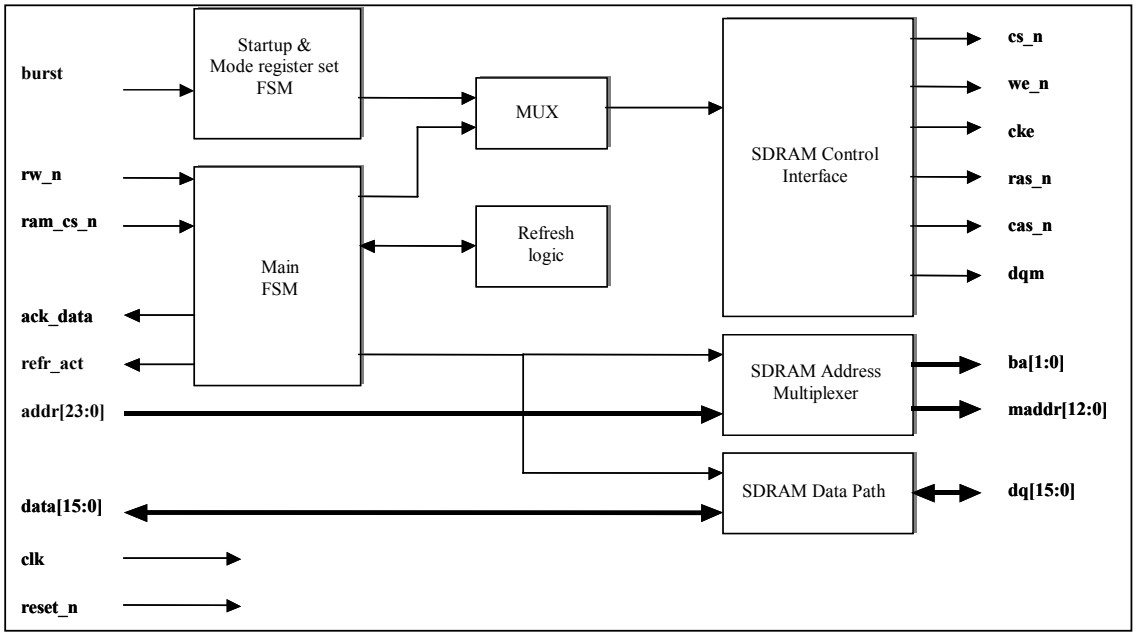

Figure 1: SDRAM Controller Block Diagram

Main FSM

The Main Control state machine arbitrates between processor read/write demands and refresh cycles, as well as generating the appropriate cycling of the RAS_N and CAS_N signals. Based on the request signals RAM_CS_N, the state machine sends control signals to the SDRAM Address Mulitiplexer, the SDRAM Control Interface and the SDRAM Data Path to access SDRAM. ACK_DATA is asserted for each read data that is returned from the SDRAM, or for each data that is written to the SDRAM.

Startup & Mode register set FSM

SDRAMs must be powered up and initialized in a pre-defined manner to prevent undefined operations. A FSM is implemented to control the start-up sequence. The mode register is set in this FSM and with the input signal BURST the SDRAM controller can switch between single- and burst mode accesses without performing a new initialization.

SDRAM Data Path

The SDRAM Data Path unit handles the direction of data flow and provides the appropriate drive and timing to and from the SDRAM data pins.

Refresh logic

The storage cells of the SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells.

The internal SDRAM counter is incremented automatically on every auto refresh cycle (= 1 row). Therefore the refresh can be split up in parts, which means that the auto refresh cycle is activated several times within 64ms. Two timers control the refresh. Timer one keeps track of the active time for one part of the refresh sequence. Timer two controls the logic for the refresh interval. For the default configuration ¼ of the memory is refreshed every 16ms. This split-up logic can of course be customized for a specific application.

SDRAM Control Interface

The SDRAM control signals CS_N, RAS_N, CAS_N, DQM, WE_N and CKE are synchronously generated from the state machine outputs.

SDRAM Adress Multiplexer

The SDRAM Address Multiplexer splits the full address bus to a row- and a column address, controlled by the Main State Machine. The Main State Machine also drives the correct 2-bit bank address to the SDRAM.

Core Modifications

The SDRAM controller is designed and verified in a XC2V1000 device. Cores for other packages are also supported.

Contact RealFast to customize the core for your application.

Verification Methods

Functional simulation has been done using Model Technology Modelsim™ SE 5.7e. Static timing analysis has been done for all paths using the timing analyzer in XilinxISE 6.2i.

Recommended Design Experience

Users should be familiar with SDRAM, VHDL and Xilinx design flows.

Core I/O Signals

The core signal I/O:s have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all I/O signals are provided in Table 2:

Signal	Dir	Description
System Interface Signals		
ADDR[23:0]	I	Address input
CLK	I	System clock
DATA[15:0]	I/O	Data bus
RAM_CS_N	I	Chip Select
RESET_N	I	System reset
RW_N	I	Direction of data transfer
BURST	I	Burst mode selection
ACK_DATA	O	Valid data is on the bus
REFR_ACT	O	Auto refresh active
SDRAM Interface Signals		
BA[1:0]	O	SDRAM bank address
RAS_N	O	SDRAM row address strobe
CAS_N	O	SDRAM column address strobe
CKE	O	SDRAM clock enable
CS_N	O	SDRAM chip select
WE_N	O	SDRAM write enable
MADDR[12:0]	O	SDRAM address multiplexed
DQ[15:0]	I/O	SDRAM data
DQM	O	SDRAM Data mask bit

Table 2: SDRAM Controller I/O Signals

Design Services

RealFast also offers core integration, core customization and other design services.

Ordering Information

This product is available from RealFast, under terms of the SignOnce IP License. See www.realfast.se for pricing or contact RealFast for additional information about this product.

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Related Information

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