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PreLab06: Keypad Input Using 74C922 16-Key
Encoder

ESE280-L03

Bench #3
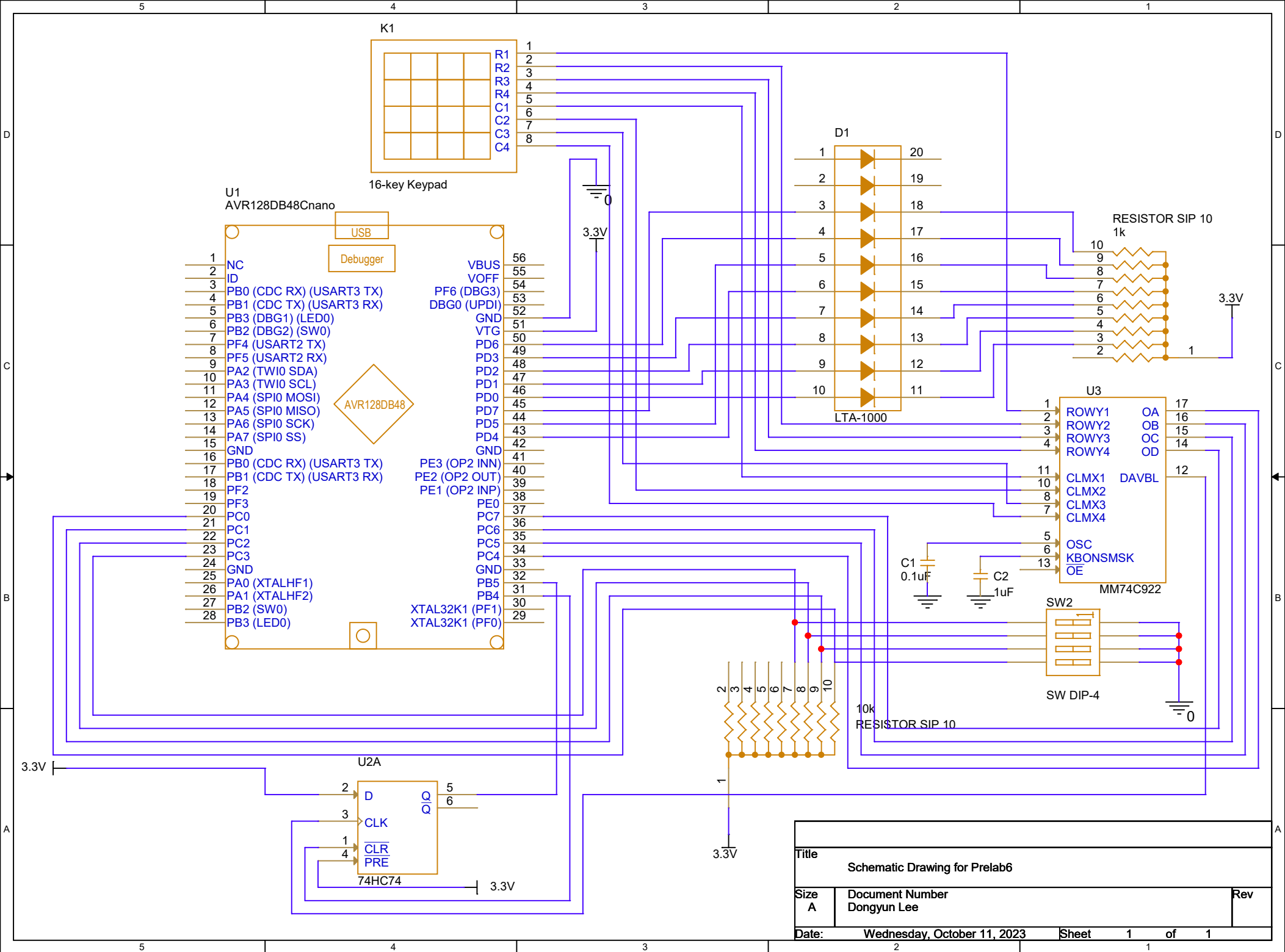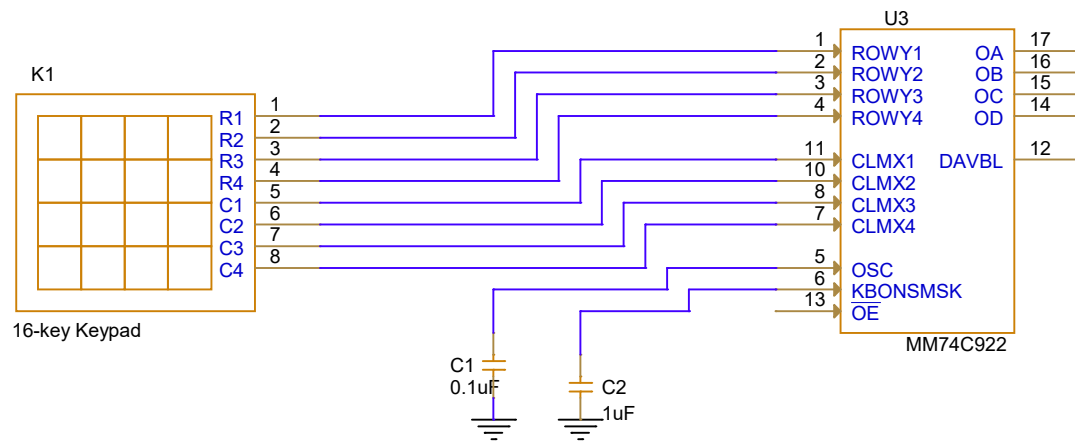
Schematic Drawing for Prelab6

Title	Schematic Drawing for Prelab6
Size A	Document Number: Dongyun Lee
Date:	Wednesday, October 11, 2023

Sheet 1 of 1

K1 — 16-key Keypad

U1 — AVR128DB48Cnano

D1 — LTA-1000

RESISTOR SIP 10 — 1k

U3 — MM74C922

SW2 — SW DIP-4

10k — RESISTOR SIP 10

U2A — 74HC74

K1

16-key Keypad

R1	1
R2	2
R3	3
R4	4
C1	5
C2	6
C3	7
C4	8

U3

1	ROWY1	OA	17
2	ROWY2	OB	16
3	ROWY3	OC	15
4	ROWY4	OD	14
11	CLMX1	DAVBL	12
10	CLMX2		
8	CLMX3		
7	CLMX4		
5	OSC		
6	KBONSMSK		
13	OE		

MM74C922

C1
0.1uF

C2
1uF

```asm
;
; ************************************
;   Keypad Test
; ************************************
; Created: 10/11/2023 2:18:39 PM
; Author : CAD
;


start:
    ldi r16, 0xFF    //make into output
    out VPORTD_DIR, r16
    ldi r16, 0x00    //make into input
    out VPORTC_DIR, r16

    sbi VPORTB_DIR, 4   ; makes PB4(clear) to output
    cbi VPORTB_DIR, 5   // input directly from pushbutton



wait_for_1:
    sbis VPORTB_IN, 5    ;wait for PB5 being 1
rjmp wait_for_1       ;skip this line if PE0 is 1


output:

in r18, VPORTC_IN    // gets the input from DIP switch and keypad

mov r18, 19          // copy it to another register

com r19              // complement r19 for display
out VPORTD_OUT, r19 // display


delay_break:              ;delay lable for break delay
    ldi r16, 80
    outer_loop_break:
        ldi r17, 133
        inner_loop_break:
            dec r17
    brne inner_loop_break
        dec r16
brne outer_loop_break

clear_flipflop:      // clear the flip flop for next input
    cbi VPORTB_OUT, 4
    sbi VPORTB_OUT, 4

clear_check:         // check if the clear has worked properly
    sbic VPORTB_IN, 5
    rjmp delay_break
```

```
rjmp wait_for_1     // go back to the start
```

```asm
;
; Keypad mapping test
;
; Created: 10/11/2023 3:17:11 PM
; Author : CAD
;


start:
    ldi r16, 0xFF    //make into output
    out VPORTD_DIR, r16
    ldi r16, 0x00    //make into input
    out VPORTC_DIR, r16

    sbi VPORTB_DIR, 4   ; makes PB4(clear) to output
    cbi VPORTB_DIR, 5   // input directly from pushbutton



wait_for_1:
    sbis VPORTB_IN, 5    ;wait for PB5 being 1
rjmp wait_for_1      ;skip this line if PE0 is 1


bcd_7seg:
    andi r18, $0F
    cpi r18, 10
    brlo lookup
    clc
    ldi r18, 0
    ret
lookup:
    ldi ZH, high (segtable * 2)
    ldi ZL, low (segtable * 2)
    ldi r16, $00
    add ZL, r18
    adc ZH, r16
    lpm r18, Z
    sec
    ret

segtable: .db $0001, $0010, $0011, $1111, $0100, $0101, $0110, $1110, $0111, $1000,  ⏎
    $1001, $1101, $1010, $0000, $1011, $1011


output:

in r18, VPORTC_IN   // gets the input from DIP switch and keypad

mov r18, 19         // copy it to another register

com r19             // complement r19 for display
```

```asm
out VPORTD_OUT, r19 // display


delay_break:                ;delay lable for break delay
    ldi r16, 80
    outer_loop_break:
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        inner_loop_break:
            dec r17
    brne inner_loop_break
        dec r16
brne outer_loop_break

clear_flipflop:     // clear the flip flop for next input
    cbi VPORTB_OUT, 4
    sbi VPORTB_OUT, 4

clear_check:        // check if the clear has worked properly
    sbic VPORTB_IN, 5
    rjmp delay_break

rjmp wait_for_1     // go back to the start
```