```
; conditional_input.asm
; Created: 10/2/2023 6:53:51 PM
; Author : CAD
; Replace with your application code
start:
                  //make into output
   ldi r16, 0xFF
   out VPORTD_DIR, r16
   ldi r16, 0x00
                  //make into input
   out VPORTC_DIR, r16
   cbi VPORTE_DIR, 0
                     ; makes PEO(pushbutton) to input
                     ; makes PE1(clear) to output
    sbi VPORTE_DIR, 1
   cbi VPORTE DIR, 2 // input directly from pushbutton
wait_for_0:
   sbic VPORTE_IN, 0
                      ;wait for PE0 being 0
                      ;skips this line if PEO is 0
    rjmp wait_for_0
wait_for_1:
   sbis VPORTE IN, 0
                      ;wait for PE0 being 1
    rjmp wait_for_1
                      ;skip this line if PE0 is 1
   rjmp delay_make
                      ;jump to delay when PE0 is 1
delay make:
                      ;delay label for make delay
outer_loop_make:
   ldi r17, 133
inner_loop_make:
   dec r17
   brne inner_loop_make
   dec r16
   brne outer loop make
   rjmp still_1
                      ; jump to still_1
wait_for_0_delay_after: ;comes here after output
    released
   rcall clear_flip_flop
    sbic VPORTE_IN, 0
    rjmp wait_for_0_delay_after ;skips this line if PEO is 0
    rjmp delay_break
                      ;delay lable for break delay
delay break:
outer_loop_break:
   ldi r17, 133
inner_loop_break:
   dec r17
   brne inner_loop_break
```

```
dec r16
    brne outer_loop_break
    rjmp still_0
still 1:
    sbis VPORTE_IN, 0 ; check if PE0 is still 1
    rjmp wait_for_0 ; if PEO is 0 then go jump to wait_for_0
    rjmp output
                        ; outputs the value
still_0:
    sbic VPORTE_IN, 0 ;check if PE0 is still 0
    rjmp wait_for_0_delay_after
    rjmp wait_for_0
                      ;go back to start
output:
    //code for output the values from PC ports to PD ports
    inc r16
    com r16
    out VPORTD_OUT, r16
    com r16
    rjmp wait_for_0_delay_after ; jump to wait for 0 but that has delay after
clear_flip_flop:
    cbi VPORTE_DIR, 1
    sbi VPORTE DIR, 1
    rjmp wait_for_0
display:
    in r16, VPORTC_DIR
    com r16
    out r16, VPORTD_DIR
    rjmp clear_flip_flop
check_pushbutton_released:
    rcall delay_break_pushbutton
    sbic VPORTE_IN, 2 //check if PE) which is directly connected to pushbutton is
      still 0
    rjmp check_pushbutton_released
delay break pushbutton:
                               ;delay lable for break delay for pushbutton directly
outer_loop_break:
    ldi r17, 133
inner_loop_break:
    dec r17
    brne inner_loop_break
    dec r16
    brne outer_loop_break
```