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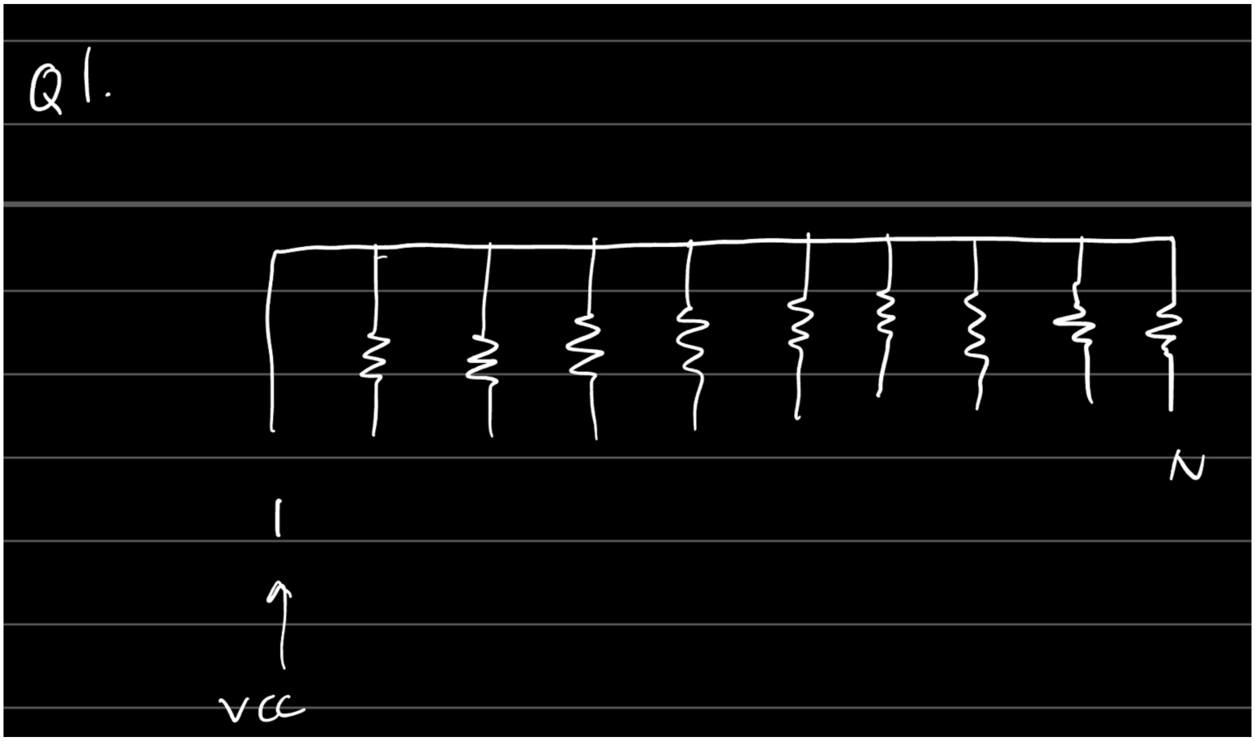
Lab04: DIP Switch Inputs and Bargraph LED Outputs – Basic I/O

ESE280-L03

Bench #3

1. Draw a circuit diagram that shows how the resistors in the 10-pin SIP resistor network are internally interconnected.

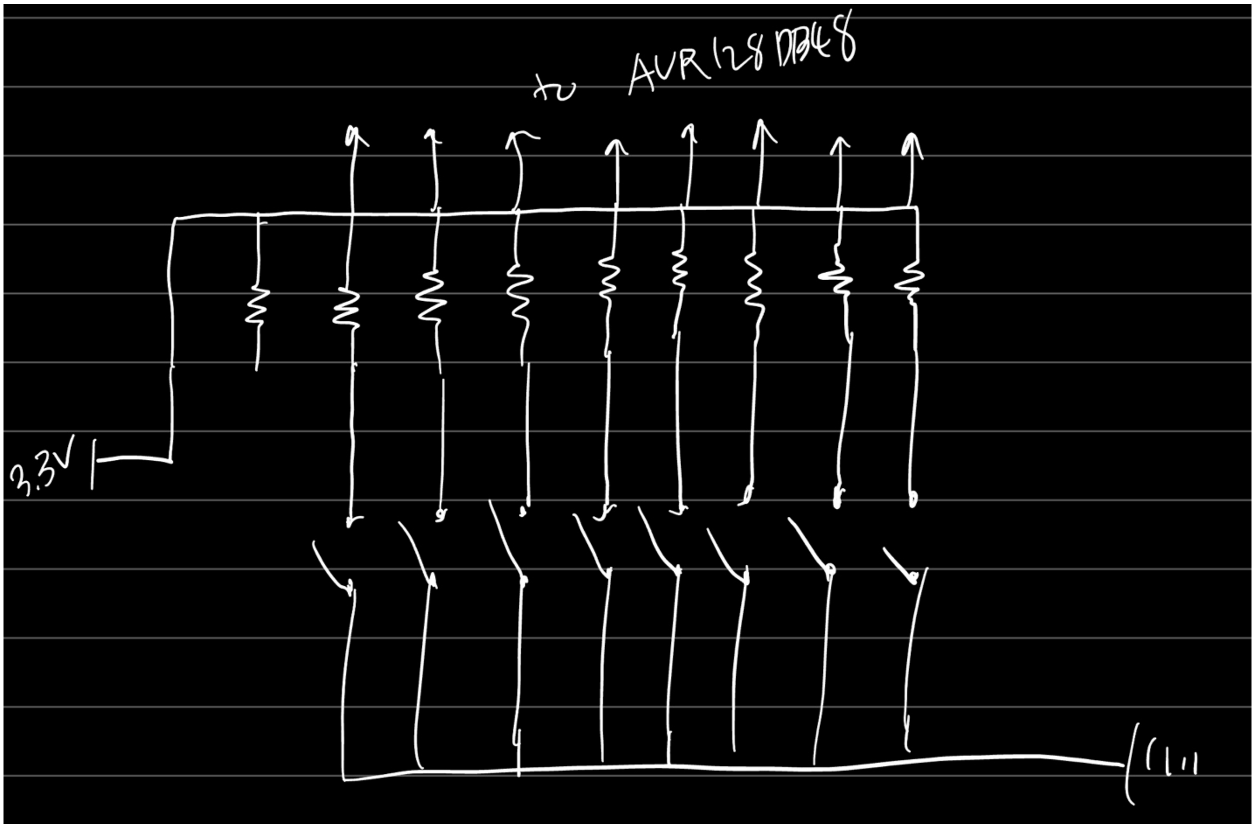


2. Determine the machine language code, in hexadecimal, for the ldi r16, 0xFF instruction from the Task1 program sws_positions. Use the 16-bit Opcode template from the AVR Instruction Set Manual to determine the hexadecimal value. List the values of KKKK in the second and fourth fields of the template. List the value of dddd in the third field. Since there are 32 general purpose registers (GPRs) in the AVR128DB48, explain how the destination GPR can be specified using only four bits (dddd) and not five.

3. Determine the machine language code, in hexadecimal, for the out VPORTD_DIR, r16 instruction from the Task 1 program. Use the 16-bit Opcode template from the AVR Instruction Set Manual to create the hexadecimal value. List the values of the AA and r in the second field, rrrr in the third field, and AAAA in the fourth field of the template. Why are 5 bits used to repre-

sent the address of the GPR used in this instruction?

4. Draw the circuit you created to interface the DIP switches to the AVR128DB48 using the 10-pin SIP network.



5. What is the purpose of the com r18 instruction in the logic_ops program for Task 2? The question is not what does a com r18 instruction do, but why is it necessary in that program.

Since com means one’s complement, this means that r18 bit will output the opposite bit from the input. Therefore, com r18 works as NOT gate in this code.

6. In the following sequence of instructions from the logic_ops program what it the purpose of the two andi instructions in the program? The question is not what does an andi instruction do, but why are they necessary in that program.

Andi means AND Immediate in assembly language, so in this case for example, andi r16, 0x03 means that excluding the two least significant bits, it will immediately change all the bits of r16 into 0. And this process is necessary in order to take another logic gate in the next loop.

7. In the sequence of instructions in Problem 6 from the logic_ops program, why is the value of B left justified?

The reason why value of B left justified is to be correctly aligned with r17 bits.

8. In the following sequence of instructions from the logic_ops program

the cpi instruction subtracts K from rd (rd - K). So, how is it possible to sequentially compare different values of K with the contents of r16 to determine the value in r16 after the andi instruction?

It uses AND operation to compare the value in r16 and 0x03 keeping the two least significant bits.

9. In the sequence of instructions in Problem 8 from the logic_ops program, why isn't there a breq instruction for the not_fcn?

This is because not_fcn is not based on a direct comparison between r16 and the constant. It only compares with the previous branch.

10. In the sws_level program for Task 3 there at two loops. What are the label names for these loops?

Main_loop, next_bit, dec_bitcounter are the label names.