

## xs3\_to\_BCD\_CPOS.vhd

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity converter_xs3_bcd_cpos is
5      port(
6          p, q, r, s : in std_logic;
7          d, c, b, a : out std_logic
8      );
9  end converter_xs3_bcd_cpos;
10
11  -- CPOS
12
13  architecture CPOS of converter_xs3_bcd_cpos is
14  begin
15      -- CPOS
16
17      -- Output d
18      d <= (p or q or not r or not s) and (p or not q or r or s) and (p or not q or r
or not s) and
19          (p or not q or not r or s) and (p or not q or not r or not s) and (not p
or q or r or s) and
20          (not p or q or r or not s) and (not p or q or not r or s);
21
22      -- Output c
23      c <= (p or q or not r or not s) and (p or not q or r or s) and (p or not q or r
or not s) and
24          (p or not q or not r or s) and (not p or q or not r or not s) and (not p
or q or not r or not s) and
25          (not p or not q or r or s);
26
27      -- Output b
28      b <= (p or q or not r or not s) and (p or not q or r or s) and (p or not q or
not r or not s) and
29          (not p or q or r or s) and (not p or q or not r or not s) and (not p or
not q or r or s);
30
31      -- Output a
32      a <= (p or q or not r or not s) and (p or not q or r or not s) and (p or not q
or not r or not s) and
33          (not p or q or r or not s) and (not p or q or not r or not s);
34
35  end cpos;
36
```