File: X:\ESE382-Lab\Lab7\lab7\two_level_gate_circuit\src\two_level_gate_tb.vhd

```
1   ----------------------------------------------------------------------------
    -------
2   --
3   -- Title       : two_level_gate_tb
4   -- Design      : two_level_gate_circuit
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    -------
9   --
10  -- File        :
    X:\ESE382-Lab\Lab7\lab7\two_level_gate_circuit\src\two_level_gate_tb.vhd
11  -- Generated   : Thu Mar 14 15:52:39 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    -------
16  --
17  -- Description : testbench for two level gates, using record.
18  --
19  ----------------------------------------------------------------------------
    -------
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26
27
28  entity two_level_gate_tb is
29  end two_level_gate_tb;
30
31
32  architecture testbench of two_level_gate_tb is
33      -- stimulus signals
34      signal a, b, c : std_logic;
35      -- observed signals
36      signal s1, f : std_logic;
37
38      type test_vector is record
39          a, b, c, s1, f : std_logic;
40      end record;
41
42      type test_vector_array is array (natural range <>) of test_vector;
43
44      constant test_vectors : test_vector_array := (
45      --    a    b    c    s1   f
46          ('0', '0', '0', '0', '0'),
47          ('0', '0', '1', '0', '1'),
48          ('0', '1', '0', '0', '0'),
49          ('0', '1', '1', '0', '1'),
50          ('1', '0', '0', '0', '0'),
51          ('1', '0', '1', '0', '1'),
52          ('1', '1', '0', '1', '1'),
53          ('1', '1', '1', '1', '1')
54          );
55
56
```

```
57
58  begin
59      UUT : entity two_level_gate
60          port map (
61              a => a, b => b, c => c, f => f
62          );
63
64      verify : process
65      begin
66          for i in test_vectors'range loop
67              a <= test_vectors(i).a;
68              b <= test_vectors(i).b;
69              c <= test_vectors(i).c;
70              s1 <= test_vectors(i).s1;
71              f <= test_vectors(i).f;
72              wait for 20ns;
73              assert (a = test_vectors(i).a) and (b = test_vectors(i).b)
    and (c = test_vectors(i).c) and (s1 = test_vectors(i).s1) and (f =
    test_vectors(i).f)
74              report "test_vector " & integer'image(i) & "failed" & " for
    input a = " & std_logic'image(a) & " b = " & std_logic'image(b) & " c =
    " & std_logic'image(c)
75              severity error;
76          end loop;
77
78          std.env.finish;
79          end process;
80
81
82
83
84  end testbench;
85
```