

1. What are the initial states of a latch and flip-flop at the very beginning of a simulation? What would be the corresponding initial states of a latch or flip-flop in an actual PLD?

The initial states for D-latch '0' initialized state and for d-flip-flop the initial state is 'U'. In an actual PLD, there is no value such as 'U', therefore the initial state is '0'.

2. Briefly describe the code for the clock signal in an automatically generated testbench.

The code for the clock signal could be generated by adjusting period, duty cycle, and offset. Therefore, I can generate the clock cycle to see the outputs from my code easily.

3. Briefly describe how the stimulus for the other (non clock) inputs is generated in automatically generated testbenches.

One of non clock stimulus is using hot key. Whenever I press the hot key on the keyboard, it changes the value of input signal. This method is also useful in a way that I can observe the intended output visually on waveform.

4. Why is it important in structural designs to check the Code2Graphics diagram after compilation or the HDL Analyst hierarchical view after synthesis?

It is important to check the structural designs and compare between Code2Graphics and HDL Analyst hierarchical view because both can help to verify if the code has been successfully synthesized.