Questions for Lab02a

1. What is the purpose of a post synthesis simulation?

   The purpose if a post synthesis simulation is the verify the synthesized design to make sure that it matches with the original VHDL mode, considering real-world constraints.

2. What model for the half-adder is used as input in post synthesis simulation and where does it come from.

We used the VHDL netlist model of the design entity half_adder. The VHDL netlist model is automatically produced by the synthesizer.

3. Is the ispGAL22V10C-10 a SPLD, CPLD, or FPGA? Explain the reason for your answer.

The ispGAL22V10C-10 is a SPLD which stands for Simple Programmable Logic Device. We used it because it is one of the simplest commercially available SPLDs.

4. Does the synthesizer have its own compiler or does it use the compiler from Aldec Active-

HDL? Explain the reason for your answer.

The synthesizer has its own compiler. If there are synthesis errors in the source code, it will be detected.

5. Is the same testbench used for both the functional simulation of Laboratory 1 and the post syn-

thesis simulation of this laboratory?

Yes, the same testbench is used for both the functional simulation of lab 1 and the post synthesis simulation.

6. Do you expect the results from the functional simulation and the post-synthesis simulation of

the same design entity to give the same exact results?

No, because post-synthesis simulation also simulates what will happen in real-world which means it considers the delay of each gates. Therefore, I expected there are will be delays shown on the waveform due to gates delay. However, the fundamental truth table will be the same.

7. What coding style is used in the automatically generated post synthesis model?

Dataflow style coding is automatically generated by post synthesis model.

8. Why are the RTL - Hierarchical view and the Technology - Flattened to Gates schematics produced by HDL Analyst for the half-adder different? Are they logically the same?

They are both logically the same. The difference is RTL shows the design structure and Flattened to Gates shows the actual gates.

9. When the waveforms from the simulation of the original design description and the synthesized

logic were compared there were slight differences. Explain the reason for these differences.

There were three differences indicated visually by blue lines for the length of the differences over the edge of the signal transitions. They appear because Synplify has put 100 ps delay in the model of each of the gates in the file .vhm.

Questions for Lab02b

1. What model of the half-adder design entity is used for timing simulation? What is the source of

this model?

The timing model is given the name half_adder.vhq. The source of this model comes from place-and-route tool.

2. Why does performing a timing simulation obviate the need to perform a post synthesis simulation?

This is because the timing simulation also includes post synthesis simulation.

3. What is the purpose of the loc attributes in the entity declaration? What do the simulation and

synthesis tools do with the loc attributes?

The purpose of the loc attributes in the entity declaration is to allow a user to provide pin-locking information to the place-and-route tool to control the processing of this design description. The simulation verify each pin numbers assigned to input signals are input pins of the PLD.

4. What does the place-and-route tool do with the loc attributes?

It is assigning exact pin numbers that user wants to use. If you do not specify pin assignments, the place-and-route tool will make its own choice of pin assignments.

5. How are propagation delays denoted in the file half_adder.vhq?

The propagation delays are denoted in VHDL program waveform. By adding cursor, you can position the cursors so that the time between any two points is displayed and measure the delay.