route_tb.vhd

```
1  ----------------------------------------------------------------------------
2  --
3  -- Title       : route_tb
4  -- Design      : testbench
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  ----------------------------------------------------------------------------
9  --
10 -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11 -- Generated   : 2024-03-04  15:00:00
12 -- From        : interface description file
13 -- By          : Itf2Vhdl ver. 1.22
14 --
15 ----------------------------------------------------------------------------
16 --
17 -- Description : testbench for route using record
18 ----------------------------------------------------------------------------
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use ieee.numeric_std.all;
23 use work.all;
24
25 entity route_tb is
26 end route_tb;
27
28 architecture tb_architecture of route_tb is
29
30     -- Stimulus signals - signals mapped to the inputs of tested entity
31     signal a, ae, b, be: std_logic;
32     -- Observed signals - signals mapped to the outputs of tested entity
33     signal y : std_logic;
34
35
36     type test_vector is record
37         a : std_logic;
38         ae : std_logic;
39         b : std_logic;
40         be : std_logic;
41         y : std_logic;
42
43     end record;
44
45     type test_vector_array is array (natural range <>) of test_vector;
46
47
48     constant test_vectors : test_vector_array := (
49     --    a,   ae,  b,   be,  y
50         ('0', '0', '0', '0', '1'),
51         ('0', '0', '0', '1', '1'),
52         ('0', '0', '1', '0', '1'),
53         ('0', '0', '1', '1', '0'),
54         ('0', '1', '0', '0', '1'),
55         ('0', '1', '0', '1', '1'),
56         ('0', '1', '1', '0', '1'),
57         ('0', '1', '1', '1', '0'),
```

```
        ('1', '0', '0', '0', '1'),
        ('1', '0', '0', '1', '1'),
        ('1', '0', '1', '0', '1'),
        ('1', '0', '1', '1', '0'),
        ('1', '1', '0', '0', '0'),
        ('1', '1', '0', '1', '0'),
        ('1', '1', '1', '0', '0'),
        ('1', '1', '1', '1', '0')
    );

    -- time between application of input stimulus vectors
    --constant period : time := 20ns;

begin
    -- Unit Under Test port map
    UUT : entity route
    port map (
            a => a, ae => ae, b => b, be => be, y => y
        );

    verify: process
    begin
    for i in test_vectors'range loop
        a <= test_vectors(i).a;
        ae <= test_vectors(i).ae;
        b <= test_vectors(i).b;
        be <= test_vectors(i).be;
        wait for 20 ns;
        assert (a = test_vectors(i).a) and (ae = test_vectors(i).ae) and (b = test_vectors(i).b) and (be = test_vectors(i).be)
        report "test vector " & integer'image(i)& " failed" & " for input a = " & std_logic'image(a) & " and ae = " & std_logic'image(ae) & " and b = " & std_logic'image(b) & " and be = " & std_logic'image(be)
        severity error;
    end loop;

        std.env.finish; --stop simulation
    end process;

end tb_architecture;

```