

xs3_to_BCD_CSOP.vhd

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity converter_xs3_bcd_selected is
5      port(
6          p, q, r, s : in std_logic;
7          d, c, b, a : out std_logic
8      );
9  end converter_xs3_bcd_selected;
10
11
12
13  architecture CSOP of converter_xs3_bcd_selected is
14  begin
15      -- CSOP
16
17      process(p, q, r, s)
18      begin
19          if (p = '1' and q = '0' and r = '1' and s = '1') or
20             (p = '1' and q = '1' and r = '0' and s = '0') then
21              d <= '1';
22          elsif
23             (p = '0' and q = '1' and r = '1' and s = '1') or
24             (p = '1' and q = '0' and r = '0' and s = '0') or
25             (p = '1' and q = '0' and r = '0' and s = '1') or
26             (p = '1' and q = '0' and r = '1' and s = '0') then
27              c <= '1';
28          elsif
29             (p = '0' and q = '1' and r = '0' and s = '1') or
30             (p = '0' and q = '1' and r = '1' and s = '0') or
31             (p = '1' and q = '0' and r = '0' and s = '1') or
32             (p = '1' and q = '0' and r = '1' and s = '1') then
33              b <= '1';
34          elsif
35             (p = '0' and q = '1' and r = '0' and s = '0') or
36             (p = '0' and q = '1' and r = '1' and s = '0') or
37             (p = '1' and q = '0' and r = '0' and s = '0') or
38             (p = '1' and q = '0' and r = '1' and s = '0') or
39             (p = '1' and q = '1' and r = '0' and s = '0') then
40              a <= '1';
41          else
42              d <= 'Z';
43              c <= 'Z';
44              b <= 'Z';
45              a <= 'Z';
46          end if;
47      end process;
48  end process;
49
50  end csop;
51
```