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Lab6: Testbenches for Combinational Designs

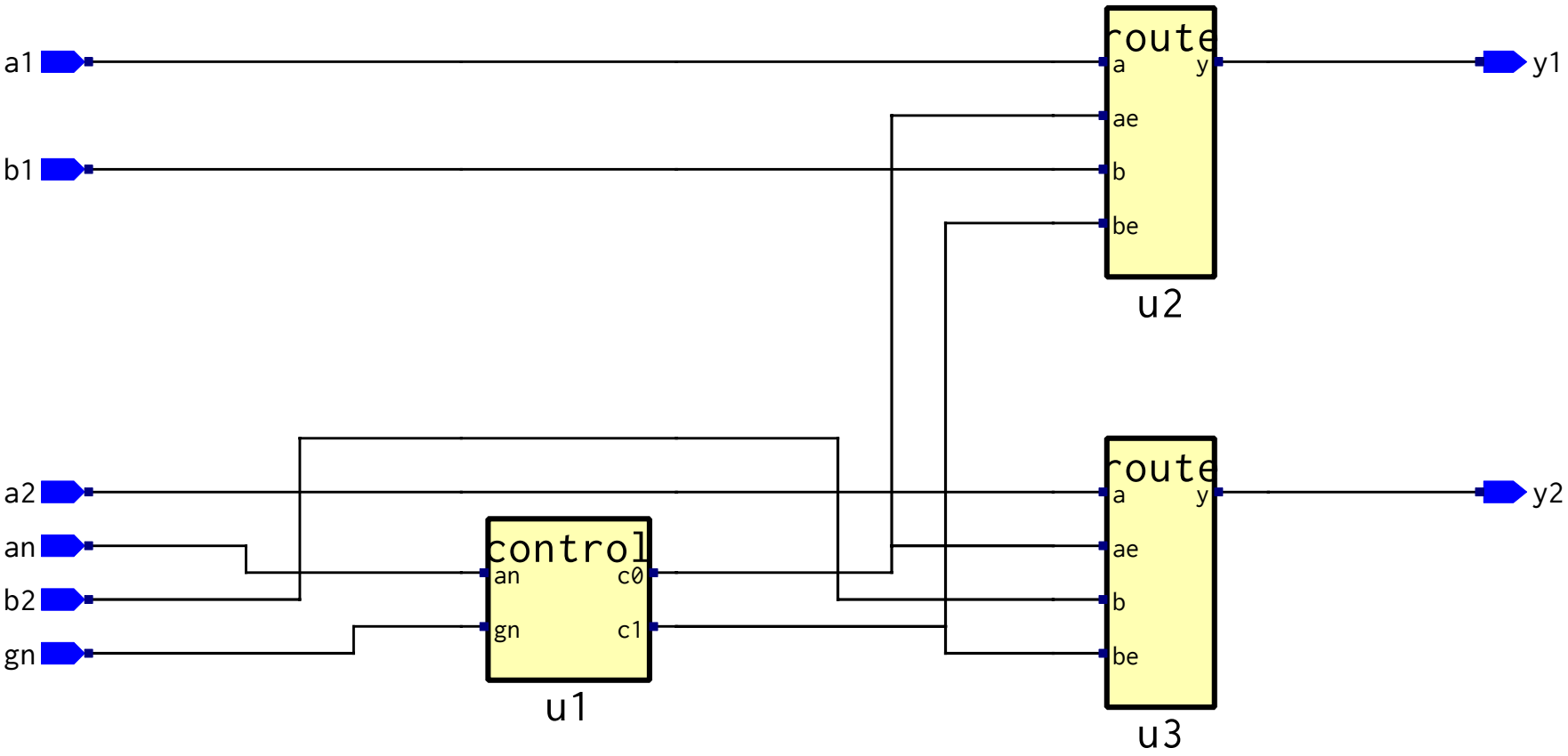
ESE382-L01

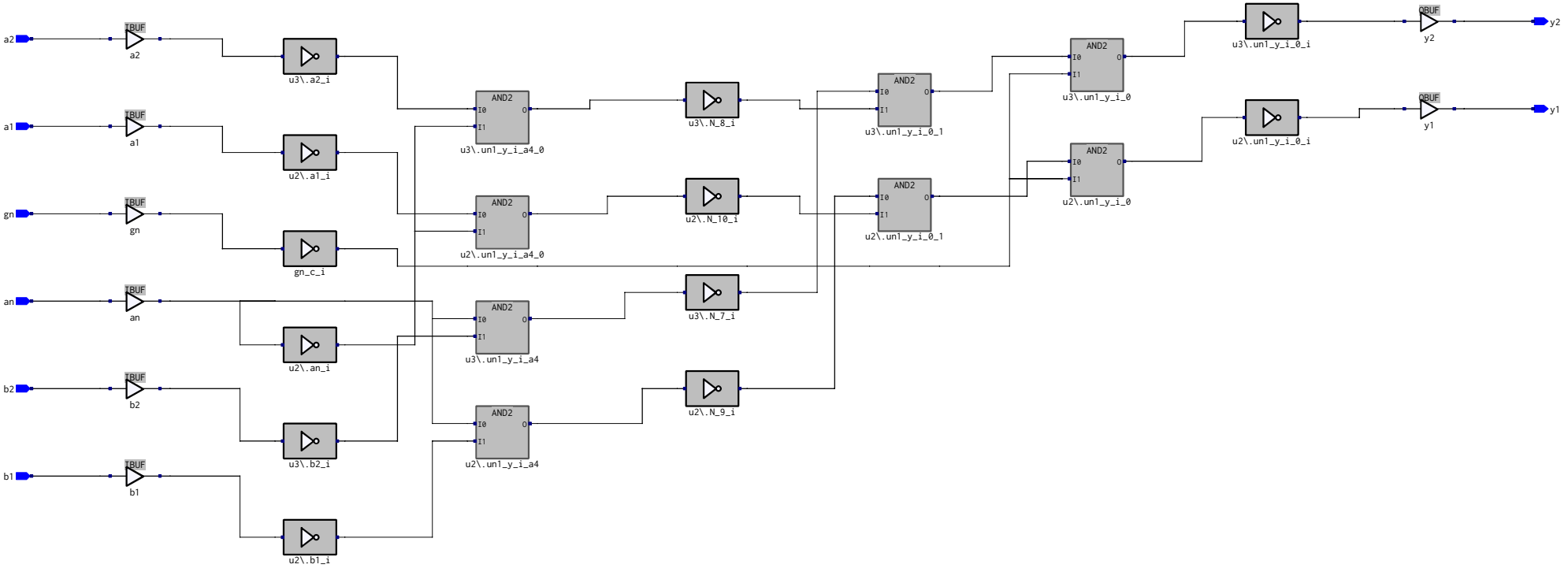
Bench #4

```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : control_route_mux
4   -- Design      :
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11  -- Generated   : 2024-03-04  15:00:00
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description : using structual style
18  ----------------------------------------------------------------------------
    ----
19  library ieee;
20  use ieee.std_logic_1164.all;
21
22  entity route is
23      port(
24          a : in std_logic;
25          ae : in std_logic;
26          b : in std_logic;
27          be : in std_logic;
28          y : out std_logic
29      );
30
31  end route;
32
33  architecture bool of route is
34  begin
35      y <= not ((a and ae) or (b and be));
36  end bool;
37
38
39  library ieee;
40  use ieee.std_logic_1164.all;
41
42  entity control is
43      port(
44          gn, an : in std_logic;
45          c0, c1 : out std_logic
46      );
47  end control;
48
49  architecture csop of control is
50  begin
51      c0 <= not gn and not an;
52      c1 <= not gn and an;
53  end csop;
```

```
54
55
56  library ieee;
57  use ieee.std_logic_1164.all;
58  use work.all;
59
60  entity data_selector is
61    port(
62      a1, b1, a2, b2, gn, an : in std_logic;
63      y1, y2 : out std_logic
64    );
65      attribute loc : string;
66      attribute loc of gn : signal is "P3";
67      attribute loc of an : signal is "P4";
68      attribute loc of a2 : signal is "P14";
69      attribute loc of a1 : signal is "P15";
70      attribute loc of b2 : signal is "P16";
71      attribute loc of b1 : signal is "P17";
72      attribute loc of y2 : signal is "P43";
73      attribute loc of y1 : signal is "P42";
74  end data_selector;
75
76  architecture structural of data_selector is
77    signal s1, s2 : std_logic;
78  begin
79    u1: entity control port map (gn => gn, an => an, c0 => s1, c1 => s2);
80    u2: entity route port map (a => a1, ae => s1, b => b1, be => s2, y => y1
    );
81    u3: entity route port map (a => a2, ae => s1, b => b2, be => s2, y => y2
    );
82  end structural;
83
```

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title      : control_route_mux_tb
4   -- Design     : testbench
5   -- Author     : Dongyun Lee
6   -- Company    : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File       : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11  -- Generated  : 2024-03-04  15:00:00
12  -- From       : interface description file
13  -- By         : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : for loop 0 to all 1
18  ------------------------------------------------------------------------
    ----
19
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use ieee.numeric_std.all;
23  use work.all;
24
25  entity control_route_mux_tb is
26  end control_route_mux_tb;
27
28  architecture tb_architecture of control_route_mux_tb is
29
30      -- Stimulus signals - signals mapped to the inputs of tested entity
31      signal a2, a1, b2, b1, gn, an: std_logic;
32      -- Observed signals - signals mapped to the outputs of tested entity
33      signal y2, y1 : std_logic;
34
35  begin
36      UUT : entity data_selector
37      port map (
38              gn => gn, an =>an, a2 => a2, a1 => a1, b2 => b2, b1 => b1, y2
    => y2, y1 => y1
39          );
40      verify : process
41      begin
42          for i in 0 to 2**6 - 1 loop
43              (gn, an, a2, a1, b2, b1) <= std_logic_vector(to_unsigned(i, 6
    ));
44              wait for 10 ns;
45
46          end loop;
47          std.env.finish;
48      end process verify;
49
50  end tb_architecture;
51
```


a1
b1
a2
an
b2
gn
route
a
y
ae
b
be
u2
y1
control
an
c0
gn
c1
u1
route
a
y
ae
b
be
u3
y2


a2
TBUF
a2
u3\.a2_i
a1
TBUF
a1
u2\.a1_i
gn
TBUF
gn
gn_c_i
an
TBUF
an
u2\.an_i
b2
TBUF
b2
u3\.b2_i
b1
TBUF
b1
u2\.b1_i
AND2
I0
I1
O
u3\.un1_y_i_a4_0
u2\.un1_y_i_a4_0
u3\.un1_y_i_a4
u2\.un1_y_i_a4
u3\.N_8_i
u2\.N_10_i
u3\.N_7_i
u2\.N_9_i
u3\.un1_y_i_0_1
u2\.un1_y_i_0_1
u3\.un1_y_i_0
u2\.un1_y_i_0
u3\.un1_y_i_0_i
u2\.un1_y_i_0_i
QBUF
y2
y1

```
|--------------------------------------------|
|- ispLEVER Fitter Report File              -|
|- Version 2.1.00.02.49.20                  -|
|- (c)Copyright, Lattice Semiconductor 2002 -|
|--------------------------------------------|
```

Project_Summary
~~~~~~~~~~~~~~~

```
Project Name :          untitled
Project Path :          F:\ESE382-Lab\Lab6\P_R
Project Fitted on :     Wed Mar 06 10:31:05 2024

Device :                M4A5-64/32
Package :               44PLCC
Speed :                 -10
Partnumber :            M4A5-64/32-10JC
Source Format :         EDIF
```

// Project 'untitled' was Fitted Successfully! //

Compilation_Times
~~~~~~~~~~~~~~~~~

Reading/DRC	0 sec
Partition	0 sec
Place	0 sec
Route	0 sec
Jedec/Report generation	0 sec

Fitter	00:00:00

Design_Summary
~~~~~~~~~~~~~~

Total Input Pins :	6
Total Output Pins :	2
Total Bidir I/O Pins :	0
Total Flip-Flops :	0
Total Product Terms :	4
Total Reserved Pins :	0
Total Reserved Blocks :	0

Device_Resource_Summary
~~~~~~~~~~~~~~~~~~~~~~~

	Total Available	Used	Available	Utilization
Dedicated Pins				
Input-Only Pins	..	..	.. -->	..
Clock/Input Pins	2	0	2 -->	0%
I/O Pins	32	8	24 -->	25%
Logic Macrocells	64	2	62 -->	3%
Input Registers	32	0	32 -->	0%
Unusable Macrocells	..	0	..	
CSM Outputs/Total Block Inputs	132	6	126 -->	4%
Logical Product Terms	320	4	316 -->	1%

Product Term Clusters 64 2 62 --> 3%

Blocks_Resource_Summary
~~~~~~~~~~~~~~~~~~~~~~~

	I/O Fanin	Inp Pins	Macrocells Reg	Macrocells Used	Macrocells Unusable	# of PT logic available	clusters PTs available	Pwr
Maximum	33	8	8	--	--	16	80	16	-
Block A	0	2	0	0	0	16	0	16	Hi
Block B	0	4	0	0	0	16	0	16	Hi
Block C	0	0	0	0	0	16	0	16	Hi
Block D	6	2	0	2	0	14	4	14	Hi

<Note> Four rightmost columns above reflect last status of the placement process.
<Note> Pwr (Power) : Hi = High
Lo = Low.

Optimizer_and_Fitter_Options
~~~~~~~~~~~~~~~~~~~~~~~~~~~~

Pin Assignment : Yes
Group Assignment : No
Pin Reservation : No (1)
Block Reservation : No

@Ignore_Project_Constraints :
Pin Assignments : No
Keep Block Assignment --
Keep Segment Assignment --
Group Assignments : No
Macrocell Assignment : No
Keep Block Assignment --
Keep Segment Assignment --

@Backannotate_Project_Constraints
Pin Assignments : No
Pin And Block Assignments : No
Pin, Macrocell and Block : No

@Timing_Constraints : No

@Global_Project_Optimization :
Balanced Partitioning : Yes
Spread Placement : Yes

Note :
Pack Design :
Balanced Partitioning = No
Spread Placement = No
Spread Design :
Balanced Partitioning = Yes
Spread Placement = Yes

@Logic_Synthesis :
Logic Reduction : Yes
Node Collapsing : Yes
D/T Synthesis : Yes
Clock Optimization : No

```
  Input Register Optimization :        Yes
  XOR Synthesis :                     Yes
  Max. P-Term for Collapsing :         16
  Max. P-Term for Splitting :          16
  Max. Equation Fanin :                32
  Keep Xor :                          Yes

@Utilization_options
  Max. % of macrocells used :          100
  Max. % of block inputs used :        100
  Max. % of segment lines used :        ---
  Max. % of macrocells used :          ---


@Import_Source_Constraint_Option       No

@Zero_Hold_Time                        No

@Pull_up                           No

@User_Signature                        #H0

@Output_Slew_Rate                      Default = Fast(2)

@Power                             Default = High(2)


Device Options:
<Note> 1 : Reserved unused I/Os can be independently driven to Low or High, and does not
          follow the drive level set for the Global Configure Unused I/O Option.
<Note> 2 : For user-specified constraints on individual signals, refer to the Output,
          Bidir and Burried Signal Lists.
```

Pinout_Listing
~~~~~~~~~~~~~~~

```
      | Pin  |Blk |Assigned|
Pin No| Type |Pad |Pin     | Signal name
-------------------------------------------------------------------------
   1 |  GND |    |        |
   2 |  I_O | A7 |        |
3     |  I_O | A6 |   *    |gn
4     |  I_O | A5 |   *    |an
5     |  I_O | A4 |        |
6     |  I_O | A3 |        |
7     |  I_O | A2 |        |
8     |  I_O | A1 |        |
9     |  I_O | A0 |        |
10    | JTAG |    |        |
11    | CkIn |    |        |
12    |  GND |    |        |
13    | JTAG |    |        |
14    |  I_O | B0 |   *    |a2
15    |  I_O | B1 |   *    |a1
16    |  I_O | B2 |   *    |b2
17    |  I_O | B3 |   *    |b1
18    |  I_O | B4 |        |
19    |  I_O | B5 |        |
20    |  I_O | B6 |        |
21    |  I_O | B7 |        |
```
~~~~~~~~~~~~~~~

```
22    |  Vcc |    |       |
23    |  GND |    |       |
24    |  I_O | C7 |       |
25    |  I_O | C6 |       |
26    |  I_O | C5 |       |
27    |  I_O | C4 |       |
28    |  I_O | C3 |       |
29    |  I_O | C2 |       |
30    |  I_O | C1 |       |
31    |  I_O | C0 |       |
32    | JTAG |    |       |
33    | CkIn |    |       |
34    |  GND |    |       |
35    | JTAG |    |       |
36    |  I_O | D0 |       |
37    |  I_O | D1 |       |
38    |  I_O | D2 |       |
39    |  I_O | D3 |       |
40    |  I_O | D4 |       |
41    |  I_O | D5 |       |
42    |  I_O | D6 |   *   |y1
43    |  I_O | D7 |   *   |y2
44    |  Vcc |    |       |
```

<Note> Blk Pad : This notation refers to the Block I/O pad number in the device.
<Note> Assigned Pin : user or dedicated input assignment (E.g. Clock pins).
<Note> Pin Type :
CkIn : Dedicated input or clock pin
CLK : Dedicated clock pin
INP : Dedicated input pin
JTAG : JTAG Control and test pin
NC : No connected

Input_Signal_List
~~~~~~~~~~~~~~~~~

Pin	Blk	PTs	Type	P r e s	O E	Input Fanout	Pwr	Slew	Signal
15	B	.	I/O		---	D	Hi	Fast	a1
14	B	.	I/O		---	D	Hi	Fast	a2
4	A	.	I/O		---	D	Hi	Fast	an
17	B	.	I/O		---	D	Hi	Fast	b1
16	B	.	I/O		---	D	Hi	Fast	b2
3	A	.	I/O		---	D	Hi	Fast	gn

<Note> Power : Hi = High
MH = Medium High
ML = Medium Low
Lo = Low

Output_Signal_List
~~~~~~~~~~~~~~~~~~

Pin	P r e s	O E	Output

```
Pin Blk PTs Type e s E   Fanout Pwr Slew      Signal
-------------------------------------------------------------------------------
 42  D   2  COM          ----   Hi Fast      y1
 43  D   2  COM          ----   Hi Fast      y2
-------------------------------------------------------------------------------

<Note> Power : Hi = High
               MH = Medium High
               ML = Medium Low
               Lo = Low
```

Bidir_Signal_List
~~~~~~~~~~~~~~~~~~

```
                P R
           Pin  r e O   Bidir
Pin Blk PTs Type e s E   Fanout Pwr Slew      Signal
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------

<Note> Power : Hi = High
               MH = Medium High
               ML = Medium Low
               Lo = Low
```

Buried_Signal_List
~~~~~~~~~~~~~~~~~~~

```
                P R
           Pin  r e O   Node
#Mc Blk PTs Type e s E   Fanout Pwr Slew      Signal
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------

<Note> Power : Hi = High
               MH = Medium High
               ML = Medium Low
               Lo = Low
```

Signals_Fanout_List
~~~~~~~~~~~~~~~~~~~~

```
Signal Source  :    Fanout List
-------------------------------------------------------------------------------
        a1{ C}:             y1{ D}
        b1{ C}:             y1{ D}
        a2{ C}:             y2{ D}
        b2{ C}:             y2{ D}
        gn{ B}:             y1{ D}             y2{ D}
        an{ B}:             y1{ D}             y2{ D}
-------------------------------------------------------------------------------

<Note> {.} : Indicates block location of signal
```

Set_Reset_Summary
~~~~~~~~~~~~~~~~~~

Block A
block level set pt :
block level reset pt :
Equations :

			Block	Block	Signal
Reg	Mode	Set	Reset		Name
					an
					gn

Block B
block level set pt :
block level reset pt :
Equations :

			Block	Block	Signal
Reg	Mode	Set	Reset		Name
					b1
					b2
					a1
					a2

Block C
block level set pt :
block level reset pt :
Equations :

			Block	Block	Signal
Reg	Mode	Set	Reset		Name

Block D
block level set pt :
block level reset pt :
Equations :

			Block	Block	Signal
Reg	Mode	Set	Reset		Name
					y2
					y1

<Note> (S) means the macrocell is configured in synchronous mode
i.e. it uses the block-level set and reset pt.
(A) means the macrocell is configured in asynchronous mode
i.e. it can have its independant set or reset pt.
(BS) means the block-level set pt is selected.
(BR) means the block-level reset pt is selected.

BLOCK_D_LOGIC_ARRAY_FANIN

CSM	Signal	Source	CSM	Signal	Source
mx D0	...	...	mx D17	...	...
mx D1	gn	pin 3	mx D18	...	...
mx D2	...	...	mx D19	...	...
mx D3	a2	pin 14	mx D20	b1	pin 17

mx D4 ... ... mx D21 ... ...
mx D5 ... ... mx D22 ... ...
mx D6 b2 pin 16 mx D23 ... ...
mx D7 ... ... mx D24 a1 pin 15
mx D8 ... ... mx D25 ... ...
mx D9 ... ... mx D26 ... ...
mx D10 ... ... mx D27 ... ...
mx D11 ... ... mx D28 ... ...
mx D12 an pin 4 mx D29 ... ...
mx D13 ... ... mx D30 ... ...
mx D14 ... ... mx D31 ... ...
mx D15 ... ... mx D32 ... ...
mx D16 ... ...

<Note> CSM indicates the mux inputs from the Central Switch Matrix.
<Note> Source indicates where the signal comes from (pin or macrocell).

PostFit_Equations
~~~~~~~~~~~~~~~~~

P-Terms	Fan-in	Fan-out	Type	Name (attributes)
2	4	1	Pin	y1-
2	4	1	Pin	y2-
4		P-Term Total: 4		
		Total Pins: 8		
		Total Nodes: 0		
		Average P-Term/Output: 2		

Equations:

```
!y1 = (b1 & !gn & an
    # a1 & !gn & !an);

!y2 = (b2 & !gn & an
    # a2 & !gn & !an);
```

Reverse-Polarity Equations:
~~~~~~~~~~~~~~~~~