```
1    -- Jed2svhdl, ispLEVER version 2.01
2    -- Header :
3    --    File Name :
4    --       half_adder
5    --    Circuit Name :
6    --       half_adder
7    --    Last Update :
8    --       Wed Feb 07 09:50:31 2024
9    --    Device Information :
10   --       PLD Type P22V10GC
11   --    Manufacturer and Part Information :
12   --       LAT ISPGAL22V10C-10LJ GAL
13   --    Delay Model Selected :MAX
14   --    Jedec Information :
15   --  ispLEVER Classic 2.1.00.02.49.20 Lattice Semiconductor Corp.
16   --  JEDEC file for: P22V10GC V1.1
17   --  Created on: Wed Feb 07 09:50:30 2024
18   --
19   --
20   -- endHeader
21
22   LIBRARY j2svlib;
23   USE j2svlib.j2svlib.all;
24   LIBRARY IEEE;
25   USE IEEE.std_logic_1164.all;
26   USE std.textio.all;
27   ---------------------------------------------------------------------------
28   --                                                                       --
29   --              MAIN PLD NETLIST MODULE                                  --
30   --                                                                       --
31   ---------------------------------------------------------------------------
32
33   ENTITY half_adder IS
34      GENERIC (
35   -- Delay Parameters:
36   --   MAX delay used
37         tpLH09 : time := 0 ns;
38         tpHL09 : time := 0 ns;
39         tpLH11 : time := 0 ns;
40         tpHL11 : time := 0 ns;
41         tpLH_iob : time := 0 ns;
42         tpHL_iob : time := 0 ns;
43         tpLH03 : time := 0 ns;
44         tpHL03 : time := 0 ns;
45         tpLH05 : time := 0 ns;
46         tpHL05 : time := 0 ns;
47         tpLH_inco_lump : time := 10 ns;
48         tpHL_inco_lump : time := 10 ns;
49         tpLH_oe : time := 0 ns;
50         tpHL_oe : time := 0 ns;
51         tpLH_oe_pterm : time := 10 ns;
52         tpHL_oe_pterm : time := 10 ns;
53         t_preset : time := 0 ns;
54         t_reset : time := 13 ns;
55         t_cnt : time := 10 ns;
56         T_ckout : time := 7 ns;
57         t_setup : time := 7 ns;
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58          t_hold  : time := 0 ns;
59          t_co    : time := 7 ns;
60          t_cf    : time := 3 ns;
61          tpLH_fo_lump : time:= 4 ns;
62          tpHL_fo_lump : time := 4 ns);
63       PORT (
64
65        PIN02: IN STD_LOGIC := '0';
66        a: IN STD_LOGIC := '0';
67        b: IN STD_LOGIC := '0';
68        PIN05: IN STD_LOGIC := '0';
69        PIN06: IN STD_LOGIC := '0';
70        PIN07: IN STD_LOGIC := '0';
71        PIN09: IN STD_LOGIC := '0';
72        PIN10: IN STD_LOGIC := '0';
73        PIN11: IN STD_LOGIC := '0';
74        PIN12: IN STD_LOGIC := '0';
75        PIN13: IN STD_LOGIC := '0';
76        PIN16: IN STD_LOGIC := '0';
77        PIN17: INOUT STD_LOGIC;
78        PIN18: INOUT STD_LOGIC;
79        PIN19: INOUT STD_LOGIC;
80        PIN20: INOUT STD_LOGIC;
81        PIN21: INOUT STD_LOGIC;
82        PIN23: INOUT STD_LOGIC;
83        PIN24: INOUT STD_LOGIC;
84        PIN25: INOUT STD_LOGIC;
85        carry_out: OUT STD_LOGIC;
86        sum: OUT STD_LOGIC);
87
88    --Pin Assignments:
89        -- alias PIN03 is: STD_LOGIC a;
90        -- alias PIN04 is: STD_LOGIC b;
91        -- alias PIN26 is: STD_LOGIC carry_out;
92        -- alias PIN27 is: STD_LOGIC sum;
93
94    END half_adder;
95
96    ARCHITECTURE structure OF half_adder IS
97
98    -- Signal Declaration :
99       SIGNAL  sum_ODUMMY, carry_out_ODUMMY, NODE30_ob, NODE30_o,
100              NODE29_ob, NODE29_o, FO_OUTREG25_o, FO_OUTREG24_o,
101              FO_OUTREG23_o, FO_OUTREG21_o, FO_OUTREG20_o, FO_OUTREG19_o,
102              FO_OUTREG18_o, FO_OUTREG17_o, NODE38_ob, NODE38_o, NODE37_ob,
103              NODE37_o, NODE36_ob, NODE36_o, NODE35_ob, NODE35_o,
104              NODE34_ob, NODE34_o, NODE33_ob, NODE33_o, NODE32_ob, NODE32_o,
105              NODE31_ob, NODE31_o, OUTREG25_ob, OUTREG25_o, OUTREG24_ob,
106              OUTREG24_o, OUTREG23_ob, OUTREG23_o, OUTREG21_ob, OUTREG21_o,
107              OUTREG20_ob, OUTREG20_o, OUTREG19_ob, OUTREG19_o, OUTREG18_ob,
108              OUTREG18_o, OUTREG17_ob, OUTREG17_o, O2O_CKDR_o, ST027_o,
109              ST026_o, PT011_484_o, PT003_132_o, PT002_88_o, INBUF27_ob,
110              INBUF27_o, INBUF26_ob, INBUF26_o, INBUF16_ob, INBUF16_o,
111              INBUF13_ob, INBUF13_o, INBUF12_ob, INBUF12_o, INBUF11_ob,
112              INBUF11_o, INBUF10_ob, INBUF10_o, INBUF09_ob, INBUF09_o,
113              INBUF07_ob, INBUF07_o, INBUF06_ob, INBUF06_o, INBUF05_ob,
114              INBUF05_o, INBUF04_ob, INBUF04_o, INBUF03_ob, INBUF03_o,
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115             CLKIN1_ob, CLKIN1_o
116             : STD_LOGIC ;
117     SIGNAL  PWR : STD_LOGIC := '1' ;
118     SIGNAL  GND : STD_LOGIC := '0' ;
119     SIGNAL  PWRUPSTATE : STD_LOGIC := '0' ;
120
121   --   PLD Netlist ---------
122     BEGIN
123
124   --   Input Buffer:
125         CLKIN1_o <= PIN02 after g_delay ( CLKIN1_o,tpLH_iob,tpHL_iob);
126         CLKIN1_ob <=  not(PIN02) after g_delay ( CLKIN1_ob,tpLH_iob,tpHL_iob
    );
127         INBUF03_o <= a after g_delay ( INBUF03_o,tpLH_iob,tpHL_iob);
128         INBUF03_ob <=  not(a) after g_delay ( INBUF03_ob,tpLH_iob,tpHL_iob);
129         INBUF04_o <= b after g_delay ( INBUF04_o,tpLH_iob,tpHL_iob);
130         INBUF04_ob <=  not(b) after g_delay ( INBUF04_ob,tpLH_iob,tpHL_iob);
131         INBUF05_o <= PIN05 after g_delay ( INBUF05_o,tpLH_iob,tpHL_iob);
132         INBUF05_ob <=  not(PIN05) after g_delay ( INBUF05_ob,tpLH_iob,
    tpHL_iob);
133         INBUF06_o <= PIN06 after g_delay ( INBUF06_o,tpLH_iob,tpHL_iob);
134         INBUF06_ob <=  not(PIN06) after g_delay ( INBUF06_ob,tpLH_iob,
    tpHL_iob);
135         INBUF07_o <= PIN07 after g_delay ( INBUF07_o,tpLH_iob,tpHL_iob);
136         INBUF07_ob <=  not(PIN07) after g_delay ( INBUF07_ob,tpLH_iob,
    tpHL_iob);
137         INBUF09_o <= PIN09 after g_delay ( INBUF09_o,tpLH_iob,tpHL_iob);
138         INBUF09_ob <=  not(PIN09) after g_delay ( INBUF09_ob,tpLH_iob,
    tpHL_iob);
139         INBUF10_o <= PIN10 after g_delay ( INBUF10_o,tpLH_iob,tpHL_iob);
140         INBUF10_ob <=  not(PIN10) after g_delay ( INBUF10_ob,tpLH_iob,
    tpHL_iob);
141         INBUF11_o <= PIN11 after g_delay ( INBUF11_o,tpLH_iob,tpHL_iob);
142         INBUF11_ob <=  not(PIN11) after g_delay ( INBUF11_ob,tpLH_iob,
    tpHL_iob);
143         INBUF12_o <= PIN12 after g_delay ( INBUF12_o,tpLH_iob,tpHL_iob);
144         INBUF12_ob <=  not(PIN12) after g_delay ( INBUF12_ob,tpLH_iob,
    tpHL_iob);
145         INBUF13_o <= PIN13 after g_delay ( INBUF13_o,tpLH_iob,tpHL_iob);
146         INBUF13_ob <=  not(PIN13) after g_delay ( INBUF13_ob,tpLH_iob,
    tpHL_iob);
147         INBUF16_o <= PIN16 after g_delay ( INBUF16_o,tpLH_iob,tpHL_iob);
148         INBUF16_ob <=  not(PIN16) after g_delay ( INBUF16_ob,tpLH_iob,
    tpHL_iob);
149         INBUF26_o <= carry_out_ODUMMY after g_delay ( INBUF26_o,tpLH_iob,
    tpHL_iob);
150         INBUF26_ob <=  not(carry_out_ODUMMY) after g_delay ( INBUF26_ob,
    tpLH_iob,tpHL_iob);
151         INBUF27_o <= sum_ODUMMY after g_delay ( INBUF27_o,tpLH_iob,tpHL_iob
    );
152         INBUF27_ob <=  not(sum_ODUMMY) after g_delay ( INBUF27_ob,tpLH_iob,
    tpHL_iob);
153
154   --   Product Terms (AND array):
155         PT002_88_o <= INBUF03_ob AND INBUF04_o after g_delay ( PT002_88_o,
    tpLH03,tpHL03);
156         PT003_132_o <= INBUF03_o AND INBUF04_ob after g_delay ( PT003_132_o,
    tpLH03,tpHL03);
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157         PT011_484_o <= INBUF03_o AND INBUF04_o after g_delay ( PT011_484_o,
    tpLH03,tpHL03);
158
159   --    Sum Terms (OR arrray):
160         ST026_o <= PT011_484_o after g_delay ( ST026_o,tpLH_inco_lump,
    tpHL_inco_lump);
161         ST027_o <= PT002_88_o OR PT003_132_o after g_delay ( ST027_o,
    tpLH_inco_lump,tpHL_inco_lump);
162
163   --    Macro Cells:
164         O2O_CKDR_o <= CLKIN1_o after g_delay ( O2O_CKDR_o,tpLH05,tpHL05);
165         g_dff_spar( OUTREG17_o, OUTREG17_ob, GND, O2O_CKDR_o, NODE30_o,
    NODE29_o, PWRUPSTATE, t_cf, t_reset);
166         process (GND, O2O_CKDR_o) variable lastd, lastc: time; begin
167              p_chksuho (GND, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG17");
168         end process;
169         process (NODE30_o, O2O_CKDR_o) variable lastd, lastc: time; begin
170              p_chksuho (NODE30_o, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG17");
171         end process;
172         g_dff_spar( OUTREG18_o, OUTREG18_ob, GND, O2O_CKDR_o, NODE30_o,
    NODE29_o, PWRUPSTATE, t_cf, t_reset);
173         process (GND, O2O_CKDR_o) variable lastd, lastc: time; begin
174              p_chksuho (GND, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG18");
175         end process;
176         process (NODE30_o, O2O_CKDR_o) variable lastd, lastc: time; begin
177              p_chksuho (NODE30_o, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG18");
178         end process;
179         g_dff_spar( OUTREG19_o, OUTREG19_ob, GND, O2O_CKDR_o, NODE30_o,
    NODE29_o, PWRUPSTATE, t_cf, t_reset);
180         process (GND, O2O_CKDR_o) variable lastd, lastc: time; begin
181              p_chksuho (GND, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG19");
182         end process;
183         process (NODE30_o, O2O_CKDR_o) variable lastd, lastc: time; begin
184              p_chksuho (NODE30_o, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG19");
185         end process;
186         g_dff_spar( OUTREG20_o, OUTREG20_ob, GND, O2O_CKDR_o, NODE30_o,
    NODE29_o, PWRUPSTATE, t_cf, t_reset);
187         process (GND, O2O_CKDR_o) variable lastd, lastc: time; begin
188              p_chksuho (GND, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG20");
189         end process;
190         process (NODE30_o, O2O_CKDR_o) variable lastd, lastc: time; begin
191              p_chksuho (NODE30_o, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG20");
192         end process;
193         g_dff_spar( OUTREG21_o, OUTREG21_ob, GND, O2O_CKDR_o, NODE30_o,
    NODE29_o, PWRUPSTATE, t_cf, t_reset);
194         process (GND, O2O_CKDR_o) variable lastd, lastc: time; begin
195              p_chksuho (GND, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG21");
196         end process;
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197         process (NODE30_o, O2O_CKDR_o) variable lastd, lastc: time; begin
198              p_chksuho (NODE30_o, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG21");
199         end process;
200         g_dff_spar( OUTREG23_o, OUTREG23_ob, GND, O2O_CKDR_o, NODE30_o,
    NODE29_o, PWRUPSTATE, t_cf, t_reset);
201         process (GND, O2O_CKDR_o) variable lastd, lastc: time; begin
202              p_chksuho (GND, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG23");
203         end process;
204         process (NODE30_o, O2O_CKDR_o) variable lastd, lastc: time; begin
205              p_chksuho (NODE30_o, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG23");
206         end process;
207         g_dff_spar( OUTREG24_o, OUTREG24_ob, GND, O2O_CKDR_o, NODE30_o,
    NODE29_o, PWRUPSTATE, t_cf, t_reset);
208         process (GND, O2O_CKDR_o) variable lastd, lastc: time; begin
209              p_chksuho (GND, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG24");
210         end process;
211         process (NODE30_o, O2O_CKDR_o) variable lastd, lastc: time; begin
212              p_chksuho (NODE30_o, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG24");
213         end process;
214         g_dff_spar( OUTREG25_o, OUTREG25_ob, GND, O2O_CKDR_o, NODE30_o,
    NODE29_o, PWRUPSTATE, t_cf, t_reset);
215         process (GND, O2O_CKDR_o) variable lastd, lastc: time; begin
216              p_chksuho (GND, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG25");
217         end process;
218         process (NODE30_o, O2O_CKDR_o) variable lastd, lastc: time; begin
219              p_chksuho (NODE30_o, O2O_CKDR_o, t_setup, t_hold, lastc, lastd,
    "OUTREG25");
220         end process;
221
222    --   Feedback Node:
223         NODE31_o <= OUTREG17_ob after g_delay ( NODE31_o,tpLH_iob,tpHL_iob);
224         NODE31_ob <=  not(OUTREG17_ob) after g_delay ( NODE31_ob,tpLH_iob,
    tpHL_iob);
225         NODE32_o <= OUTREG18_ob after g_delay ( NODE32_o,tpLH_iob,tpHL_iob);
226         NODE32_ob <=  not(OUTREG18_ob) after g_delay ( NODE32_ob,tpLH_iob,
    tpHL_iob);
227         NODE33_o <= OUTREG19_ob after g_delay ( NODE33_o,tpLH_iob,tpHL_iob);
228         NODE33_ob <=  not(OUTREG19_ob) after g_delay ( NODE33_ob,tpLH_iob,
    tpHL_iob);
229         NODE34_o <= OUTREG20_ob after g_delay ( NODE34_o,tpLH_iob,tpHL_iob);
230         NODE34_ob <=  not(OUTREG20_ob) after g_delay ( NODE34_ob,tpLH_iob,
    tpHL_iob);
231         NODE35_o <= OUTREG21_ob after g_delay ( NODE35_o,tpLH_iob,tpHL_iob);
232         NODE35_ob <=  not(OUTREG21_ob) after g_delay ( NODE35_ob,tpLH_iob,
    tpHL_iob);
233         NODE36_o <= OUTREG23_ob after g_delay ( NODE36_o,tpLH_iob,tpHL_iob);
234         NODE36_ob <=  not(OUTREG23_ob) after g_delay ( NODE36_ob,tpLH_iob,
    tpHL_iob);
235         NODE37_o <= OUTREG24_ob after g_delay ( NODE37_o,tpLH_iob,tpHL_iob);
236         NODE37_ob <=  not(OUTREG24_ob) after g_delay ( NODE37_ob,tpLH_iob,
    tpHL_iob);
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237         NODE38_o <= OUTREG25_ob after g_delay ( NODE38_o,tpLH_iob,tpHL_iob);
238         NODE38_ob <=  not(OUTREG25_ob) after g_delay ( NODE38_ob,tpLH_iob,
    tpHL_iob);
239
240   --   Output Buffer:
241         FO_OUTREG17_o <= OUTREG17_o after g_delay ( FO_OUTREG17_o,
    tpLH_fo_lump,tpHL_fo_lump);
242         g_notif1( PIN17, FO_OUTREG17_o, GND, tpLH09,tpHL09);
243         FO_OUTREG18_o <= OUTREG18_o after g_delay ( FO_OUTREG18_o,
    tpLH_fo_lump,tpHL_fo_lump);
244         g_notif1( PIN18, FO_OUTREG18_o, GND, tpLH09,tpHL09);
245         FO_OUTREG19_o <= OUTREG19_o after g_delay ( FO_OUTREG19_o,
    tpLH_fo_lump,tpHL_fo_lump);
246         g_notif1( PIN19, FO_OUTREG19_o, GND, tpLH09,tpHL09);
247         FO_OUTREG20_o <= OUTREG20_o after g_delay ( FO_OUTREG20_o,
    tpLH_fo_lump,tpHL_fo_lump);
248         g_notif1( PIN20, FO_OUTREG20_o, GND, tpLH09,tpHL09);
249         FO_OUTREG21_o <= OUTREG21_o after g_delay ( FO_OUTREG21_o,
    tpLH_fo_lump,tpHL_fo_lump);
250         g_notif1( PIN21, FO_OUTREG21_o, GND, tpLH09,tpHL09);
251         FO_OUTREG23_o <= OUTREG23_o after g_delay ( FO_OUTREG23_o,
    tpLH_fo_lump,tpHL_fo_lump);
252         g_notif1( PIN23, FO_OUTREG23_o, GND, tpLH09,tpHL09);
253         FO_OUTREG24_o <= OUTREG24_o after g_delay ( FO_OUTREG24_o,
    tpLH_fo_lump,tpHL_fo_lump);
254         g_notif1( PIN24, FO_OUTREG24_o, GND, tpLH09,tpHL09);
255         FO_OUTREG25_o <= OUTREG25_o after g_delay ( FO_OUTREG25_o,
    tpLH_fo_lump,tpHL_fo_lump);
256         g_notif1( PIN25, FO_OUTREG25_o, GND, tpLH09,tpHL09);
257         g_bufif1( carry_out_ODUMMY, ST026_o, PWR, tpLH11,tpHL11);
258         g_bufif1( sum_ODUMMY, ST027_o, PWR, tpLH11,tpHL11);
259         NODE29_o <= GND after g_delay ( NODE29_o,tpLH_iob,tpHL_iob);
260         NODE29_ob <=  not(GND) after g_delay ( NODE29_ob,tpLH_iob,tpHL_iob);
261         NODE30_o <= GND after g_delay ( NODE30_o,t_preset,t_preset);
262         NODE30_ob <=  not(GND) after g_delay ( NODE30_ob,t_preset,t_preset);
263         carry_out <= carry_out_ODUMMY;
264         sum <= sum_ODUMMY;
265   END structure;
266
```