
Module : 'half_adder'

Input files:

ABEL PLA file : half_adder.tt3
Device library : P22V10GC.dev

Output files:

Report file : half_adder.rpt
Programmer load file : half_adder.jed



P22V10GC Programmed Logic:

```
sum  = ( !a & b
        #  a & !b );

carry_out  = ( a & b );
```



P22V10GC Chip Diagram: (PLCC package)

P22V10GC

```

      c
      a
      r
      r
      y
      -
    s o
    u u
  b a   m t
/-----
```

/	4	3	2	1	28	27	26	
	5				25			
	6				24			
	7				23			
	8				22			
	9				21			
	10				20			
	11				19			
	12	13	14	15	16	17	18	

SIGNATURE: N/A



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P22V10GC Chip Diagram: (SSOP package)

P22V10GC

	1	28		Vcc
	2	27		sum
a	3	26		carry_out
b	4	25		
	5	24		
	6	23		
	7	22		
	8	21		
	9	20		
	10	19		
	11	18		
	12	17		
	13	16		



SIGNATURE: N/A



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P22V10GC Resource Allocations:

Device Resources	Resource Available	Design Requirement	Unused
Input Pins:			
Input:	12	2	10 (83 %)
Output Pins:			
In/Out:	10	2	8 (80 %)
Output:	-	-	-
Buried Nodes:			
Input Reg:	-	-	-
Pin Reg:	10	0	10 (100 %)
Buried Reg:	-	-	-



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P22V10GC Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
sum	27	2	8	6
carry_out	26	1	10	9

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
a	3	INPUT
b	4	INPUT



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P22V10GC Unused Resources:

Pin Number	Pin Type	Product Terms	Flip-flop Type
5	INPUT	-	-
6	INPUT	-	-
7	INPUT	-	-
9	INPUT	-	-
10	INPUT	-	-
11	INPUT	-	-
12	INPUT	-	-
13	INPUT	-	-
16	INPUT	-	-
17	BIDIR	NORMAL 8	D
18	BIDIR	NORMAL 10	D
19	BIDIR	NORMAL 12	D
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D
24	BIDIR	NORMAL 14	D
25	BIDIR	NORMAL 12	D