File: X:\ESE382-Lab\Lab8\prelab8\prelab8\src\d_structural.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : d_structural
4   -- Design      : prelab8
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : X:\ESE382-Lab\Lab8\prelab8\prelab8\src\d_latch.vhd
11  -- Generated   : Mon Mar 25 21:59:07 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ------------------------------------------------------------------------
    ----
20
21  ----- d latch -------
22  library ieee;
23  use ieee.std_logic_1164.all;
24
25
26  entity d_latch is
27      port(
28      d : in std_logic;       -- data input
29      le_bar : in std_logic;  -- latch enable input
30      ql  : out std_logic     --latch output
31      );
32  end d_latch;
33
34
35  architecture behavioral of d_latch is
36  begin
37      latch: process (d, le_bar)
38      begin
39          if le_bar = '0' then
40              ql <= d;    -- updates the output to the value of data(input)
41          end if;
42      end process;
43
44  end behavioral;
45
46  -------- flip flop ----
47  library ieee;
48  use ieee.std_logic_1164.all;
49
50
51
52  entity d_flip_flop is
53      port(
```

```
54          d : in std_logic;
55          clk : in std_logic;
56          qff : out std_logic
57      );
58  end d_flip_flop;
59
60
61  architecture behavioral of d_flip_flop is
62  begin
63      flipflop: process (clk)
64      begin
65          if clk'event and clk = '1' then
66              qff <= d;
67          end if;
68      end process;
69
70  end behavioral;
71
72  ------- top level entity -----
73  library ieee;
74  use ieee.std_logic_1164.all;
75  use work.all;
76
77  entity latch_vs_flip_flop is
78    port (
79      d   : in  std_logic;  -- data input
80      clk : in  std_logic;  -- clock input
81      ql  : out std_logic;  -- latch output
82      qff : out std_logic   -- flip-flop output
83    );
84  end latch_vs_flip_flop;
85
86  architecture structural of latch_vs_flip_flop is
87  begin
88      u1 : entity d_latch port map (d => d, le_bar => clk, ql => ql);
89      u2 : entity d_flip_flop port map (d => d, clk => clk, qff => qff);
90  end structural;
91
92
93
94
```