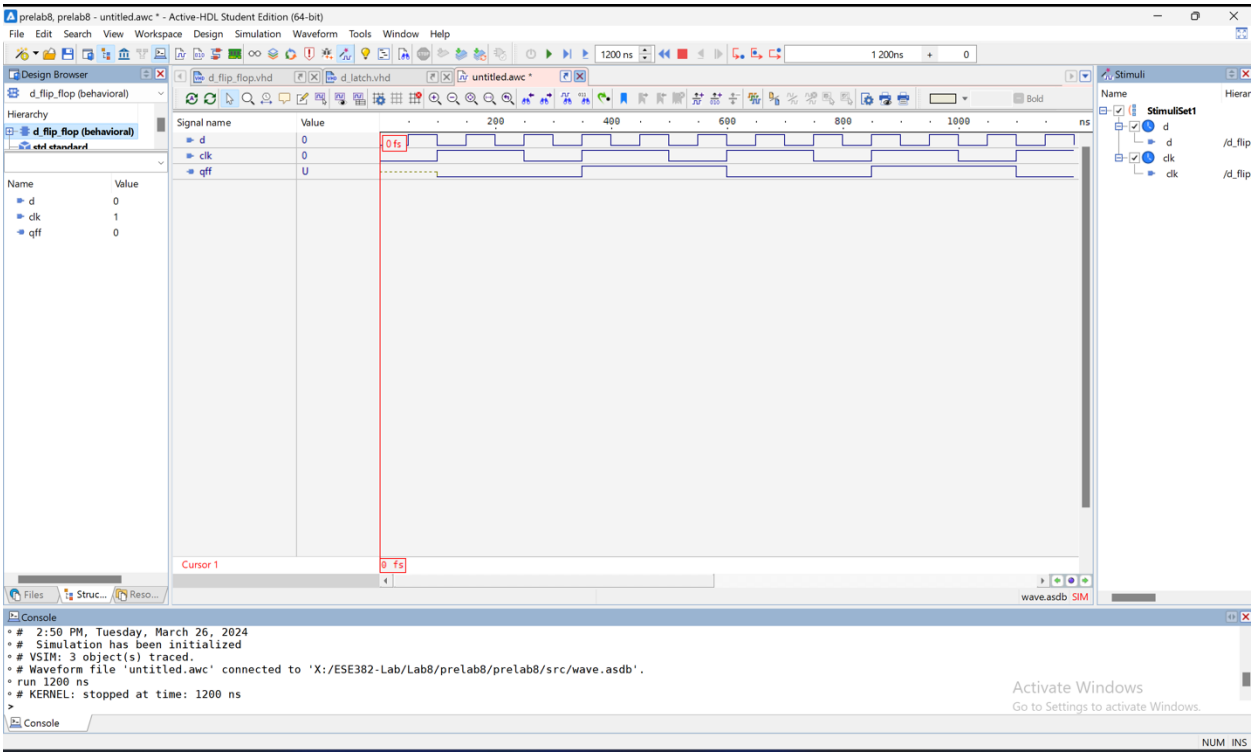
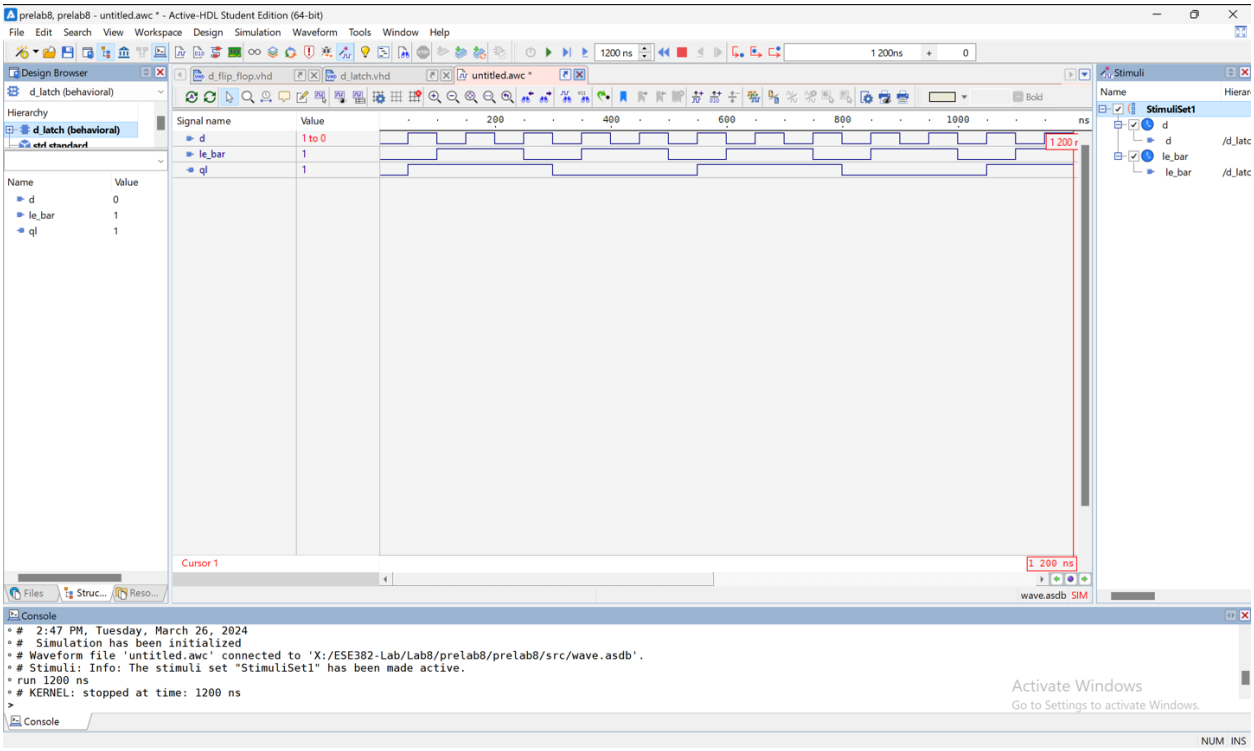
Design task 1

D-flip-flop waveform



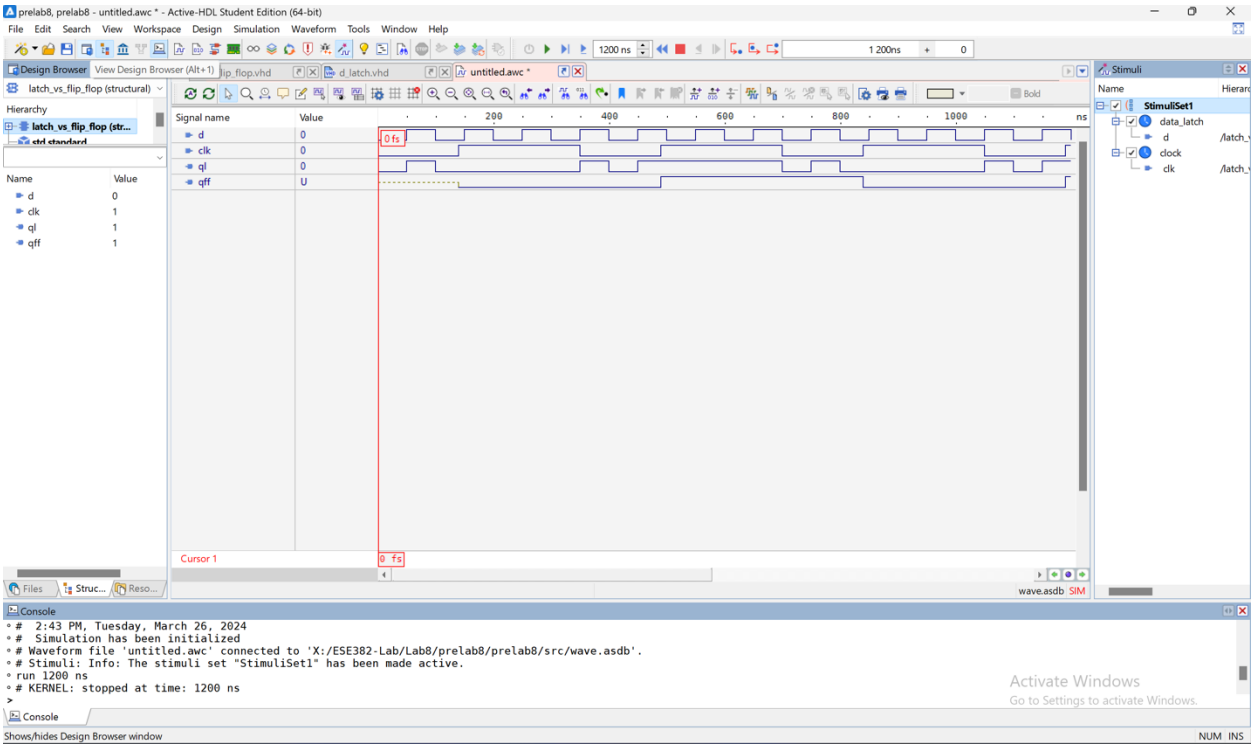
Qff copy d at rising clock edge.

D-latch waveform



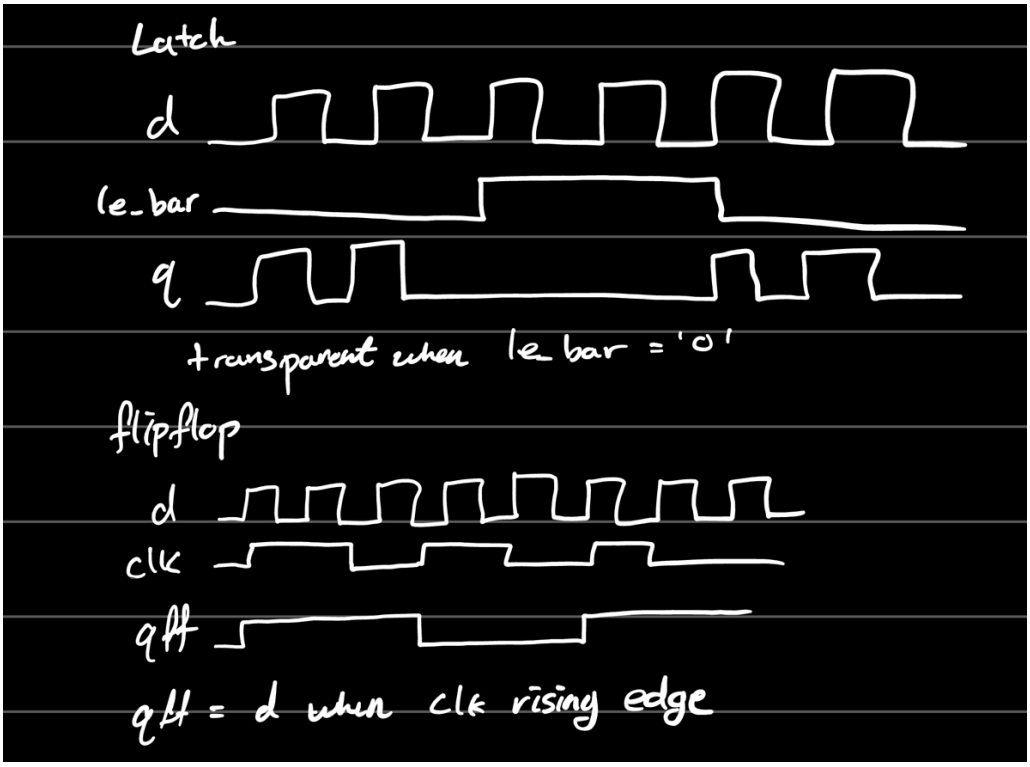
Ql copy d when le_bar = ‘0’.

Latch vs. flipflop waveform



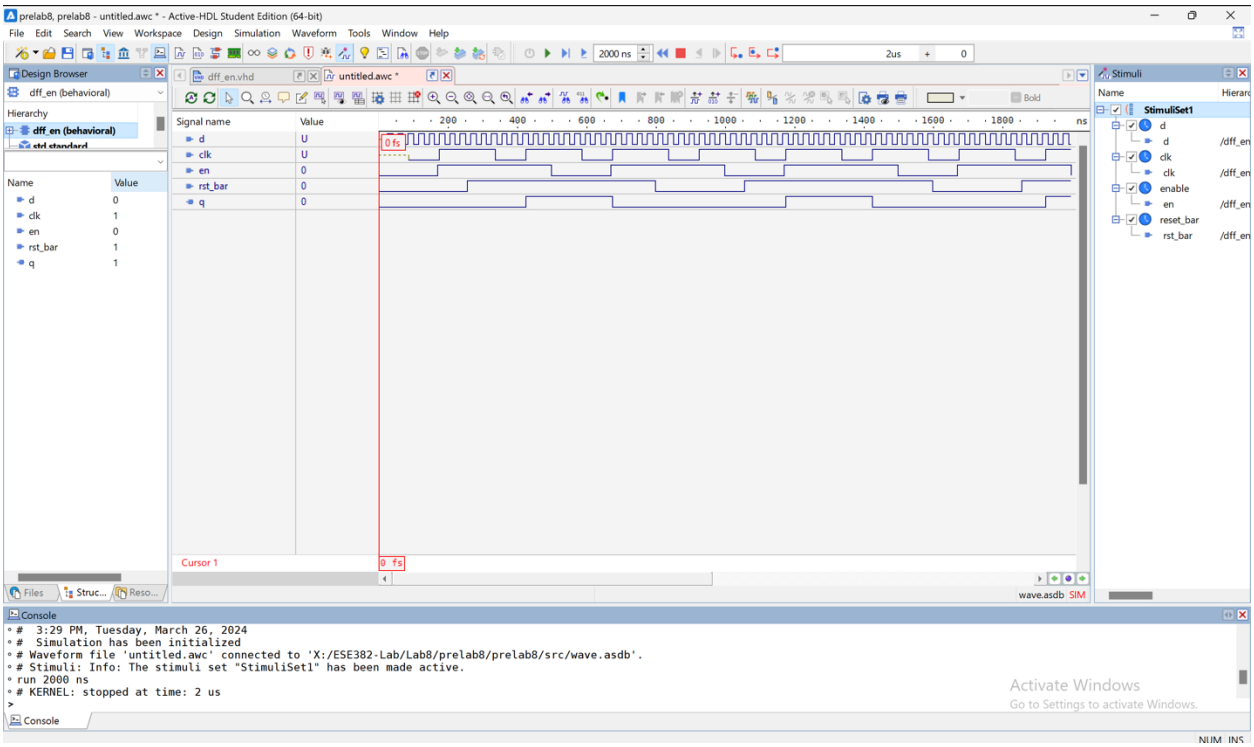
Qff copy d when rising clock edge and ql copy d when clock = ‘0’.

Sketch of the verification waveform



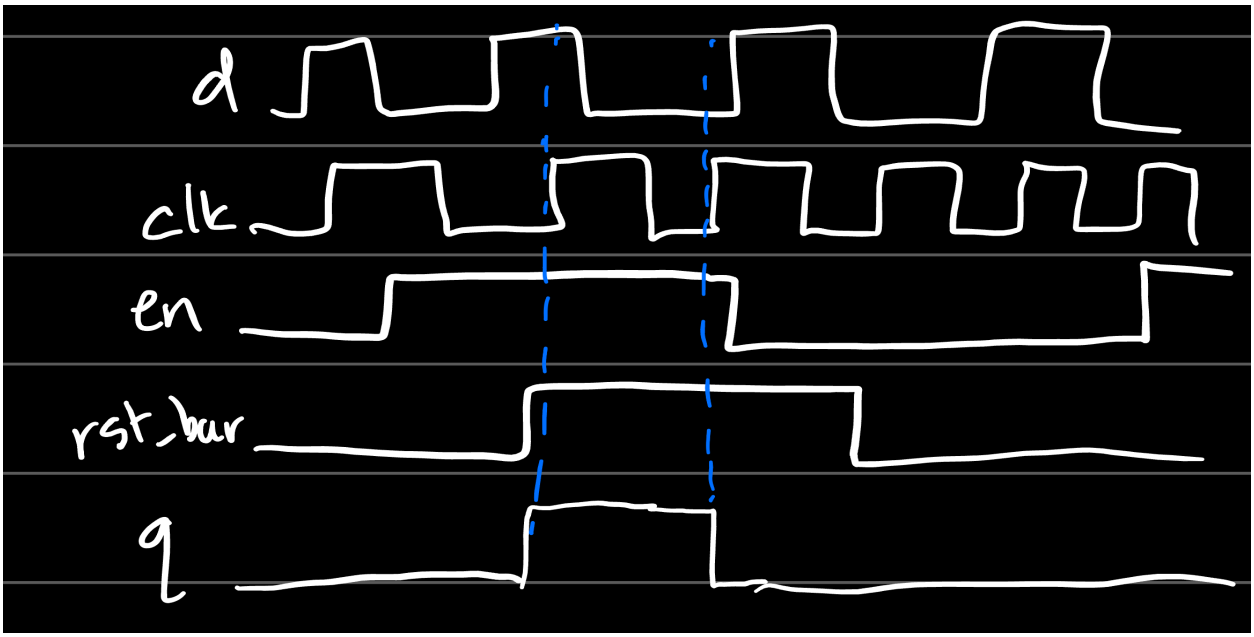
Design task 2

waveform



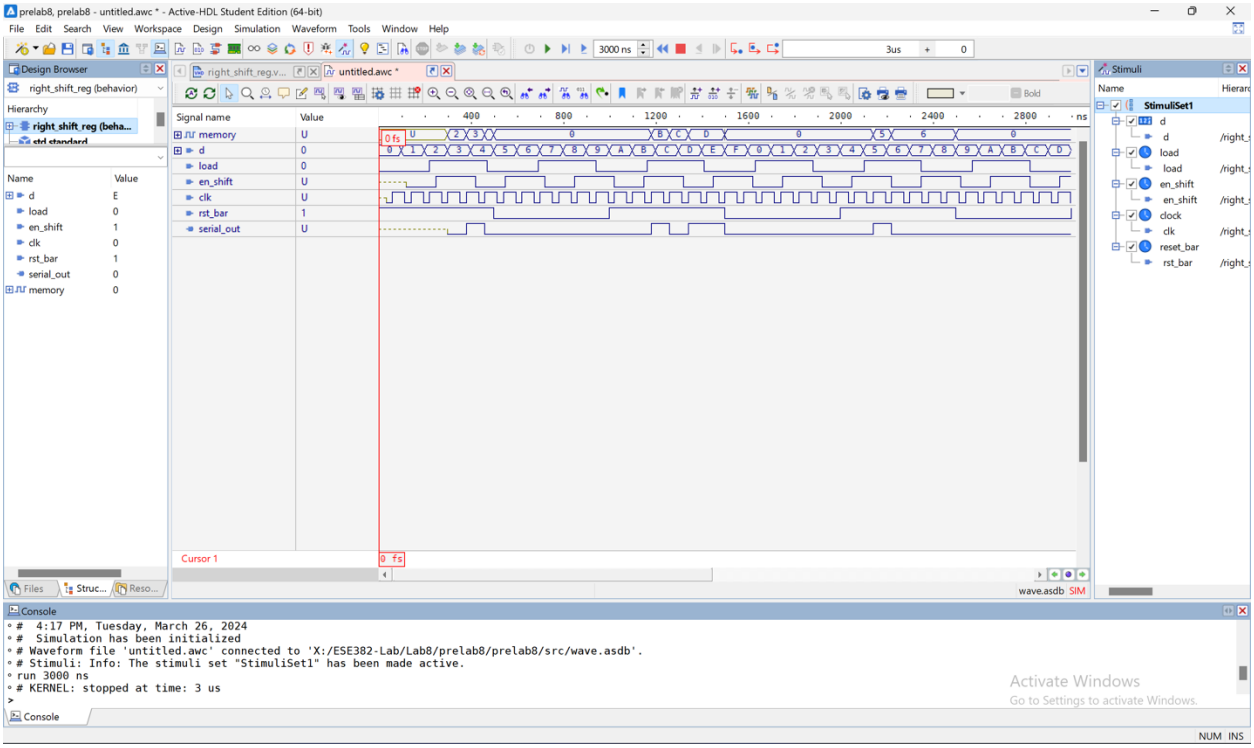
When en = ‘1’ and rst_bar = ‘1’ q copy d when rising clock edge.

Sketch of the verification waveform



Design task 3

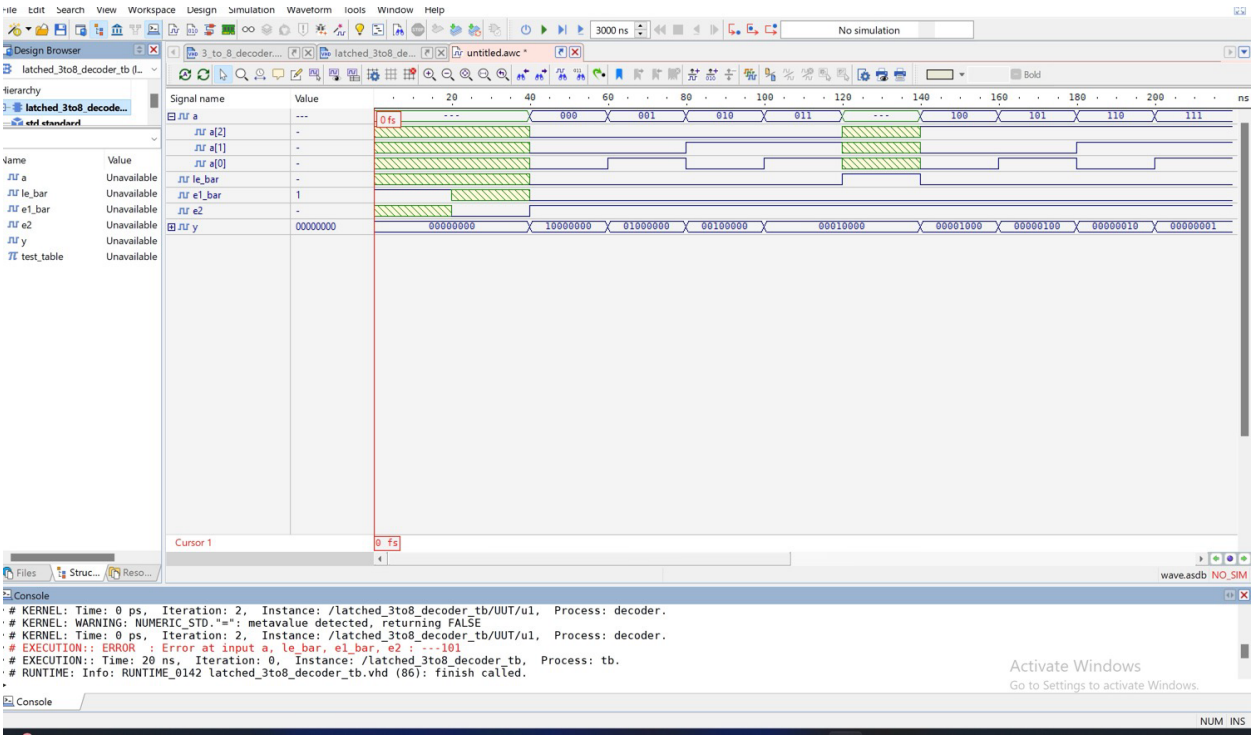
Waveform



Rst_bar is the only asynchronous input. When rst_bar = ‘0’ all the bits of the shift register are 0s. The output loads four bits of input on a rising clock edge when load = ‘1’.

Design task4

Waveform



When either e1_bar = ‘1’ and e2 = ‘0’ , the output must be all 0s. When le_bar = ‘0’ e1_bar = ‘0’ and e2 = ‘1’ then the output y is as expected on the truth table. When le_bar = ‘1’, the output stays the same (as it is shown for y = “00010000”.