```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : control_route_mux
4   -- Design      :
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11  -- Generated   : 2024-03-04  15:00:00
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description : using structual style
18  ----------------------------------------------------------------------------
    ----
19  library ieee;
20  use ieee.std_logic_1164.all;
21
22  entity route is
23      port(
24          a : in std_logic;
25          ae : in std_logic;
26          b : in std_logic;
27          be : in std_logic;
28          y : out std_logic
29      );
30
31  end route;
32
33  architecture bool of route is
34  begin
35      y <= not ((a and ae) or (b and be));
36  end bool;
37
38
39  library ieee;
40  use ieee.std_logic_1164.all;
41
42  entity control is
43      port(
44          gn, an : in std_logic;
45          c0, c1 : out std_logic
46      );
47  end control;
48
49  architecture csop of control is
50  begin
51      c0 <= not gn and not an;
52      c1 <= not gn and an;
53  end csop;
```

```
54
55
56  library ieee;
57  use ieee.std_logic_1164.all;
58  use work.all;
59
60  entity data_selector is
61    port(
62      a1, b1, a2, b2, gn, an : in std_logic;
63      y1, y2 : out std_logic
64    );
65      attribute loc : string;
66      attribute loc of gn : signal is "P3";
67      attribute loc of an : signal is "P4";
68      attribute loc of a2 : signal is "P14";
69      attribute loc of a1 : signal is "P15";
70      attribute loc of b2 : signal is "P16";
71      attribute loc of b1 : signal is "P17";
72      attribute loc of y2 : signal is "P43";
73      attribute loc of y1 : signal is "P42";
74  end data_selector;
75
76  architecture structural of data_selector is
77    signal s1, s2 : std_logic;
78  begin
79    u1: entity control port map (gn => gn, an => an, c0 => s1, c1 => s2);
80    u2: entity route port map (a => a1, ae => s1, b => b1, be => s2, y => y1
    );
81    u3: entity route port map (a => a2, ae => s1, b => b2, be => s2, y => y2
    );
82  end structural;
83
```