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2  --
3  -- Title       : xs3_to_BCD_case
4  -- Design      : xe3_to_BCD_case
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  -----
9  --
10 -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11 -- Generated   : Sun Feb 25 18:09:46 2024
12 -- From        : interface description file
13 -- By          : Itf2Vhdl ver. 1.22
14 --
15 -----
16 --
17 -- Description : converts a 4-bit Excess-3 (XS-3) input (p, q, r, s) to its
18 --               corresponding Binary-Coded Decimal (BCD) output (d, c, b, a) using a case
19 --               statement for the mapping.
20 --
21 -----
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 entity converter_xs3_bcd is
26     port ( p,q,r,s : in  std_logic;
27           d,c,b,a : out std_logic
28     );
29 end entity converter_xs3_bcd;
30
31 architecture xs3_bcd_case of converter_xs3_bcd is
32     signal temp : std_logic_vector(3 downto 0);
33
34 begin
35     (d,c,b,a) <= temp;
36     case : process (p,q,r,s)
37     begin
38         case std_logic_vector'(p,q,r,s) is
39             when "0011" => temp <= "0000";
40             when "0100" => temp <= "0001";
41             when "0101" => temp <= "0010";
42             when "0110" => temp <= "0011";
43             when "0111" => temp <= "0100";
44             when "1000" => temp <= "0101";
45             when "1001" => temp <= "0110";
46             when "1010" => temp <= "0111";
47             when "1011" => temp <= "1000";
48             when "1100" => temp <= "1001";
49             when others => temp <= "----";
50
51         end case;
52     end process;
53

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52  end architecture xs3_bcd_case;
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