Dongyun Lee

ID: 112794190

Lab1: VHDL/PLD Flow – Compilation and Functional Simulation

ESE382-L01

Bench #4

Questions

1. What is a design entity?

A design entity is a basic hardware module in VHDL that includes entity declaration and architecture body. It has a well defined set of inputs and outputs and a behavior.

2. What is the purpose of an entity declaration?

The purpose of an entity declaration is declaring the system's interface. Basically, it is creating the big structure of the system such as declaring the inputs and outputs.

3. What is the purpose of an architecture body?

The purpose of an architecture body is where you write a code that describes system function or its structure. This part is where the function of the system is implemented in.

4. List the name of each design entity in the file `half_adder.vhd`. Also give the names of the inputs and outputs declared in each entity declaration.

The name of design entity is "half_adder." The name of inputs are "a" and "b". The name of outputs are "sum" and "carry_out".

5. What is the purpose of a functional simulation?

The purpose of a functional simulation is you can observe the signals in waveforms and the truth table that connect the half-adder (in this lab) to the testbench.

File: F:/ESE382-Lab/Lab1/Lab01_half_adder/Lab01_half_adder/src/half_adder.vhd (/testbench/uu

```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : half_adder
4   -- Design      : Lab01_half_adder
5   -- Author      : ESDL User
6   -- Company     : Stony Brook
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        :
    F:\ESE382-Lab\Lab1\Lab01_half_adder\Lab01_half_adder\src\half_adder.vhd
11  -- Generated   : Wed Jan 31 09:02:10 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  --{{ Section below this comment is automatically maintained
22  --   and may be overwritten
23  --{entity {half_adder} architecture {dataflow}}
24
25  library IEEE;
26  use IEEE.std_logic_1164.all;
27
28  entity half_adder is
29       port(
30           a : in STD_LOGIC;
31           b : in STD_LOGIC;
32           carry_out : out STD_LOGIC;
33           sum : out STD_LOGIC
34           );
35  end half_adder;
36
37  --}} End of automatically maintained section
38
39  architecture dataflow of half_adder is
40  begin
41
42      sum <= (not a and b) or (a and not b);
43      carry_out <= a and b;
44
45  end dataflow;
46
```