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Lab4: Dataflow Style Combinational Design Using  
Table Lookup – XS3 to BCD Code Converter

ESE382-L01

Bench #4

**xs3\_to\_BCD\_selected.vhd**

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity xs3_to_BCD_selected is
5      port (
6          p, q, r, s : in std_logic;
7          d, c, b, a : out std_logic
8      );
9  end entity xs3_to_BCD_selected;
10
11 architecture selected of xs3_to_BCD_selected is
12     signal temp : std_logic_vector(3 downto 0);
13 begin
14
15     (b, c, d, a) <= temp;
16
17     with std_logic_vector'(p, q, r, s) select
18         temp <= "0000" when "0011",
19                 "0001" when "0100",
20                 "0010" when "0101",
21                 "0011" when "0110",
22                 "0100" when "0111",
23                 "0101" when "1000",
24                 "0110" when "1001",
25                 "0111" when "1010",
26                 "1000" when "1011",
27                 "1001" when "1100",
28                 "____" when others;
29
30     -- with std_logic_vector'(p, q, r, s) select
31     --     d <= '0' when "0011" | "0100" | "0101" | "0110" | "0111" | "1000" | "
1001" | "1010",
32     --         '1' when "1011" | "1100",
33     --         '-' when others;
34
35     -- with std_logic_vector'(p, q, r, s) select
36     --     c <= '0' when "0011" | "0100" | "0101" | "0110" | "1011" | "1100",
37     --         '1' when "0111" | "1000" | "1001" | "1010",
38     --         '-' when others;
39
40     -- with std_logic_vector'(p, q, r, s) select
41     --     b <= '0' when "0011" | "0100" | "0111" | "1000" | "1011" | "1100",
42     --         '1' when "0101" | "0110" | "1001" | "1010",
43     --         '-' when others;
44
45     -- with std_logic_vector'(p, q, r, s) select
46     --     a <= '0' when "0011" | "0101" | "0111" | "1001" | "1011",
47     --         '1' when "0100" | "0110" | "1000" | "1010" | "1100",
48     --         '-' when others;
49
50
51 end architecture selected;
```

## xs3\_to\_BCD\_conditional.vhd

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity xs3_to_BCD_conditional is
5      port (
6          p, q, r, s : in std_logic;
7          d, c, b, a : out std_logic
8      );
9  end entity xs3_to_BCD_conditional;
10
11 architecture conditional of xs3_to_BCD_conditional is
12 begin
13     d <= '1' when p = '1' and q = '0' and r = '1' and s = '1' else
14         '1' when p = '1' and q = '1' and r = '0' and s = '0' else
15         '-' when (p = '0' and q = '0' and r = '0' and s = '0') or
16             (p = '0' and q = '0' and r = '0' and s = '1') or
17             (p = '0' and q = '0' and r = '1' and s = '0') or
18             (p = '1' and q = '1' and r = '0' and s = '1') or
19             (p = '1' and q = '1' and r = '1' and s = '0') or
20             (p = '1' and q = '1' and r = '1' and s = '1') else
21         '0';
22
23     c <= '1' when p = '0' and q = '1' and r = '1' and s = '1' else
24         '1' when p = '1' and q = '0' and r = '0' and s = '0' else
25         '1' when p = '1' and q = '0' and r = '0' and s = '1' else
26         '1' when p = '1' and q = '0' and r = '1' and s = '0' else
27         '-' when (p = '0' and q = '0' and r = '0' and s = '0') or
28             (p = '0' and q = '0' and r = '0' and s = '1') or
29             (p = '0' and q = '0' and r = '1' and s = '0') or
30             (p = '1' and q = '1' and r = '0' and s = '1') or
31             (p = '1' and q = '1' and r = '1' and s = '0') or
32             (p = '1' and q = '1' and r = '1' and s = '1') else
33         '0';
34
35     b <= '1' when p = '0' and q = '1' and r = '0' and s = '1' else
36         '1' when p = '0' and q = '1' and r = '1' and s = '0' else
37         '1' when p = '1' and q = '0' and r = '0' and s = '1' else
38         '1' when p = '1' and q = '0' and r = '1' and s = '0' else
39         '-' when (p = '0' and q = '0' and r = '0' and s = '0') or
40             (p = '0' and q = '0' and r = '0' and s = '1') or
41             (p = '0' and q = '0' and r = '1' and s = '0') or
42             (p = '1' and q = '1' and r = '0' and s = '1') or
43             (p = '1' and q = '1' and r = '1' and s = '0') or
44             (p = '1' and q = '1' and r = '1' and s = '1') else
45         '0';
46
47     a <= '1' when p = '0' and q = '1' and r = '0' and s = '0' else
48         '1' when p = '0' and q = '1' and r = '1' and s = '0' else
49         '1' when p = '1' and q = '0' and r = '0' and s = '0' else
50         '1' when p = '1' and q = '0' and r = '1' and s = '0' else
51         '1' when p = '1' and q = '1' and r = '0' and s = '0' else
52         '-' when (p = '0' and q = '0' and r = '0' and s = '0') or
53             (p = '0' and q = '0' and r = '0' and s = '1') or
54             (p = '0' and q = '0' and r = '1' and s = '0') or
55             (p = '1' and q = '1' and r = '0' and s = '1') or
56             (p = '1' and q = '1' and r = '1' and s = '0') or
57             (p = '1' and q = '1' and r = '1' and s = '1') else

```

```
58 |         '0';  
59 |     end architecture conditional;
```

**xs3\_to\_BCD\_LUT.vhd**

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4
5  entity xs3_to_BCD_LUT is
6      port( p, q, r, s : in std_logic;
7            d, c, b, a : out std_logic);
8  end entity xs3_to_BCD_LUT;
9
10 architecture table_lookup of xs3_to_BCD_LUT is
11
12     subtype LUT_out is std_logic_vector(3 downto 0);
13
14     type truth_table is array (0 to 15) of std_logic_vector(3 downto 0);
15
16     constant xs3_to_BCD_LUT_out : truth_table := (
17         "----", "----", "----", "0000",
18         "0001", "0010", "0011", "0100",
19         "0101", "0110", "0111", "1000",
20         "1001", "----", "----", "----"
21     );
22
23 begin
24
25     d <= xs3_to_BCD_LUT_out(to_integer(unsigned'(p, q, r, s)))(0);
26     c <= xs3_to_BCD_LUT_out(to_integer(unsigned'(p, q, r, s)))(1);
27     b <= xs3_to_BCD_LUT_out(to_integer(unsigned'(p, q, r, s)))(2);
28     a <= xs3_to_BCD_LUT_out(to_integer(unsigned'(p, q, r, s)))(3);
29
30 end architecture table_lookup;
```