Dongyun Lee

ID: 112794190

PreLab3: Dataflow Style Combinational Design – XS3 to BCD Code Converter

ESE382-L01

Bench #4

Task1

xs3_to_BCD_CSOP.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;

entity converter_xs3_bcd_selected is
    port(
        p, q, r, s : in std_logic;
        d, c, b, a : out std_logic
    );
end converter_xs3_bcd_selected;



architecture CSOP of converter_xs3_bcd_selected is
begin
-- CSOP

    process(p, q, r, s)
    begin
        if (p = '1' and q = '0' and r = '1' and s = '1') or
            (p = '1' and q = '1' and r = '0' and s = '0') then
            d <= '1';
        elsif
            (p = '0' and q = '1' and r = '1' and s = '1') or
            (p = '1' and q = '0' and r = '0' and s = '0') or
            (p = '1' and q = '0' and r = '0' and s = '1') or
            (p = '1' and q = '0' and r = '1' and s = '0') then
            c <= '1';
        elsif
            (p = '0' and q = '1' and r = '0' and s = '1') or
            (p = '0' and q = '1' and r = '1' and s = '0') or
            (p = '1' and q = '0' and r = '0' and s = '1') or
            (p = '1' and q = '0' and r = '1' and s = '1') then
            b <= '1';
        elsif
            (p = '0' and q = '1' and r = '0' and s = '0') or
            (p = '0' and q = '1' and r = '1' and s = '0') or
            (p = '1' and q = '0' and r = '0' and s = '0') or
            (p = '1' and q = '0' and r = '1' and s = '0') or
            (p = '1' and q = '1' and r = '0' and s = '0') then
            a <= '1';
        else
            d <= 'Z';
            c <= 'Z';
            b <= 'Z';
            a <= 'Z';
        end if;

    end process;

end csop;

```

Task2

xs3_to_BCD_CPOS.vhd

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity converter_xs3_bcd_cpos is
5      port(
6          p, q, r, s : in std_logic;
7          d, c, b, a : out std_logic
8      );
9  end converter_xs3_bcd_cpos;
10
11 -- CPOS
12
13 architecture CPOS of converter_xs3_bcd_cpos is
14 begin
15 -- CPOS
16
17     -- Output d
18     d <= (p or q or not r or not s) and (p or not q or r or s) and (p or not q or r
   or not s) and
19          (p or not q or not r or s) and (p or not q or not r or not s) and (not p
   or q or r or s) and
20          (not p or q or r or not s) and (not p or q or not r or s);
21
22     -- Output c
23     c <= (p or q or not r or not s) and (p or not q or r or s) and (p or not q or r
   or not s) and
24          (p or not q or not r or s) and (not p or q or not r or not s) and (not p
   or q or not r or not s) and
25          (not p or not q or r or s);
26
27     -- Output b
28     b <= (p or q or not r or not s) and (p or not q or r or s) and (p or not q or
   not r or not s) and
29          (not p or q or r or s) and (not p or q or not r or not s) and (not p or
   not q or r or s);
30
31     -- Output a
32     a <= (p or q or not r or not s) and (p or not q or r or not s) and (p or not q
   or not r or not s) and
33          (not p or q or r or not s) and (not p or q or not r or not s);
34
35 end cpos;
36
```