File: F:/ESE382-Lab/Lab1/Lab01_half_adder/Lab01_half_adder/src/half_adder.vhd (/testbench/uu

```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : half_adder
4   -- Design      : Lab01_half_adder
5   -- Author      : ESDL User
6   -- Company     : Stony Brook
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        :
    F:\ESE382-Lab\Lab1\Lab01_half_adder\Lab01_half_adder\src\half_adder.vhd
11  -- Generated   : Wed Jan 31 09:02:10 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  --{{ Section below this comment is automatically maintained
22  --   and may be overwritten
23  --{entity {half_adder} architecture {dataflow}}
24
25  library IEEE;
26  use IEEE.std_logic_1164.all;
27
28  entity half_adder is
29       port(
30           a : in STD_LOGIC;
31           b : in STD_LOGIC;
32           carry_out : out STD_LOGIC;
33           sum : out STD_LOGIC
34           );
35  end half_adder;
36
37  --}} End of automatically maintained section
38
39  architecture dataflow of half_adder is
40  begin
41
42      sum <= (not a and b) or (a and not b);
43      carry_out <= a and b;
44
45  end dataflow;
46
```