File: X:\ESE382-Lab\Lab5\converter_xs3_to_BCD\xs3_to_BCD_case\src\xs3_bcd_loop.vhd (/conv

```
1   ----------------------------------------------------------------------------
    -------
2   --
3   -- Title       : xs3_to_BCD_loop
4   -- Design      : xe3_to_BCD_loop
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    -------
9   --
10  -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11  -- Generated   : Sun Feb 25 18:09:46 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    -------
16  --
17  -- Description : converts a 4-bit Excess-3 (XS-3) input (p, q, r, s) to
    its corresponding Binary-Coded Decimal (BCD) output (d, c, b, a) using
    looping.
18  --               using vectors instead of scalars.
19  --                  no don't cares
20  ----------------------------------------------------------------------------
    -------
21  library IEEE;
22  use IEEE.STD_LOGIC_1164.ALL;
23  use ieee.numeric_std.all;
24
25  entity converter_xs3_bcd is
26      port ( pqrs : in  std_logic_vector(3 downto 0);
27             dcba : out  std_logic_vector(3 downto 0)
28      );
29  end entity converter_xs3_bcd;
30
31  architecture xs3_bcd_loop of converter_xs3_bcd is
32  begin
33      comp: process (pqrs)
34
35      variable bcd_var : std_logic_vector(3 downto 0);
36      begin
37          bcd_var := "0000";  -- default value
38
39          for i in 0 to 9 loop
40              if unsigned(pqrs) = to_unsigned(i + 3, 4) then -- if i + 3 =
    pqrs then assgin to bcd_var
41                  bcd_var := std_logic_vector(to_unsigned(i, 4));
42                  exit;
43              end if;
44          end loop;
45
46          dcba <= bcd_var;
47      end process;
48
49  end architecture xs3_bcd_loop;
```