

1. For a Boolean function that has a smaller number of input combinations where its output is 0 than it does where its output is 1, why would it be better to write a CSOP expression for the input combinations where the output is 0 and then complement that expression or write a CPOS expression for the function than write a CSOP expression for the input combinations where the output is 1?

It would be better to write a CSOP expression when there are more number of output '0's than '1's because it makes the expression more simple and short. It depends on '0's or '1's on the output.

2. Compare the HDL Analyst hierarchical views of your four designs. Are the diagrams identical? If not, how do they differ? Are they functionally the same? If not, how do they differ functionally?

They are functionally the same. However the diagrams are not perfectly identical. This is because one is in CSOP form and the other one is in CPOS form. The implementations of AND gates and OR gates would be different. However, they functions the same.

3. Compare the pre-fit equations and post-fit equations from ispLEVER Classic for the four designs. Are the equations the same? If not, how do they differ?

Both pre-fit equations and post-fit equations are showing the same information. However, pre-fit equation focus more on the logic gates and post-fit equation shows more the actual gates and integrated circuit inside. Therefore, pre-fit equation represents logical design and post-fit equation represents how the design is mapped into an actual PLD.

Notes

a. In the pre-fit and post-fit equations the # symbol represents OR, the & symbol represents AND, and the ! symbol represents NOT.

b. The pre-fit and post-fit equations listings give equations for both the normal and complement of each function. This is done because it is sometimes easier (requires fewer product terms) to implement the complement of a function and then configure the PLD to complement the output of the OR gate creating the desired function than it is to implement the normal form of the function.

4. From the ispLEVER Classic chip report how much of the isp22V10's resources (inputs, outputs, gates, flip-flops) were used for the decoder design?

The ispLEVER Classic chip report represents 4 inputs, 4 outputs, 12 product terms used, no flip-flops are used.

5. From the chip report determine exactly which equations were actually implemented in the PLD.

The equation shown in chip report is in CSOP form and it is post-fit equation. The program has optimized the equation from VHDL code to make it fit to the PLD.

6. Explain the differences in the output values when input combinations that are not valid XS3 codes are applied to your four designs. What determined these output values for each of your designs? If the system providing inputs to your design generates only valid XS3 codes, does each of your designs meet the design requirements? answer these question based on the lab instruction. conditional signal and selected signal are not done. so avoid those two when answering the questions

There are not big differences between CSOP form and CPOS form. However, using the selected signal or conditional signal, it would be different because the code can implement 'don't cares.' The logic expressions that I have written in VHDL determines the output. Also, the synthesis program might optimize the expressions. If I wanted the design to be only valid on XS3 code then the design has met the requirements. From the hardware test, I have observe that it converts from XS3. To BCD.