

```
1  -----
2  --
3  -- Title       : two_level_gate
4  -- Design      : two_level_gate_circuit
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  -----
9  --
10 -- File        :
11 X:\ESE382-Lab\Lab7\lab7\two_level_gate_circuit\src\two_level_gate.vhd
12 -- Generated   : Thu Mar 14 15:45:52 2024
13 -- From        : interface description file
14 -- By          : Itf2Vhdl ver. 1.22
15 -----
16 --
17 -- Description :two level gate using two process
18 --
19 -----
20
21 library ieee;
22 use ieee.std_logic_1164.all;
23
24
25
26 entity two_level_gate is
27     port(
28         a, b, c: in std_logic;
29         f : out std_logic
30     );
31 end two_level_gate;
32
33 --}} End of automatically maintained section
34
35 architecture behavioral of two_level_gate is
36     signal s1 : std_logic;
37 begin
38     u0 : process(a, b)
39     begin
40         s1 <= a and b;
41     end process u0;
42
43     u1 : process(s1, c)
44     begin
45         f <= s1 or c;
46     end process u1;
47
48
49
50 end behavioral;
51
```