File: F:/ESE382-Lab/Lab8/lab8/left_shift_reg/src/latched_3to8_decoder_tb.vhd

```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : latched_3to8_decoder_tb
4   -- Design      : prelab8
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : Z:\Desktop\SBU 2024 Spring\ESE
    382\lab-backup\Lab8\prelab8\prelab8\src\latched_3to8_decoder_tb.vhd
11  -- Generated   : Sat Mar 30 16:39:02 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description : testbench for latched 3 to 8 decoder
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26  entity latched_3to8_decoder_tb is
27  end latched_3to8_decoder_tb;
28
29
30  architecture latched_3to8_decoder_tb of latched_3to8_decoder_tb is
31     signal a      : std_logic_vector(2 downto 0);
32     signal le_bar : std_logic;
33     signal e1_bar : std_logic;
34     signal e2     : std_logic;
35     signal y      : std_logic_vector(0 to 7);
36
37  type test_vector is record
38      le_bar : std_logic;
39      e1_bar : std_logic;
40      e2     : std_logic;
41      a      : std_logic_vector(2 downto 0);
42      y      : std_logic_vector(0 to 7);
43  end record;
44
45  type test_vectors is array (natural range <>) of test_vector;
46
47  constant test_table : test_vectors := (
48    -- el_   e1_  e2     a       y
49      ( '-', '1', '-', "---", "00000000"), -- When E1 is low, all outputs are
    low
50      ( '-', '-', '0', "---", "00000000"), -- When E2 is low, all outputs are
    low
```

```
51      -- Latch enabled and E1 is low, decoder is active
52      ( '0', '0', '1', "000", "10000000"), -- Input A is 0, Y0 is high
53      ( '0', '0', '1', "001", "01000000"), -- Input A is 1, Y1 is high
54      ( '0', '0', '1', "010", "00100000"), -- Input A is 2, Y2 is high
55      ( '0', '0', '1', "011", "00010000"), -- Input A is 3, Y3 is high
56          ( '1', '0', '1', "---", "--------"), -- When LE is high, outputs
    are stable
57      ( '0', '0', '1', "100", "00001000"), -- Input A is 4, Y4 is high
58      ( '0', '0', '1', "101", "00000100"), -- Input A is 5, Y5 is high
59      ( '0', '0', '1', "110", "00000010"), -- Input A is 6, Y6 is high
60      ( '0', '0', '1', "111", "00000001") -- Input A is 7, Y7 is high
61  );
62
63  begin
64      UUT : entity latched_3to8_decoder port map (
65            a => a,
66            le_bar => le_bar,
67            e1_bar => e1_bar,
68            e2 => e2,
69            y => y
70            );
71      tb : process
72      variable memory : std_logic_vector(7 downto 0);
73      begin
74
75          for i in test_table'range loop
76              a <= test_table(i).a;
77              le_bar <= test_table(i).le_bar;
78              e1_bar <= test_table(i).e1_bar;
79              e2 <= test_table(i).e2;
80              wait for 20ns;
81              if le_bar = '1' and e1_bar = '0' and e2 = '1' then
82                  assert y = memory;
83                  report "Error at le_bar = '1' and e1_bar = '0' and e2 =
    '1'. Output should be stable"
84                  severity error;
85              else
86                  memory := test_table(i).y;
87                  assert y = test_table(i).y
88                  report "Error at input a, le_bar, e1_bar, e2 : " &
    to_string(a) & to_string(le_bar) & to_string(e1_bar) & to_string(e2)
89                  severity error;
90              end if;
91
92
93          end loop;
94          std.env.finish;
95      end process;
96
97
98  end latched_3to8_decoder_tb;
99
```