

## Questions

1. Why does the testbench provided use three loops for stimulus instead of just one?

This is because the first part of truth table is 3 don't cares, and the rest 10 values are actual valid values and the last 3 values are don't cares. Therefore the first and last loop is for don't cares and the second loop is the loop where it actually tests the program. We need separate loops for don't cares since the VHDL program does not know what don't cares are.

2. Compare the HDL Analyst hierarchical view of the design you synthesized for this Laboratory with the HDL Analyst hierarchical view of your design from Laboratory 03. Are the diagrams identical? If not, how do they differ? Are they functionally the same? If not, how do they differ functionally?

The diagrams are not identical because for Lab 3 I used CSOP architecture and lab 4 I used Lookup Table. While CSOP hierarchical view, I see steps of signal and AND gates are placed in a row. On the other hand, Lookup table hierarchical view I see the inverters and 4input AND gates and 10 to 4 multiplexer.

3. Compare the pre-fit equations and post-fit equations from ispLEVER Classic for the design you synthesized for this laboratory with the equations from your design for Laboratory 03. Are the equations the same? If not, how do they differ?

The pre-fit equations and post-fit equations are exactly the same. It shows a logic equation for each outputs: d, c, b, and a.

Equations:

```
d = (p & q
    # !p & !q & !r
    # p & r & s
    # !p & !q & !s);
```

```
c = (!q & !r
    # !q & !s
    # q & r & s);
```

```
b = (!r & s
```

```
# r & !s);
```

```
a = (!s);
```

4. Explain the differences in the output values when input combinations that are not valid inputs to the decoder are applied to your functional simulation and to your timing simulation. What determined these output values for each of your designs?

In the functional simulation, it marked as shaded box which indicates 'don't cares,' however, in the timing simulation, the output values where it is supposed to be 'don't cares' are assigned as random values. The random values for don't cares are for synthesizer to synthesize a simpler circuit.