File: X:\ESE382-Lab\Lab8\prelab8\prelab8\src\dff_en.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : dff_en
4   -- Design      : prelab8
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : X:\ESE382-Lab\Lab8\prelab8\prelab8\src\dff_en.vhd
11  -- Generated   : Tue Mar 26 14:56:15 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23
24  entity dff_en is
25    port (
26      d       : in  std_logic;  -- data input
27      clk     : in  std_logic;  -- clock input
28      en      : in  std_logic;  -- enable input
29      rst_bar : in  std_logic;  -- asynchronous reset
30      q       : out std_logic   -- output
31    );
32  end dff_en;
33
34  architecture behavioral of dff_en is
35  begin
36      flipflop : process (clk, rst_bar)
37      begin
38          if rst_bar = '0' then
39              q <= '0';
40          elsif rising_edge(clk) then
41              if en = '1' then
42                  q <= d;
43              end if;
44
45          end if;
46      end process;
47  end behavioral;
48
49
50
```