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Lab7: Event Driven Simulation

ESE382-L01

Bench #4

Questions for Lab7

1. Immediately after initializing a simulation, what is the value of the inputs and outputs?

Immediately after initializing a simulation, all signals are set the ‘U’ value for both inputs and output.

2. Explain what the first five lines of the simulation listing represent.

The very first line is initialization so all the signals are set to ‘U’. The second line is 0ps+1delta time which all the signals except for output f is set to value ‘0’ because the value is what testbench is giving to UUT. The third line which is 0ps + 3delta time after processing the output f. Therefore, the output f is set to value ‘0’ due to the logic in the source code. The fourth line is at the time 20000ps + 1delta time which is the first change of any signals’ value since 0ps + 3delta. Signal c value changes to ‘1’ at the time. The fifth line is the next process after 20000ps + 1delta which is change of output signal f value to ‘1’ due to changed value of signal c.

3. Is Design 2 functionally correct? Compare the simulations of Designs 1 and 2 and explain your answer.

Design to is not correct because since b is not on the sensitivity list, b is no more on the active process queue even if its value has changed. Therefore, the simulation is different from Design 1 as well. On the waveform, there is a ‘X’ value for output f during 120000ps to 140000ps because b signal has changed, however, u0 process cannot detect the event since b is not on the sensitivity list.

4. Does the timing simulation indicate that Design 3 is functionally correct? If so, explain how this is possible.

The timing simulation is functionally correct, because after enable becomes ‘1’ then the output of NAND gate will follow whatever the feedback is. However, since the feedback is coming from the output of NAND gate it will be repeating ‘1’ and ‘0’ and make it look like a square wave on the waveform.

5. Describe the results of the simulation and explain why you got these results. Pay particular attention to the Listing window contents.

The simulation shows that when enable is ‘0’ sigout is ‘1’ which is correct because for NAND gate, if one of the signal is ‘0’ then output must be ‘1’. However as soon as enable value changes to ‘1’ it stops the waveform and you can see the sigout becomes ‘0’. In the Listing window, it shows the value of output after enable value changes to ‘1’ which, as expected, output becomes continuously ‘0’ and ‘1’.

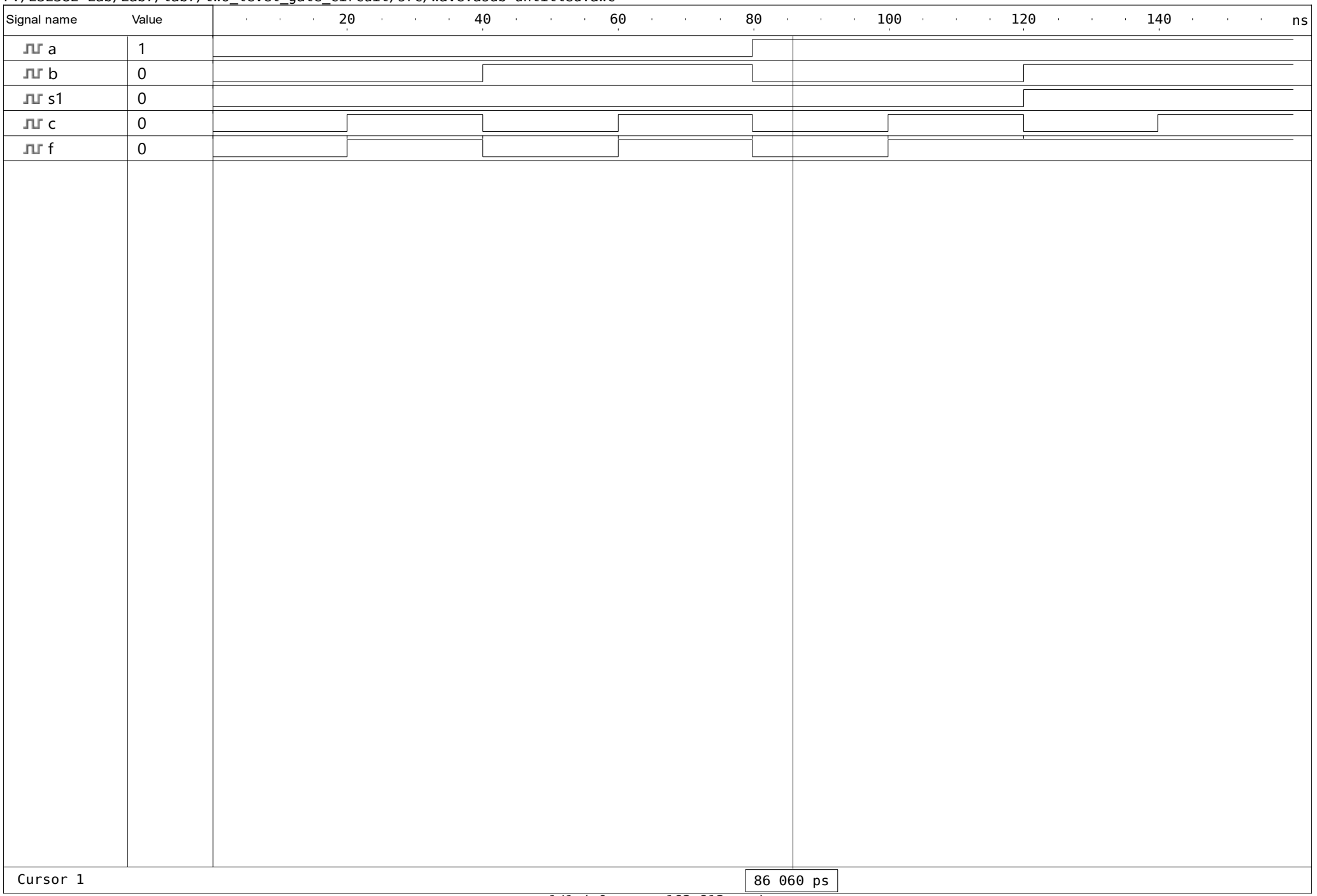
6. Describe the result of the timing simulation. Are these results different from those of the functional simulation? If so, explain why. What result would you expect from a PLD programmed with this design and why?

As I answered in the previous questions. The result of simulation looks right because after enable becomes ‘1’ the output which is sigout is following the value whatever the feedback is. Therefore, the value of output will be repeating ‘1’ and ‘0.’ Also, this result shows on the Listing window that the NAND gate is outputting ‘1’ and then ‘0’ and back to ‘1’ after enable is ‘1’. I would expect the PLD will turn on and off the LED repeatedly.

7. What are the similarities and differences between the output from the timing simulation and the output from the programmed PLD? Give an explanation for any differences.

The similarities was the it showed both waves but for the timing simulation, it was square wave and the actual output from the PLD was sine wave. This is because the actual voltage from input and output are oscillating, that is why the actual PLD output is in sine wave including noise in the feedback “wire” (even though it is not an actual wire). Therefore it shows as a sine wave in the actual PLD. On the other hand, for timing simulation, the simulation only shows logic values which in this case either ‘1’ or ‘0’. This is why the output shows in a sqaure wave in the timing simulation.

F:/ESE382-Lab/Lab7/lab7/two_level_gate_circuit/src/wave.asdb untitled.awc



1/1 (0 ps - 162 813 ps)

Time	Delta	/two_level_gate_tb/a	/two_level_gate_tb/b	/two_level_gate_tb/c	/two_level_gate_tb/s1	/two...
0 ps	0	U	U	U	U	U
0 ps	1	0	0	0	0	U
0 ps	3	0	0	0	0	0
20000 ps	1	0	0	1	0	X
20000 ps	2	0	0	1	0	1
40000 ps	1	0	1	0	0	X
40000 ps	2	0	1	0	0	0
60000 ps	1	0	1	1	0	X
60000 ps	2	0	1	1	0	1
80000 ps	1	1	0	0	0	X
80000 ps	2	1	0	0	0	0
100000 ...	1	1	0	1	0	X
100000 ...	2	1	0	1	0	1
120000 ...	1	1	1	0	1	1
120000 ...	2	1	1	0	1	X
120000 ...	3	1	1	0	1	1
140000 ...	1	1	1	1	1	1

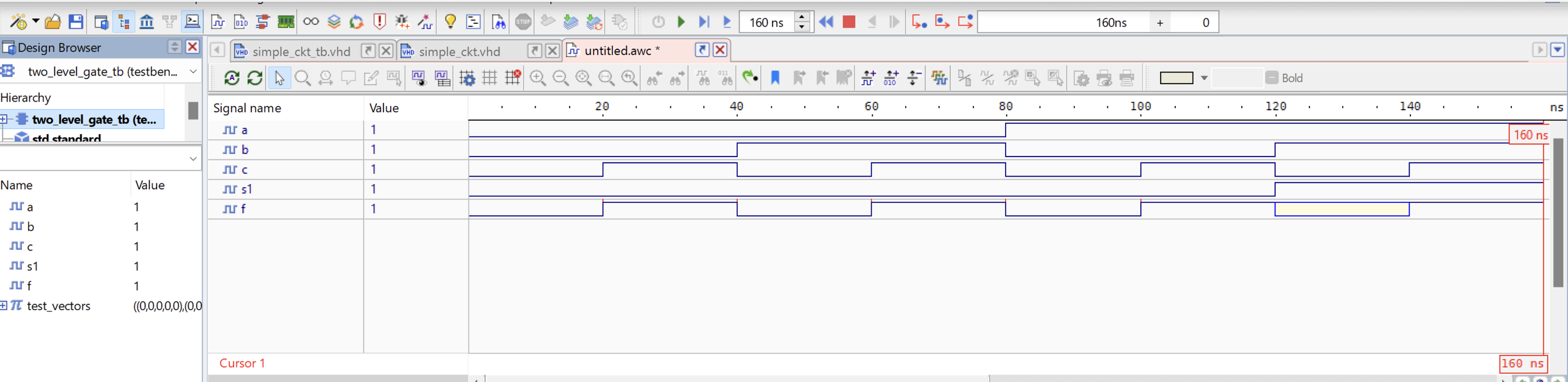
Console

```
  initialization done.
# Allocation: Simulator
  allocated 6464 kB
  (elbread=427 elab2=5897
  kernel=139 sdf=0)
# KERNEL: ASDB file was
  created in location
  F:\ESE382-Lab\Lab7\lab7\two_le
  vel_gate_circuit\src\wave.asdb
#  9:09 AM, Wednesday, March
  20, 2024
#  Simulation has been
  initialized
>
```

Console

Processes

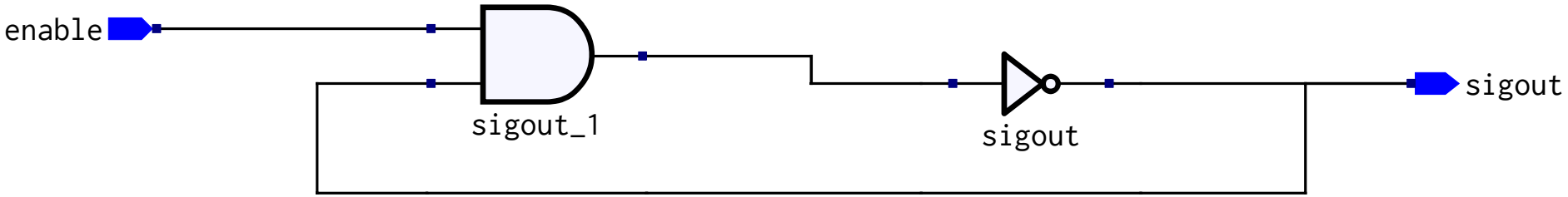
Label	Hierarchy path	Status
verify	/two_level_gate_tb	Ready
u0	/two_level_gate_tb/UUT	Ready
u1	/two_level_gate_tb/UUT	Ready


160 ns
160ns + 0
Design Browser
two_level_gate_tb (testben...
Hierarchy
two_level_gate_tb (te...
std.standard
simple_ckt_tb.vhd
simple_ckt.vhd
untitled.awc *
Bold
Name
Value
a 1
b 1
c 1
s1 1
f 1
test_vectors ((0,0,0,0,0),(0,0
Signal name
Value
20
40
60
80
100
120
140
ns
160 ns
Cursor 1
160 ns

Time	Delta	/two_level_gate_tb/a	/two_level_gate_tb/b	/two_level_gate_tb/c	/two_level_gate_tb/s1	/two_level_gate_tb/f
0 ps	0	U	U	U	U	U
0 ps	1	0	0	0	0	U
0 ps	3	0	0	0	0	0
20000 ps	1	0	0	1	0	X
20000 ps	2	0	0	1	0	1
40000 ps	1	0	1	0	0	X
40000 ps	2	0	1	0	0	0
60000 ps	1	0	1	1	0	X
60000 ps	2	0	1	1	0	1
80000 ps	1	1	0	0	0	X
80000 ps	2	1	0	0	0	0
100000 ps	1	1	0	1	0	X
100000 ps	2	1	0	1	0	1
120000 ps	1	1	1	0	1	1
120000 ps	2	1	1	0	1	X
140000 ps	1	1	1	1	1	X
140000 ps	2	1	1	1	1	1

wave.asdb

```
test_vector 6failed for input a = '1' b = '1' c = '0'
 ns,  Iteration: 0,  Instance: /two_level_gate_tb,  Process: verify.
E_0142 simple_ckt_tb.vhd (78): finish called.
  Iteration: 0,  Instance: /two_level_gate_tb,  Process: verify.
me: 160 ns
```


enable
sigout_1
sigout
sigout