
Module : 'xs3_to_bcd_lut'

Input files:

ABEL PLA file : xs3_to_bcd_lut.tt3
Device library : P22V10GC.dev

Output files:

Report file : xs3_to_bcd_lut.rpt
Programmer load file : xs3_to_bcd_lut.jed

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P22V10GC Programmed Logic:

```
d    = (  p & q
       #   !p & !q & !r
       #   p & r & s
       #   !p & !q & !s );

c    = (  !q & !r
       #   q & r & s
       #   !q & !s );

b    = (  !r & s
       #   r & !s );

a    = (  !s );
```

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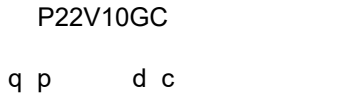
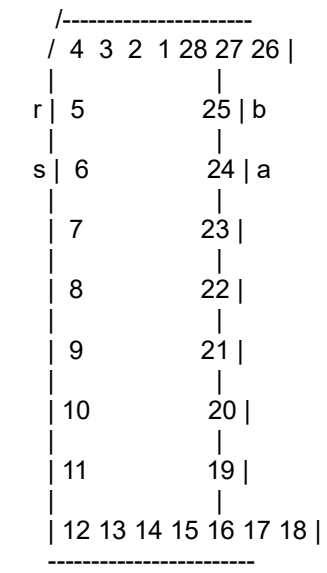
P22V10GC Chip Diagram: (PLCC package)

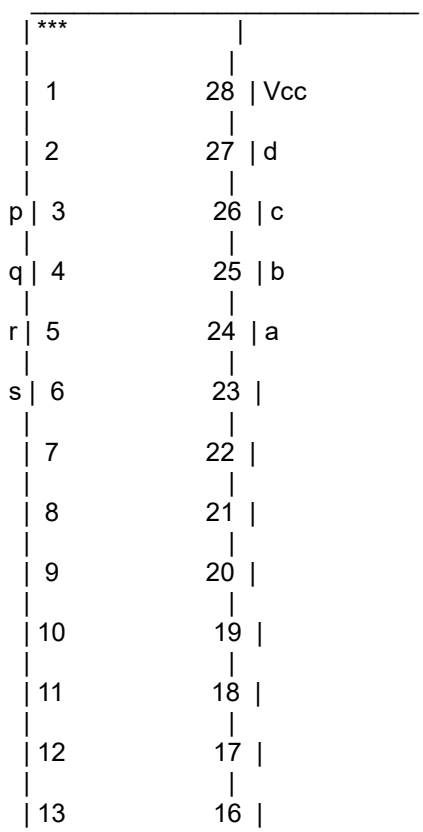




SIGNATURE: N/A

P22V10GC Chip Diagram: (SSOP package)

P22V10GC



SIGNATURE: N/A

P22V10GC Resource Allocations:

Device Resources	Resource Available	Design Requirement	Unused
Input Pins:			
Input:	12	4	8 (66 %)
Output Pins:			
In/Out:	10	4	6 (60 %)
Output:	-	-	-
Buried Nodes:			
Input Reg:	-	-	-
Pin Reg:	10	0	10 (100 %)
Buried Reg:	-	-	-

P22V10GC Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
d	27	4	8	4
c	26	3	10	7
b	25	2	12	10
a	24	1	14	13

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
p	3	INPUT
q	4	INPUT
r	5	INPUT
s	6	INPUT

P22V10GC Unused Resources:

Pin Number	Pin Type	Product Terms	Flip-flop Type
7	INPUT	-	-
9	INPUT	-	-
10	INPUT	-	-
11	INPUT	-	-
12	INPUT	-	-
13	INPUT	-	-
16	INPUT	-	-
17	BIDIR	NORMAL 8	D
18	BIDIR	NORMAL 10	D
19	BIDIR	NORMAL 12	D
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D