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PreLab6: Testbenches for Combinational Designs

ESE382-L01

Bench #4

bcd_to_84_2_1_tb.vhd

```
1  ----------------------------------------------------------------------------------
2  --
3  -- Title       : bcd_to_84_2_1 testbench
4  -- Design      :
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  ----------------------------------------------------------------------------------
9  --
10 -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11 -- Generated   : 2024-03-04  15:00:00
12 -- From        : interface description file
13 -- By          : Itf2Vhdl ver. 1.22
14 --
15 ----------------------------------------------------------------------------------
16 --
17 -- Description : testbench for bcd_to_84_2_1 using truth table with single process
   testbench
18 ----------------------------------------------------------------------------------
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use ieee.numeric_std.all;
23 use work.all;
24
25 entity bcd_to_84_2_1_tb is
26 end bcd_to_84_2_1_tb;
27
28 architecture tb_architecture of bcd_to_84_2_1_tb is
29
30     -- Stimulus signals - signals mapped to the inputs of tested entity
31     signal d, c, b, a : std_logic;
32     -- Observed signals - signals mapped to the outputs of tested entity
33     signal p, q, r, s : std_logic;
34
35 begin
36     -- Unit Under Test port map
37     UUT : entity bcd_to_84_2_1
38     port map (
39             p => p, q => q, r => r, s => s,
40             d => d, c => c, b => b, a => a
41         );
42
43     verify : process
44     constant period : time := 20 ns;
45
46     begin
47
48         d <= '0';
49         c <= '0';
50         b <= '0';
51         a <= '0';
52         wait for period;
53         assert (p = '0' and q = '0' and r = '0' and s = '0')
54         report "Test failed for input combination 0000"
55         severity error;
56
```

```
57          d <= '0';
58          c <= '0';
59          b <= '0';
60          a <= '1';
61          wait for period;
62          assert (p = '0' and q = '1' and r = '1' and s = '1')
63          report "Test failed for input combination 0001"
64          severity error;
65
66          d <= '0';
67          c <= '0';
68          b <= '1';
69          a <= '0';
70          wait for period;
71          assert (p = '0' and q = '1' and r = '1' and s = '0')
72          report "Test failed for input combination 0010"
73          severity error;
74
75          d <= '0';
76          c <= '0';
77          b <= '1';
78          a <= '1';
79          wait for period;
80          assert (p = '0' and q = '1' and r = '0' and s = '1')
81          report "Test failed for input combination 0011"
82          severity error;
83
84          d <= '0';
85          c <= '1';
86          b <= '0';
87          a <= '0';
88          wait for period;
89          assert (p = '0' and q = '1' and r = '0' and s = '0')
90          report "Test failed for input combination 0100"
91          severity error;
92
93          d <= '0';
94          c <= '1';
95          b <= '0';
96          a <= '1';
97          wait for period;
98          assert (p = '1' and q = '0' and r = '1' and s = '1')
99          report "Test failed for input combination 0101"
100         severity error;
101
102         d <= '0';
103         c <= '1';
104         b <= '1';
105         a <= '0';
106         wait for period;
107         assert (p = '1' and q = '0' and r = '1' and s = '0')
108         report "Test failed for input combination 0110"
109         severity error;
110
111         d <= '0';
112         c <= '1';
113         b <= '1';
114         a <= '1';
115         wait for period;
116         assert (p = '1' and q = '0' and r = '0' and s = '1')
```

```
        report "Test failed for input combination 0111"
        severity error;

        d <= '1';
        c <= '0';
        b <= '0';
        a <= '0';
        wait for period;
        assert (p = '1' and q = '0' and r = '0' and s = '0')
        report "Test failed for input combination 1000"
        severity error;

        d <= '1';
        c <= '0';
        b <= '0';
        a <= '1';
        wait for period;
        assert (p = '1' and q = '1' and r = '1' and s = '1')
        report "Test failed for input combination 1001"
        severity error;

    end process verify;
end tb_architecture;

```

control_tb.vhd

```
1  ----------------------------------------------------------------------------
2  --
3  -- Title       : control_tb
4  -- Design      : testbench
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  ----------------------------------------------------------------------------
9  --
10 -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11 -- Generated   : 2024-03-04  15:00:00
12 -- From        : interface description file
13 -- By          : Itf2Vhdl ver. 1.22
14 --
15 ----------------------------------------------------------------------------
16 --
17 -- Description : testbench for control
18 ----------------------------------------------------------------------------
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use ieee.numeric_std.all;
23 use work.all;
24
25 entity control_tb is
26 end control_tb;
27
28 architecture tb_architecture of control_tb is
29
30     -- Stimulus signals - signals mapped to the inputs of tested entity
31     signal gn, an: std_logic;
32     -- Observed signals - signals mapped to the outputs of tested entity
33     signal c0, c1 : std_logic;
34
35
36     type test_vector is record
37         gn : std_logic;
38         an : std_logic;
39         c0 : std_logic;
40         c1 : std_logic;
41     end record;
42
43     type test_vector_array is array (natural range <>) of test_vector;
44
45
46     constant test_vectors : test_vector_array := (
47     --    gn,   an,  c0,  c1
48         ( '0', '0', '1', '0'),
49         ( '0', '1', '0', '1'),
50         ( '1', '0', '0', '0'),
51         ( '1', '1', '0', '0')
52         );
53
54     -- time between application of input stimulus vectors
55     --constant period : time := 20ns;
56
57 begin
```

```
    -- Unit Under Test port map
    UUT : entity control
    port map (
            gn => gn, an => an, c0 => c0, c1 => c1
        );

    verify: process
    begin
    for i in test_vectors'range loop
        gn <= test_vectors(i).gn;
        an <= test_vectors(i).an;
        c0 <= test_vectors(i).c0;
        c1 <= test_vectors(i).c1;
        wait for 20 ns;
        assert (gn = test_vectors(i).gn) and (an = test_vectors(i).an) and (c0 = test_vectors(i).c0) and (c1 = test_vectors(i).c1)
        report "test vector " & integer'image(i)& " failed" & " for input gn = " & std_logic'image(gn) & " and an = " & std_logic'image(an)
        severity error;
    end loop;

        --std.env.finish;   --stop simulation
    end process;

end tb_architecture;

```

route_tb.vhd

```
1  ----------------------------------------------------------------------------
2  --
3  -- Title       : route_tb
4  -- Design      : testbench
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  ----------------------------------------------------------------------------
9  --
10 -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11 -- Generated   : 2024-03-04  15:00:00
12 -- From        : interface description file
13 -- By          : Itf2Vhdl ver. 1.22
14 --
15 ----------------------------------------------------------------------------
16 --
17 -- Description : testbench for route using record
18 ----------------------------------------------------------------------------
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use ieee.numeric_std.all;
23 use work.all;
24
25 entity route_tb is
26 end route_tb;
27
28 architecture tb_architecture of route_tb is
29
30     -- Stimulus signals - signals mapped to the inputs of tested entity
31     signal a, ae, b, be: std_logic;
32     -- Observed signals - signals mapped to the outputs of tested entity
33     signal y : std_logic;
34
35
36     type test_vector is record
37         a : std_logic;
38         ae : std_logic;
39         b : std_logic;
40         be : std_logic;
41         y : std_logic;
42
43     end record;
44
45     type test_vector_array is array (natural range <>) of test_vector;
46
47
48     constant test_vectors : test_vector_array := (
49     --    a,   ae,  b,   be,  y
50         ('0', '0', '0', '0', '1'),
51         ('0', '0', '0', '1', '1'),
52         ('0', '0', '1', '0', '1'),
53         ('0', '0', '1', '1', '0'),
54         ('0', '1', '0', '0', '1'),
55         ('0', '1', '0', '1', '1'),
56         ('0', '1', '1', '0', '1'),
57         ('0', '1', '1', '1', '0'),
```

```
        ('1', '0', '0', '0', '1'),
        ('1', '0', '0', '1', '1'),
        ('1', '0', '1', '0', '1'),
        ('1', '0', '1', '1', '0'),
        ('1', '1', '0', '0', '0'),
        ('1', '1', '0', '1', '0'),
        ('1', '1', '1', '0', '0'),
        ('1', '1', '1', '1', '0')
    );

    -- time between application of input stimulus vectors
    --constant period : time := 20ns;

begin
    -- Unit Under Test port map
    UUT : entity route
    port map (
            a => a, ae => ae, b => b, be => be, y => y
        );

    verify: process
    begin
    for i in test_vectors'range loop
        a <= test_vectors(i).a;
        ae <= test_vectors(i).ae;
        b <= test_vectors(i).b;
        be <= test_vectors(i).be;
        wait for 20 ns;
        assert (a = test_vectors(i).a) and (ae = test_vectors(i).ae) and (b = test_vectors(i).b) and (be = test_vectors(i).be)
        report "test vector " & integer'image(i)& " failed" & " for input a = " & std_logic'image(a) & " and ae = " & std_logic'image(ae) & " and b = " & std_logic'image(b) & " and be = " & std_logic'image(be)
        severity error;
    end loop;

        std.env.finish; --stop simulation
    end process;

end tb_architecture;

```

control_route_mux_tb.vhd

```
1  ----------------------------------------------------------------------------------
2  --
3  -- Title       : control_route_mux_tb
4  -- Design      : testbench
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  ----------------------------------------------------------------------------------
9  --
10 -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11 -- Generated   : 2024-03-04  15:00:00
12 -- From        : interface description file
13 -- By          : Itf2Vhdl ver. 1.22
14 --
15 ----------------------------------------------------------------------------------
16 --
17 -- Description : testbench for control_route_mux without self checking
18 ----------------------------------------------------------------------------------
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use ieee.numeric_std.all;
23 use work.all;
24
25 entity control_route_mux_tb is
26 end control_route_mux_tb;
27
28 architecture tb_architecture of control_route_mux_tb is
29
30     -- Stimulus signals - signals mapped to the inputs of tested entity
31     signal a2, a1, b2, b1, gn, an: std_logic;
32     -- Observed signals - signals mapped to the outputs of tested entity
33     signal y2, y1 : std_logic;
34
35 begin
36     -- Instantiate the tested entity
37     UUT : entity data_selector
38     port map (
39             gn => gn, an =>an, a2 => a2, a1 => a1, b2 => b2, b1 => b1, y2 => y2, y1
   => y1
40         );
41
42     -- Stimulus process
43     verify : process
44     begin
45         for i in 0 to 2**6 - 1 loop -- 2^6 = 64
46             (gn, an, a2, a1, b2, b1) <= std_logic_vector(to_unsigned(i, 6));
47             wait for 10 ns;
48
49         end loop;
50         std.env.finish;
51     end process verify;
52
53 end tb_architecture;
54
```