

bcd_to_84_2_1_tb.vhd

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2  --
3  -- Title      : bcd_to_84_2_1 testbench
4  -- Design     :
5  -- Author     : Dongyun Lee
6  -- Company    : Stony Brook University
7  --
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9  --
10 -- File       : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11 -- Generated  : 2024-03-04 15:00:00
12 -- From       : interface description file
13 -- By         : Itf2Vhdl ver. 1.22
14 --
15 -----
16 --
17 -- Description : testbench for bcd_to_84_2_1 using truth table with single process
testbench
18 -----
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use ieee.numeric_std.all;
23 use work.all;
24
25 entity bcd_to_84_2_1_tb is
26 end bcd_to_84_2_1_tb;
27
28 architecture tb_architecture of bcd_to_84_2_1_tb is
29
30     -- Stimulus signals - signals mapped to the inputs of tested entity
31     signal d, c, b, a : std_logic;
32     -- Observed signals - signals mapped to the outputs of tested entity
33     signal p, q, r, s : std_logic;
34
35 begin
36     -- Unit Under Test port map
37     UUT : entity bcd_to_84_2_1
38     port map (
39         p => p, q => q, r => r, s => s,
40         d => d, c => c, b => b, a => a
41     );
42
43     verify : process
44     constant period : time := 20 ns;
45
46     begin
47
48         d <= '0';
49         c <= '0';
50         b <= '0';
51         a <= '0';
52         wait for period;
53         assert (p = '0' and q = '0' and r = '0' and s = '0')
54         report "Test failed for input combination 0000"
55         severity error;
56

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57 d <= '0';
58 c <= '0';
59 b <= '0';
60 a <= '1';
61 wait for period;
62 assert (p = '0' and q = '1' and r = '1' and s = '1')
63 report "Test failed for input combination 0001"
64 severity error;
65
66 d <= '0';
67 c <= '0';
68 b <= '1';
69 a <= '0';
70 wait for period;
71 assert (p = '0' and q = '1' and r = '1' and s = '0')
72 report "Test failed for input combination 0010"
73 severity error;
74
75 d <= '0';
76 c <= '0';
77 b <= '1';
78 a <= '1';
79 wait for period;
80 assert (p = '0' and q = '1' and r = '0' and s = '1')
81 report "Test failed for input combination 0011"
82 severity error;
83
84 d <= '0';
85 c <= '1';
86 b <= '0';
87 a <= '0';
88 wait for period;
89 assert (p = '0' and q = '1' and r = '0' and s = '0')
90 report "Test failed for input combination 0100"
91 severity error;
92
93 d <= '0';
94 c <= '1';
95 b <= '0';
96 a <= '1';
97 wait for period;
98 assert (p = '1' and q = '0' and r = '1' and s = '1')
99 report "Test failed for input combination 0101"
100 severity error;
101
102 d <= '0';
103 c <= '1';
104 b <= '1';
105 a <= '0';
106 wait for period;
107 assert (p = '1' and q = '0' and r = '1' and s = '0')
108 report "Test failed for input combination 0110"
109 severity error;
110
111 d <= '0';
112 c <= '1';
113 b <= '1';
114 a <= '1';
115 wait for period;
116 assert (p = '1' and q = '0' and r = '0' and s = '1')
```

```
117     report "Test failed for input combination 0111"
118     severity error;
119
120     d <= '1';
121     c <= '0';
122     b <= '0';
123     a <= '0';
124     wait for period;
125     assert (p = '1' and q = '0' and r = '0' and s = '0')
126     report "Test failed for input combination 1000"
127     severity error;
128
129     d <= '1';
130     c <= '0';
131     b <= '0';
132     a <= '1';
133     wait for period;
134     assert (p = '1' and q = '1' and r = '1' and s = '1')
135     report "Test failed for input combination 1001"
136     severity error;
137
138     end process verify;
139 end tb_architecture;
140
```