control_route_mux_tb.vhd

```
1  ----------------------------------------------------------------------------------
2  --
3  -- Title       : control_route_mux_tb
4  -- Design      : testbench
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  ----------------------------------------------------------------------------------
9  --
10 -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11 -- Generated   : 2024-03-04  15:00:00
12 -- From        : interface description file
13 -- By          : Itf2Vhdl ver. 1.22
14 --
15 ----------------------------------------------------------------------------------
16 --
17 -- Description : testbench for control_route_mux without self checking
18 ----------------------------------------------------------------------------------
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use ieee.numeric_std.all;
23 use work.all;
24
25 entity control_route_mux_tb is
26 end control_route_mux_tb;
27
28 architecture tb_architecture of control_route_mux_tb is
29
30     -- Stimulus signals - signals mapped to the inputs of tested entity
31     signal a2, a1, b2, b1, gn, an: std_logic;
32     -- Observed signals - signals mapped to the outputs of tested entity
33     signal y2, y1 : std_logic;
34
35 begin
36     -- Instantiate the tested entity
37     UUT : entity data_selector
38     port map (
39             gn => gn, an =>an, a2 => a2, a1 => a1, b2 => b2, b1 => b1, y2 => y2, y1
   => y1
40         );
41
42     -- Stimulus process
43     verify : process
44     begin
45         for i in 0 to 2**6 - 1 loop -- 2^6 = 64
46             (gn, an, a2, a1, b2, b1) <= std_logic_vector(to_unsigned(i, 6));
47             wait for 10 ns;
48
49         end loop;
50         std.env.finish;
51     end process verify;
52
53 end tb_architecture;
54
```