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Lab5: Behavioral Style Combinational Design Using Case, If, and Loop Statements – XS3 to BCD Converter

ESE382-L01

Bench #4

1. What rules insure that a process statement properly describes a combinational circuit, and not a circuit with latches or flip-flops (memory)?

Every signal that affect outputs should be in the sensitivity list or process must contain wait statement. If a variable is declared, it must assign to the actual signals at the end of the process.

2. For this decoder, which of the three behavioral approaches to describing the architecture leads to the most efficient description? Explain your answer.

In my opinion, case statement is the most efficient description. This is because it allows direct mapping from input to output without unnecessary logic.

3. Are the signal assignment statements inside a process sequential or concurrent statements?

The signal assignment statements in side a process are sequential. It executes statements from top to bottom.

4. In terms of a simulation, what causes your process to be executed? How long does a process in a design description take, in simulated time, to execute during a functional simulation?

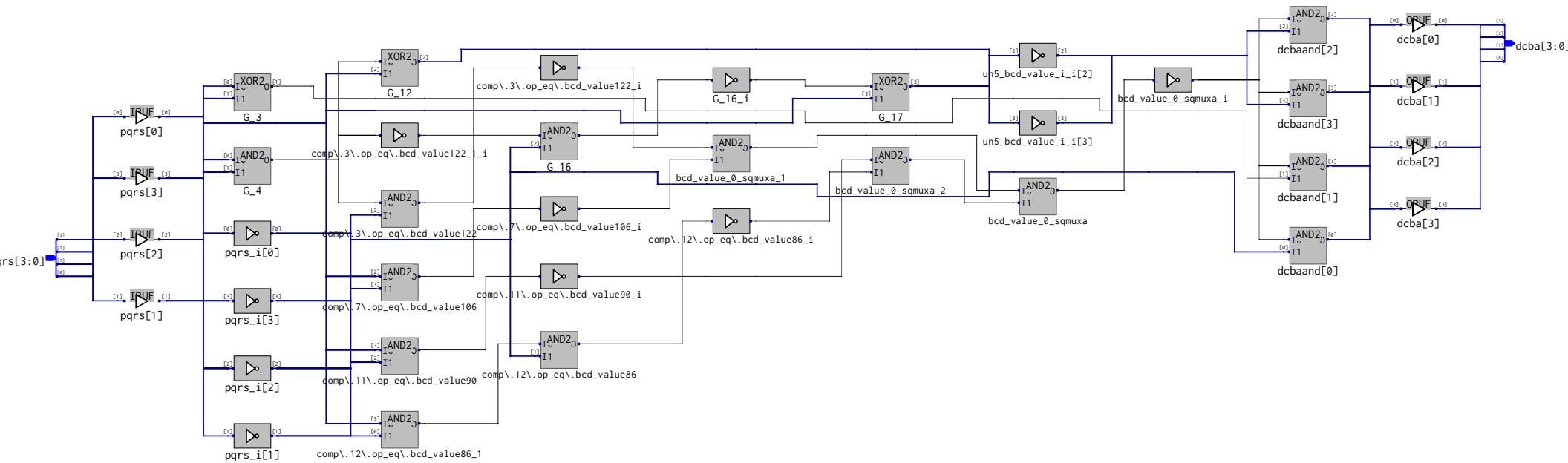
When the signals that are in the seneitivity list have an event or its value changes, the process executes. There was almost no delay of process to execute during a functioanl simulation. There would be a delay if process had wait statement.

5. What is the propagation delay for the designs for which you performed a timing simulation?

The propagation delay was about 30,000 microseconds when I ran the timing simulation.

6. Assuming 20 ns delay between applying each input combination, for how many ns must the simulation be run for all possible input combinations to be applied by the testbench?

There are 8 gates in the flattened-to-gate diagram. If each has 20ns delay, then the propagtion delay would be 8 * 20ns = 160ns.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pqrs_i[2]
pqrs_i[1]
G_12
comp\.3\.op_eq\.bcd_value122_1_i
comp\.3\.op_eq\.bcd_value122
comp\.7\.op_eq\.bcd_value106
comp\.11\.op_eq\.bcd_value90
comp\.12\.op_eq\.bcd_value86_1
comp\.3\.op_eq\.bcd_value122_i
G_16
comp\.7\.op_eq\.bcd_value106_i
comp\.11\.op_eq\.bcd_value90_i
comp\.12\.op_eq\.bcd_value86
G_16_i
bcd_value_0_sqmuxa_1
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