```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title      : control_route_mux_tb
4   -- Design     : testbench
5   -- Author     : Dongyun Lee
6   -- Company    : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File       : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11  -- Generated  : 2024-03-04  15:00:00
12  -- From       : interface description file
13  -- By         : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : for loop 0 to all 1
18  ------------------------------------------------------------------------
    ----
19
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use ieee.numeric_std.all;
23  use work.all;
24
25  entity control_route_mux_tb is
26  end control_route_mux_tb;
27
28  architecture tb_architecture of control_route_mux_tb is
29
30      -- Stimulus signals - signals mapped to the inputs of tested entity
31      signal a2, a1, b2, b1, gn, an: std_logic;
32      -- Observed signals - signals mapped to the outputs of tested entity
33      signal y2, y1 : std_logic;
34
35  begin
36      UUT : entity data_selector
37      port map (
38              gn => gn, an =>an, a2 => a2, a1 => a1, b2 => b2, b1 => b1, y2
    => y2, y1 => y1
39          );
40      verify : process
41      begin
42          for i in 0 to 2**6 - 1 loop
43              (gn, an, a2, a1, b2, b1) <= std_logic_vector(to_unsigned(i, 6
    ));
44              wait for 10 ns;
45
46          end loop;
47          std.env.finish;
48      end process verify;
49
50  end tb_architecture;
51
```