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Lab4: Dataflow Style Combinational Design Using Table Lookup – XS3 to BCD Code Converter

ESE382-L01

Bench #4

Questions

1. Why does the testbench provided use three loops for stimulus instead of just one?

This is because the first part of truth table is 3 don't cares, and the rest 10 values are actual valid values and the last 3 values are don't cares. Therefore the first and last loop is for don't cares and the second loop is the loop where it actually tests the program. We need separate loops for don't cares since the VHDL program does not know what don't cares are.

2. Compare the HDL Analyst hierarchical view of the design you synthesized for this Laboratory with the HDL Analyst hierarchical view of your design from Laboratory 03. Are the diagrams identical? If not, how do they differ? Are they functionally the same? If not, how do they differ functionally?

The diagrams are not identical because for Lab 3 I used CSOP architecture and lab 4 I used Lookup Table. While CSOP hierarchical view, I see steps of signal and AND gates are placed in a row. On the other hand, Lookup table hierarchical view I see the inverters and 4input AND gates and 10 to 4 multiplexer.

3. Compare the pre-fit equations and post-fit equations from ispLEVER Classic for the design you synthesized for this laboratory with the equations from your design for Laboratory 03. Are the equations the same? If not, how do they differ?

The pre-fit equations and post-fit equations are exactly the same. It shows a logic equation for each outputs: d, c, b, and a.

Equations:

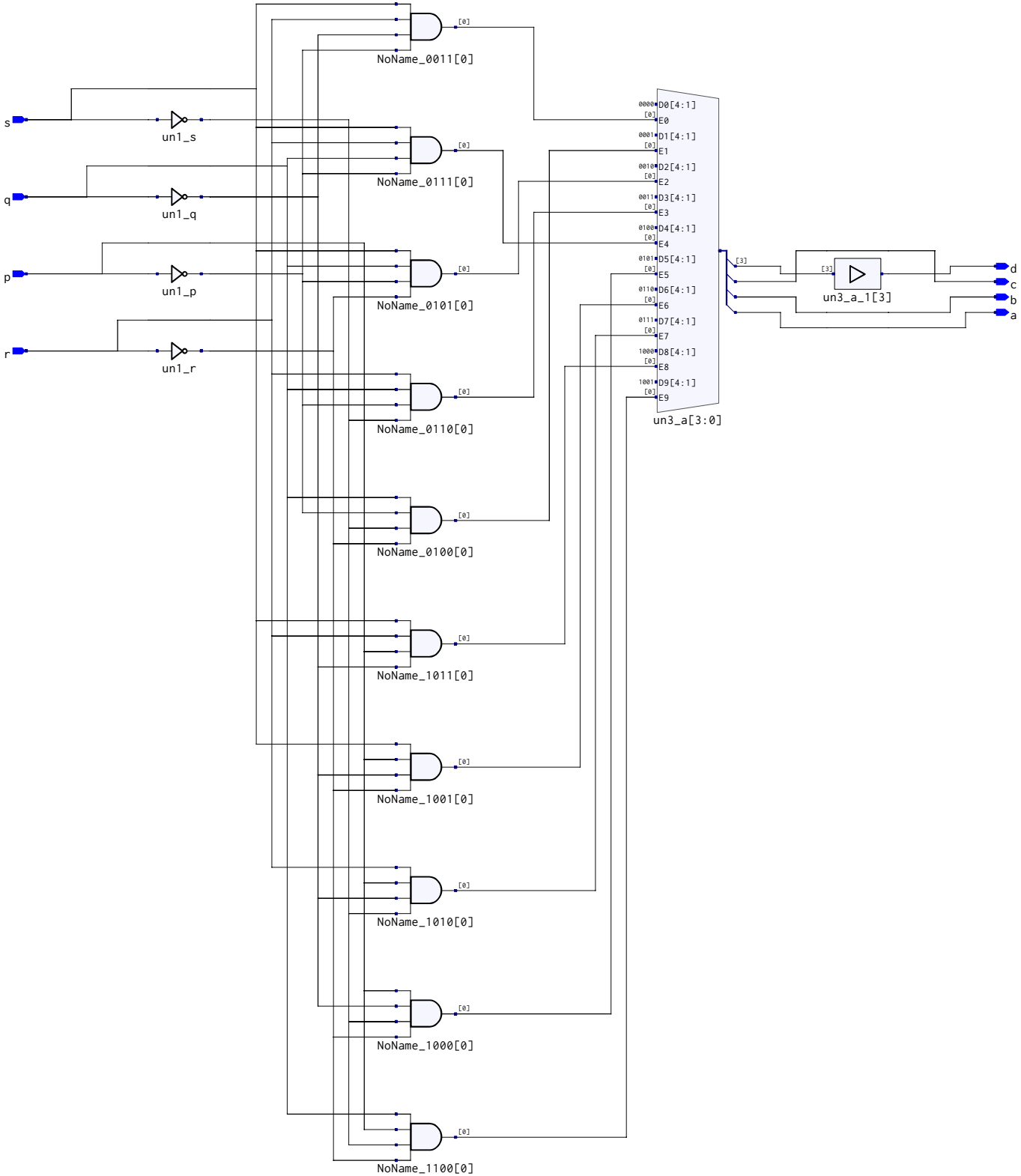
```
d = (p & q
    # !p & !q & !r
    # p & r & s
    # !p & !q & !s);
c = (!q & !r
    # !q & !s
    # q & r & s);
b = (!r & s
```

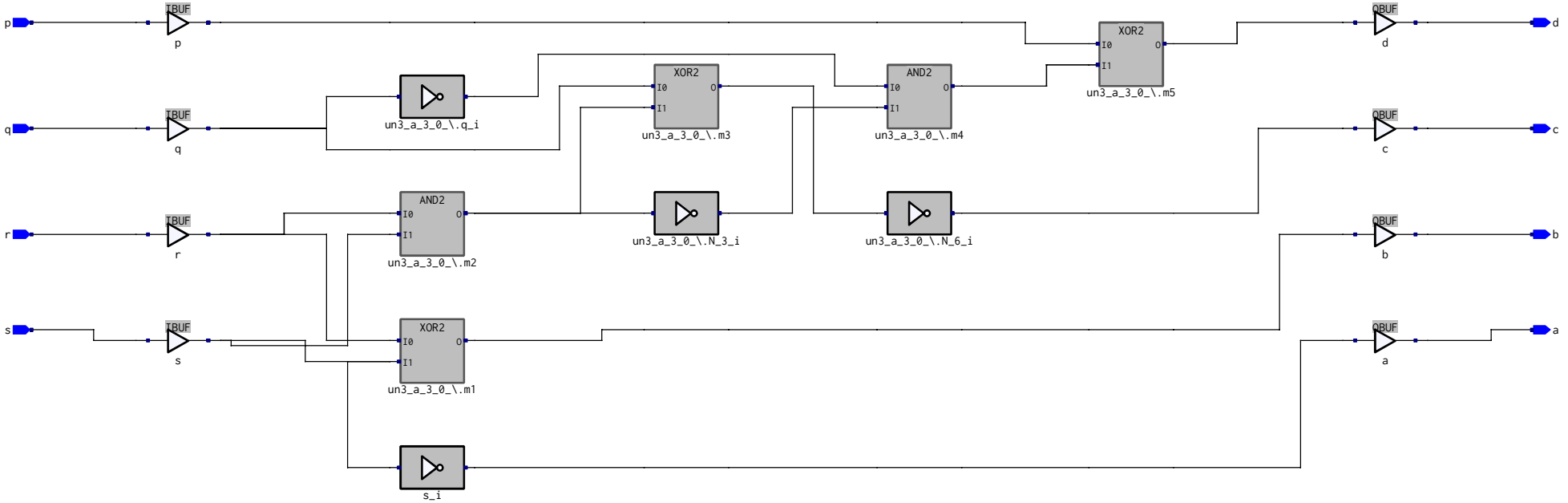
r & !s);

a = (!s);

4. Explain the differences in the output values when input combinations that are not valid inputs to the decoder are applied to your functional simulation and to your timing simulation. What determined these output values for each of your designs?

In the functional simulation, it marked as shaded box which indicates ‘don’t cares,’ however, in the timing simulation, the output values where it is supposed to be ‘don’t cares’ are assigned as random values. The random values for don’t cares are for synthesizer to synthesize a simpler circuit.


s
q
p
r
un1_s
un1_q
un1_p
un1_r
NoName_0011[0]
NoName_0111[0]
NoName_0101[0]
NoName_0110[0]
NoName_0100[0]
NoName_1011[0]
NoName_1001[0]
NoName_1010[0]
NoName_1000[0]
NoName_1100[0]
D0[4:1]
E0
D1[4:1]
E1
D2[4:1]
E2
D3[4:1]
E3
D4[4:1]
E4
D5[4:1]
E5
D6[4:1]
E6
D7[4:1]
E7
D8[4:1]
E8
D9[4:1]
E9
un3_a[3:0]
un3_a_1[3]
d
c
b
a


p
IBUF
p
q
IBUF
q
r
IBUF
r
s
IBUF
s
un3_a_3_0_\.q_i
AND2
I0
O
I1
un3_a_3_0_\.m2
XOR2
un3_a_3_0_\.m1
s_i
XOR2
un3_a_3_0_\.m3
un3_a_3_0_\.N_3_i
AND2
un3_a_3_0_\.m4
un3_a_3_0_\.N_6_i
XOR2
un3_a_3_0_\.m5
OBUF
d
c
b
a

Module : 'xs3_to_bcd_lut'

Input files:

ABEL PLA file : xs3_to_bcd_lut.tt3
Device library : P22V10GC.dev

Output files:

Report file : xs3_to_bcd_lut.rpt
Programmer load file : xs3_to_bcd_lut.jed

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P22V10GC Programmed Logic:

```
d    = (  p & q
       #   !p & !q & !r
       #   p & r & s
       #   !p & !q & !s );

c    = (  !q & !r
       #   q & r & s
       #   !q & !s );

b    = (  !r & s
       #   r & !s );

a    = (  !s );
```

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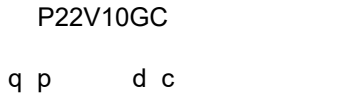
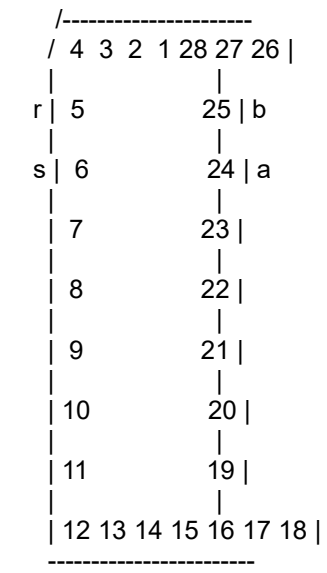
P22V10GC Chip Diagram: (PLCC package)

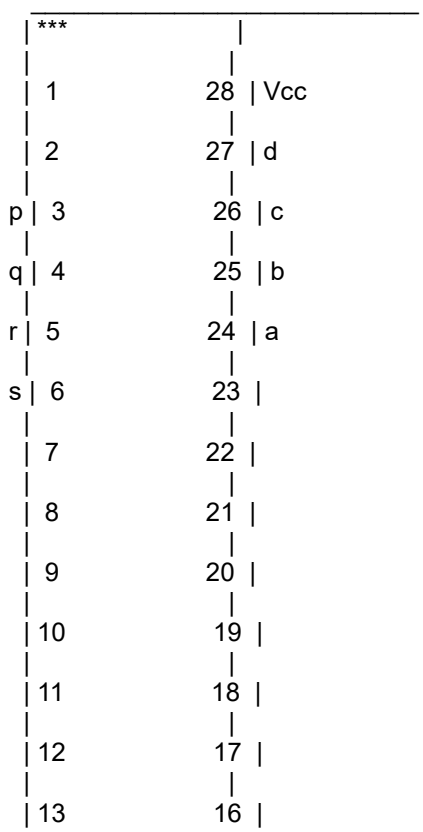




SIGNATURE: N/A

P22V10GC Chip Diagram: (SSOP package)

P22V10GC



SIGNATURE: N/A

P22V10GC Resource Allocations:

Device Resources	Resource Available	Design Requirement	Unused
Input Pins:			
Input:	12	4	8 (66 %)
Output Pins:			
In/Out:	10	4	6 (60 %)
Output:	-	-	-
Buried Nodes:			
Input Reg:	-	-	-
Pin Reg:	10	0	10 (100 %)
Buried Reg:	-	-	-

P22V10GC Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
d	27	4	8	4
c	26	3	10	7
b	25	2	12	10
a	24	1	14	13

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
p	3	INPUT
q	4	INPUT
r	5	INPUT
s	6	INPUT

P22V10GC Unused Resources:

Pin Number	Pin Type	Product Terms	Flip-flop Type
7	INPUT	-	-
9	INPUT	-	-
10	INPUT	-	-
11	INPUT	-	-
12	INPUT	-	-
13	INPUT	-	-
16	INPUT	-	-
17	BIDIR	NORMAL 8	D
18	BIDIR	NORMAL 10	D
19	BIDIR	NORMAL 12	D
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D