File: X:/ESE382-Lab/Lab8/prelab8/prelab8/src/right_shift_reg.vhd

```vhdl
1   ----------------------------------------------------------------------------
    -------
2   --
3   -- Title       : right_shift_reg
4   -- Design      : prelab8
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    -------
9   --
10  -- File        :
    X:\ESE382-Lab\Lab8\prelab8\prelab8\src\right_shift_reg.vhd
11  -- Generated   : Tue Mar 26 15:31:56 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    -------
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    -------
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23
24  entity right_shift_reg is
25    port (
26      d          : in std_logic_vector(3 downto 0);  -- parallel input
    data
27      load       : in std_logic;                     -- synchronous load
    parallel input
28      en_shift   : in std_logic;                     -- enable shift if
    load is unasserted
29      clk        : in std_logic;                     -- clk
30      rst_bar    : in std_logic;                     -- asynchronous reset
31      serial_out : out std_logic                     -- serial output
32    );
33  end right_shift_reg;
34
35
36  architecture behavior of right_shift_reg is
37  signal memory : std_logic_vector(3 downto 0);
38  begin
39      reg : process (clk, rst_bar)
40      begin
41          if rst_bar = '0' then
42              memory <= "0000";
43          elsif rising_edge(clk) then
44              if load = '1' then
45                  memory <= d;
46              elsif en_shift = '1' then
47                  memory <= memory(3 downto 1) & '0';
48              end if;
49          end if;
50      end process;
51
52      serial_out <= memory(0);
53
```

```
54  end behavior;
55
```