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Lab8: Simple Sequential Circuit

ESE382-L01

Bench #4

1. What are the initial states of a latch and flip-flop at the very beginning of a simulation? What would be the corresponding initial states of a latch or flip-flop in an actual PLD?

   The initial states for D-latch ‘0’ initialized state and for d-flip-flop the initial state is ‘U’. In an actual PLD, there is no value such as ‘U’, therefore the initial state is ‘0’.

2. Briefly describe the code for the clock signal in an automatically generated testbench.

   The code for the clock signal could be generated by adjusting period, duty cycle, and offset. Therefore, I can generate the clock cycle to see the outputs from my code easily.

3. Briefly describe how the stimulus for the other (non clock) inputs is generated in automatically generated testbenches.

   One of non clock stimulus is using hot key. Whenever I press the hot jey on the keyboard, it changes the value of input signal. This method is also useful in a way that I can observe the intended output visually on waveform.

4. Why is it important in structural designs to check the Code2Graphics diagram after compilation or the HDL Analyst hierarchical view after synthesis?

   It is important to check the structural designs and compare between Code2Graphics and HDL Analyst hierarchical veiw because both can help to verify if the code has been sucessfully synthesized.

File: F:/ESE382-Lab/Lab8/lab8/left_shift_reg/src/3_to_8_decoder.vhd

```
1    ----------------------------------------------------------------------------
     -----
2    --
3    -- Title       : \3_to_8_decoder\
4    -- Design      : prelab8
5    -- Author      : Dongyun Lee
6    -- Company     : Stony Brook University
7    --
8    ----------------------------------------------------------------------------
     -----
9    --
10   -- File        : X:\ESE382-Lab\Lab8\prelab8\prelab8\src\3_to_8_decoder.vhd
11   -- Generated   : Tue Mar 26 16:29:37 2024
12   -- From        : interface description file
13   -- By          : Itf2Vhdl ver. 1.22
14   --
15   ----------------------------------------------------------------------------
     -----
16   --
17   -- Description :
18   --
19   ----------------------------------------------------------------------------
     -----
20   -------------input latch -----------------------------------
21   library ieee;
22   use ieee.std_logic_1164.all;
23
24   entity input_latch is
25       port(
26       a : in std_logic_vector(2 downto 0);
27       le_bar : in std_logic;
28       a_lat : out std_logic_vector(2 downto 0)
29       );
30   end input_latch;
31
32   architecture behavioral of input_latch is
33   begin
34       latch: process (a, le_bar)
35       begin
36           if le_bar = '0' then
37               a_lat <= a; -- updates the output to the value of data(input)
38           end if;
39       end process;
40   end behavioral;
41
42   -------------3 to 8 decoder --------------------------------
43   library ieee;
44   use ieee.std_logic_1164.all;
45   use ieee.numeric_std.all;
46
47   entity decoder_3to8 is
48       port(
49       a_lat : in std_logic_vector(2 downto 0);
50       g : in std_logic;
51       y : out std_logic_vector(0 to 7)
52       );
53   end decoder_3to8;
```

```
54
55  architecture cond of decoder_3to8 is
56  begin
57      decoder : process (a_lat, g)
58      begin
59          y <= "00000000";
60          if g = '1' then
61              for i in 0 to 7 loop
62                  if unsigned(a_lat) = to_unsigned(i,3) then
63                      y(i) <= '1';
64                  end if;
65                  end loop;
66          end if;
67      end process;
68  end cond;
69
70
71  --------------top level entity latched 3 to 8 decoder -----
72  library ieee;
73  use ieee.std_logic_1164.all;
74  use ieee.numeric_std.all;
75  use work.all;
76
77  entity latched_3to8_decoder is
78      port(
79      a   : in std_logic_vector(2 downto 0);
80      le_bar, e1_bar, e2 : in std_logic;
81      y   : out std_logic_vector(0 to 7)
82      );
83      attribute loc : string;
84      attribute loc of a      : signal is "P2,P3,P4";
85      attribute loc of e1_bar : signal is "P14";
86      attribute loc of e2     : signal is "P15";
87      attribute loc of le_bar : signal is "P16";
88      attribute loc of y      : signal is "P43,P42,P41,P40,P39,P38,P37,P36";
89
90  end latched_3to8_decoder;
91
92  architecture structural of latched_3to8_decoder is
93  signal a_lat : std_logic_vector(2 downto 0);
94  signal g     : std_logic;
95  begin
96      u0 : entity input_latch port map (a => a, le_bar => le_bar, a_lat =>
    a_lat);
97      u1 : entity decoder_3to8 port map (a_lat => a_lat, g => g, y => y);
98      u2 : g <= '1' when (e1_bar = '0') and (e2 = '1') else '0';
99
100 end structural;
101
```

File: F:/ESE382-Lab/Lab8/lab8/left_shift_reg/src/latched_3to8_decoder_tb.vhd

```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : latched_3to8_decoder_tb
4   -- Design      : prelab8
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : Z:\Desktop\SBU 2024 Spring\ESE
    382\lab-backup\Lab8\prelab8\prelab8\src\latched_3to8_decoder_tb.vhd
11  -- Generated   : Sat Mar 30 16:39:02 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description : testbench for latched 3 to 8 decoder
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26  entity latched_3to8_decoder_tb is
27  end latched_3to8_decoder_tb;
28
29
30  architecture latched_3to8_decoder_tb of latched_3to8_decoder_tb is
31     signal a      : std_logic_vector(2 downto 0);
32     signal le_bar : std_logic;
33     signal e1_bar : std_logic;
34     signal e2     : std_logic;
35     signal y      : std_logic_vector(0 to 7);
36
37  type test_vector is record
38      le_bar : std_logic;
39      e1_bar : std_logic;
40      e2     : std_logic;
41      a      : std_logic_vector(2 downto 0);
42      y      : std_logic_vector(0 to 7);
43  end record;
44
45  type test_vectors is array (natural range <>) of test_vector;
46
47  constant test_table : test_vectors := (
48    -- el_   e1_  e2     a       y
49      ( '-', '1', '-', "---", "00000000"), -- When E1 is low, all outputs are
    low
50      ( '-', '-', '0', "---", "00000000"), -- When E2 is low, all outputs are
    low
```

```
51      -- Latch enabled and E1 is low, decoder is active
52      ( '0', '0', '1', "000", "10000000"), -- Input A is 0, Y0 is high
53      ( '0', '0', '1', "001", "01000000"), -- Input A is 1, Y1 is high
54      ( '0', '0', '1', "010", "00100000"), -- Input A is 2, Y2 is high
55      ( '0', '0', '1', "011", "00010000"), -- Input A is 3, Y3 is high
56          ( '1', '0', '1', "---", "--------"), -- When LE is high, outputs
    are stable
57      ( '0', '0', '1', "100", "00001000"), -- Input A is 4, Y4 is high
58      ( '0', '0', '1', "101", "00000100"), -- Input A is 5, Y5 is high
59      ( '0', '0', '1', "110", "00000010"), -- Input A is 6, Y6 is high
60      ( '0', '0', '1', "111", "00000001") -- Input A is 7, Y7 is high
61  );
62
63  begin
64      UUT : entity latched_3to8_decoder port map (
65            a => a,
66            le_bar => le_bar,
67            e1_bar => e1_bar,
68            e2 => e2,
69            y => y
70            );
71      tb : process
72      variable memory : std_logic_vector(7 downto 0);
73      begin
74
75          for i in test_table'range loop
76              a <= test_table(i).a;
77              le_bar <= test_table(i).le_bar;
78              e1_bar <= test_table(i).e1_bar;
79              e2 <= test_table(i).e2;
80              wait for 20ns;
81              if le_bar = '1' and e1_bar = '0' and e2 = '1' then
82                  assert y = memory;
83                  report "Error at le_bar = '1' and e1_bar = '0' and e2 =
    '1'. Output should be stable"
84                  severity error;
85              else
86                  memory := test_table(i).y;
87                  assert y = test_table(i).y
88                  report "Error at input a, le_bar, e1_bar, e2 : " &
    to_string(a) & to_string(le_bar) & to_string(e1_bar) & to_string(e2)
89                  severity error;
90              end if;
91
92
93          end loop;
94          std.env.finish;
95      end process;
96
97
98  end latched_3to8_decoder_tb;
99
```