File: F:/ESE382-Lab/Lab8/lab8/left_shift_reg/src/3_to_8_decoder.vhd

```
1    ----------------------------------------------------------------------------
     -----
2    --
3    -- Title       : \3_to_8_decoder\
4    -- Design      : prelab8
5    -- Author      : Dongyun Lee
6    -- Company     : Stony Brook University
7    --
8    ----------------------------------------------------------------------------
     -----
9    --
10   -- File        : X:\ESE382-Lab\Lab8\prelab8\prelab8\src\3_to_8_decoder.vhd
11   -- Generated   : Tue Mar 26 16:29:37 2024
12   -- From        : interface description file
13   -- By          : Itf2Vhdl ver. 1.22
14   --
15   ----------------------------------------------------------------------------
     -----
16   --
17   -- Description :
18   --
19   ----------------------------------------------------------------------------
     -----
20   -------------input latch -----------------------------------
21   library ieee;
22   use ieee.std_logic_1164.all;
23
24   entity input_latch is
25       port(
26       a : in std_logic_vector(2 downto 0);
27       le_bar : in std_logic;
28       a_lat : out std_logic_vector(2 downto 0)
29       );
30   end input_latch;
31
32   architecture behavioral of input_latch is
33   begin
34       latch: process (a, le_bar)
35       begin
36           if le_bar = '0' then
37               a_lat <= a; -- updates the output to the value of data(input)
38           end if;
39       end process;
40   end behavioral;
41
42   -------------3 to 8 decoder --------------------------------
43   library ieee;
44   use ieee.std_logic_1164.all;
45   use ieee.numeric_std.all;
46
47   entity decoder_3to8 is
48       port(
49       a_lat : in std_logic_vector(2 downto 0);
50       g : in std_logic;
51       y : out std_logic_vector(0 to 7)
52       );
53   end decoder_3to8;
```

```
54
55  architecture cond of decoder_3to8 is
56  begin
57      decoder : process (a_lat, g)
58      begin
59          y <= "00000000";
60          if g = '1' then
61              for i in 0 to 7 loop
62                  if unsigned(a_lat) = to_unsigned(i,3) then
63                      y(i) <= '1';
64                  end if;
65                  end loop;
66          end if;
67      end process;
68  end cond;
69
70
71  --------------top level entity latched 3 to 8 decoder -----
72  library ieee;
73  use ieee.std_logic_1164.all;
74  use ieee.numeric_std.all;
75  use work.all;
76
77  entity latched_3to8_decoder is
78      port(
79      a   : in std_logic_vector(2 downto 0);
80      le_bar, e1_bar, e2 : in std_logic;
81      y   : out std_logic_vector(0 to 7)
82      );
83      attribute loc : string;
84      attribute loc of a      : signal is "P2,P3,P4";
85      attribute loc of e1_bar : signal is "P14";
86      attribute loc of e2     : signal is "P15";
87      attribute loc of le_bar : signal is "P16";
88      attribute loc of y      : signal is "P43,P42,P41,P40,P39,P38,P37,P36";
89
90  end latched_3to8_decoder;
91
92  architecture structural of latched_3to8_decoder is
93  signal a_lat : std_logic_vector(2 downto 0);
94  signal g     : std_logic;
95  begin
96      u0 : entity input_latch port map (a => a, le_bar => le_bar, a_lat =>
    a_lat);
97      u1 : entity decoder_3to8 port map (a_lat => a_lat, g => g, y => y);
98      u2 : g <= '1' when (e1_bar = '0') and (e2 = '1') else '0';
99
100 end structural;
101
```