File: X:/ESE382-Lab/Lab5/converter_xs3_to_BCD/xs3_to_BCD_case/src/xs3_bcd_case_vect.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : xs3_to_BCD_case_vect
4   -- Design      : xe3_to_BCD_case_vect
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\Aldec_Codes\test\test\src\test.vhd
11  -- Generated   : Sun Feb 25 18:09:46 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : converts a 4-bit Excess-3 (XS-3) input (p, q, r, s) to its
    corresponding Binary-Coded Decimal (BCD) output (d, c, b, a) using a case
    statement for the mapping.
18  --               using vectors instead of scalars.
19  ------------------------------------------------------------------------
    ----
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use ieee.numeric_std.all;
23
24  entity converter_xs3_bcd is
25      port ( pqrs : in  std_logic_vector(3 downto 0);
26             dcba : out  std_logic_vector(3 downto 0)
27      );
28  end entity converter_xs3_bcd;
29
30  architecture xs3_bcd_case_vect of converter_xs3_bcd is
31  begin
32      casey : process (pqrs)
33      begin
34          case pqrs is
35              when "0011" => dcba <= "0000";
36              when "0100" => dcba <= "0001";
37              when "0101" => dcba <= "0010";
38              when "0110" => dcba <= "0011";
39              when "0111" => dcba <= "0100";
40              when "1000" => dcba <= "0101";
41              when "1001" => dcba <= "0110";
42              when "1010" => dcba <= "0111";
43              when "1011" => dcba <= "1000";
44              when "1100" => dcba <= "1001";
45              when others => dcba <= "----";
46
47          end case;
48      end process;
49
50  end architecture xs3_bcd_case_vect;
```