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Lab4: Dataflow Style Combinational Design Using Table Lookup – XS3 to BCD Code Converter

ESE382-L01

Bench #4

xs3_to_BCD_selected.vhd

```
library ieee;
use ieee.std_logic_1164.all;

entity xs3_to_BCD_selected is
    port (
        p, q, r, s : in std_logic;
        d, c, b, a : out std_logic
    );
end entity xs3_to_BCD_selected;

architecture selected of xs3_to_BCD_selected is
    signal temp : std_logic_vector(3 downto 0);
begin

    (b, c, d, a) <= temp;

    with std_logic_vector'(p, q, r, s) select
        temp <= "0000" when "0011",
                "0001" when "0100",
                "0010" when "0101",
                "0011" when "0110",
                "0100" when "0111",
                "0101" when "1000",
                "0110" when "1001",
                "0111" when "1010",
                "1000" when "1011",
                "1001" when "1100",
                "----" when others;

    -- with std_logic_vector'(p, q, r, s) select
    --     d <= '0' when "0011" | "0100" | "0101" | "0110" | "0111" | "1000" | "1001" | "1010",
    --          '1' when "1011" | "1100",
    --          '-' when others;

    -- with std_logic_vector'(p, q, r, s) select
    --     c <= '0' when "0011" | "0100" | "0101" | "0110" | "1011" | "1100",
    --          '1' when "0111" | "1000" | "1001" | "1010",
    --          '-' when others;

    -- with std_logic_vector'(p, q, r, s) select
    --     b <= '0' when "0011" | "0100" | "0111" | "1000" | "1011" | "1100",
    --          '1' when "0101" | "0110" | "1001" | "1010",
    --          '-' when others;

    -- with std_logic_vector'(p, q, r, s) select
    --     a <= '0' when "0011" | "0101" | "0111" | "1001" | "1011",
    --          '1' when "0100" | "0110" | "1000" | "1010" | "1100",
    --          '-' when others;


end architecture selected;
```

xs3_to_BCD_conditional.vhd

```
library ieee;
use ieee.std_logic_1164.all;

entity xs3_to_BCD_conditional is
    port (
        p, q, r, s : in std_logic;
        d, c, b, a : out std_logic
    );
end entity xs3_to_BCD_conditional;

architecture conditional of xs3_to_BCD_conditional is
begin
    d <= '1' when p = '1' and q = '0' and r = '1' and s = '1' else
            '1' when p = '1' and q = '1' and r = '0' and s = '0' else
            '-' when (p = '0' and q = '0' and r = '0' and s = '0') or
                    (p = '0' and q = '0' and r = '0' and s = '1') or
                    (p = '0' and q = '0' and r = '1' and s = '0') or
                    (p = '1' and q = '1' and r = '0' and s = '1') or
                    (p = '1' and q = '1' and r = '1' and s = '0') or
                    (p = '1' and q = '1' and r = '1' and s = '1') else
            '0';

    c <= '1' when p = '0' and q = '1' and r = '1' and s = '1' else
            '1' when p = '1' and q = '0' and r = '0' and s = '0' else
            '1' when p = '1' and q = '0' and r = '0' and s = '1' else
            '1' when p = '1' and q = '0' and r = '1' and s = '0' else
            '-' when (p = '0' and q = '0' and r = '0' and s = '0') or
                    (p = '0' and q = '0' and r = '0' and s = '1') or
                    (p = '0' and q = '0' and r = '1' and s = '0') or
                    (p = '1' and q = '1' and r = '0' and s = '1') or
                    (p = '1' and q = '1' and r = '1' and s = '0') or
                    (p = '1' and q = '1' and r = '1' and s = '1') else
            '0';

    b <= '1' when p = '0' and q = '1' and r = '0' and s = '1' else
            '1' when p = '0' and q = '1' and r = '1' and s = '0' else
            '1' when p = '1' and q = '0' and r = '0' and s = '1' else
            '1' when p = '1' and q = '0' and r = '1' and s = '0' else
            '-' when (p = '0' and q = '0' and r = '0' and s = '0') or
                    (p = '0' and q = '0' and r = '0' and s = '1') or
                    (p = '0' and q = '0' and r = '1' and s = '0') or
                    (p = '1' and q = '1' and r = '0' and s = '1') or
                    (p = '1' and q = '1' and r = '1' and s = '0') or
                    (p = '1' and q = '1' and r = '1' and s = '1') else
            '0';

    a <= '1' when p = '0' and q = '1' and r = '0' and s = '0' else
            '1' when p = '0' and q = '1' and r = '1' and s = '0' else
            '1' when p = '1' and q = '0' and r = '0' and s = '0' else
            '1' when p = '1' and q = '0' and r = '1' and s = '0' else
            '1' when p = '1' and q = '1' and r = '0' and s = '0' else
            '-' when (p = '0' and q = '0' and r = '0' and s = '0') or
                    (p = '0' and q = '0' and r = '0' and s = '1') or
                    (p = '0' and q = '0' and r = '1' and s = '0') or
                    (p = '1' and q = '1' and r = '0' and s = '1') or
                    (p = '1' and q = '1' and r = '1' and s = '0') or
                    (p = '1' and q = '1' and r = '1' and s = '1') else
```

```
            '0';
end architecture conditional;
```

xs3_to_BCD_LUT.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity xs3_to_BCD_LUT is
    port( p, q, r, s : in std_logic;
        d, c, b, a : out std_logic);
end entity xs3_to_BCD_LUT;

architecture table_lookup of xs3_to_BCD_LUT is

    subtype LUT_out is std_logic_vector(3 downto 0);

    type truth_table is array (0 to 15) of std_logic_vector(3 downto 0);

    constant xs3_to_BCD_LUT_out : truth_table := (
        "----", "----", "----", "0000",
        "0001", "0010", "0011", "0100",
        "0101", "0110", "0111", "1000",
        "1001", "----", "----", "----"
    );

begin

    d <= xs3_to_BCD_LUT_out(to_integer(unsigned'(p, q, r, s)))(0);
    c <= xs3_to_BCD_LUT_out(to_integer(unsigned'(p, q, r, s)))(1);
    b <= xs3_to_BCD_LUT_out(to_integer(unsigned'(p, q, r, s)))(2);
    a <= xs3_to_BCD_LUT_out(to_integer(unsigned'(p, q, r, s)))(3);

end architecture table_lookup;
```