Here are brief answers to your questions:

Post-synthesis simulation: Verifies the behavior of the synthesized design to ensure it matches the original VHDL model, considering real-world constraints and limitations of the hardware.

Model for Half-Adder: The input model used in post-synthesis simulation is the synthesized gate-level model, which is derived from the original VHDL description.

ispGAL22V10C-10: This is a SPLD (Simple Programmable Logic Device) because it's designed for simpler logic circuits compared to the complexity and reprogrammability offered by CPLDs and FPGAs.

Synthesizer's Compiler: The synthesizer typically has its own compiler to translate VHDL to a hardware-specific format, separate from the Aldec Active-HDL compiler which is more focused on simulation.

Testbench Usage: Generally, the same testbench can be used for both functional and post-synthesis simulations to ensure consistent testing conditions.

Simulation Results: The results might not be exactly the same due to differences in timing and hardware constraints considered in post-synthesis simulation.

Coding Style in Post Synthesis Model: Typically, it's a gate-level or low-level representation focusing on the hardware implementation aspects.

RTL vs. Technology Schematics: They are different in representation (hierarchical vs. flattened), but logically they represent the same circuit. RTL shows the design structure, while the technology view shows the actual gates.

Differences in Waveforms: Slight differences can arise due to the timing and physical constraints applied in the synthesis process, which are not present in the original design simulation.

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Model for Timing Simulation: The model used for timing simulation is typically the synthesized VHDL model, which includes timing information. This model is derived from the synthesis process.

Timing Simulation vs. Post Synthesis Simulation: Timing simulation is more comprehensive, as it includes the effects of timing constraints and propagation delays, making a post synthesis simulation less necessary.

Purpose of 'loc' Attributes: These attributes specify the physical location of elements in the PLD. Synthesis and simulation tools use these to adhere to specific hardware constraints during the design process.

Place-and-Route Tool and 'loc' Attributes: The place-and-route tool uses 'loc' attributes to physically allocate logic components on the PLD, according to the specified locations.

Propagation Delays in half\_adder.vhq: Propagation delays are typically denoted in the VHDL file as specific time values associated with the logic elements, representing the time it takes for signals to propagate through the circuit.