**Design task 1**

D-flip-flop waveform

A screenshot of a computer

Description automatically generated

Qff copy d at rising clock edge.

D-latch waveform

A screenshot of a computer

Description automatically generated

Ql copy d when le\_bar = ‘0’.

Latch vs. flipflop waveform

A screenshot of a computer

Description automatically generated

Qff copy d when rising clock edge and ql copy d when clock = ‘0’.

Sketch of the verification waveform

A blackboard with white text

Description automatically generated

**Design task 2**

waveform

A screenshot of a computer

Description automatically generated

When en = ‘1’ and rst\_bar = ‘1’ q copy d when rising clock edge.

Sketch of the verification waveform

A black background with white lines

Description automatically generated

**Design task 3**

Waveform

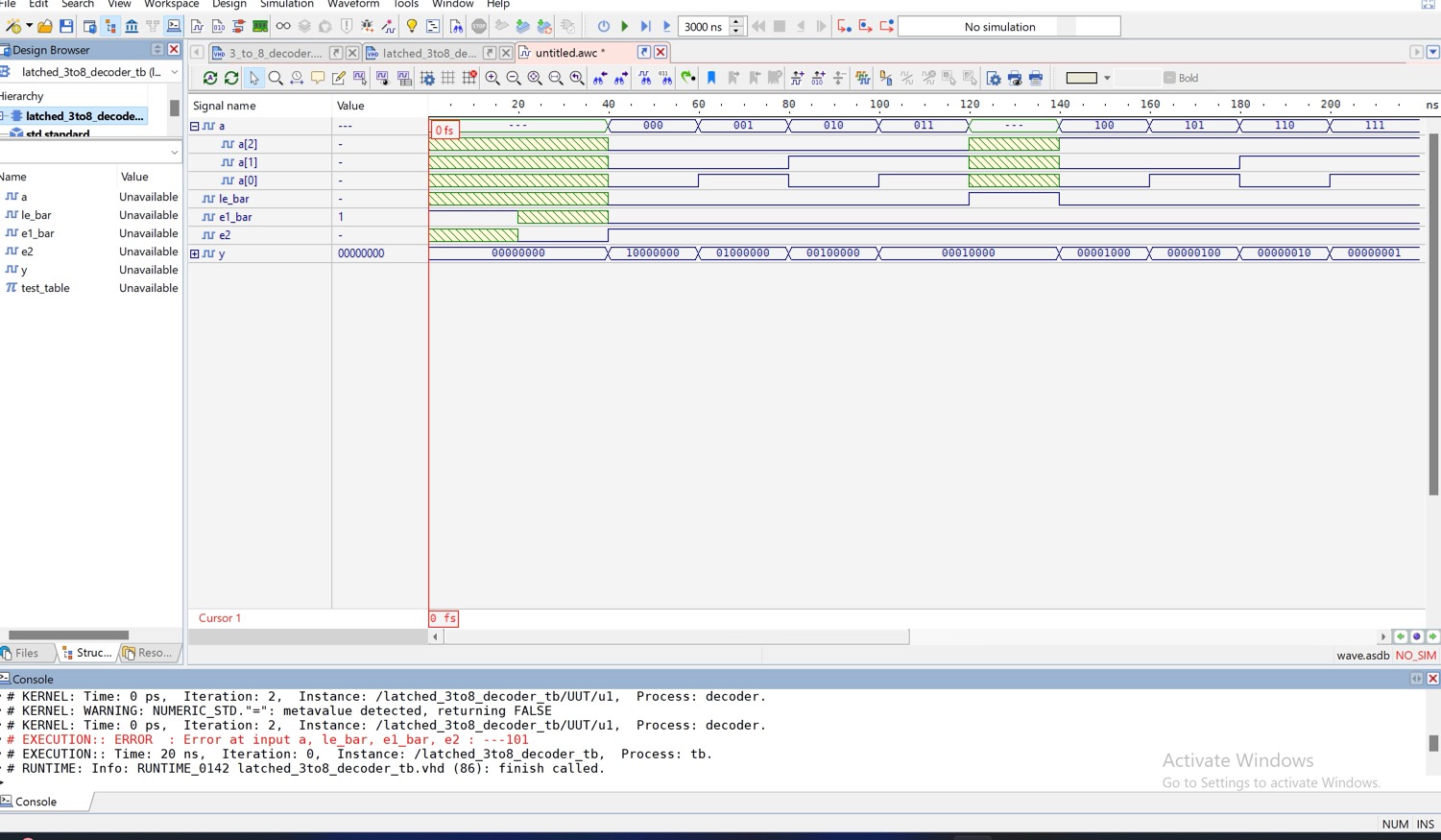
A screenshot of a computer

Description automatically generated

Rst\_bar is the only asynchronous input. When rst\_bar = ‘0’ all the bits of the shift register are 0s. The output loads four bits of input on a rising clock edge when load = ‘1’.

**Design task4**

Waveform



When either e1\_bar = ‘1’ and e2 = ‘0’ , the output must be all 0s. When le\_bar = ‘0’ e1\_bar = ‘0’ and e2 = ‘1’ then the output y is as expected on the truth table. When le\_bar = ‘1’, the output stays the same (as it is shown for y = “00010000”.