```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : load_digit_fsm_tb
4   -- Design      : prelab11
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\load_digit_fsm_tb.vhd
11  -- Generated   : Tue Apr 30 01:08:38 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26  entity load_digit_fsm_tb is
27  end load_digit_fsm_tb;
28
29  architecture load_digit_fsm_tb of load_digit_fsm_tb is
30  -- Signals for the FSM inputs and outputs
31  signal rst_bar   : std_logic;
32  signal clk       : std_logic;
33  signal ss_bar_pe : std_logic;
34  signal ld_cmd    : std_logic;
35  signal load_dig  : std_logic;
36
37  begin
38  UUT: entity load_digit_fsm
39          port map (
40              rst_bar   => rst_bar,
41              clk       => clk,
42              ss_bar_pe => ss_bar_pe,
43              ld_cmd    => ld_cmd,
44              load_dig  => load_dig
45          );
46
47      -- Clock process
48      clocking : process
49      begin
50          while true loop
51              clk <= '0';
52              wait for 10 ns;  -- Clock low for 10 ns
```

```
53              clk <= '1';
54              wait for 10 ns;  -- Clock high for 10 ns
55          end loop;
56      end process;
57  -- Test stimulus process
58  stim_proc : process
59  begin
60      -- Initial Reset
61      rst_bar <= '0';
62      ss_bar_pe <= '0';
63      ld_cmd <= '0';
64      wait for 100 ns;  -- Hold reset for a few clock cycles
65      rst_bar <= '1';
66      wait for 100 ns;  -- Wait after reset is de-asserted
67
68      -- First event: simulating ss_bar_pe positive edge
69      ss_bar_pe <= '1';
70      wait for 40 ns;  -- Wait long enough for FSM to detect ss_bar_pe
71
72      -- Second event: simulating ld_cmd being '1'
73      ld_cmd <= '1';
74      wait for 80 ns;  -- Wait long enough for FSM to detect ld_cmd
75
76      -- Both ss_bar_pe and ld_cmd are '1', now the FSM should transition to
    output_state
77      -- FSM should now output '1' on load_dig signal
78      -- Wait and observe the load_dig signal in the waveform viewer
79      wait for 40 ns;
80
81      -- De-assert ld_cmd and ss_bar_pe to observe FSM returning to wait
    state
82      ld_cmd <= '0';
83      ss_bar_pe <= '0';
84      wait for 40 ns;
85
86      -- Asserting only ss_bar_pe to '1' to ensure FSM does not transition to
    output_state incorrectly
87      ss_bar_pe <= '1';
88      wait for 40 ns;
89
90      -- End the simulation
91      wait;
92  end process;
93
94  end load_digit_fsm_tb;
95
```