```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : rx_buff_reg
4   -- Design      : prelab11
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\rx_buff_reg.vhd
11  -- Generated   : Mon Apr 29 16:13:14 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24
25  entity rx_buff_reg is
26      port (
27          rst_bar : in std_logic; -- asynchronous reset
28          clk : in std_logic; -- system clock
29          load_en : in std_logic; -- enable shift
30          rx_buff_in : in std_logic_vector(7 downto 0); -- received data in
31          rx_buff_out : out std_logic_vector(7 downto 0) -- received data out
32      );
33  end rx_buff_reg;
34
35  architecture Behavioral of rx_buff_reg is
36  begin
37      double_buffer : process (clk, rst_bar)
38      begin
39          if rst_bar = '0' then
40              rx_buff_out <= (others => '0');
41          elsif rising_edge(clk) then
42              if load_en = '1' then
43                  rx_buff_out <= rx_buff_in;
44              end if;
45
46          end if;
47      end process;
48  end Behavioral;
49
```