```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : load_digit_fsm
4   -- Design      : prelab11
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\load_digit_fsm.vhd
11  -- Generated   : Tue Apr 30 00:02:22 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24
25
26  entity load_digit_fsm is
27      port (
28          rst_bar : in std_logic; -- asynchronous system reset
29          clk : in std_logic; -- system clock
30          ss_bar_pe : in std_logic; -- positive edge of ss_bar detected
31          ld_cmd : in std_logic; -- bit 7 is '1' for load command
32          load_dig : out std_logic -- enable a hex_digit to be loaded
33      );
34  end load_digit_fsm;
35
36  architecture moore_fsm of load_digit_fsm is
37  type state is (wait_for_sb_0, wait_for_sb_1, wait_ldc_1, output_state);
38  signal present_state, next_state : state;
39  begin
40      -- first state : detects rst_bar
41      state_reg : process (clk, rst_bar)
42      begin
43          if rst_bar = '0' then
44              present_state <= wait_for_sb_0;
45          elsif rising_edge(clk) then
46              present_state <= next_state;
47          end if;
48      end process;
49
50      -- process where it outputs
51      outputs: process (present_state)
52      begin
```

```
53          case present_state is
54              when output_state => load_dig <= '1';
55              when others => load_dig <= '0';
56          end case;
57      end process;
58
59      nxt_state: process (present_state, ss_bar_pe, ld_cmd)
60      begin
61          case present_state is
62              when wait_for_sb_0 =>
63              if ss_bar_pe = '0' then
64                  next_state <= wait_for_sb_1;
65              else
66                  next_state <= wait_for_sb_0;
67              end if;
68
69              when wait_for_sb_1 =>
70              if ss_bar_pe = '1' then
71                  next_state <= wait_ldc_1;
72              else
73                  next_state <= wait_for_sb_1;
74              end if;
75
76              when wait_ldc_1 =>
77              if ld_cmd = '1' then
78                  next_state <= output_state;
79              else
80                  next_state <= wait_ldc_1;
81              end if;
82
83              when output_state =>
84              next_state <= wait_for_sb_0;
85
86              when others =>
87              next_state <= wait_for_sb_0;
88
89          end case;
90      end process;
91
92  end moore_fsm;
93
```