```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : rx_buff_reg_tb
4   -- Design      : prelab11
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\rx_buff_reg_tb.vhd
11  -- Generated   : Mon Apr 29 16:33:59 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26  entity rx_buff_reg_tb is
27  end rx_buff_reg_tb;
28
29  architecture rx_buff_reg_tb of rx_buff_reg_tb is
30  signal rst_bar, clk, load_en : std_logic; --input
31  signal rx_buff_in : std_logic_vector(7 downto 0); -- input load
32  signal rx_buff_out : std_logic_vector(7 downto 0); -- output load
33
34  constant clk_period : time := 10ns;
35  begin
36
37  UUT: entity rx_buff_reg
38      port map (
39      rst_bar => rst_bar,
40      clk => clk,
41      load_en => load_en,
42      rx_buff_in => rx_buff_in,
43      rx_buff_out => rx_buff_out
44  );
45
46      clock_tb : process
47      begin
48          while true loop
49          clk <= '0';
50          wait for clk_period/2;
51          clk <= '1';
52          wait for clk_period/2;
```

```
53          end loop;
54      end process;
55
56      tb : process
57      begin
58          -- reset
59          rst_bar <= '0';
60          wait for clk_period * 2;
61          rst_bar <= '1';
62          wait for clk_period * 2;
63
64          -- load buffer
65          rx_buff_in <= "10101010";
66          load_en <= '1';
67          wait for clk_period;
68          load_en <= '0';
69
70          wait for clk_period * 5;
71
72          for i in 0 to 255 loop
73              rx_buff_in <= std_logic_vector(to_unsigned(i, 8));
74              load_en <= '1';
75              wait for clk_period;
76              load_en <= '0';
77              wait for clk_period;
78              assert rx_buff_out = std_logic_vector(to_unsigned(i,8))
79              report "Error at " & integer'image(i)
80              severity error;
81          end loop;
82          std.env.finish;
83      end process;
84
85  end rx_buff_reg_tb;
86
```