```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : hex_digit_reg
4   -- Design      : prelab11
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\hex_digit_reg.vhd
11  -- Generated   : Mon Apr 29 20:18:24 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24
25  entity hex_digit_reg is
26      port (
27          rst_bar : in std_logic; -- asynchronous reset
28          clk : in std_logic; -- system clock
29          load_en1 : in std_logic; -- enable load
30          load_en2 : in std_logic; -- enable load
31          hex_dig_in : in std_logic_vector(3 downto 0); -- received data in
32          hex_dig_out : out std_logic_vector(3 downto 0) -- received data out
33      );
34  end hex_digit_reg;
35
36  architecture behavioral of hex_digit_reg is
37  begin
38      reg : process (clk, rst_bar)
39      begin
40          if rst_bar = '0' then
41              hex_dig_out <= (others => '0');
42          elsif rising_edge(clk) then
43              if (load_en1 = '1') and (load_en2 = '1') then
44                  hex_dig_out <= hex_dig_in;
45              end if;
46          end if;
47      end process;
48  end behavioral;
49
```