```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : hex_digit_reg_tb
4   -- Design      : prelab11
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\hex_digit_reg_tb.vhd
11  -- Generated   : Mon Apr 29 20:28:44 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26  entity hex_digit_reg_tb is
27  end hex_digit_reg_tb;
28
29
30  architecture hex_digit_reg_tb of hex_digit_reg_tb is
31  signal rst_bar, clk, load_en1, load_en2 : std_logic;
32  signal hex_dig_in : std_logic_vector (3 downto 0);
33  signal hex_dig_out : std_logic_vector (3 downto 0);
34
35  constant clk_period : time := 20ns;
36  begin
37      UUT: entity hex_digit_reg
38          port map(
39          rst_bar => rst_bar,
40          clk => clk,
41          load_en1 => load_en1,
42          load_en2 => load_en2,
43          hex_dig_in => hex_dig_in,
44          hex_dig_out => hex_dig_out
45          );
46
47
48      clk_tb : process
49      begin
50          while true loop
51          clk <= '0';
52          wait for clk_period/2;
```

```
53          clk <= '1';
54          wait for clk_period/2;
55          end loop;
56      end process;
57
58  -- Stimulus process
59  tb : process
60  begin
61      -- reset
62      rst_bar <= '0';
63      wait for clk_period * 2;
64      rst_bar <= '1';
65      wait for clk_period * 2;
66
67      -- Testing different inputs
68      for i in 0 to 15 loop -- only 16 possible values for 4 bits
69          hex_dig_in <= std_logic_vector(to_unsigned(i, 4));
70          load_en1 <= '1';
71          load_en2 <= '1';
72          wait for clk_period;
73          load_en1 <= '0';
74          load_en2 <= '0';
75
76          -- Conditional assertion check
77          if load_en1 = '1' and load_en2 = '1' then
78              assert hex_dig_out = std_logic_vector(to_unsigned(i, 4))
79                  report "Error at : " & integer'image(i)
80                  severity error;
81          end if;
82
83          -- Wait a bit before the next test to see changes clearly in
    simulation
84          wait for clk_period * 2;
85      end loop;
86
87      -- Finish test
88      std.env.finish;
89  end process;
90
91
92
93  end hex_digit_reg_tb;
94
```