```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : hex_dig_mux
4   -- Design      : prelab11
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\hex_dig_mux.vhd
11  -- Generated   : Tue Apr 30 12:04:27 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ----------------------------------------------------------------------------
    ----
20  library ieee;
21  use ieee.std_logic_1164.all;
22  use ieee.numeric_std.all;
23
24  entity hex_dig_mux is
25      port (
26          hex_dig_0 : in std_logic_vector(3 downto 0); -- mux input vectors
27          hex_dig_1 : in std_logic_vector(3 downto 0); -- mux input vectors
28          hex_dig_2 : in std_logic_vector(3 downto 0); -- mux input vectors
29          hex_dig_3 : in std_logic_vector(3 downto 0); -- mux input vectors
30          sel : in std_logic_vector(1 downto 0); -- multiplexer select inputs
31          hex_dig_out : out std_logic_vector(3 downto 0) -- multiplexer
    output
32      );
33  end hex_dig_mux;
34
35  architecture behavioral of hex_dig_mux is
36  begin
37      with sel select
38      hex_dig_out <= hex_dig_0 when "00",
39      hex_dig_1 when "01",
40      hex_dig_2 when "10",
41      hex_dig_3 when "11",
42      "----" when others;
43
44  end behavioral;
45
```