File: W:/ESE382-Lab/Lab10/prelab10/prelab10/src/edge_det_tb.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : edge_det_tb
4   -- Design      : prelab10
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : W:\ESE382-Lab\Lab10\prelab10\prelab10\src\edge_det_tb.vhd
11  -- Generated   : Sun Apr 21 17:44:51 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26
27
28  entity edge_det_tb is
29  end edge_det_tb;
30
31  architecture edge_det_tb of edge_det_tb is
32  signal rst_bar, clk, sig, pos : std_logic; -- input
33  signal sig_edge : std_logic; -- output
34
35  constant clk_period : time := 20ns; -- time constant
36
37  begin
38      UUT: entity edge_det
39      port map (
40         rst_bar   => rst_bar,
41         clk       => clk,
42         sig       => sig,
43         pos       => pos,
44         sig_edge  => sig_edge
45     );
46
47      -- Clock process
48      clk_process : process
49      begin
50          while true loop
51              clk <= '0';
52              wait for clk_period / 2;
53              clk <= '1';
```

```
54              wait for clk_period / 2;
55          end loop;
56      end process;
57
58      tb : process
59      begin
60          rst_bar <= '0';
61          wait for 40ns;
62          rst_bar <= '1';
63
64  -- Test for Positive Edge Detection
65          pos <= '1';  -- Set to detect positive edges
66          wait for clk_period * 2;
67
68          -- Generate a positive edge
69          sig <= '0';
70          wait for clk_period * 2;
71          sig <= '1';
72          wait for clk_period;
73
74          wait for clk_period;
75          sig <= '0';
76          wait for clk_period * 3;
77
78          -- Test for Negative Edge Detection
79          pos <= '0';  -- Set to detect negative edges
80          wait for clk_period * 2;
81
82          -- Generate a negative edge
83          sig <= '1';
84          wait for clk_period * 2;
85          sig <= '0';
86          wait for clk_period;
87
88
89          wait for clk_period;
90          sig <= '1';
91          wait for clk_period * 3;
92
93          -- End of simulation
94          wait;
95       end process;
96  end edge_det_tb;
97
```