```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : hex_dig_mux_tb
4   -- Design      : prelab11
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\hex_dig_mux_tb.vhd
11  -- Generated   : Tue Apr 30 13:06:07 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26  entity hex_dig_mux_tb is
27  end hex_dig_mux_tb;
28
29  architecture hex_dig_mux_tb of hex_dig_mux_tb is
30  signal hex_dig_0, hex_dig_1, hex_dig_2, hex_dig_3 : std_logic_vector(3
    downto 0);
31  signal sel : std_logic_vector(1 downto 0);
32  signal hex_dig_out : std_logic_vector(3 downto 0);
33
34  type test_vector is record
35      hex_dig_0 : std_logic_vector(3 downto 0);
36      hex_dig_1 : std_logic_vector(3 downto 0);
37      hex_dig_2 : std_logic_vector(3 downto 0);
38      hex_dig_3 : std_logic_vector(3 downto 0);
39      sel       : std_logic_vector(1 downto 0);
40      hex_dig_out : std_logic_vector(3 downto 0);
41  end record;
42
43  type test_table is array (natural range <>) of test_vector;
44
45  constant LUT : test_table := (
46      ("0001", "0010", "0100", "1000", "00", "0001"),
47      ("0001", "0010", "0100", "1000", "01", "0010"),
48      ("0001", "0010", "0100", "1000", "10", "0100"),
49      ("0001", "0010", "0100", "1000", "11", "1000")
50      );
51
```

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52
53  begin
54      UUT : entity hex_dig_mux
55          port map (
56              hex_dig_0 => hex_dig_0,
57              hex_dig_1 => hex_dig_1,
58              hex_dig_2 => hex_dig_2,
59              hex_dig_3 => hex_dig_3,
60              sel       => sel,
61              hex_dig_out => hex_dig_out
62          );
63
64
65      tb : process
66      begin
67          for i in LUT'range loop
68              hex_dig_0 <= LUT(i).hex_dig_0;
69              hex_dig_1 <= LUT(i).hex_dig_1;
70              hex_dig_2 <= LUT(i).hex_dig_2;
71              hex_dig_3 <= LUT(i).hex_dig_3;
72              sel       <= LUT(i).sel;
73              wait for 20 ns;
74              assert hex_dig_out = LUT(i).hex_dig_out
75              report "Error at select input : " & to_string(sel)
76              severity error;
77          end loop;
78          std.env.finish;
79      end process;
80
81
82
83  end hex_dig_mux_tb;
84
```