```vhdl
1   -------------------------------------------------------------------------
    ----
2   --
3   -- Title      : decoder_2to4
4   -- Design     : prelab11
5   -- Author     : Dongyun Lee
6   -- Company    : Stony Brook University
7   --
8   -------------------------------------------------------------------------
    ----
9   --
10  -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
    382\Prelab11\Prelab11\prelab11\src\decoder_2to4.vhd
11  -- Generated   : Mon Apr 29 22:16:17 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  -------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  -------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24
25  entity decoder_2to4 is
26      port (
27          b : in std_logic; -- most significant address bit
28          a : in std_logic; -- least significant address bit
29          Y : out std_logic_vector(3 downto 0) -- selected output asserted
    high
30      );
31  end decoder_2to4;
32
33  architecture dataflow of decoder_2to4 is
34  begin
35      Y <= "0001" when (a & b = "00") else
36      "0010" when (a & b = "01") else
37      "0100" when (a & b = "10") else
38      "1000" when (a & b = "11") else
39      (others => '0');  -- default case to handle undefined statesend
    dataflow;
40  end dataflow;
```