```
1
   ______
2
   -- Title : slv_spi_rx_shifter_tb
-- Design : prelab10
-- Author : Dongyun Lee
-- Company : Stony Brook University
3
5
7
   ______
8
9
10 -- File : \\Mac\Home\Documents\Aldec_Codes\prelab10\prelab10\src\slv_spi_rx_shift
   b.vhd
11 -- Generated : Sun Apr 21 22:43:23 2024
12 -- From : interface description file
13 -- By : Itf2Vhdl ver. 1.22
14 --
15
   ______
16
17 -- Description :
18 --
19 -----
20
21 library ieee;
22 use ieee.std logic 1164.all;
23 use ieee.numeric std.all;
24 use work.all;
25
26
27 entity slv_spi_rx_shifter_tb is
28 end slv_spi_rx_shifter_tb;
29
30 architecture slv spi rx shifter tb of slv spi rx shifter tb is
31
32
   signal rxd, rst_bar, sel_bar, clk, shift_en : std_logic; -- input
33
   signal rx_data_out : std_logic_vector(7 downto 0); --output
34
35 constant clk period : time := 20 ns;
36
37 begin
      UUT : entity slv spi rx shifter
38
39
          port map(
40
          rxd => rxd,
          rst bar => rst_bar,
41
42
          sel bar => sel bar,
43
          clk => clk,
44
          shift en => shift_en,
45
          rx data out => rx_data_out
46
47
48
      clk process : process
49
      begin
50
         while true loop
51
             clk <= '0';
52
             wait for clk period / 2;
```

```
53
                 clk <= '1';
54
                 wait for clk period / 2;
55
             end loop;
56
        end process;
57
58
   -- Stimulus process
59
        stim proc: process
60
        begin
61
             -- Initialize Inputs
             rst_bar <= '0'; -- Apply reset</pre>
62
            wait for 55 ns; -- Keep reset active for 110 ns
rst_bar <= '1'; -- Release reset</pre>
63
64
             shift en <= '1'; -- Enable shift</pre>
65
66
             sel bar <= '0';
67
             -- Simulate input data
68
            wait for 40 ns; -- Wait some time before starting data
    transmission
69
             rxd <= '1'; wait for 20 ns; -- Send bit 1
70
             rxd <= '0'; wait for 20 ns; -- Send bit 0</pre>
71
             rxd <= '1'; wait for 20 ns; -- Send bit 1</pre>
             rxd <= '1'; wait for 20 ns; -- Send bit 1</pre>
72
73
             rxd <= '0'; wait for 20 ns; -- Send bit 0
74
            shift_en <= '0'; -- Disable shifting</pre>
75
            wait for 100 ns; -- Wait while shift is disabled
76
77
78
             rxd <= '1'; wait for 20 ns; -- Attempt to send more data
79
             shift en <= '1'; -- Re-enable shifting</pre>
80
             rxd <= '0'; wait for 20 ns; -- Continue sending data
81
            wait for 100 ns; -- Observe the output
82
83
            wait;
84
        end process;
85
86 end slv spi rx shifter tb;
87
```