File: //Mac/Home/Documents/Aldec_Codes/prelab10/prelab10/src/hex_seven_tb.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : hex_seven_tb
4   -- Design      : prelab10
5   -- Author      : Dongyun Lee
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        :
    \\Mac\Home\Documents\Aldec_Codes\prelab10\prelab10\src\hex_seven_tb.vhd
11  -- Generated   : Mon Apr 22 13:49:47 2024
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :
18  --
19  ------------------------------------------------------------------------
    ----
20
21  library ieee;
22  use ieee.std_logic_1164.all;
23  use ieee.numeric_std.all;
24  use work.all;
25
26
27
28  entity hex_seven_tb is
29  end hex_seven_tb;
30
31
32  architecture hex_seven_tb of hex_seven_tb is
33  signal hex : std_logic_vector(3 downto 0); --input
34  signal seg_drive : std_logic_vector(7 downto 0); -- output
35  begin
36      UUT : entity hex_seven
37          port map(
38          hex => hex,
39          seg_drive => seg_drive
40          );
41
42      tb: process
43      begin
44          -- Test all 16 hexadecimal digits
45          for i in 0 to 15 loop
46              hex <= std_logic_vector(to_unsigned(i, 4));  -- Apply test
    input
47              wait for 20 ns;  -- Wait for 20 ns to observe the output
48          end loop;
49
50          std.env.finish;
51      end process;
```

```
52  end hex_seven_tb;
53
```