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2  --
3  -- Title       : decoder_2to4_tb
4  -- Design      : prelab11
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
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9  --
10 -- File        : \\Mac\Home\Documents\SBU 2024 Spring\ESE
11 382\Prelab11\Prelab11\prelab11\src\decoder_2to4_tb.vhd
12 -- Generated   : Mon Apr 29 22:33:59 2024
13 -- From        : interface description file
14 -- By          : Itf2Vhdl ver. 1.22
15 -----
16 --
17 -- Description :
18 --
19 -----
20 --
21 library ieee;
22 use ieee.std_logic_1164.all;
23 use ieee.numeric_std.all;
24 use work.all;
25
26
27 entity decoder_2to4_tb is
28 end decoder_2to4_tb;
29
30 architecture decoder_2to4_tb of decoder_2to4_tb is
31 signal a, b : std_logic;
32 signal Y : std_logic_vector(3 downto 0);
33
34 type test_vector is record
35     a : std_logic;
36     b : std_logic;
37     Y : std_logic_vector(3 downto 0);
38 end record;
39
40 type test_vector_table is array (natural range <>) of test_vector;
41
42 constant LUT : test_vector_table := (
43     --      a      b      Y
44     ('0', '0', "0001"),
45     ('0', '1', "0010"),
46     ('1', '0', "0100"),
47     ('1', '1', "1000")
48 );
49
50
51 begin
52     UUT : entity decoder_2to4

```

```
53     port map (
54         a => a,
55         b => b,
56         Y => Y
57     );
58
59     tb : process
60     begin
61         for i in LUT'range loop
62             a <= LUT(i).a;
63             b <= LUT(i).b;
64             wait for 20ns;
65             assert Y = LUT(i).Y
66             report "Error at input : " & std_logic'image(a) & std_logic'
image(b)
67                 severity error;
68         end loop;
69         std.env.finish;
70     end process;
71
72 end decoder_2to4_tb;
73
```