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1  -----
2  --
3  -- Title       : hex_seven
4  -- Design      : prelab10
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  -----
9  --
10 -- File        :
11 --             ||Mac\Home\Documents\Aldec_Codes\prelab10\prelab10\src\hex_seven.vhd
12 -- Generated   : Sun Apr 21 23:51:29 2024
13 -- From        : interface description file
14 -- By          : Itf2Vhdl ver. 1.22
15 -----
16 --
17 -- Description :
18 --
19 -----
20
21 library ieee;
22 use ieee.std_logic_1164.all;
23 use ieee.numeric_std.all;
24
25
26 entity hex_seven is
27     port(
28         hex : in std_logic_vector(3 downto 0); -- hexadecimal input
29         -- segs. a..g right justified
30         seg_drive : out std_logic_vector(7 downto 0)
31     );
32 end hex_seven;
33
34
35 architecture behavioral of hex_seven is
36 begin
37     with hex select
38         seg_drive <=
39             "01111110" when "0000", -- 0
40             "00110000" when "0001", -- 1
41             "01101101" when "0010", -- 2
42             "01111001" when "0011", -- 3
43             "00110011" when "0100", -- 4
44             "01011011" when "0101", -- 5
45             "01011111" when "0110", -- 6
46             "01110000" when "0111", -- 7
47             "01111111" when "1000", -- 8
48             "01111011" when "1001", -- 9
49             "01110111" when "1010", -- A
50             "00011111" when "1011", -- b
51             "01001110" when "1100", -- C
52             "00111101" when "1101", -- d

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53         "01001111" when "1110", -- E
54         "01000111" when others; -- F
55     end architecture behavioral;
56
```