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2  --
3  -- Title       : slv_spi_rx_shifter
4  -- Design      : prelab10
5  -- Author      : Dongyun Lee
6  -- Company     : Stony Brook University
7  --
8  -----
9  --
10 -- File        :
11 W:\ESE382-Lab\Lab10\prelab10\prelab10\src\slv_spi_rx_shifter.vhd
12 -- Generated   : Sun Apr 21 18:24:49 2024
13 -- From        : interface description file
14 -- By          : Itf2Vhdl ver. 1.22
15 -----
16 --
17 -- Description :
18 --
19 -----
20
21 library ieee;
22 use ieee.std_logic_1164.all;
23 use ieee.numeric_std.all;
24
25
26 entity slv_spi_rx_shifter is
27     port(
28         rxd          : in  std_logic;           -- Data received from master
29         rst_bar      : in  std_logic;           -- Asynchronous reset
30         sel_bar       : in  std_logic;           -- Selects shifter for
31         operation
32         clk           : in  std_logic;           -- System clock
33         shift_en      : in  std_logic;           -- Enable shift
34         rx_data_out   : out std_logic_vector(7 downto 0) -- Received data
35     );
36 end entity slv_spi_rx_shifter;
37
38 architecture slv_spi_rx_shifter of slv_spi_rx_shifter is
39 begin
40     shift: process (clk, rst_bar)
41         -- variable memory : unsigned(7 downto 0);
42     begin
43         if rst_bar = '0' then
44             rx_data_out <= (others => '0');
45         elsif rising_edge(clk) then
46             if sel_bar = '0' then
47                 if (shift_en = '1') and (rxd = '1' or rxd = '0') then
48                     rx_data_out <= rx_data_out(6 downto 0) & rxd;
49                 end if;
50             end if;
51         end if;

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52         end if;
53
54     end process;
55 end slv_spi_rx_shifter;
56
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